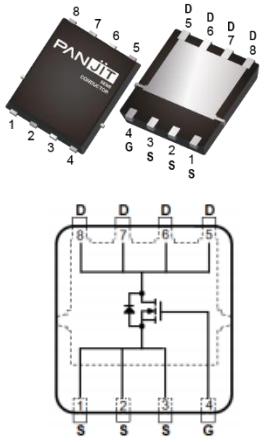
100V N-Channel Enhancement Mode MOSFET

Voltage	**100 V**	**R_{DSON}**	**7.8 mΩ**
Current	**63 A**	**$Q_{G\ (TYP)}$**	**30 nC**

DFN5060-8L



Top side view

Feature

- $R_{DS(ON)}$ < 7.8 mΩ at V_{GS} = 10 V, I_D = 35 A
- $R_{DS(ON)}$ < 11.5 mΩ at V_{GS} = 4.5 V, I_D = 17.5 A
- High switching speed
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard
- 100% UIS / Rg test in mass production

Mechanical Data

- Case: DFN5060-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 94 mg

Application

- PD Charger / Adapter / Home Appliance.

Absolute Maximum Ratings (T_A = 25 °C unless otherwise specified)

PARAMETER		SYMBOL	LIMIT	UNITS
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (Note 3)	T_C=25 °C	I_D	63	A
	T_C=100 °C		40	
Pulsed Drain Current	T_C=25 °C	I_{DM}	252	A
Single Pulse Avalanche Current (Note 5)		I_{AS}	20	A
Single Pulse Avalanche Energy (Note 5)		E_{AS}	50	mJ
Power Dissipation	T_C=25 °C	P_D	65	W
	T_C=100 °C		26	
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55~150	°C

Thermal Characteristics

PARAMETER		SYMBOL	VALUES			UNITS
			MIN.	TYP.	MAX.	
Thermal Resistance	Junction-to-Case (Bottom)	$R_{\theta JC}$	-	1.3	1.9	°C/W
	Junction-to-Ambient (Note 4)	$R_{\theta JA}$	-	-	50	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0 V, I_D=250 μA	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=135 μA	1.1	1.7	2.3	
Drain-Source On-State Resistance (Note 1)	$R_{DS(on)}$	V_{GS}=10 V, I_D=35 A	-	6.8	7.8	mΩ
		V_{GS}=4.5 V, I_D=17.5 A	-	8.7	11.5	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V, V_{GS}=0 V	-	-	1	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0 V	-	-	±100	nA
Transfer characteristics (Note 1)	g_{fs}	V_{DS}=10 V, I_D=35 A	-	85	-	S
Dynamic Characteristics (Note 6)						
Total Gate Charge	Q_g	V_{DS}=50 V, I_D=35 A, V_{GS}=4.5 V	-	14	-	nC
		V_{DS}=50 V, I_D=35 A, V_{GS}=10 V	-	30	39	nC
Gate-Source Charge	Q_{gs}		-	6.7	-	
Gate-Drain Charge	Q_{gd}		-	3.5	-	
Gate Plateau Voltage	$V_{plateau}$		-	3.5	-	V
Input Capacitance	C_{iss}	V_{DS}=50 V, V_{GS}=0 V, f=250 kHz	-	1970	2560	pF
Output Capacitance	C_{oss}		-	530	690	
Reverse Transfer Capacitance	C_{rss}		-	10	-	
Output Charge	Q_{oss}	V_{DS}=50 V, V_{GS}=0 V	-	38	50	nC
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=50 V, I_D=35 A, V_{GS}=10 V, R_G=3.0 Ω (Note 2)	-	6.2	-	ns
Rise Time	t_r		-	5.6	-	
Turn-Off Delay Time	$t_{d(off)}$		-	18	-	
Fall Time	t_f		-	4.4	-	
Gate Resistance	R_g	f =1.0 MHz	-	1.05	2.1	Ω
Drain-Source Diode						
Diode Forward Voltage	V_{SD}	I_S=35 A, V_{GS}=0 V	-	0.9	1.2	V
Reverse Recovery Charge	Q_{rr}	I_F=35 A, V_{DD}=50 V, di/dt=100 A/μs	-	39	-	nC
Reverse Recovery Time	T_{rr}		-	36	-	ns

NOTES :

1. Pulse width ≤ 300 μs, Duty cycle ≤ 2 %
2. Essentially independent of operating temperature typical characteristics.
3. The maximum drain current calculated by maximum junction temperature and thermal impedance. It can be varied by application and environment.
4. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 $inch^2$ with 2oz.square pad of copper.
5. E_{AS} is calculated based on the condition of L = 1.0 mH, I_{AS} = 10 A, V_{DD} = 50 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 20 A in production.
6. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTIC CURVES

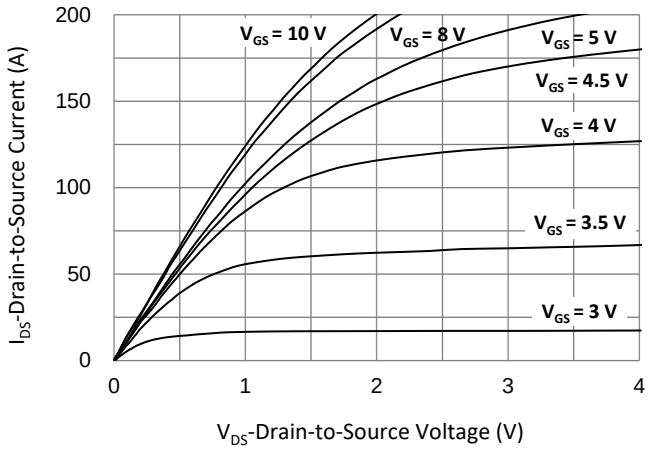


Fig.1 Output Characteristics

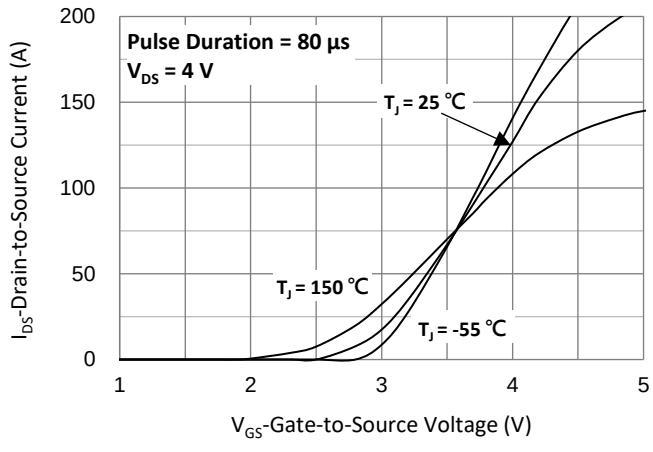


Fig.2 Transfer Characteristics

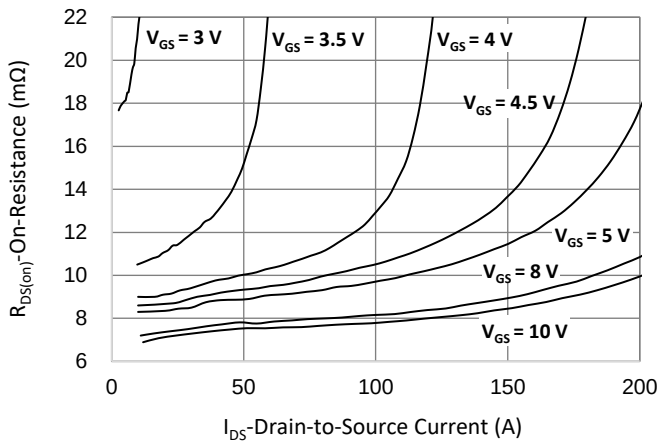


Fig.3 On-Resistance vs. Drain Current

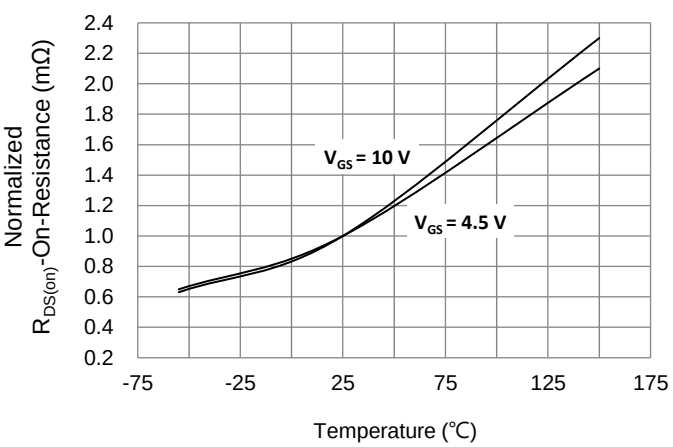


Fig.4 On-Resistance vs. Junction temperature

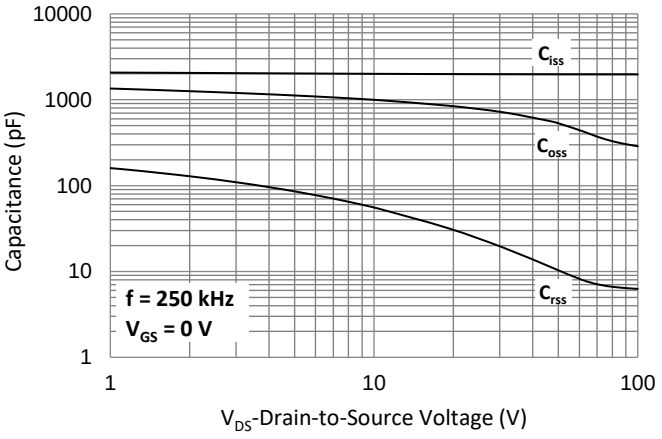


Fig.5 Capacitance vs. Drain-Source Voltage

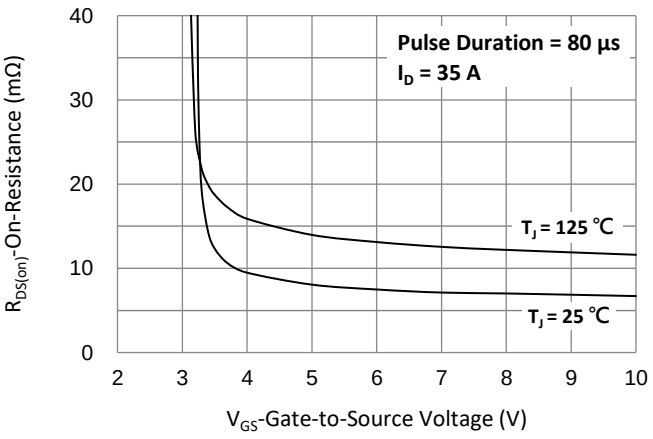


Fig.6 On-Resistance vs. Gate-Source Voltage

TYPICAL CHARACTERISTIC CURVES

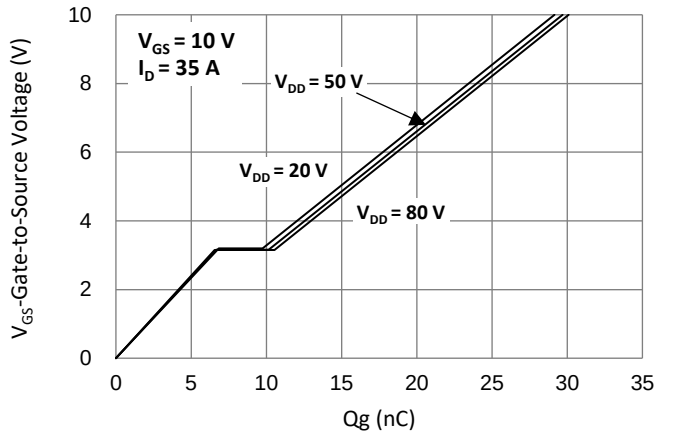


Fig.7 Gate-Charge Characteristics

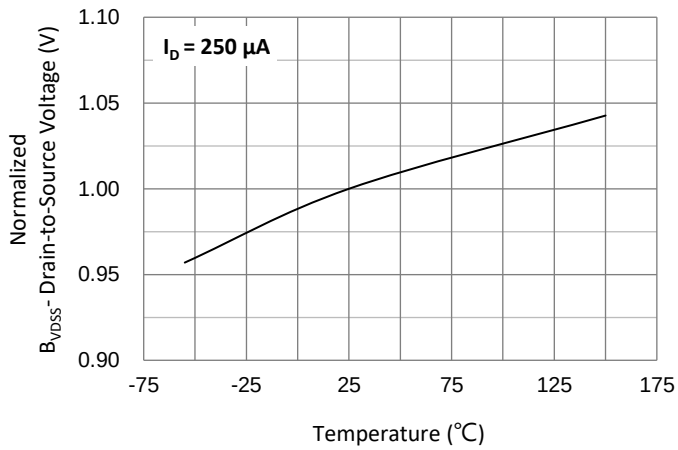


Fig.8 Breakdown Voltage Variation vs. Temperature

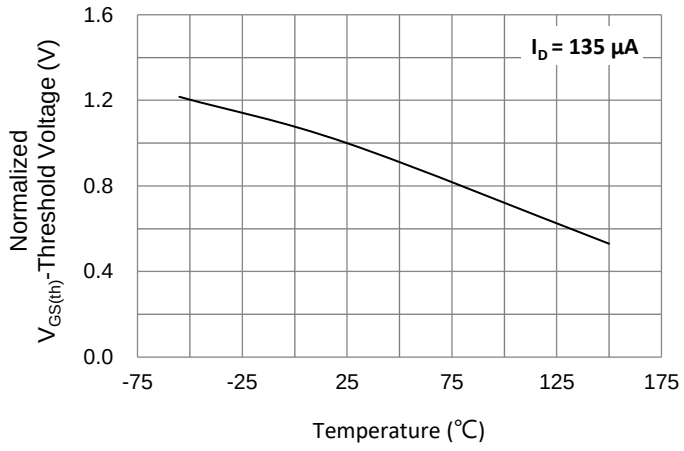


Fig.9 Threshold Voltage Variation with Temperature

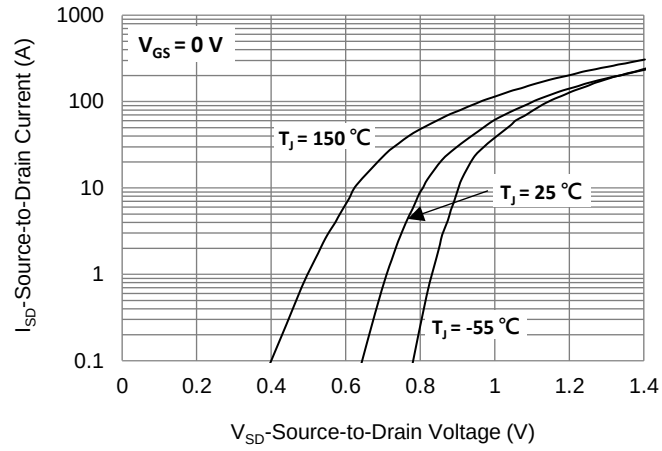


Fig.10 Source-Drain Diode Forward Voltage

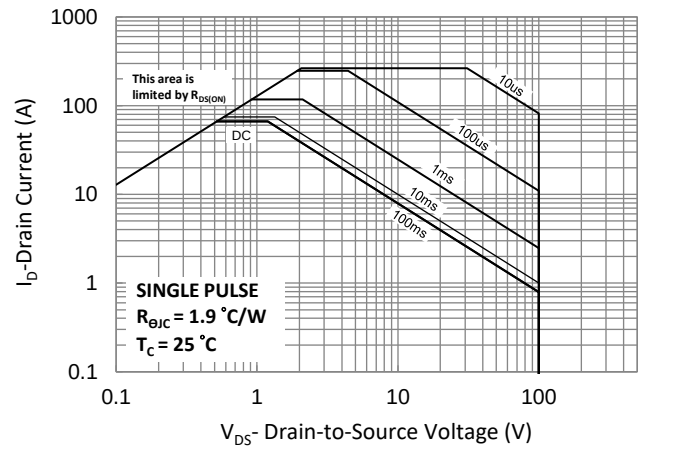


Fig.11 Maximum Safe Operating Area

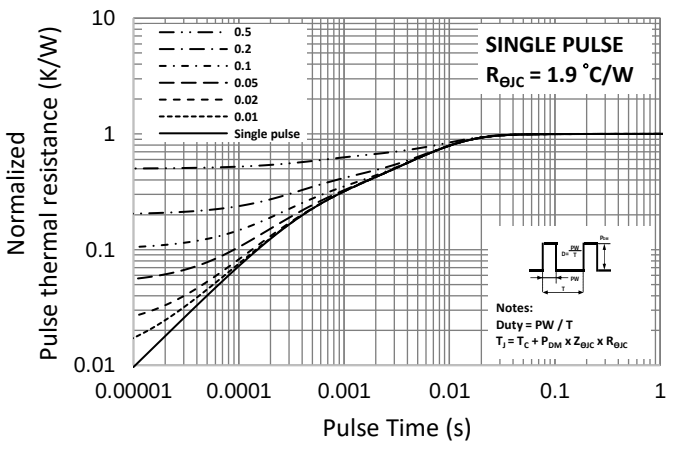


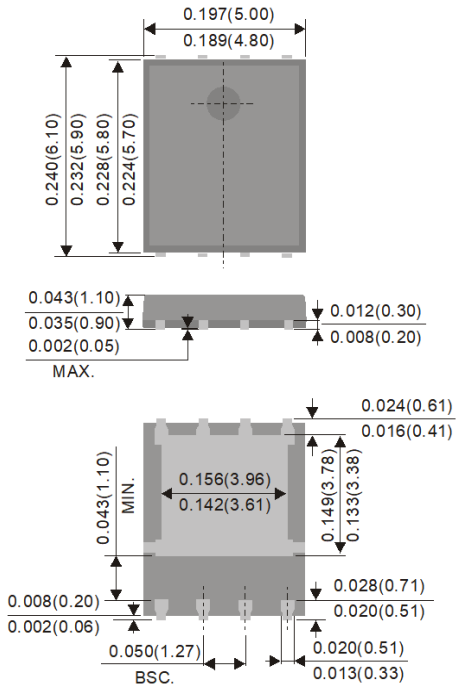
Fig.12 Normalized Transient Thermal Impedance

Product and Packing Information

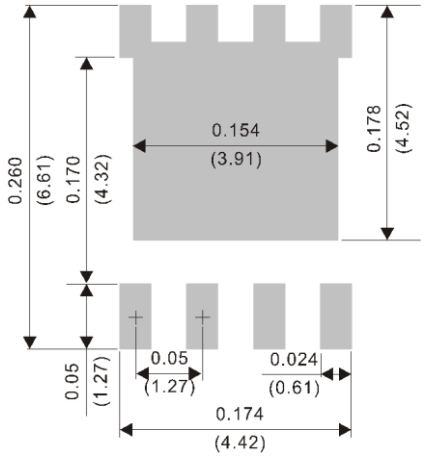
Part No.	Package Type	Packing Type	Marking
PSMQC078N10LS2	DFN5060-8L	3000pcs / 13” reel	078N10LS

Packaging Information & Mounting Pad Layout

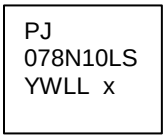
DFN5060-8L Dimension — Unit: inch(mm)



DFN5060-8L Pad Layout — Unit: inch(mm)



Marking Diagram



Y = Year Code
W = Week Code (A~Z)
LL = Lot Code (00~99)
x = Production Line Code

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