Product Specification

PE42552

SPDT UltraCMOS™ RF Switch
DC - 7500 MHz

Features

- HaRP™-Technology-Enhanced
  - Eliminates Gate and Phase Lag
  - No insertion loss or phase drift
  - Fast settling time
- High linearity: 65 dBm IIP3
- Low insertion loss: 0.65 dB at 3.0 GHz, 0.85 dB at 6.0 GHz, 1.0 at 7.5 GHz
- High isolation of 47 dB at 3.0 GHz, 44 dB at 7.5 GHz
- 1 dB compression point: +34.5 dBm typ.
- Logic Select pin to invert logic control
- High ESD: 1000 V HBM
- Absorptive switch design
- Standard 3x3 mm QFN package

Product Description

The PE42552 RF Switch is designed for use in Test/ATE, cellular and other wireless applications. This broadband general purpose switch maintains excellent RF performance and linearity from DC through 7500 MHz. The PE42552 integrates on-board CMOS control logic driven by a single-pin, low voltage CMOS control input. It also has a logic select pin which enables changing the logic definition of the control pin. Additional features include a novel user defined logic table, enabled by the on-board CMOS circuitry. The PE42552 also exhibits outstanding isolation of 44 dB at 7500 MHz, fast settling time, and is offered in a tiny 3x3 mm QFN package.

The PE42552 is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

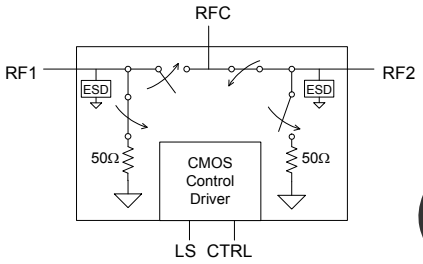


Figure 2. Package Type
16-lead 3x3 mm QFN

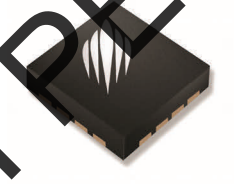


Table 1. Target Electrical Specifications Temp = 25°C, V_{DD} = 3.3V, V_{SS} = 0V / -3.3V

Parameter	Conditions	Min	Typical	Max	Units
Operation Frequency MHz		9 kHz		7.5 GHz	
Insertion Loss	9 KHz 3000 MHz 6000 MHz 7500 MHz		0.6 0.65 0.85 1.0	0.7 0.8 1.0 1.22	dB dB dB dB
Isolation – RF1 to RF2	3000 MHz 6000 MHz 7500 MHz	45 32 25	47 34 28		dB dB dB
Isolation – RFC to RFX	3000 MHz 6000 MHz 7500 MHz	44 49 37	47 55 44		dB dB dB
Return Loss	3000 MHz 6000 MHz 7500 MHz		20 25 15		dB dB dB
Settling Time	50% CTRL to 0.05 dB final value (-40 to +85 °C) *Rising Edge* 50% CTRL to 0.05 dB final value (-40 to +85 °C) *Falling Edge*		9 15	11 45	µs µs
Switching Time	50% CTRL to 90% or 10% of final value (-40 to +85 °C)		5	7	µs
Input 1 dB Compression	800 MHz 7500 MHz	32	34.5 34		dBm dBm
Input IP3	7500 MHz		65		dBm
Input IP2	7500 MHz		100		dBm

Figure 3. Pin Configuration (Top View)

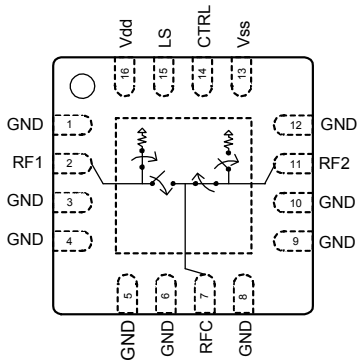


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
2	RF1	RF Port 1
1, 3, 4, 5, 6, 8, 9, 10, 12	GND	Ground
7	RFC	RF Common
11	RF2	RF Port 2
13	V_{SS}	Negative supply voltage or GND connection (Note 1)
14	CTRL	CMOS level:
15	LS	Logic Select - Used to determine the definition for the CTRL pin (see Table 5)
16	V_{DD}	Nominal 3.3 V supply connection

Note: 1. Use VSS (pin 13, VSS = -VDD) to bypass and disable internal negative voltage generator. Connect VSS (pin 13) to GND (VSS = 0V) to enable internal negative voltage generator.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Positive Power Supply Voltage	3.0	3.3	3.6	V
V_{SS} Negative Power Supply Voltage (external power supply used)	-3.6	-3.3	-3.0	V
V_{SS} Negative Power Supply Voltage (internal power supply used)	-0.1	0.0	0.0	V
I_{DD} Power Supply Current (V_{SS} = 0V, Temp = +85 °C)		15	120	µA
I_{SS} Negative Supply (V_{SS} = -V_{DD}, Temp = 25 °C)		-10	-40	µA
Control Voltage High	0.7xV_{DD}			V
Control Voltage Low			0.3xV_{DD}	V
T_{OP} Operating temperature range	-40	25	85	°C
RF Power In[1](P_{IN}): 9 kHz ≤1 MHz 1 MHz ≤7.5 GHz			*fig. 4,5* 30	dBm dBm

Note: 1. Please consult low frequency graphs on page 3 for recommended operating power level.

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42552 in the 16-lead 3x3mm QFN package is MSL1.

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input except for CTRL and LS inputs	-0.3	V_{DD}+ 0.3	V
V_{CTRL}	Voltage on CTRL input		4.0	V
V_{LS}	Voltage on LS input		4.0	V
T_{ST}	Storage temperature range	-65	150	°C
P_{IN}	Input Power: 9 kHz ≤1 MHz 1 MHz ≤7.5 GHz		 *fig. 4,5* 30	 dBm dBm
V_{ESD}	ESD voltage (HBM)[1] ESD voltage (Machine Model)		1000 100	V V

Note: 1. Human Body Model (HBM, MIL_STD 883 Method 3015.7)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 5. Control Logic Truth Table

LS	CTRL	RFC-RF1	RFC-RF2
0	0	off	on
0	1	on	off
1	0	on	off
1	1	off	on

Logic Select (LS)

The Logic Select feature is used to determine the definition for the CTRL pin.

Spurious Performance

The typical spurious performance of the PE42552 is -116 dBm when VSS=0V (pin 13 = GND). If further improvement is desired, the internal negative voltage generator can be disabled by setting VSS = -VDD.

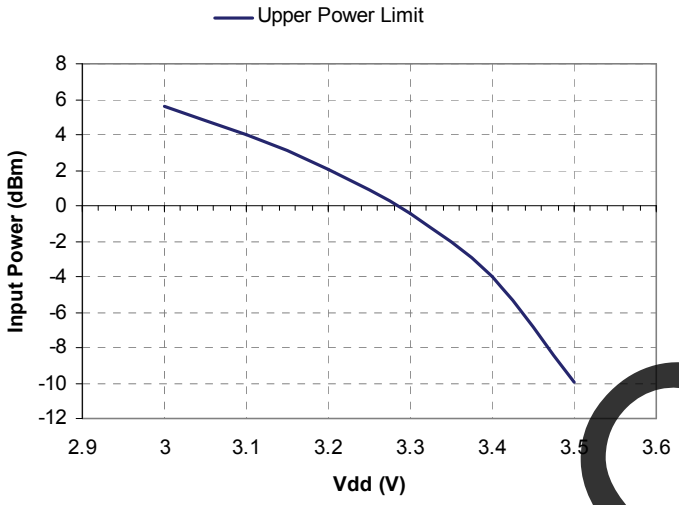
Switching Frequency

The PE42552 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 13=GND). The rate at which the PE42552 can be switched is only limited to the switching time (Table 1) if an external negative supply is provided at (pin13=VSS).

Low Frequency Power Handling: Z_L = 50Ω

Figure 4 provides guidelines of how to adjust the Vdd and input Power to the 42552 device. The upper limit curve represents the maximum Input Power vs Vdd recommended for this part.

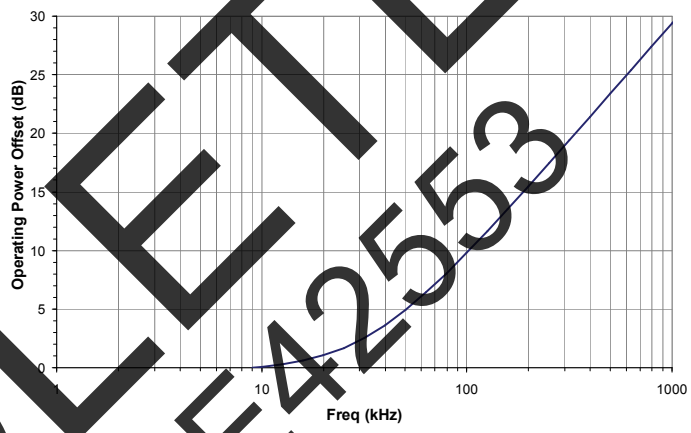
Figure 4. Maximum Operating Power Limit vs. Vdd and Input Power @ 9 KHz



To allow for sustained operation under any load VSWR condition, max power should be kept 6dB lower than max power in 50 Ohm.

Figure 5 shows how the power limit in Figure 4 will increase with frequency. As the frequency increases, the contours and Maximum Power Limit Curve will increase with the increase in power handling shown on the curve.

Figure 5. Operating Power Offset vs. Frequency (Normalized to 9kHz)



Power Handling Examples

Example 1: Maximum power handling at 100kHz, Z=50 ohms, VSWR 1:1, and Vdd=3V

- The power handling offset for 100kHz from *Fig. 5* is 10dB
- The max power handling at Vdd = 3V is 5.5dB from *Fig. 4*
- Derate power under mismatch conditions
- Total maximum power handling for this example is 10dB + 5.5dB = 15.5dBm

Performance Plots: Temperature = 25 °C, V_{DD} = 3.3 V unless otherwise indicated

Figure 6. Nominal Insertion Loss: RF1, RF2

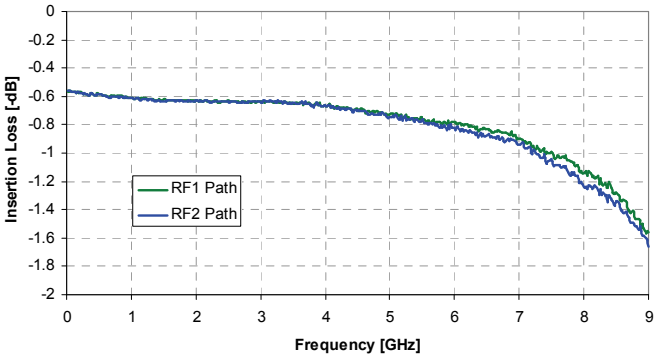


Figure 7. Insertion Loss: RFX @ 3.3 V

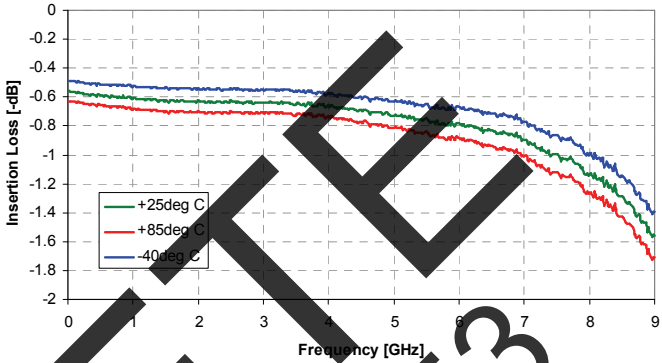


Figure 8. Insertion Loss: RFX @ 25 °C

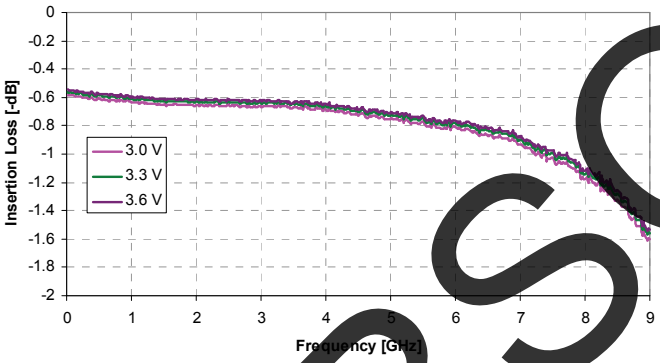


Figure 9. Isolation: Active Port to Isolated Port @ 3.3 V

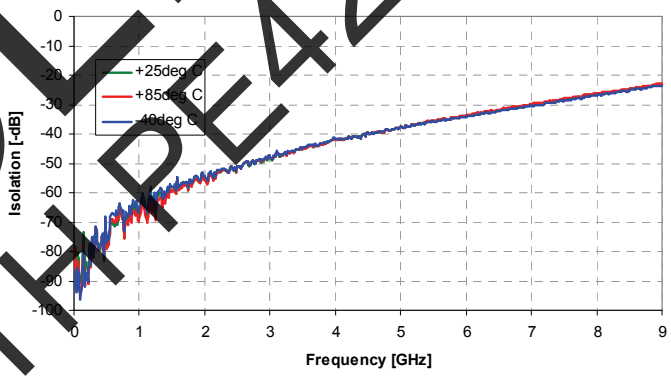


Figure 10. Isolation: Active Port to Isolated Port @ 25 °C

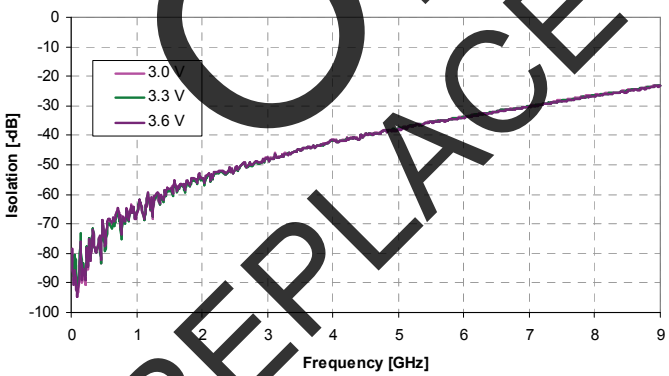
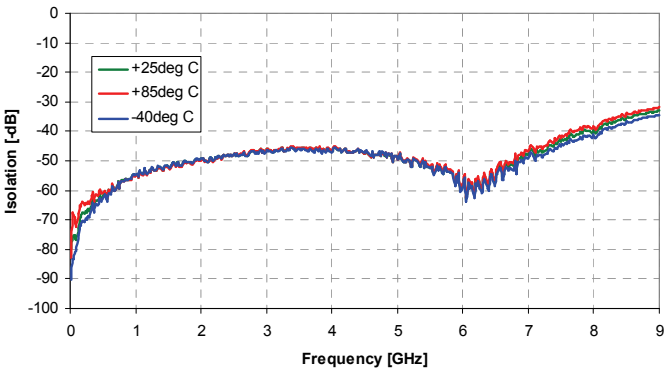


Figure 11. Isolation: RFC to Isolated Port @ 3.3 V



Performance Plots: Temperature = 25 °C, V_{DD} = 3.3 V unless otherwise indicated

Figure 12. Isolation: RFC to Isolated Port @ 25 °C

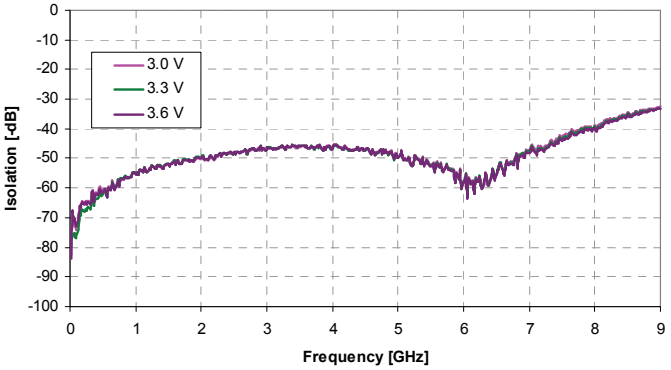


Figure 13. IIP3: Third Order Distortion from 10kHz - 7.5GHz

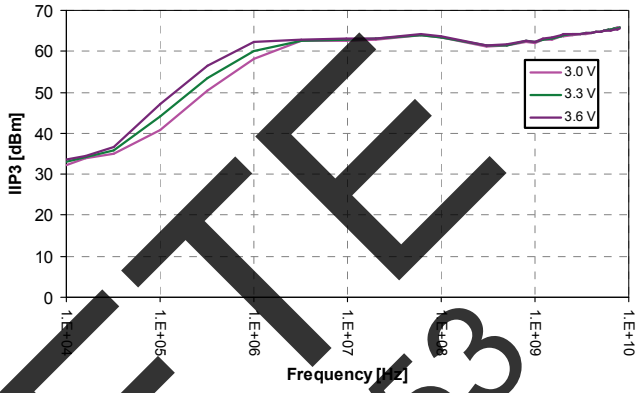


Figure 14. Return Loss at active port @ 25 °C

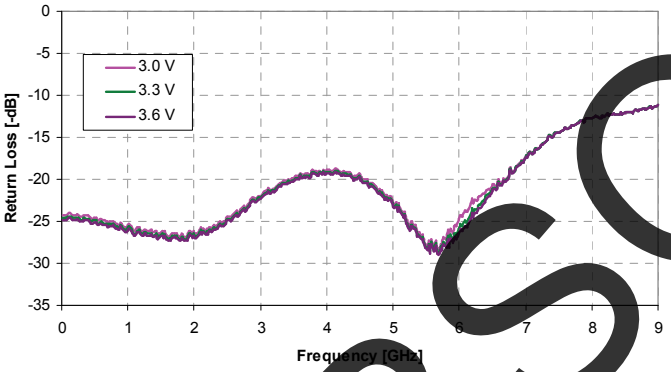
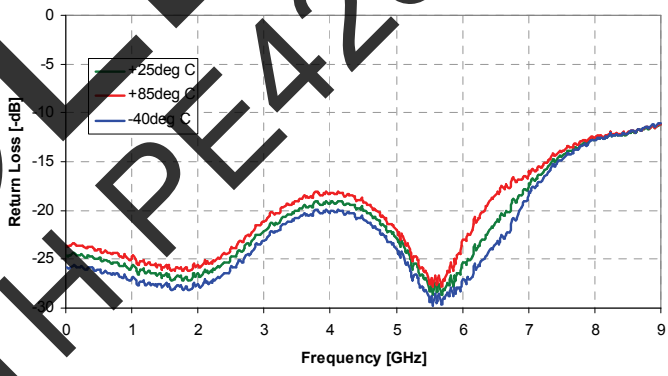


Figure 15. Return Loss at active port @ 3.3 V



Evaluation Kit

The SPDT switch EK Board was designed to ease customer evaluation of Peregrine's PE42552. The RF common port is connected through a 50 Ω transmission line via the top SMA connector, J1. RF1, RF2, RF3 and RF4 are connected through 50 Ω transmission lines via SMA connectors J3, J5, J2 and J4, respectively. A through 50 Ω transmission is available via SMA connectors J6 and J7. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The evaluation kit board is constructed of four metal layers. The dual clad top RF layer is Rogers RO4003 material with an 8 mil RF core and er = 3.55. The other two dielectric layers are FR4 for DC control and overall board strength with an cumulative board thickness of 60 mils. The RF transmission lines were designed using a Grounded co-planar waveguide with a linewidth of 15 mils and gap of 10 mils.

Figure 16. Evaluation Board Layouts
Peregrine Specification 101/0334

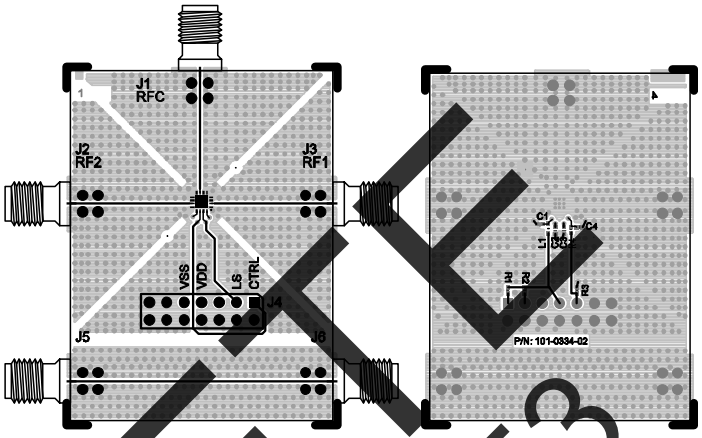


Figure 17. Evaluation Board Schematic
Peregrine Specification 102/0404

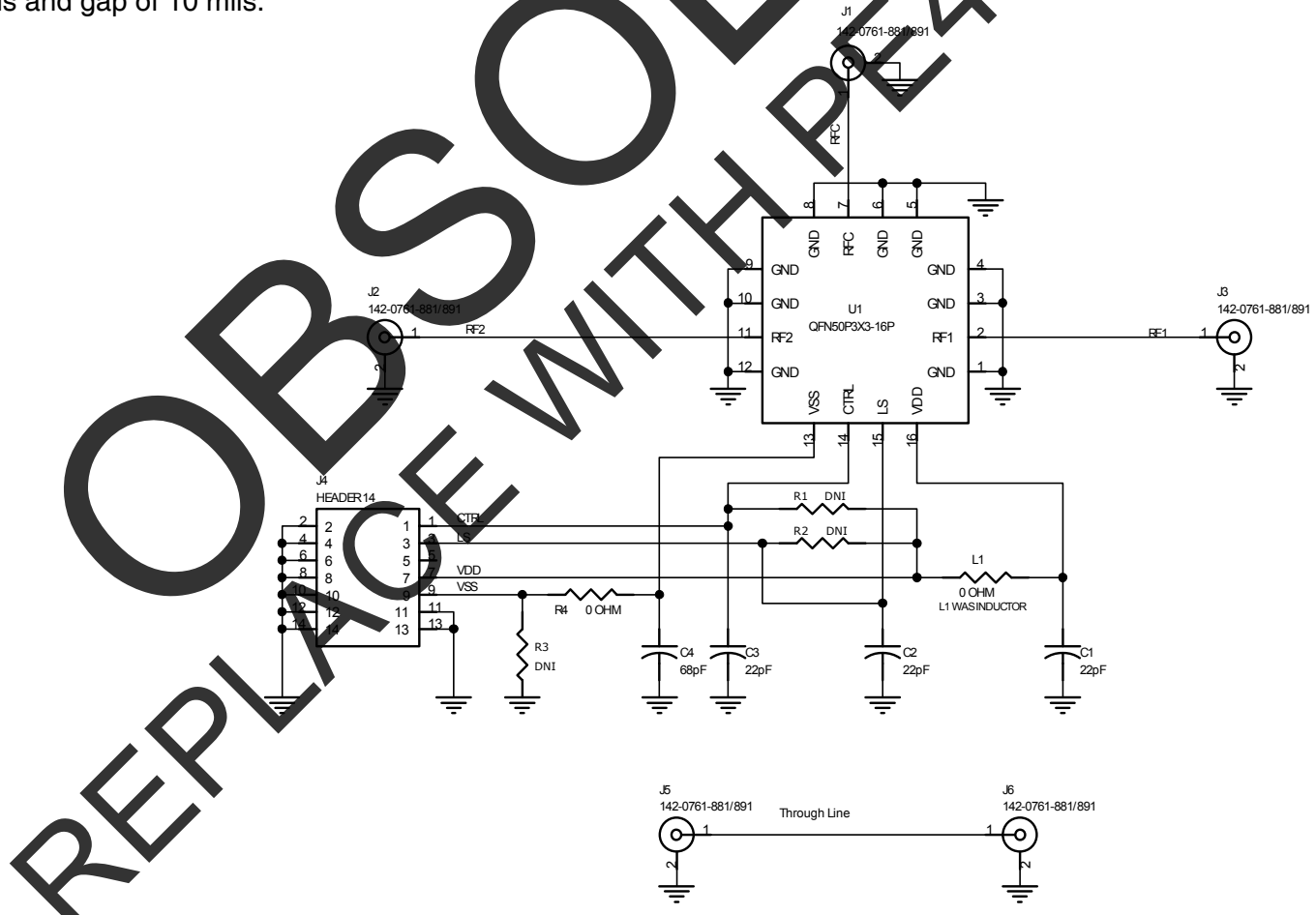
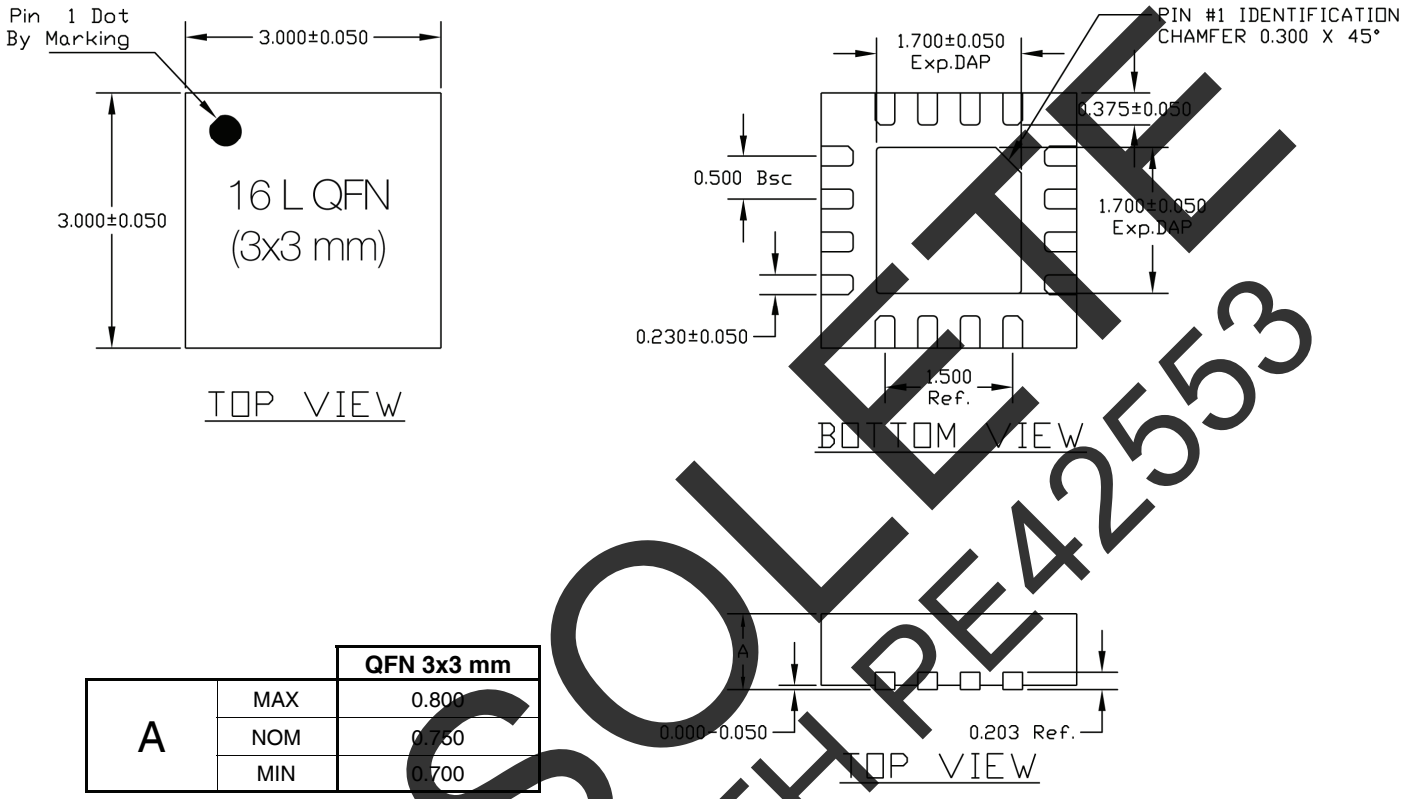


Figure 18. Package Drawing (mm)

16-lead 3x3 mm QFN



		QFN 3x3 mm
A	MAX	0.800
	NOM	0.750
	MIN	0.700

Figure 19. Tape and Reel Specifications

16-lead 3x3 mm QFN

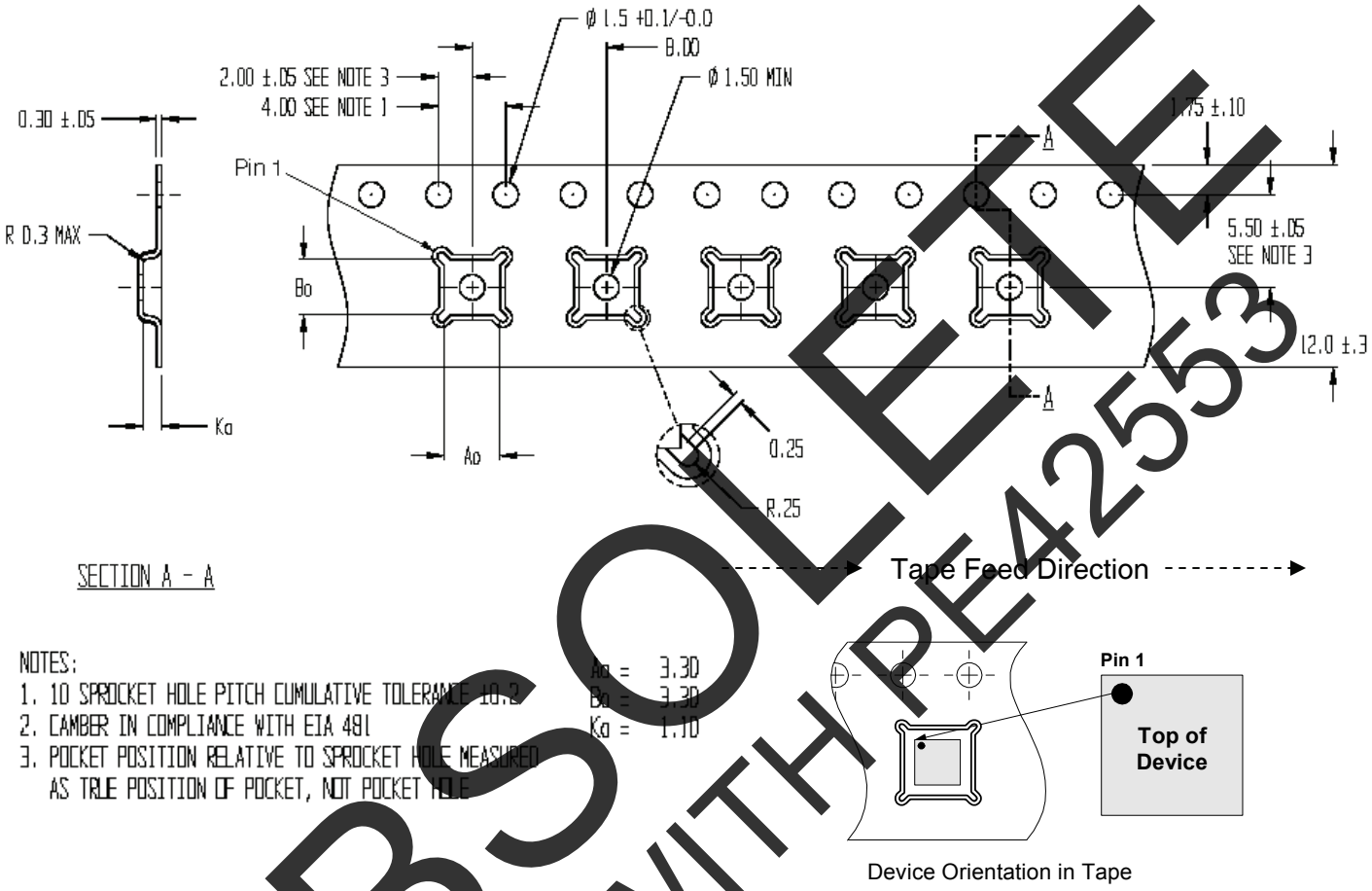


Table 6. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
PE42552MLIB	42552	PE42552G-16QFN 3x3mm-75A	Green 16-lead 3x3mm QFN	Bulk or tape cut from reel
PE42552MLIB-Z	42552	PE42552G-16QFN 3x3mm-3000C	Green 16-lead 3x3mm QFN	3000 units / T&R
EK42552-02	PE42552-EK	PE42552-16QFN 3x3mm-EK	Evaluation Kit	1 / Box

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

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