Product Specification

PE42720

UltraCMOS® SPDT RF Switch
5 – 3000 MHz

Features

- HaRP™ technology enhanced
  - High linearity
    - CTB/CSO of -104 dBc
- Supports +1.8V control logic
- Low insertion loss
  - 0.7 dB @ 1 GHz
  - 0.8 dB @ 2 GHz
  - 1.0 dB @ 3 GHz
- High isolation
  - 65 dB @ 1 GHz
  - 64 dB @ 2 GHz
  - 63 dB @ 3 GHz
- High ESD performance
  - 2500V HBM on all pins
  - 500V CDM on all pins

Product Description

The PE42720 is a HaRP™ technology-enhanced absorptive 75Ω SPDT RF switch developed on the UltraCMOS® process technology.

PE42720 is a highly linear device delivering high isolation and low insertion loss performance. It is designed for CATV applications including CATV signal switching and distribution, cable modem headend, and DBS IF switching.

PE42720 supports +1.8V control logic and offers high ESD protection. In addition, no blocking capacitors are required if DC voltage is not present on the RF ports.

Peregrine's HaRP™ technology enhancement is an innovative feature of the UltraCMOS® process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

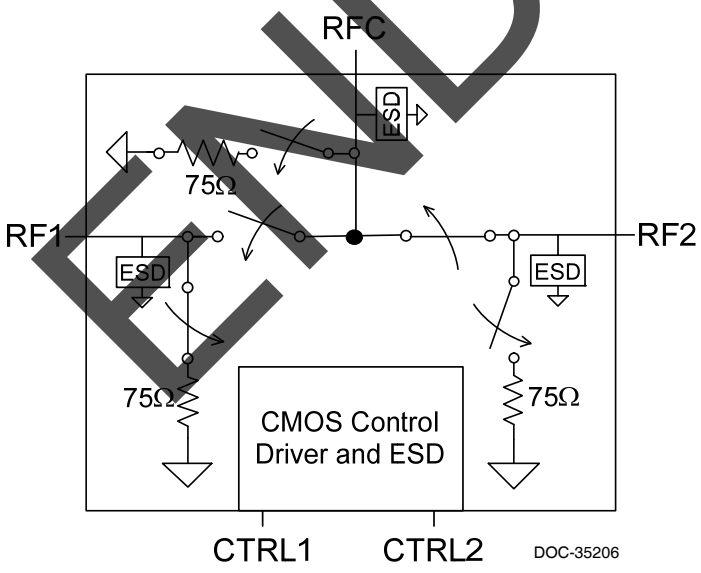


Figure 2. Package Type
20-lead 4x4 mm LGA

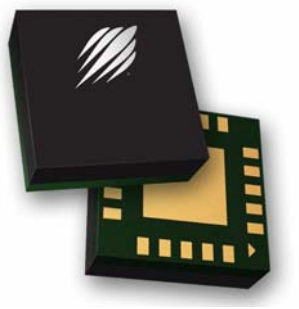


Table 1. Electrical Specifications @ 25°C, V_{DD} = 3.0V ($Z_S = Z_L = 75\Omega$)

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency			5		3000	MHz
Insertion loss	RFC–RFX	5–100 MHz 100–1000 MHz 1000–2000 MHz 2000–3000 MHz		0.6 0.7 0.8 1.0	0.8 0.9 1.0 1.3	dB dB dB dB
Isolation	RFX–RFX	5–100 MHz 100–1000 MHz 1000–2000 MHz 2000–3000 MHz	68 63 60 58	70 65 62 60		dB dB dB dB
Isolation	RFC–RFX	5–100 MHz 100–1000 MHz 1000–2000 MHz 2000–3000 MHz	68 63 62 61	70 65 64 63		dB dB dB dB
Return loss	All ports	5–2500 MHz 2500–3000 MHz		20 14		dB dB
Input 1 dB compression point[1,2]	RFC–RFX	All bands, 100% duty cycle	30	31		dBm
CTB / CSO		159 channels; 42 dBmV per channel output power		-104		dBc
Video feedthrough[3]		DC measurement		5		mV_{PP}
Switching time		50% CTRL to 90% or 10% RF		1500	2100	ns

Notes: 1. The input 1dB compression point is a linearity figure of merit. Refer to *Table 3* for the RF input power P_{IN}
2. Measured in a 50Ω system
3. Measured with a 3 ns rise time, 0/3V pulse and 500 MHz bandwidth

Figure 3. Pin Configuration (Top View)

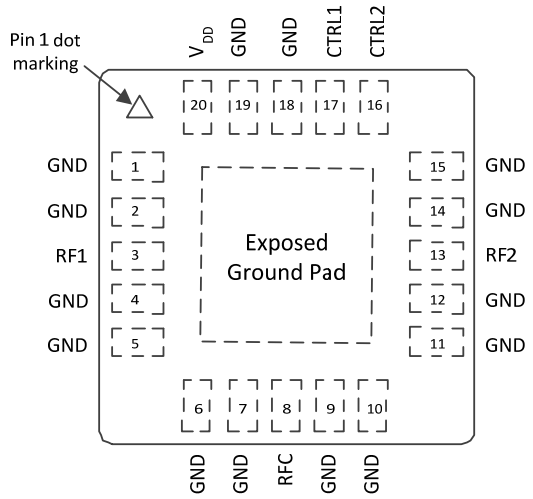


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1, 2, 4-7, 9, 10-12, 14, 15, 18, 19	GND	Ground
3	RF1[1]	RF port
8	RFC[1]	RF common
13	RF2[1]	RF port
16	CTRL2	Digital control logic input 2
17	CTRL1	Digital control logic input 1
20	V_{DD}	Supply voltage
Pad	GND	Exposed pad: ground for proper operation

Note 1: RF pins 3, 8, and 13 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0V DC requirement is met

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.7		5.5	V
Supply current V_{DD} = 2.7 to 5.5V	I_{DD}		130	200	µA
Digital input high (CTRL1, CTRL2)	V_{IH}	1.17		3.6	V
Digital input low (CTRL1, CTRL2)	V_{IL}	-0.3		0.6	V
Digital input current	I_{CTRL}		9	12	µA
RF input power (RFC–RFX)[1]	P_{IN}			28	dBm
RF input power into terminated ports (RFX)[1]	$P_{IN,TERM}$			20	dBm
Operating temperature range	T_{OP}	-40		+85	°C

Note 1: 100% duty cycle, all bands, 75Ω

Table 4. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage (CTRL1, CTRL2)	V_{CTRL}	-0.3	3.6	V
RF input power (RFC–RFX)[1]	P_{IN}		28	dBm
RF input power into terminated ports (RFX)[1]	$P_{IN,TERM}$		20	dBm
Storage temperature range	T_{ST}	-65	+150	°C
ESD voltage HBM[2], all pins	$V_{ESD,HBM}$		2500	V
ESD Voltage MM[3], all pins	$V_{ESD,MM}$		150	V
ESD Voltage CDM[4], all pins	$V_{ESD,CDM}$		500	V

Notes: 1. 100% duty cycle, all bands, 75Ω
2. Human Body Model (MIL-STD 883 Method 3015)
3. Machine Model (JEDEC JESD22-A115)
4. Charged Device Model (JEDEC JESD22-C101)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Switching Frequency

The PE42720 has a maximum 25 kHz switching rate.

Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value. Switching time is provided in *Table 1*.

Table 5. Truth Table

CTRL1	CTRL2	RFC – RF1	RFC – RF2
Low	Low	OFF	OFF
Low	High	OFF	ON
High	Low	ON	OFF
High	High	N/A[1]	N/A[1]

Note 1: CTRL1 = HIGH and CTRL2 = High are not supported

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42720 in the 20-lead 4x4 mm LGA package is MSL3.

Spurious Performance

The typical spurious performance of the PE42720 is –155 dBm.

Typical Performance Data @ 25°C and V_{DD} = 3.0V unless otherwise specified

Figure 4. Insertion Loss (RFC–RFX)

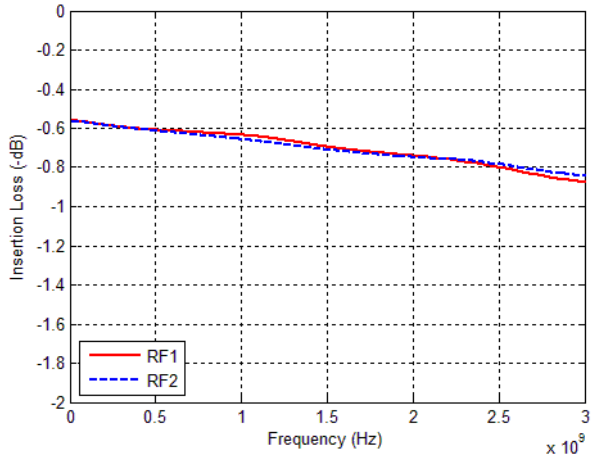


Figure 5. Insertion Loss vs. Temp (RFC–RFX)

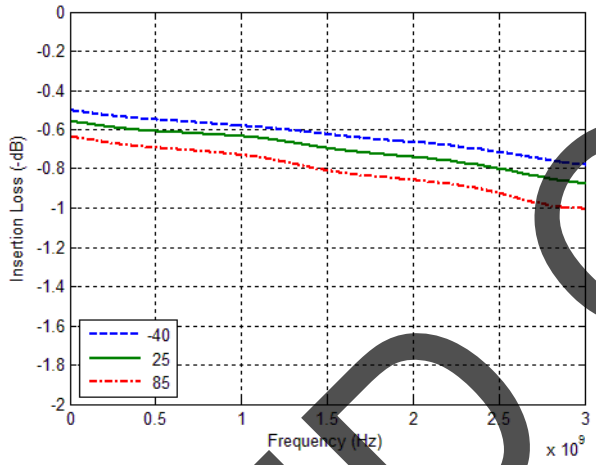


Figure 6. Insertion Loss vs. V_{DD} (RFC–RFX)

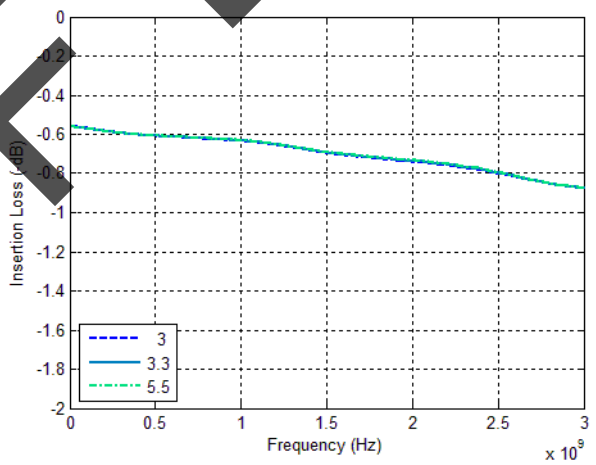


Figure 7. RFC Port Return Loss vs. Temp (RF1 Active)

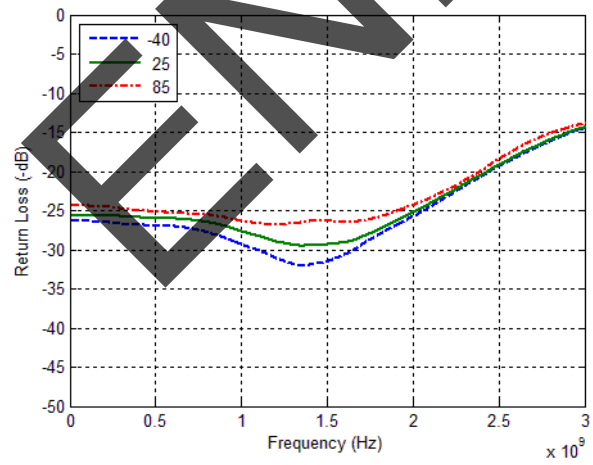
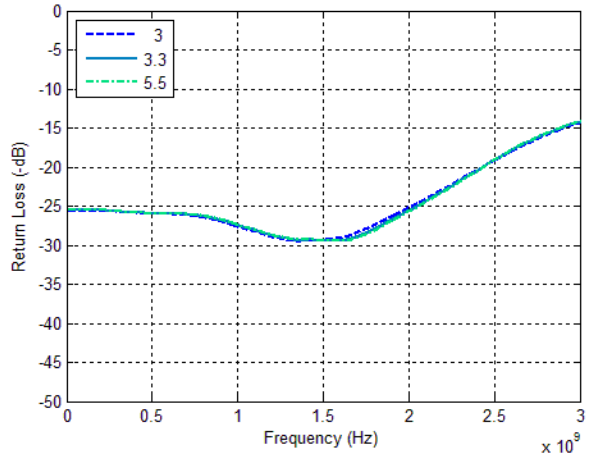


Figure 8. RFC Port Return Loss vs. V_{DD} (RF1 Active)



Typical Performance Data @ 25°C and V_{DD} = 3.0V unless otherwise specified

Figure 9. RFC Port Return Loss vs. Temp (RF2 Active)

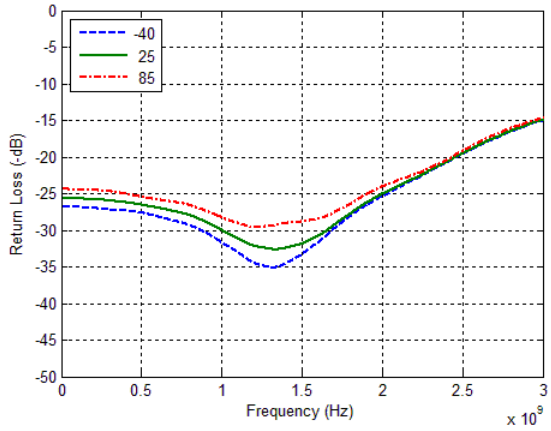


Figure 10. RFC Port Return Loss vs. V_{DD} (RF2 Active)

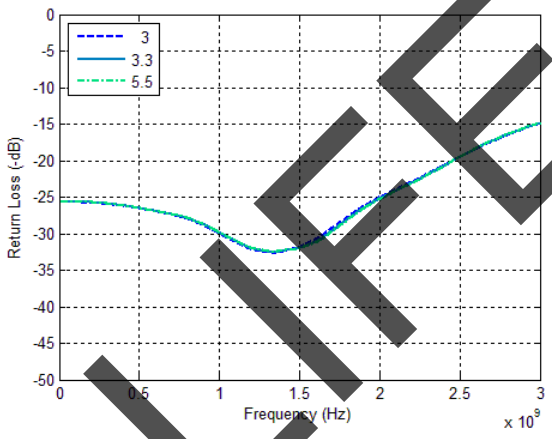


Figure 11. Active Port Return Loss vs. Temp (RF1 Active)

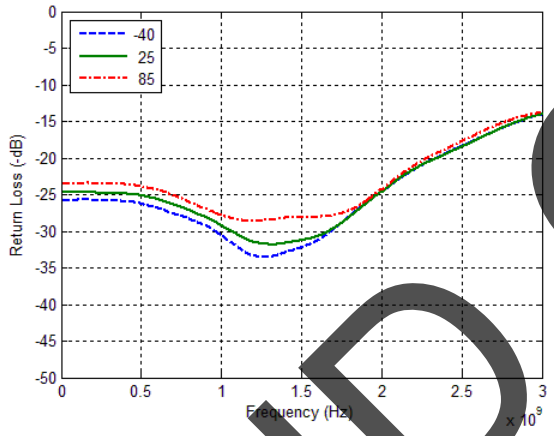


Figure 12. Active Port Return Loss vs. V_{DD} (RF1 Active)

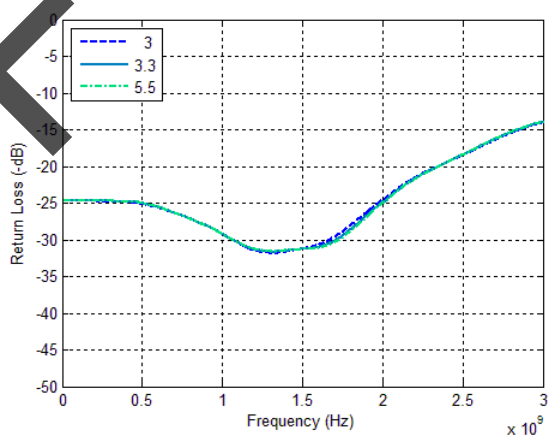


Figure 13. Active Port Return Loss vs. Temp (RF2 Active)

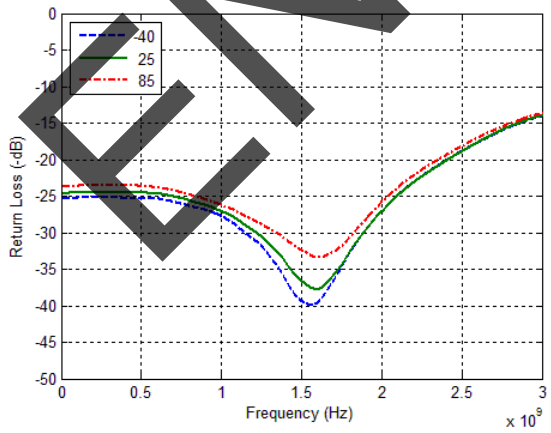
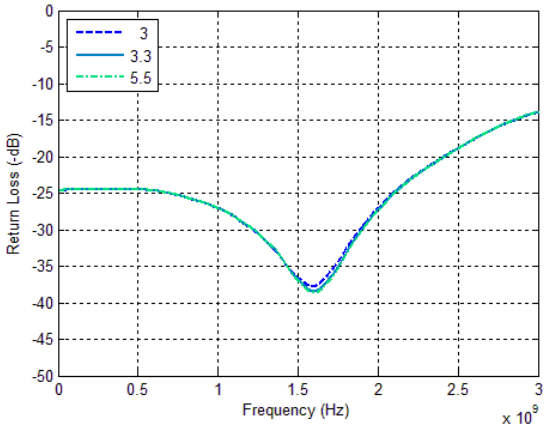


Figure 14. Active Port Return Loss vs. V_{DD} (RF2 Active)



Typical Performance Data @ 25°C and V_{DD} = 3.0V unless otherwise specified

Figure 15. Isolation vs. Temp (RFX–RFX)

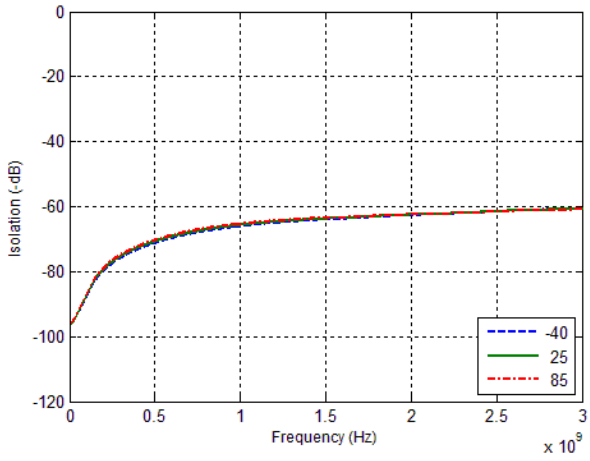


Figure 16. Isolation vs. V_{DD} (RFX–RFX)

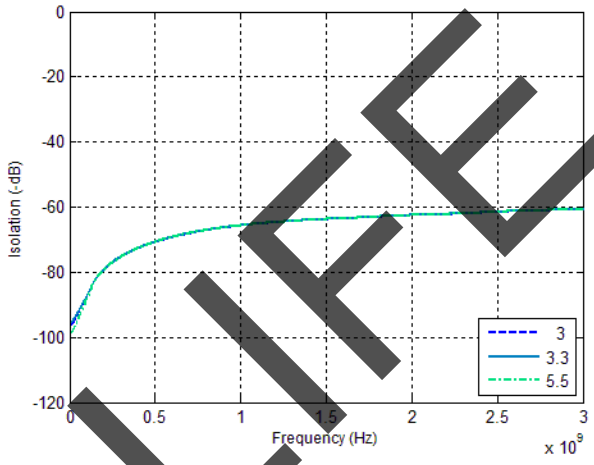


Figure 17. Isolation vs. Temp (RFC–RFX)

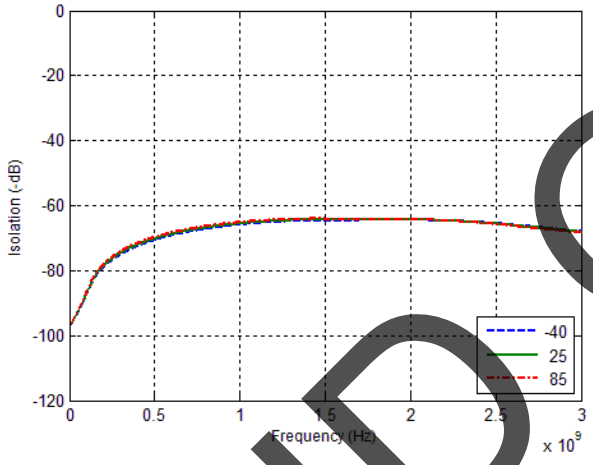
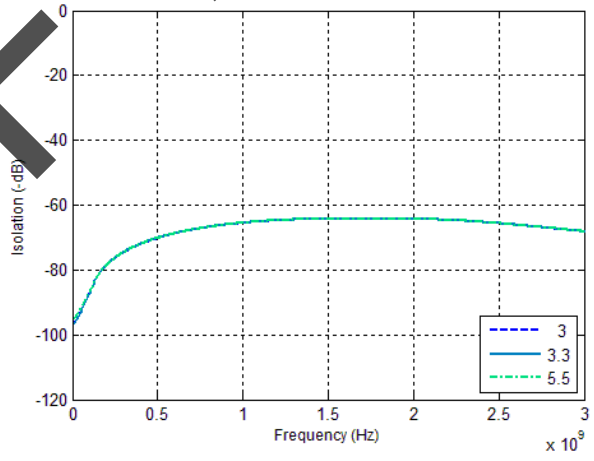


Figure 18. Isolation vs. V_{DD} (RFC–RFX)



Evaluation Kit

The SPDT switch evaluation board was designed to ease customer evaluation of Peregrine's PE42720. The RF common port is connected through a 75Ω transmission line via the F-Type connector, J2. RF1 and RF2 ports are connected through 75Ω transmission lines via F-Type connectors J1 and J3, respectively. A 75Ω through transmission line is available via F-Type connectors J4 and J5, which can be used to de-embed the loss of the PCB. J6 provides DC and digital inputs to the device.

The board is constructed of a four metal layer material with a total thickness of 60 mils. To achieve high isolation, the 75Ω transmission lines are designed in layer 2 using a stripline waveguide design. The board stack up for 75Ω transmission lines has 20 mil thickness of Rogers 4350B between layer 1 and layer 2, 20 mil thickness of Rogers 4450F between layer 2 and layer 3, and 13.3 mil thickness of Rogers 4350B between layer 3 and layer 4.

For the true performance of the PE42720 to be realized, the PCB should be designed in such a way that RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

Figure 19. Evaluation Board Layout

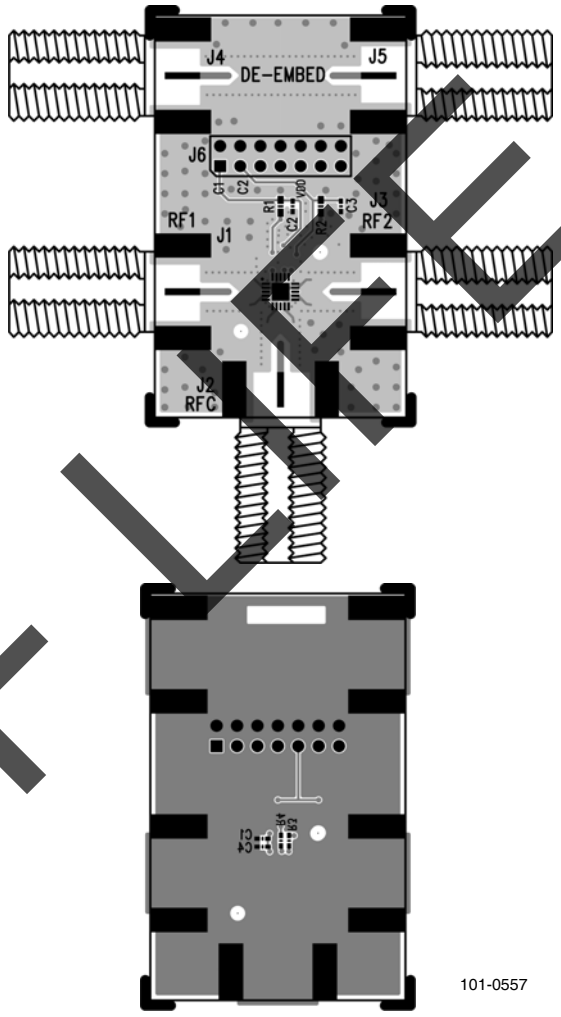


Figure 20. Evaluation Board Schematic

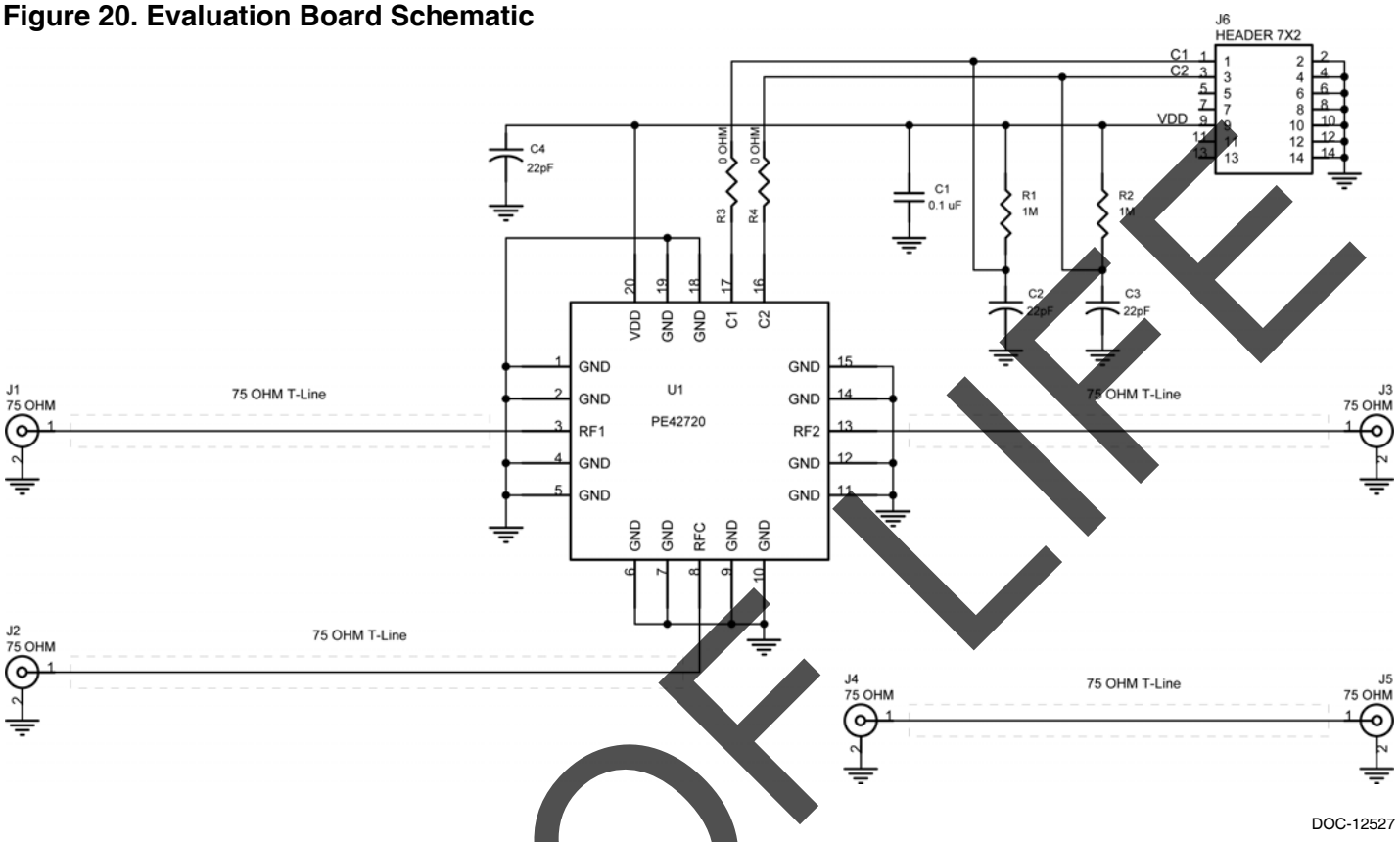


Figure 21. Package Drawing
20-lead 4x4 mm LGA

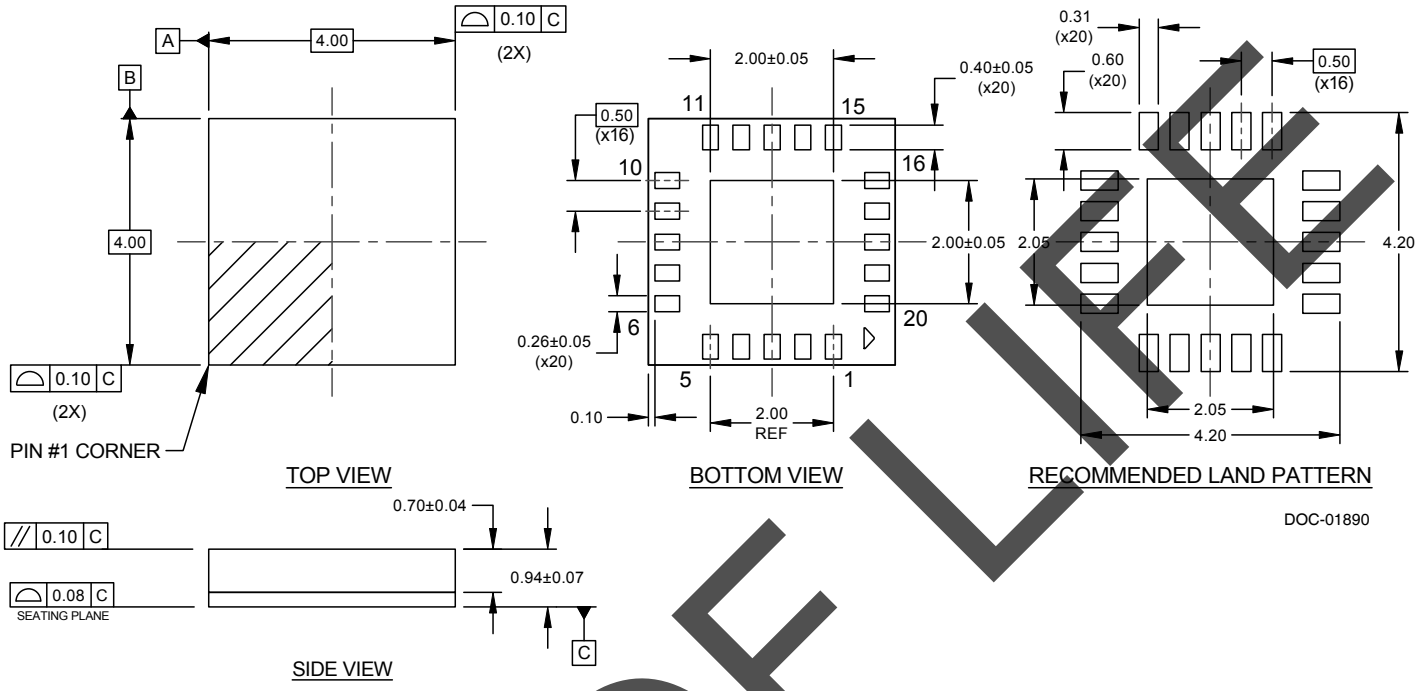
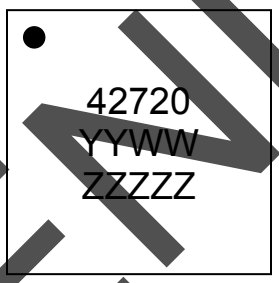
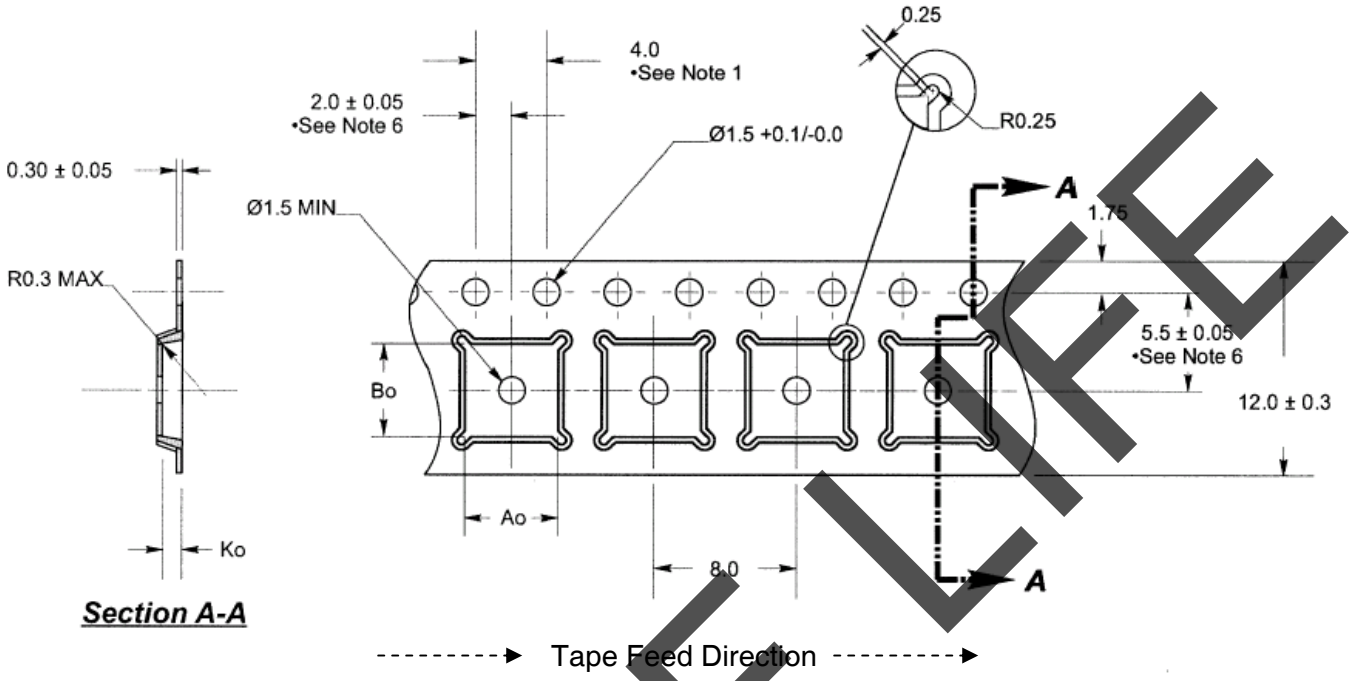


Figure 22. Top Marking Specifications



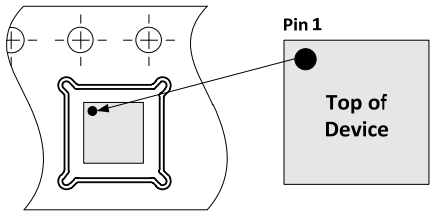
● = Pin 1 designator
YYWW = Date Code
ZZZZZ = Last five digits of Lot Number

Figure 23. Tape and Reel Drawing



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.02
2. Camber not to exceed 1 mm in 100 mm
3. Material: PS + C
4. Ao and Bo measured as indicated
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Ao = 4.35 mm
Bo = 4.35 mm
Ko = 1.1 mm



Device Orientation in Tape

Table 6. Ordering Information

Order Code	Description	Package	Shipping Method
PE42720LGBB-Z	PE42720 SPDT RF switch	Green 20-lead 4x4 mm LGA	3000 units/T&R
EK42720-02	PE42720 Evaluation kit	Evaluation kit	1/Box

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