

Description

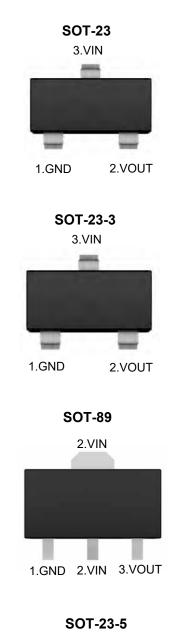
The PJ73 series is a set of three-terminal low power high voltage regulators implemented in CMOS technology. They allow input voltages as high as 20V. They are available with several fixed output voltages ranging from 2.1V to 9.0V. Because of the low power dissipation, PJ73 series are widely used in a variety of equipment such as audio device, video device, communication device and so on.

Features

- Low power consumption
- Low voltage drop
- Low temperature coefficient
- ♦ High input voltage (up to 20V)
- Quiescent current : 1.5µA
- Output voltage tolerance: ±2%

Applications

- Battery-Powered Equipment
- Ultra Low Power Microcontrollers
- Notebook Computers







Marking Code Note

Output Voltage	Package	Marking
2.1V~9V	SOT-23	73XX
2.1V~9V	SOT-23-3	73XXC
2.1V~9V	SOT-23-5	73XXE
2.1V~9V	SOT-89	73XX

Note: XX: Output Voltage

Ordering Information

PJ73- PJ73- Package Type SA : SOT-23 SC : SOT-23-3 SQ : SOT-89 SE : SOT-23-5 Output Voltage 21 : 2.1V 23 : 2.3V 25 : 2.5V 28 : 2.8V 30 : 3V 33 : 3.3V 36 : 3.6V 40 : 4V 44 : 4.4V 50 : 5V 90 : 9V Output current tap L: 300mA Revision:A



Absolute Maximum Ratings Note1

Ratings at 25°C ambient temperature unless otherwise specified.

Supply Voltage		-0.3~+22	V
	SOT-23	300	mW
	SOT-23-3	400	mW
Power Dissipation	SOT-23-5	400	mW
	SOT-89	600	mW
	SOT-23	330	°C/W
	SOT-23-3	380	°C/W
Thermal Resistance, Junction-to-Ambient	SOT-23-5	300	°C/W
	SOT-89	180	°C/W
Storage temperature range		-50~125	°C
Operating Ambient Temperature		-40~85	°C

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.



Electrical Characteristics

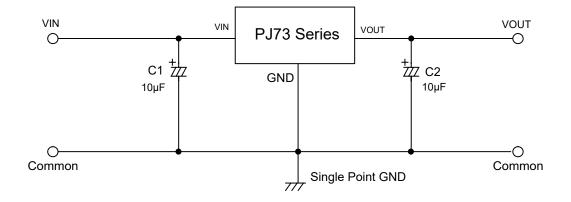
(V_{IN}=V_{OUT}+2, C_{IN}=C_{OUT}=10 μ F, T_A=25°C , unless otherwise noted.)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Voltage	V _{IN}				20	V
Output Voltage Accuracy	ΔV_{OUT}	I _{OUT} =10mA	-2		+2	%
Output Current	Ιουτ		300			mA
Quiescent Current	Ιq	I _{OUT} =0mA		1.5	3	μA
		2.1V≤V _{OUT} <2.3V		45	55	
Dropout Voltage Note1	V _{DROP}	2.3V≤V _{OUT} <2.5V		40	55	
I _{OUT} =10mA	♥ DROP	2.5V≤V _{OUT} <2.8V		35	55	
		2.8V≤V _{OUT} <3.0V		30	55	
		3.0V≤V _{OUT} <3.3V		210	300	mV
	V _{DROP}	3.3V≤V _{OUT} <3.6V		195	300	
Dropout Voltage Note1		3.6V≤V _{OUT} <4.0V		180	300	
Dropout Voltage ^{Note1} I _{OUT} =100mA		4.0V≤V _{OUT} <4.4V		170	300	
		4.4V≤V _{OUT} <5.0V		160	300	
		5.0V≤V _{OUT} <9.0V		150	300	
		9.0V≤V _{OUT}		130	300	
Line Regulation	ΔV_{LINE}	V _{IN} =V _{OUT} +2~20V I _{OUT} =1mA			0.2	%/V
Load Regulation	ΔV_{LOAD}	1mA <i<sub>OUT<300mA</i<sub>		37	100	mV
Power Supply Rejection Rate	PSRR	V _{IN} =V _{OUT} +3V,I _{OUT} =10mA f=100Hz		54		dB
Short current	I _{SHORT}	V _{OUT} =0V		400		mA
Temperature Coefficient	ΔVουτ/Vουτ χΔΤα	$V_{IN}=V_{OUT}+2V,I_{OUT}=10mA$ -40°C≤T _A ≤85°C		100		°C

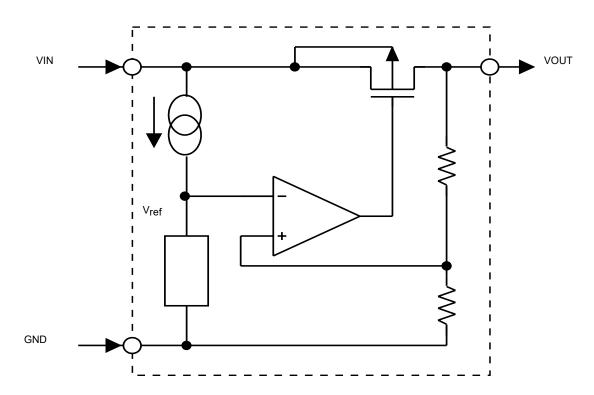
Note 1. The dropout voltage is defined as $V_{IN} - V_{OUT}$, when V_{OUT} is 98% of the normal value of V_{OUT} .



Basic Circuits



Block Diagram





Applications Information

Input Capacitor

A 1µF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended minimum output capacitance is 1µF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to VOUT and GND pins.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

 $PD(MAX) = (TJ(MAX) - TA) / R\theta JA$

Where TJ(MAX) is the maximum operation junction temperature 125°C, TA is the ambient temperature and the R θ JA is the junction to ambient thermal resistance.

The power dissipation definition in device is:

 $PD = (VIN - VOUT) \times IOUT + VIN \times IQ$

Layout Consideration

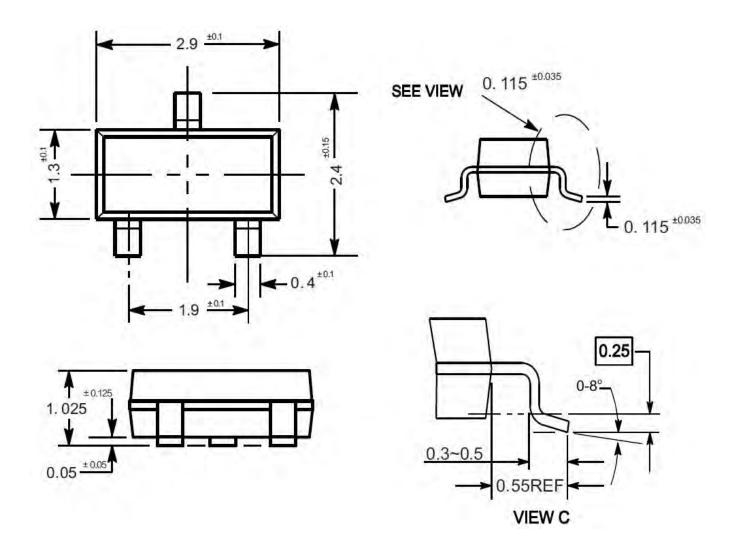
By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the ground pin using as wide and as short of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.



PJ73 Series Low Dropout Linear Regulator

Package Outline SOT-23

Dimensions in mm

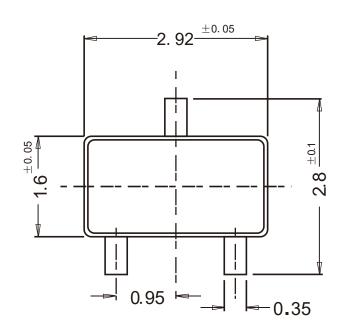


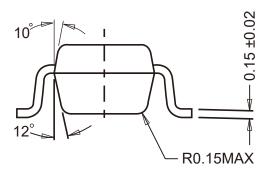
Device	Package	Shipping
PJ73 Series	SOT-23	3,000/ Tape & Reel (7 inches)

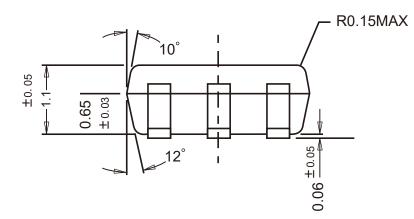


PJ73 Series Low Dropout Linear Regulator

Package Outline SOT-23-3 Dimensions in mm





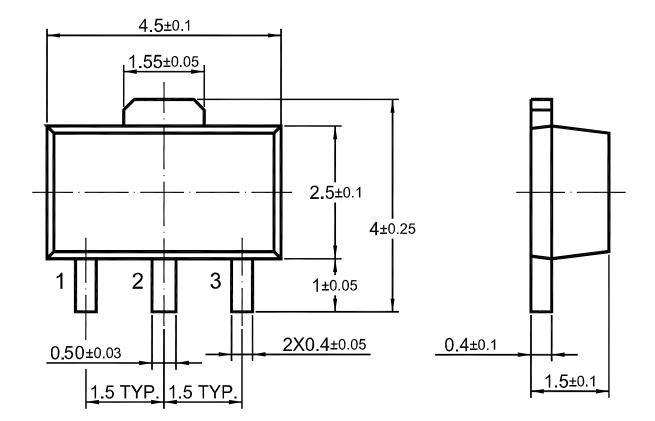


Device	Package	Shipping
PJ73 Series	SOT-23-3	3,000/ Tape & Reel (7 inches)



Package Outline SOT-89

Dimensions in mm



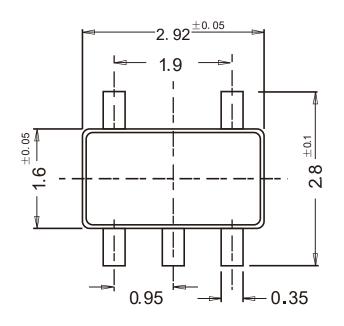
Device	Package	Shipping
PJ73 Series	SOT-89	1,000/ Tape & Reel (7 inches)

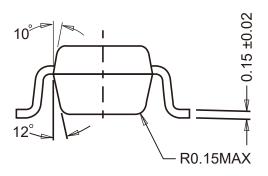


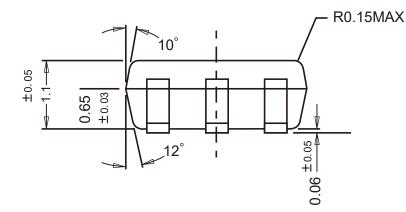
PJ73 Series Low Dropout Linear Regulator

Package Outline

SOT-23-5 Dimensions in mm







Device	Package	Shipping
PJ73 Series	SOT-23-5	3,000/ Tape & Reel (7 inches)

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