



## 40V N-Channel MOSFET

Lead Free Package and Finish

### General Features

- Proprietary New Trench Technology
- Ultra-low Miller Charge
- $R_{DS(ON),typ.} = 1.3\ m\ \Omega @ V_{GS} = 10V$
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

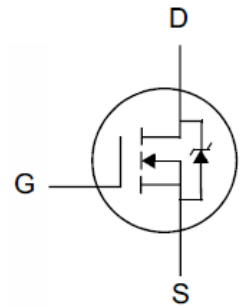
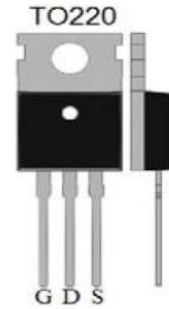
$BV_{DSS}$	$R_{DS(ON),typ.}$	$I_D^{[2]}$
40V	1.3m $\Omega$	345A

### Applications

- High efficiency DC/DC Converters
- Synchronous Rectification
- Motor Drive

### Ordering Information

Part Number	Package	Brand
PTP01N04N	TO-220	



### Absolute Maximum Ratings

$T_C = 25^\circ C$  unless otherwise specified

Symbol	Parameter	PTP01N04N	Unit
$V_{DSS}$	Drain-to-Source Voltage <sup>[1]</sup>	40	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 20$	
$I_D$	Continuous Drain Current <sup>[2]</sup> $V_{GS} @ 10V$	345	A
	Continuous Drain Current <sup>[3]</sup> $V_{GS} @ 10V$	196	
	Continuous Drain Current <sup>[2]</sup> $T_C = 100^\circ C, V_{GS} @ 10V$	244	
$I_{DM}$	Pulsed Drain Current at $V_{GS} = 10V^{[2,4]}$	1380	
$E_{AS}$	Single Pulse Avalanche Energy (L=1Mh,	2000	mJ
dv/dt	Peak Diode Recovery dv/dt <sup>[3]</sup>	5.0	V/ns
$P_D$	Power Dissipation	375	W
	Derating Factor above 25 $^\circ C$	2.5	W/ $^\circ C$
$T_L$ $T_{PAK}$	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	$^\circ C$
$T_J$ & $T_{STG}$	Operating and Storage Temperature Range	-55 to 175	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

### Thermal Characteristics Maximum Ratings

Symbol	Parameter	PTP01N04N	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.4	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	



## Electrical Characteristics

### OFF Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	40	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	1	$\mu A$	$V_{DS}=40V, V_{GS}=0V$
		--	--	100		$V_{DS}=32V, V_{GS}=0V, T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Leakage Current	--	--	+100	$nA$	$V_{GS}=+20V, V_{DS}=0V$
		--	--	-100		$V_{GS}=-20V, V_{DS}=0V$

### ON Characteristics

$T_J = 25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	1.3	1.5	$m\Omega$	$V_{GS}=10V, I_D=196A$ [3]
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$

### Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	
$C_{iss}$	Input Capacitance	--	10.8	--	$nF$	$V_{GS}=0V, V_{DS}=25V, f=1.0MHz$	
$C_{rss}$	Reverse Transfer Capacitance	--	0.9	--			
$C_{oss}$	Output Capacitance	--	1.6	--			
$R_G$	Gate Series Resistance	--	2.0	--	$\Omega$	$f=1.0MHz$	
$Q_g$	Total Gate Charge	--	148	--	$nC$	$V_{GS}=0 \text{ to } 10V$ $V_{DD}=20V, I_D=185A,$	
		--	88	--			
$Q_{gs}$	Gate-to-Source Charge	--	35	--			$V_{GS}=4.5V$
$Q_{gd}$	Gate-to-Drain (Miller) Charge	--	42	--			

### Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	29	--	$nS$	$V_{DD}=26V, I_D=195A, V_{GS}=10V, R_G=2.1\Omega$
$t_{rise}$	Rise Time	--	30	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	145	--		
$t_{fall}$	Fall Time	--	43	--		

**Source-Drain Body Diode Characteristics** $T_J=25^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
$I_{SD}$	Continuous Source Current <sup>[2]</sup>	--	--	345	A	Integral PN-diode in MOSFET
$I_{SM}$	Pulsed Source Current <sup>[2]</sup>	--	--	1380		
$V_{SD}$	Diode Forward Voltage	--	--	1.3	V	$I_S=195\text{A}$ , $V_{GS}=0\text{V}$
trr	Reverse recovery time	--	81	--	nS	$V_R=34\text{V}$ , $V_{GS}=0\text{V}$ , $I_F=195\text{A}$ , $di_F/dt=100\text{A}/\mu\text{s}$
	Reverse recovery time, $T_J = 125^{\circ}\text{C}$	--	85	--		
Qrr	Reverse recovery charge	--	70	--	nC	
	Reverse recovery charge, $T_J = 125^{\circ}\text{C}$	--	83	--		
IRRM	Reverse Recovery Current	--	1.7	--	A	

**Note:**

- [1]  $T_J=+25^{\circ}\text{C}$  to  $+175^{\circ}\text{C}$  .  
[2] Silicon limited current only.  
[3] Package limited current.  
[4] Repetitive rating; pulse width limited by maximum junction temperature.  
[5] Pulse width $\leq 380\mu\text{s}$ ; duty cycles $\leq 2\%$ .



## Typical Characteristics

Figure 1. Maximum Transient Thermal Impedance

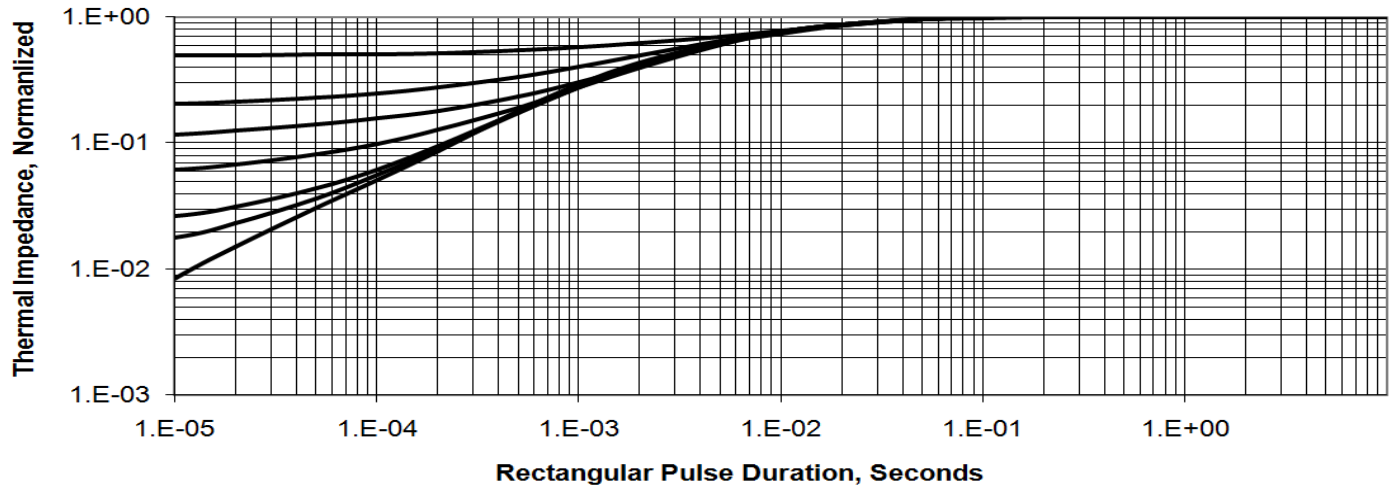


Figure 2. Maximum Power Dissipation vs Case Temperature

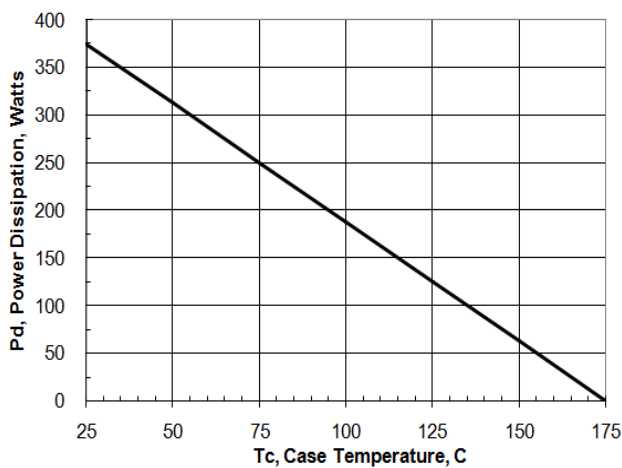


Figure 3. Maximum Continuous Drain Current vs Case Temperature

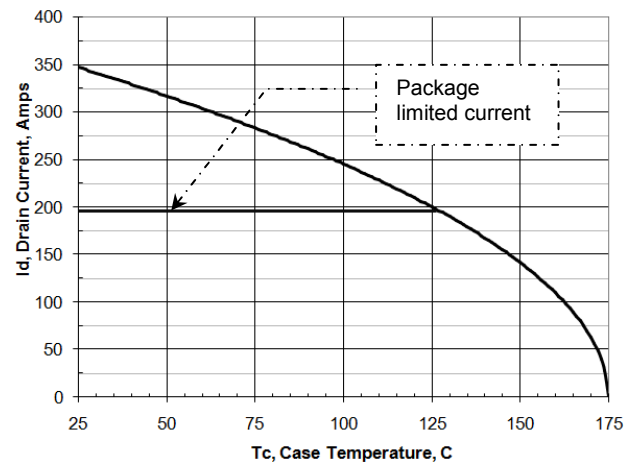


Figure 4. Typical Output Characteristics

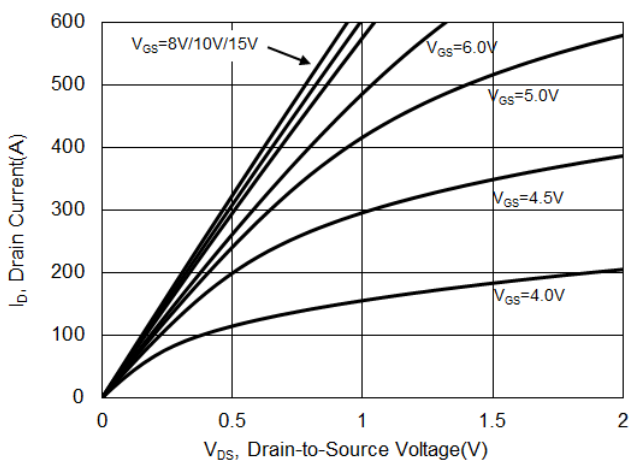
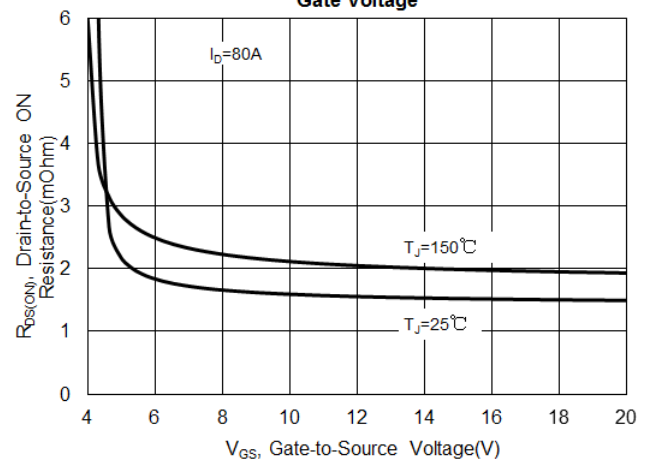


Figure 5. Typical Drain-to-Source ON Resistance vs. Gate Voltage





### Typical Characteristics(Cont.)

Figure 6. Peak Current Capability

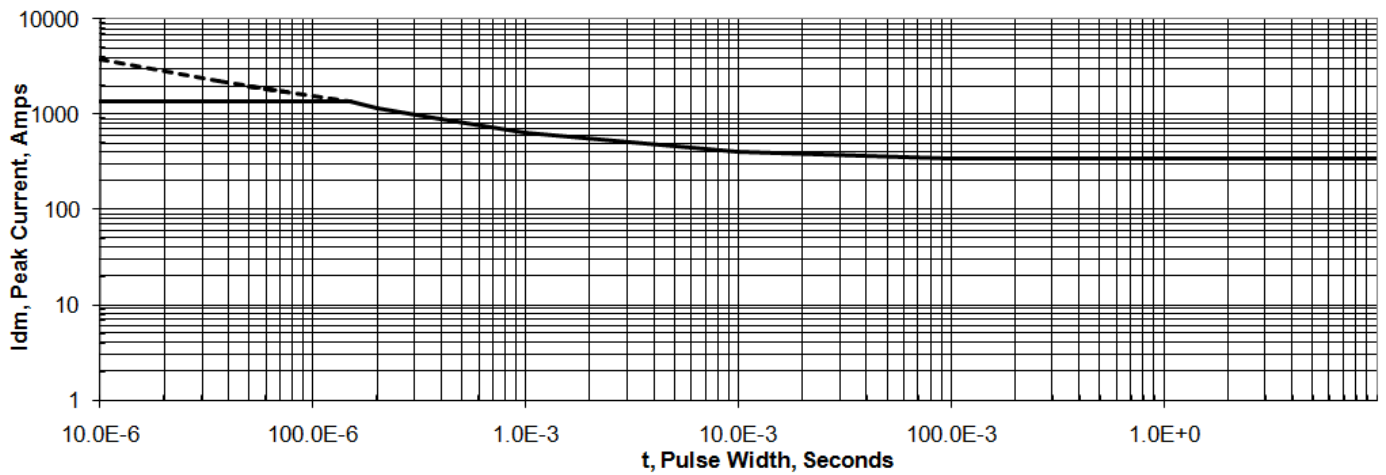


Figure 7. Typical Transfer Characteristics

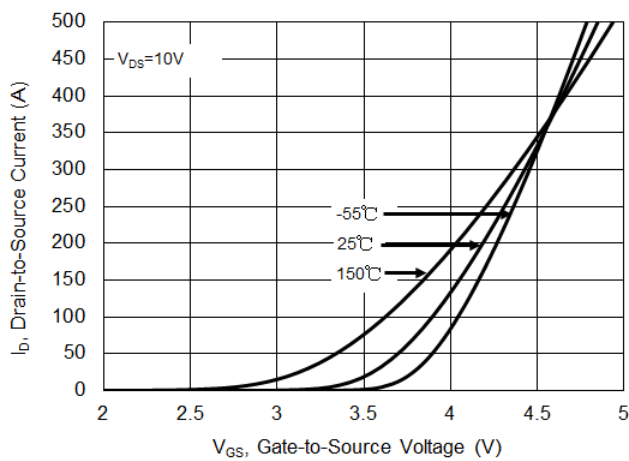


Figure 8. Unclamped Inductive Switching Capability

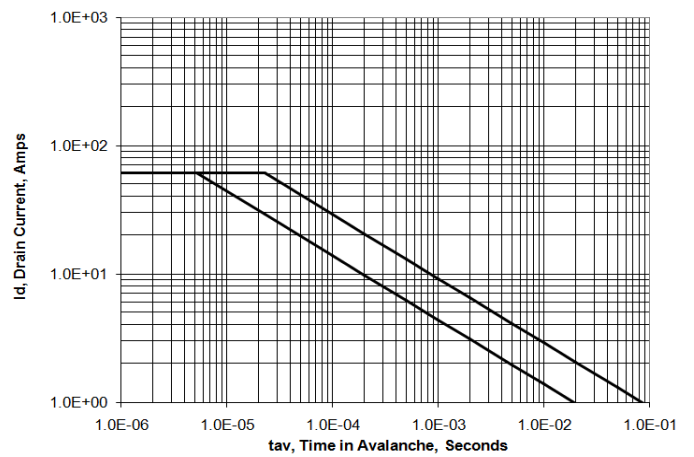


Figure 9. Typical Drain-to-Source ON Resistance

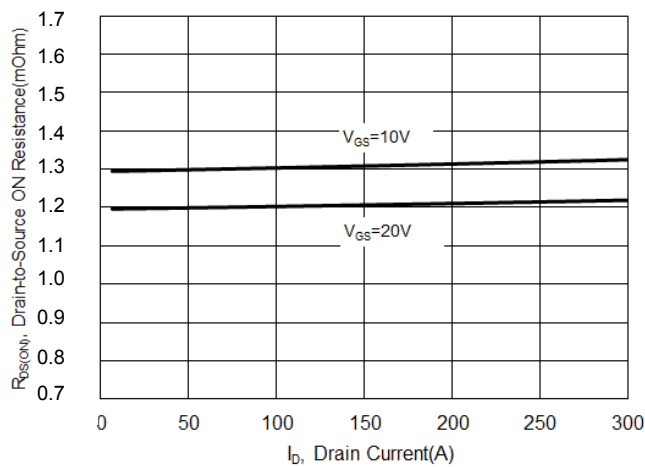
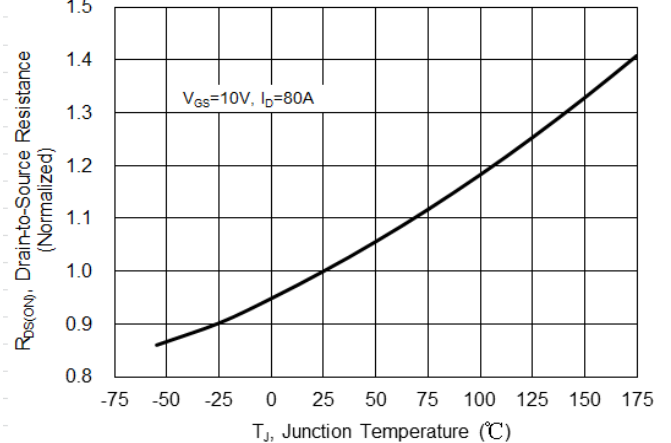


Figure 10. Typical Drain-to-Source On Resistance vs. Junction Temperature





### Typical Characteristics(Cont.)

Figure 11. Typical Breakdown Voltage vs. Junction Temperature

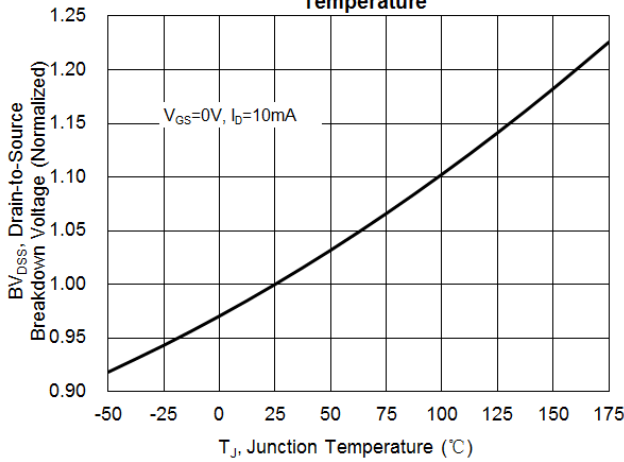


Figure 12. Typical Threshold Voltage vs. Junction Temperature

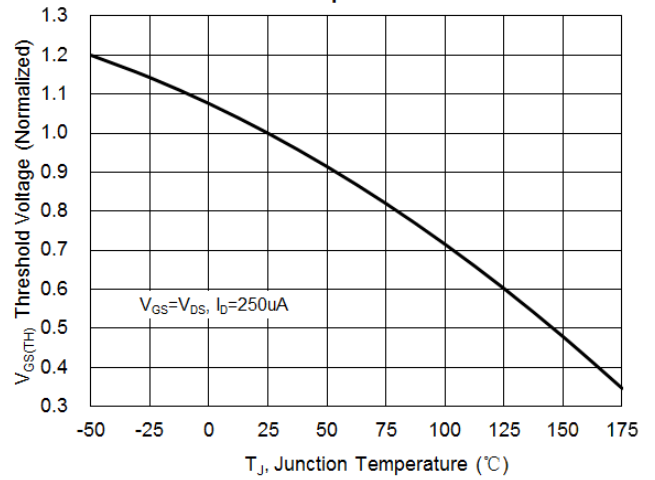


Figure 13 . Maximum Safe Operating Area

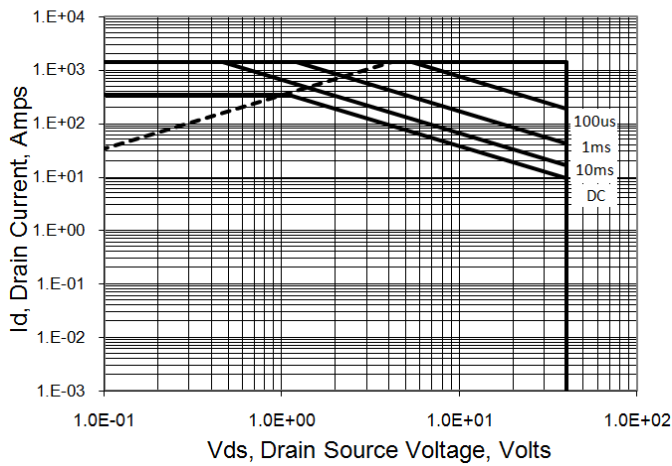


Figure 14. Capacitance vs Vds

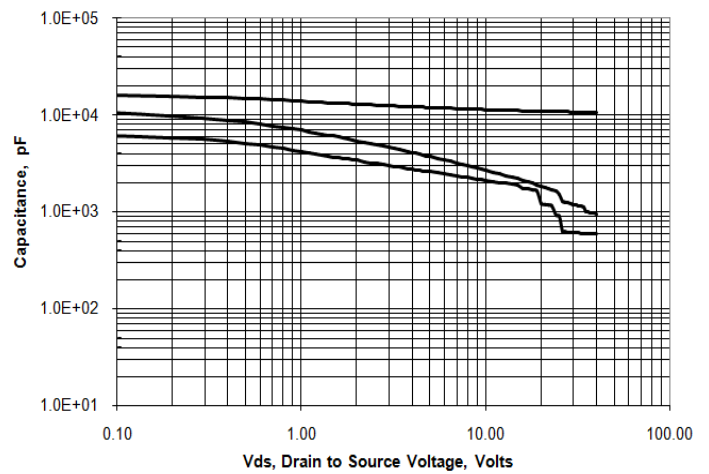


Figure 15 . Typical Gate Charge

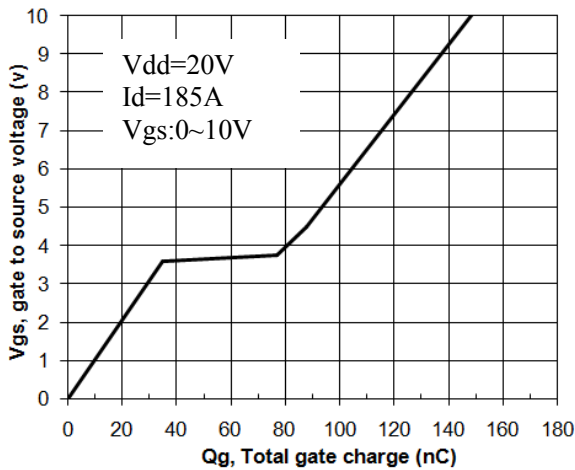
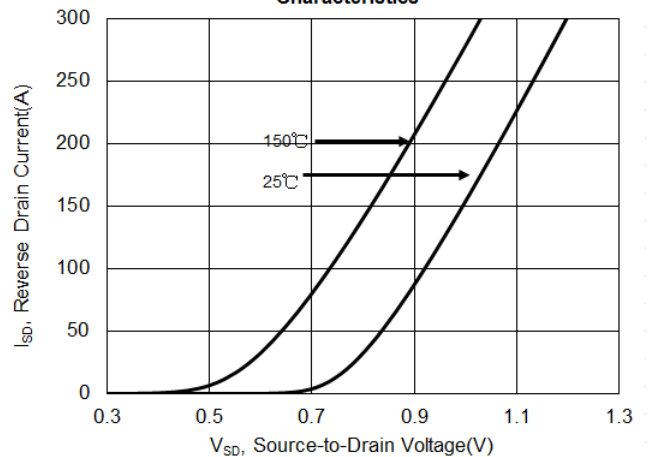


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuits and Waveforms

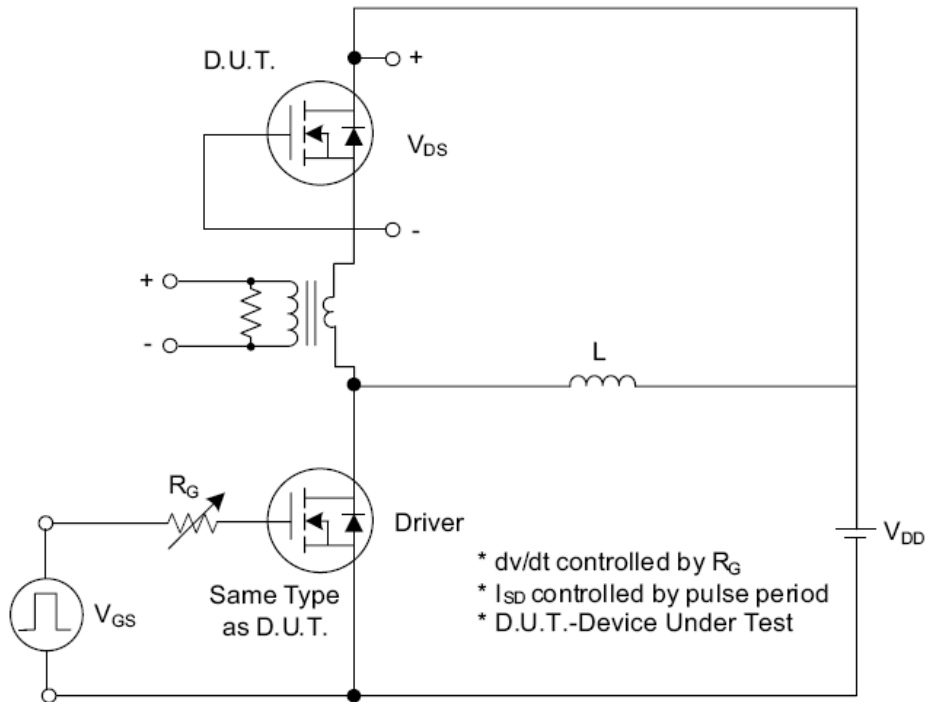


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

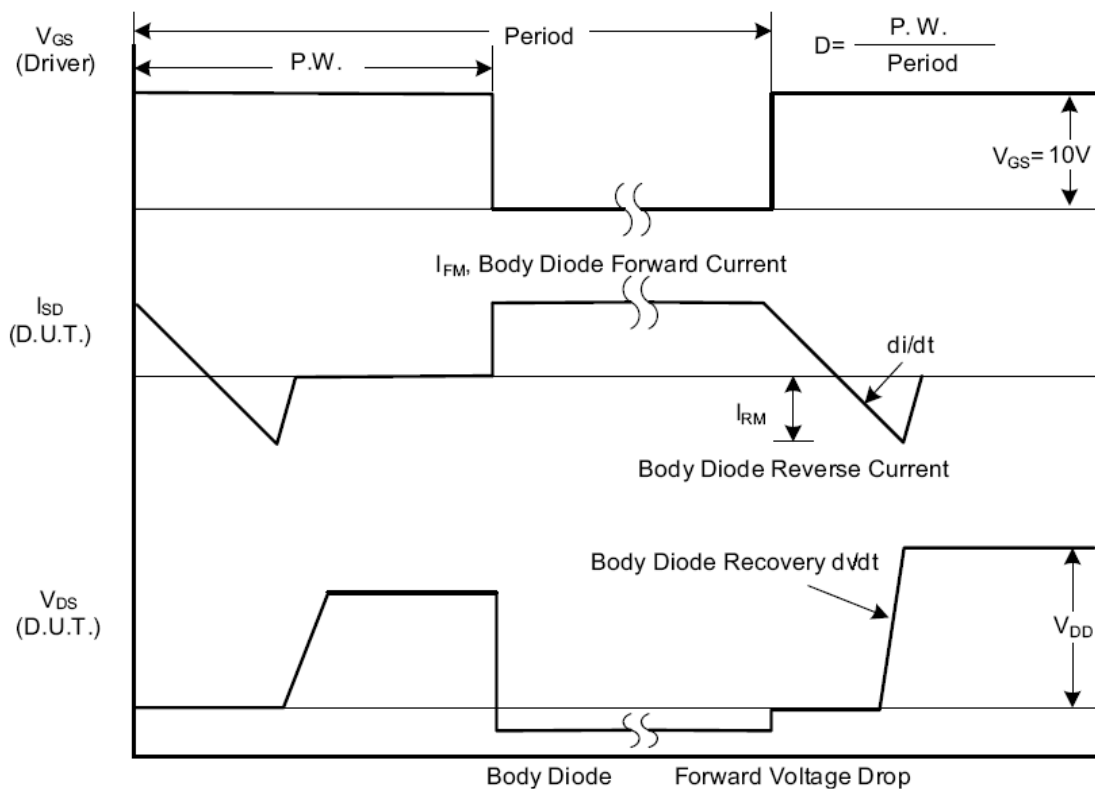


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

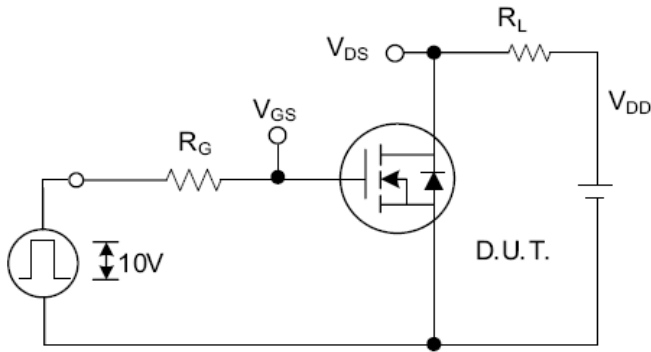


Fig. 2.1 Switching Test Circuit

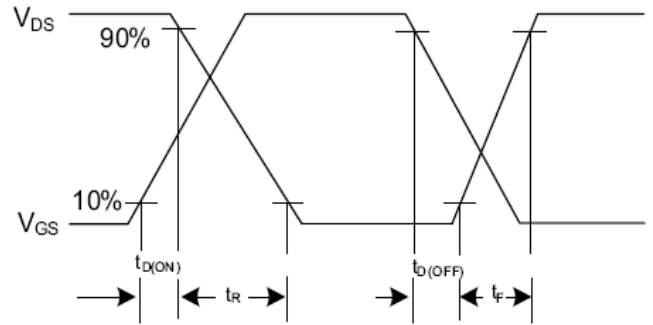


Fig. 2.2 Switching Waveforms

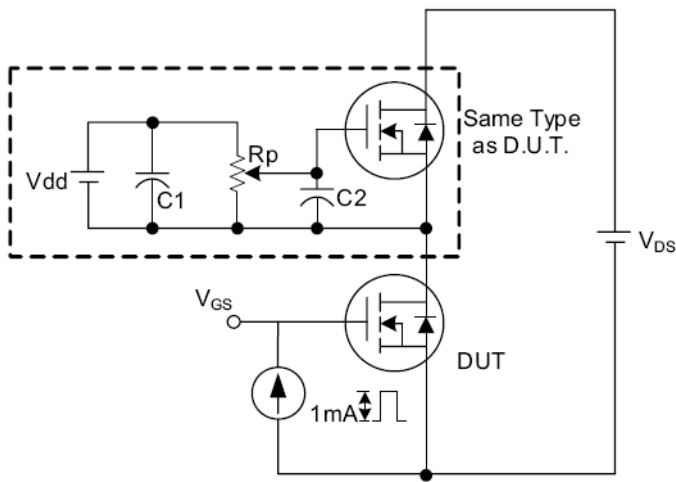


Fig. 3.1 Gate Charge Test Circuit

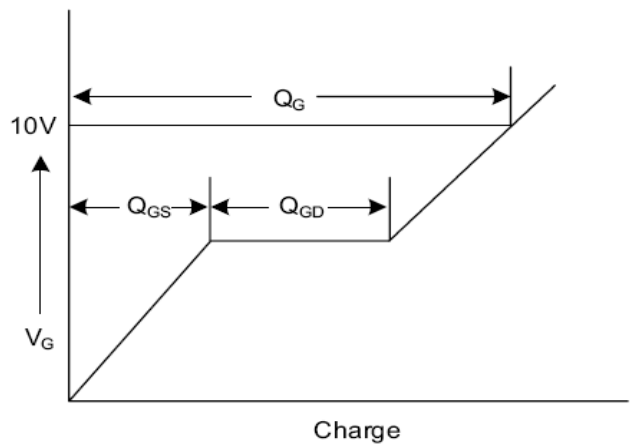


Fig. 3.2 Gate Charge Waveform

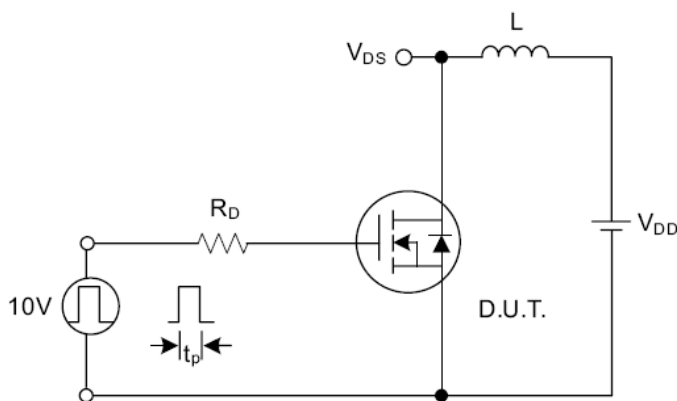


Fig. 4.1 Unclamped Inductive Switching Test Circuit

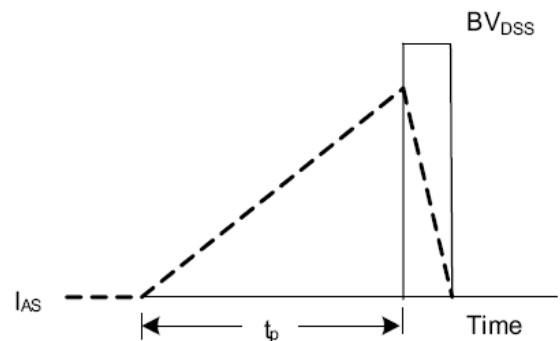


Fig. 4.2 Unclamped Inductive Switching Waveforms





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