500V N-Channel MOSFET

Lead Free Package and Finish

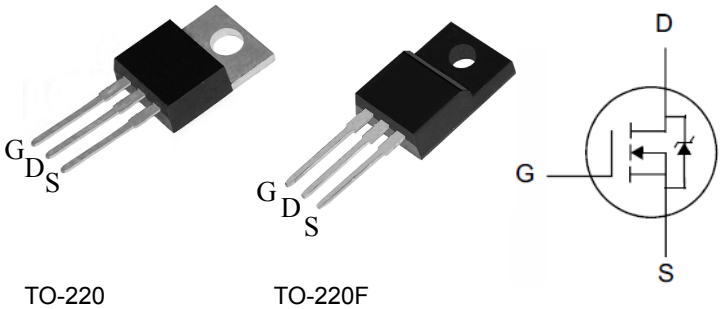
BV_{DSS}	$R_{DS(ON),typ.}$	I_D
500V	0.40Ω	13A

General Features

- Proprietary New Planar Technology
- $R_{DS(ON),typ.}$=0.40 Ω@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

Applications

- ATX Power
- LCD Panel Power



TO-220 TO-220F

Package Not to Scale

Ordering Information

Part Number	Package	Brand
PTP13N50B	TO-220	
PTA13N50B	TO-220F	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	PTP13N50B	PTA13N50B	Unit
V_{DSS}	Drain-to-Source Voltage[1]	500		V
V_{GSS}	Gate-to-Source Voltage	±30		
I_D	Continuous Drain Current	13		A
I_{DM}	Pulsed Drain Current at V_{GS}=10V[2]	48		
E_{AS}	Single Pulse Avalanche Energy	562		mJ
dv/dt	Peak Diode Recovery dv/dt[3]	5.0		V/ns
P_D	Power Dissipation	190	65	W
	Derating Factor above 25℃	1.52	0.52	W/℃
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260		℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150		

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	PTP13N50B	PTA13N50B	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.66	1.92	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	100	

Electrical Characteristics

OFF Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=500V, V_{GS}=0V
		--	--	100		V_{DS}=400V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+30V, V_{DS}=0V
		--	--	-100		V_{GS}=-30V, V_{DS}=0V

ON Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance[4]	--	0.40	0.50	Ω	V_{GS}=10V, I_D=6.0A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA
gfs	Forward Transconductance[4]	--	20	--	S	V_{DS}=20V,I_D=13A

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	1180	--	pF	V_{GS}=0V, V_{DS}=25V, f=1.0MH_Z
C_{rss}	Reverse Transfer Capacitance	--	13	--		
C_{oss}	Output Capacitance	--	120	--		
Q_g	Total Gate Charge	--	32	--	nC	V_{DD}=400V, I_D=13A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	7	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	16	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	21	--	nS	V_{DD}=250V, I_D=13A, V_{GS}= 10V R_G=25 Ω
t_{rise}	Rise Time	--	13	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	88	--		
t_{fall}	Fall Time	--	30	--		

Source-Drain Body Diode Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current[4]	--	--	13	A	Integral PN-diode in MOSFET
I_{SM}	Pulsed Source Current[4]	--	--	48		
V_{SD}	Diode Forward Voltage	--	--	1.4	V	I_S=13A, V_{GS}=0V
trr	Reverse recovery time	--	310	--	ns	V_{GS}=0V ,I_F=13A, di_F/dt=100A/μs
Qrr	Reverse recovery charge	--	4.0	--	uC	

Note:

[1] T_J=+25℃ to +150℃
[2] Repetitive rating; pulse width limited by maximum junction temperature.
[3] I_{SD}= 13A ,di/dt < 100 A/μs, V_{DD} < BV_{DSS}, T_J=+150℃.
[4] Pulse width≤380μs; duty cycle≤2%.

Typical Characteristics

Figure 1. Output Characteristics (T_J = 25ºC)

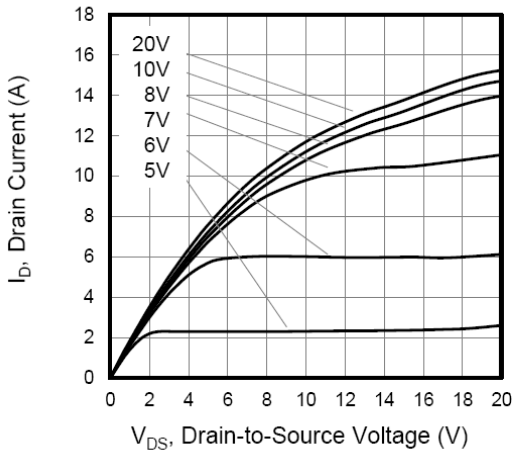


Figure 2. Body Diode Forward Voltage

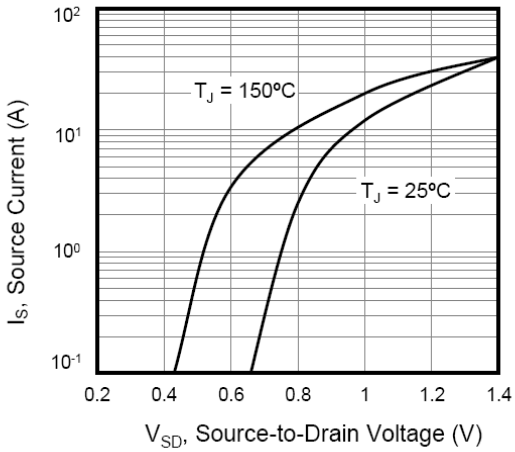


Figure 3. Drain Current vs. Temperature

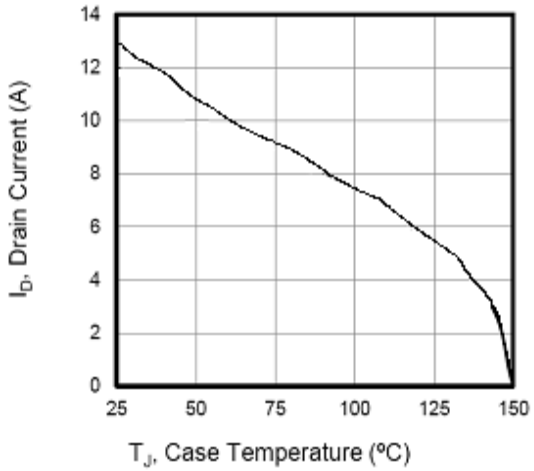


Figure 4. BV_{DSS} Variation vs. Temperature

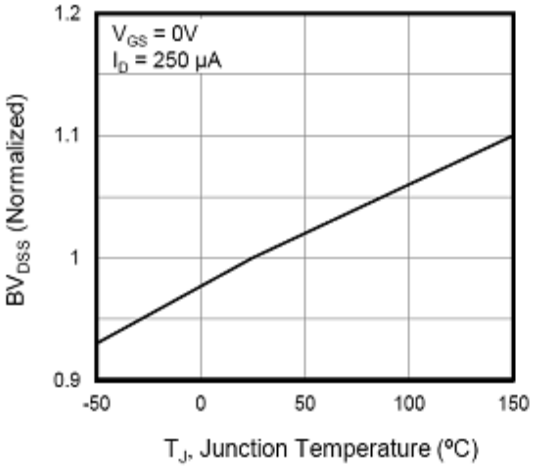


Figure 5. Transfer Characteristics

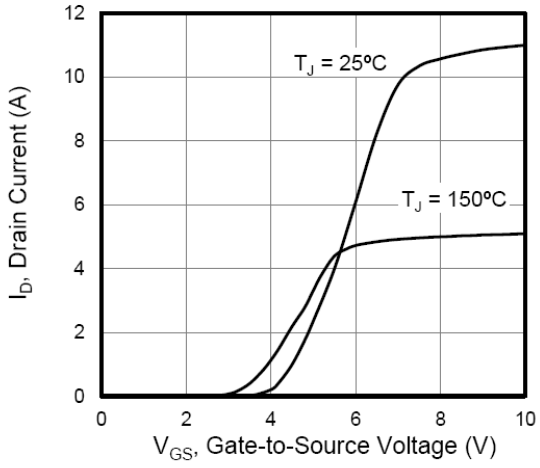
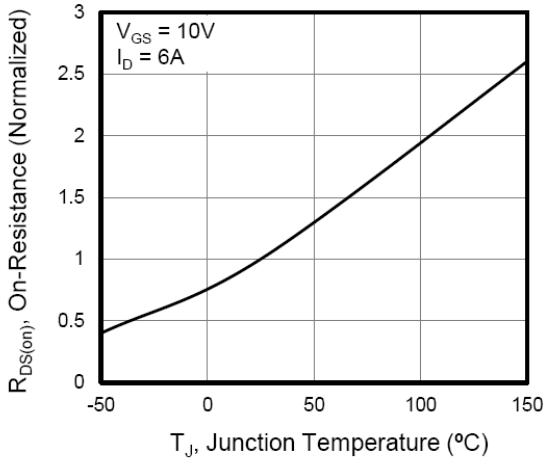


Figure 6. On-Resistance vs. Temperature



Typical Characteristics(Cont.)

Figure 7. Capacitance

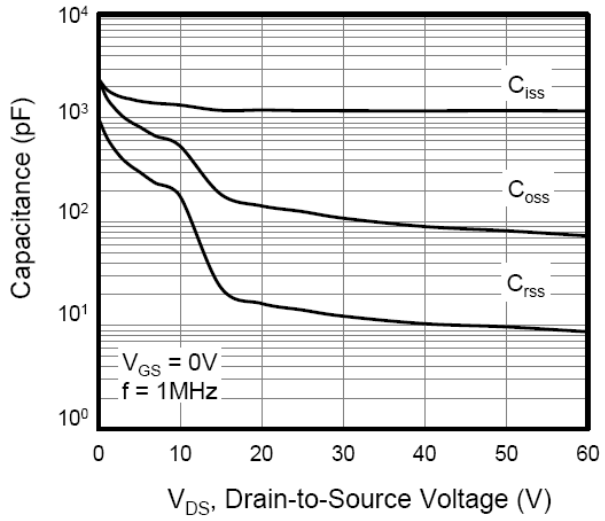


Figure 8. Gate Charge

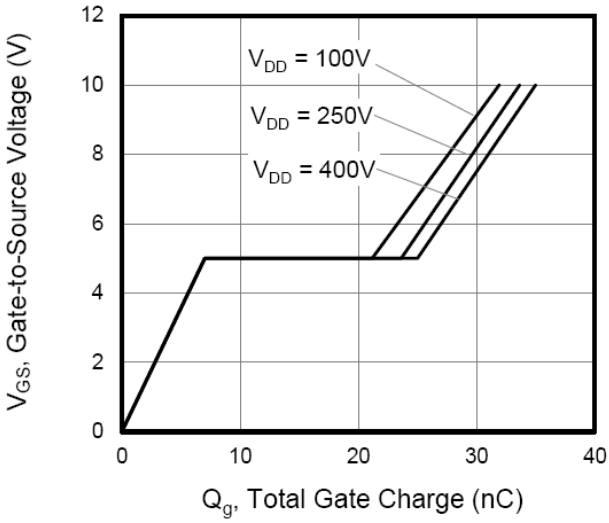
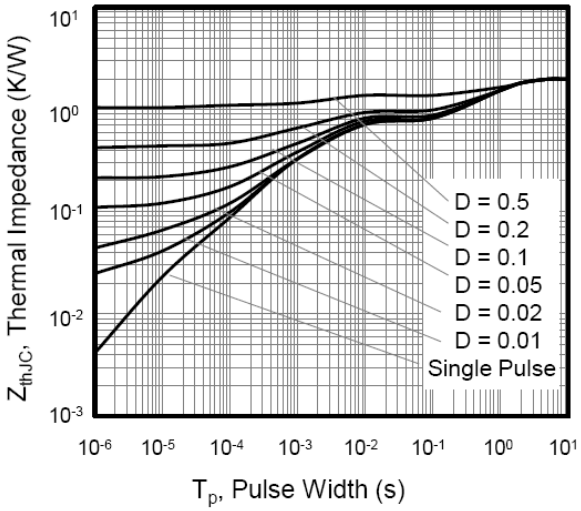


Figure 9. Transient Thermal Impedance



Test Circuits and Waveforms

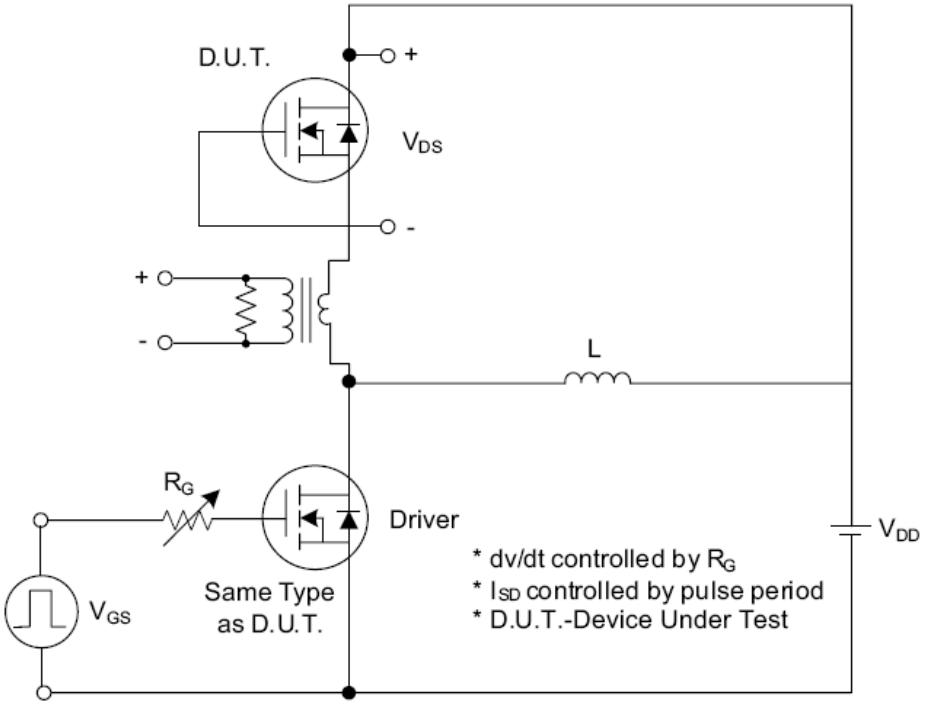


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

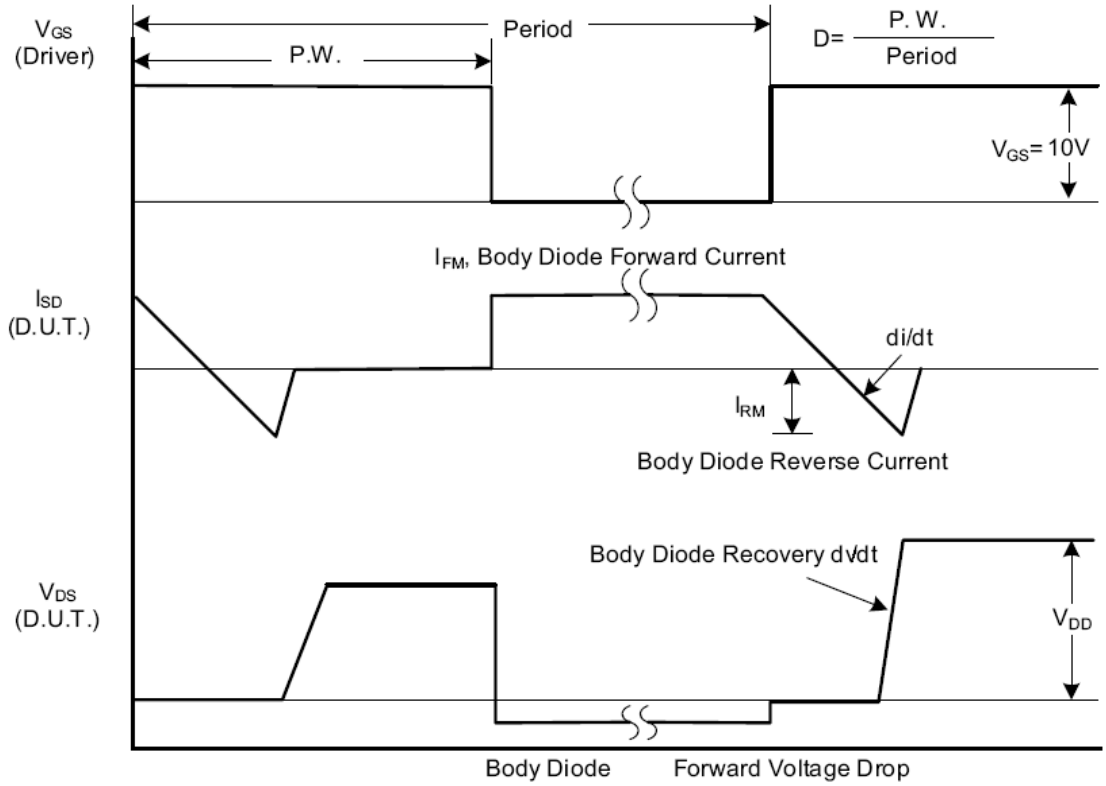


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

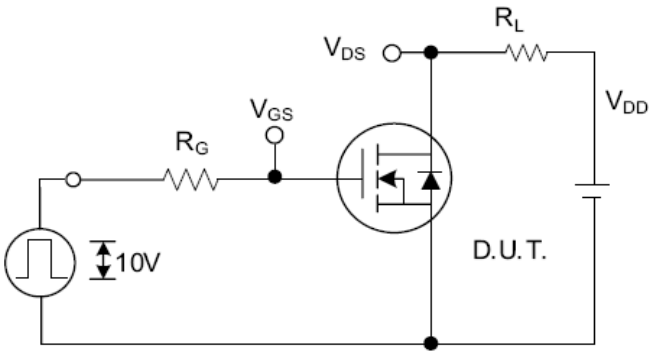


Fig. 2.1 Switching Test Circuit

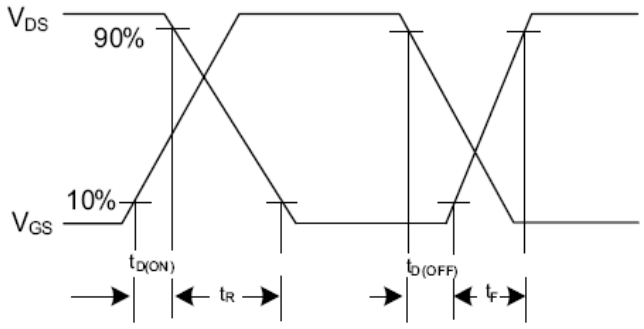


Fig. 2.2 Switching Waveforms

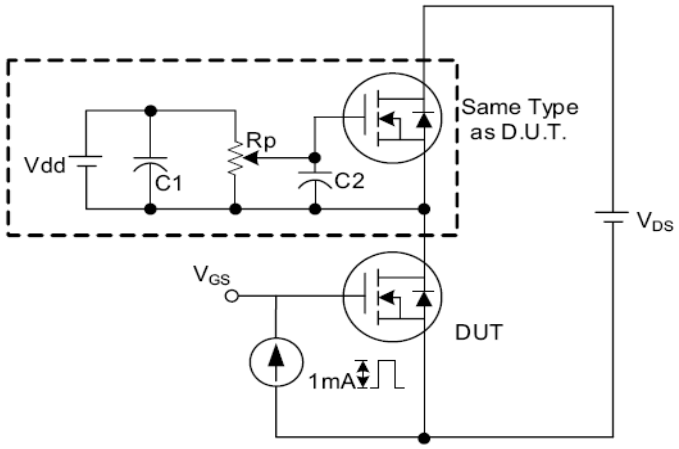


Fig. 3 . 1 Gate Charge Test Circuit

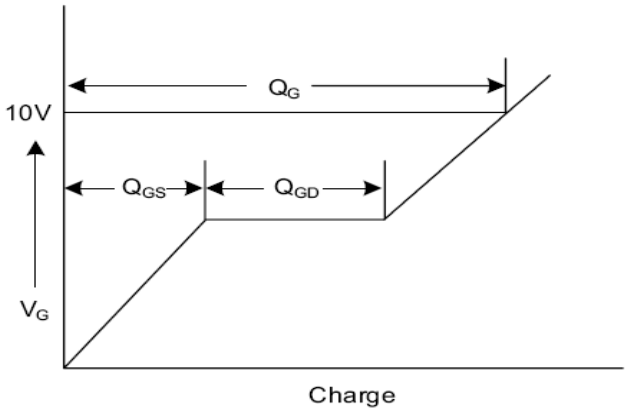


Fig. 3 . 2 Gate Charge Waveform

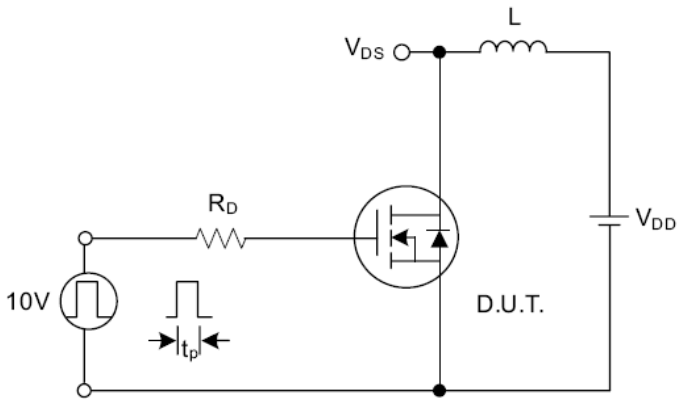


Fig. 4.1 Unclamped Inductive Switching Test Circuit

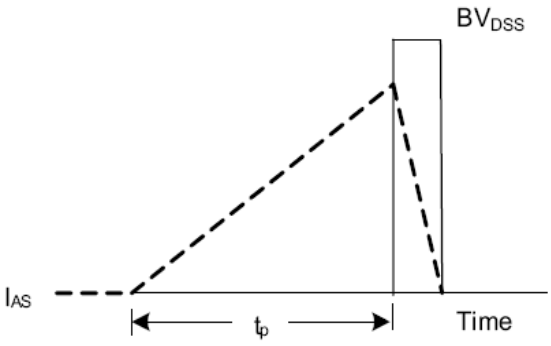


Fig. 4.2 Unclamped Inductive Switching Waveforms

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