

300V N-Channel MOSFET

General Features

- Advanced Planar Process
- > $R_{DS(ON),typ.}$ =35 m Ω @V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Rugged Poly silicon Gate Structure

Applications

- BLDC Motor Driver
- Electric Welder
- High Efficiency SMPS

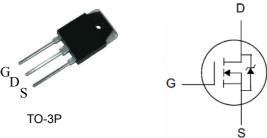
Ordering Information

Part Number	Package	Brand
PTW69N30	TO-3P	ž

Absolute Maximum Ratings

Lead Free Package and Finish

BV _{DSS}	R _{DS(ON),typ.}	I _D
300V	35mΩ	69A



Package Not to Scale

 $T_C {=} 25\,^\circ\!\mathrm{C}$ unless otherwise specified

Symbol	Parameter	PTW69N30	Unit	
V _{DSS}	Drain-to-Source Voltage	300	V	
V _{GSS}	Gate-to-Source Voltage	±30	V	
1	Continuous Drain Current	69		
I _D	Continuous Drain Current @ Tc=100℃	42	A	
I _{DM}	Pulsed Drain Current at V _{GS} =10V ^[2,4]	276		
E _{AS}	Single Pulse Avalanche Energy	5000	mJ	
dv/dt	Peak Diode Recovery dv/dt ^[3]	5.0	V/ns	
P _D	Power Dissipation	520	W	
T _L T _{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	°C	
T _J & T _{STG}	Operating and Storage Temperature Range	-55 to 150		

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	PTW69N30	Unit
$R_{ extsf{ heta}JC}$	Thermal Resistance, Junction-to-Case	0.24	10.111
R _{θJA}	Thermal Resistance, Junction-to-Ambient	50	°C /W

Electrical Characteristics

1

OFF Characteristics $T_J = 25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	300			V	V_{GS} =0V, I _D =250uA
				1		V _{DS} =300V, V _{GS} =0V
I _{DSS}	Drain-to-Source Leakage Current	-		125	uA	V _{DS} =240V, V _{GS} =0V, T _J =125℃
	Cate to Source Lookage Current			+100	-	V_{GS} =+30V, V_{DS} =0V
I _{GSS}	Gate-to-Source Leakage Current			-100	nA	V _{GS} =-30V, V _{DS} =0V

ON Characteristics

ON Characteristics				T_J =25 °C unless otherwise specified		
Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
R _{DS(ON)}	Static Drain-to-Source On-Resistance		35	49	mΩ	V _{GS} =10V, I _D =35A
V _{GS(TH)}	Gate Threshold Voltage	2.0		4.0	V	$V_{DS}=V_{GS}$, $I_D=250uA$
gfs	Forward Transconductance		55		S	VDS =15V, ID=30A

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
C _{iss}	Input Capacitance		7200		pF	V _{GS} =0V, V _{DS} =25V, f=1.0MH _Z
C _{rss}	Reverse Transfer Capacitance		130			
C _{oss}	Output Capacitance		850			
Q _g	Total Gate Charge		150		nC	V _{DD} =150V, I _D =69A, V _{GS} =0 to 10V
Q _{gs}	Gate-to-Source Charge		38			
Q_{gd}	Gate-to-Drain (Miller) Charge		60			

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
td(ON)	Turn-on Delay Time		55			
trise	Rise Time		120		nS	V _{DD} =150V, I _D =35A, V _{GS} = 10V RG=10Ω
td(OFF)	Turn-Off Delay Time		160			
tfall	Fall Time		70			

Source-Drain Body Diode Characteristics

 $T_J {=} 25\,^\circ\!\! \mathrm{C}$ unless otherwise specified

Symbol	Parameter	Min	Тур.	Max.	Unit	Test Conditions
I _{SD}	Continuous Source Current ^[2]			69	A	Integral PN-diode in MOSFET
I _{SM}	Pulsed Source Current ^[2]			276		
V _{SD}	Diode Forward Voltage			1.5	V	I _S =69A, V _{GS} =0V
trr	Reverse recovery time		500		ns	V _{GS} =0V ,IF=69A,
Qrr	Reverse recovery charge		4.5		uC	di⊧/dt=100A/µs

Note:

[1] T_J=+25℃ to +150℃.

[2] Silicon limited current only.[3] Package limited current.

[4] Repetitive rating; pulse width limited by maximum junction temperature.
[5] Pulse width≤380µs; duty cycle≤2%.

Typical Characteristics

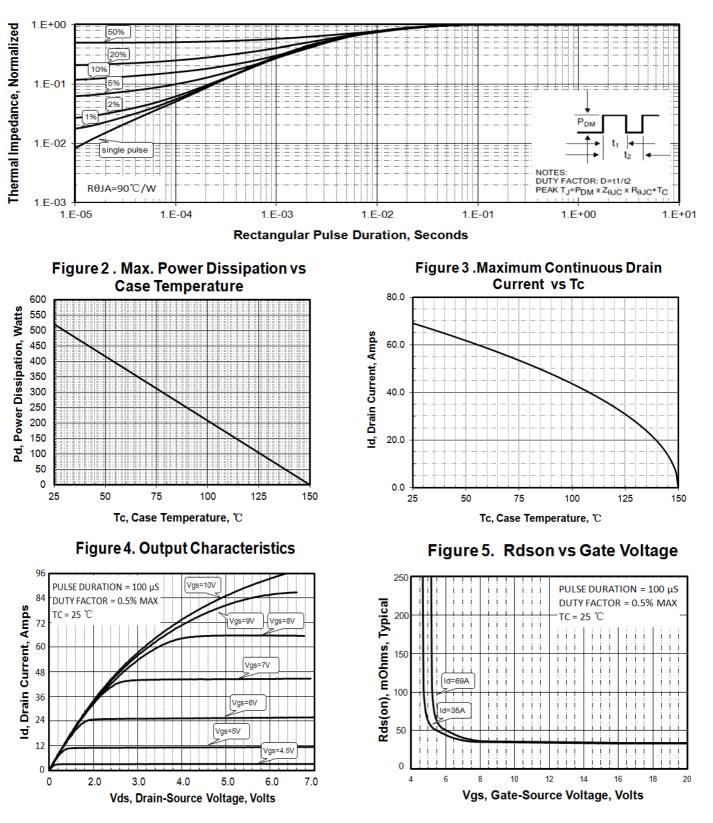
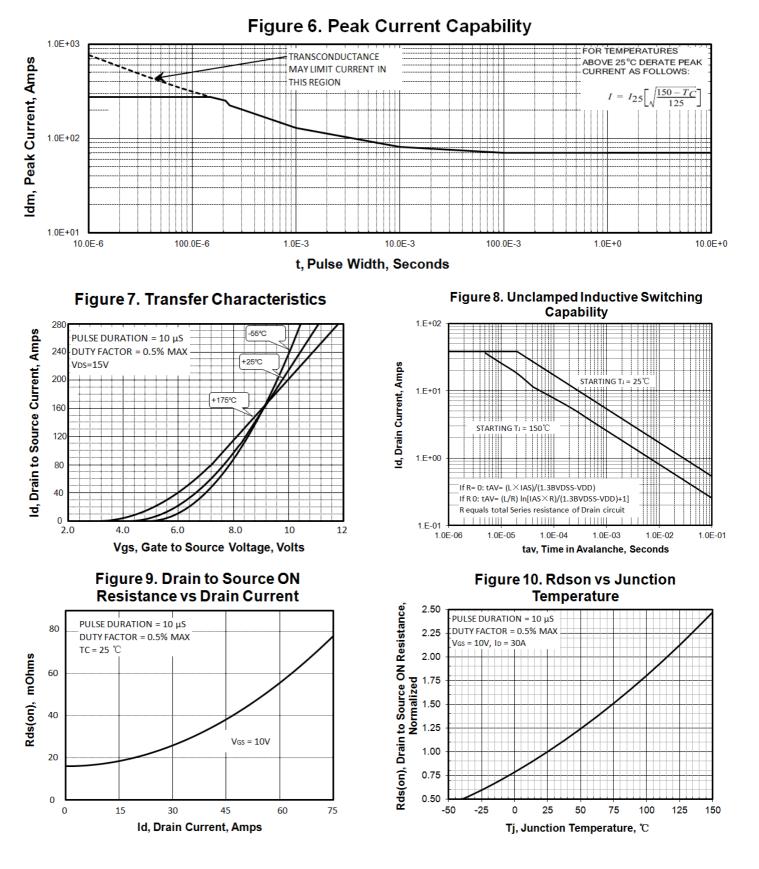


Figure 1. Maximum Transient Thermal Impedance

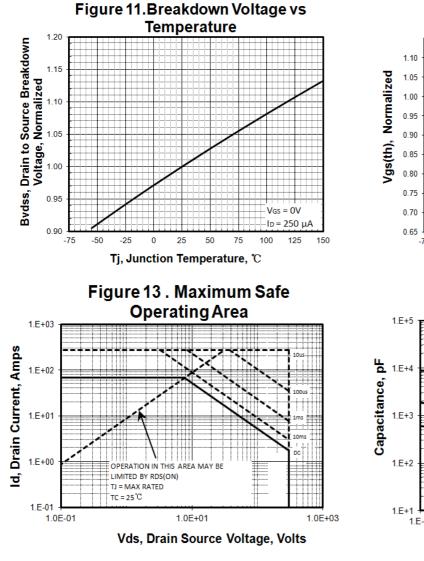


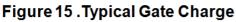
Typical Characteristics(Cont.)

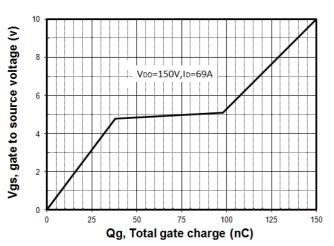




Typical Characteristics(Cont.)







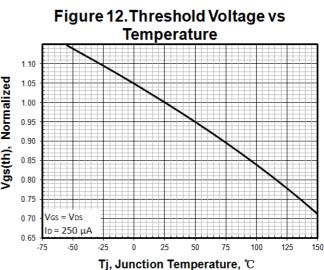


Figure 14. Capacitance vs Vds

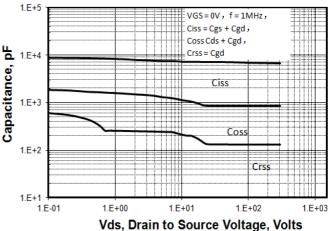
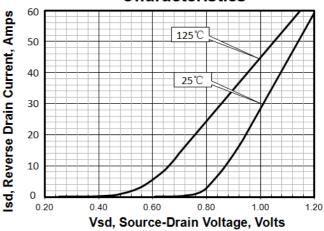
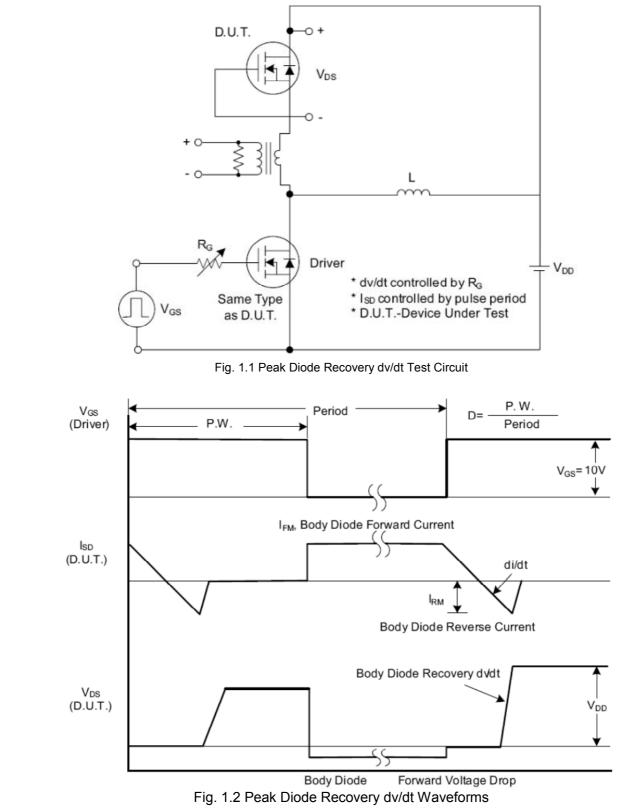


Figure 16.Body Diode Transfer Characteristics



Test Circuits and Waveforms



PTW69N30

Test Circuits and Waveforms (Cont.)

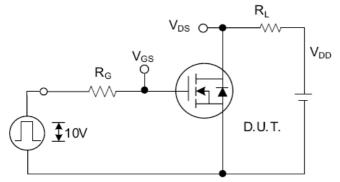


Fig. 2.1 Switching Test Circuit

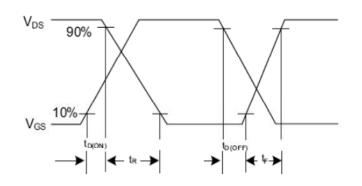


Fig. 2.2 Switching Waveforms

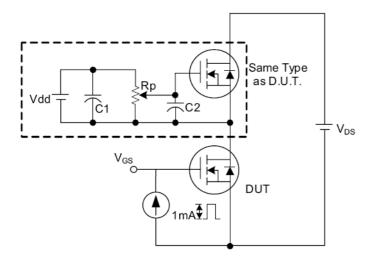


Fig. 3.1 Gate Charge Test Circuit

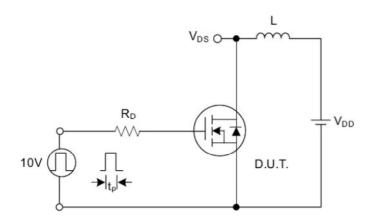


Fig. 4.1 Unclamped Inductive Switching Test Circuit

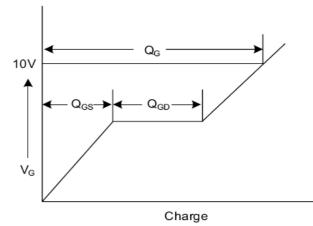
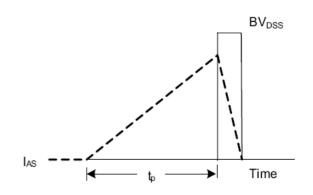


Fig. 3.2 Gate Charge Waveform





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