InnoMux Family of ICs

2 Constant Voltage and 4 Channel Dimming LED Backlight CC Controller

Product Highlights

CV and 4-Channel LED Backlight Controller

- Eliminates buck and LED backlight boost converters
- One or two constant voltage outputs
  - Independently regulated outputs with instantaneous transient response ±5% CV on 0%-100%-0% load step
- Typical output voltages
  - One CV mode: 5 V to 22 V
  - Two CV mode: 5 V and 12 V to 22 V
- 1-4 string LED backlight
  - 3% matching accuracy for LED strings
  - Analog, PWM, sequenced PWM and filtered PWM operation
  - Up to 100 V string voltage / up to 960 mA total string current
  - Up to 2:1 LED string voltage range

Advanced Protection / Safety Features

- Individual overload protection for all outputs
- String imbalanced / short / open protection
- Output overvoltage set for auto-restart

Convenient Packages

- 28-Lead HSOP for single-sided wave soldered PCBs or small 28-Lead QFN (5x5 mm Body) for compact multilayer designs

Applications

- ENERGY STAR 8, CEC, and 2021/2023 EU labeling for monitors and TVs

Description

When paired with InnoSwitch3-MX, InnoMux dramatically improves the system efficiency of monitors and TVs by eliminating the boost and buck converter stages using a single-stage flyback topology. This enables very high system efficiency up to 91%, on a small PCB footprint.

The LED backlight control offers excellent minimum threshold regulation as well as analog and several PWM dimming options. The sequenced PWM dimming option further improves visual performance and stabilizes power demand. Extensive protection features are provided.

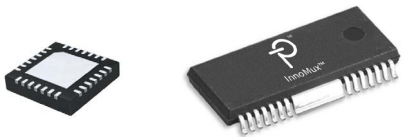


Figure 2. Left – InnoMux in QFN-28, Reflow Process.
Right – InnoMux in HSOP-28, Wave Solder Process.

InnoMux

Product	Output Configuration	Package
IMX101J	1 CV, 1 LED string	QFN
IMX101U	1 CV, 1 LED string	HSOP
IMX111U	2 CV, 1 LED string	HSOP
IMX111J	2 CV, 1 LED string	QFN
IMX102U	1 CV, 4 LED strings	HSOP
IMX112U	2 CV, 4 LED strings	HSOP

Table 1. InnoMux Controller Part Numbers.

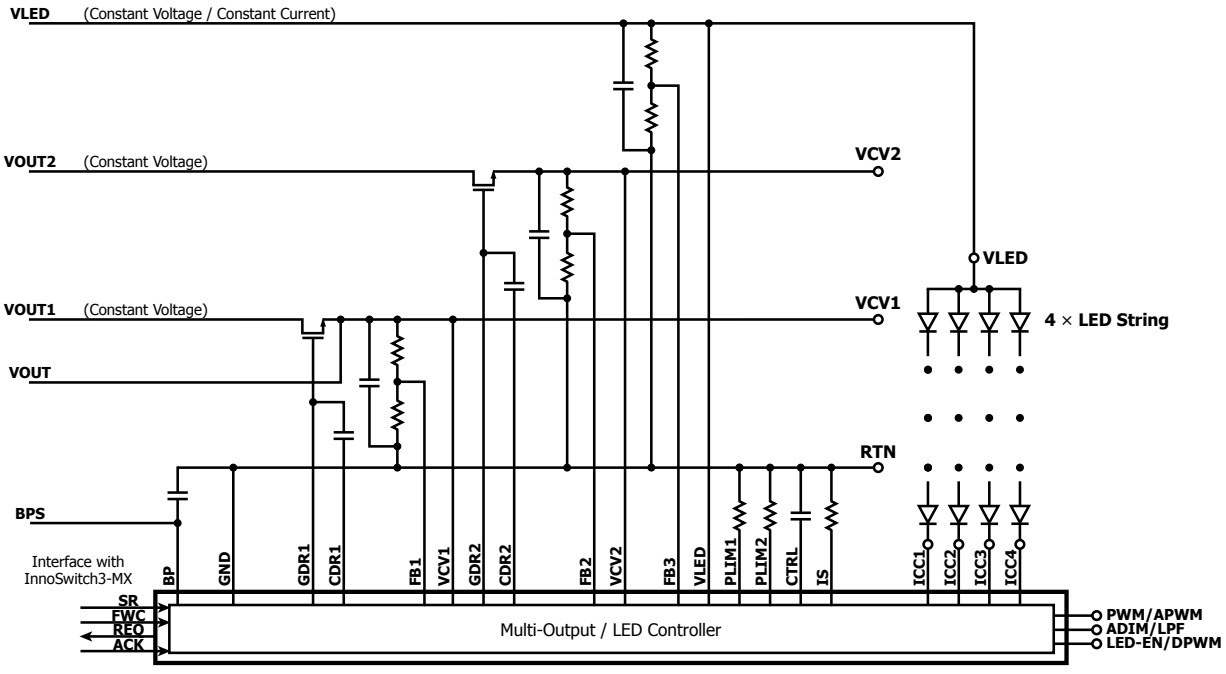


Figure 1. Typical Schematic.

InnoMux

PI-8370-100318

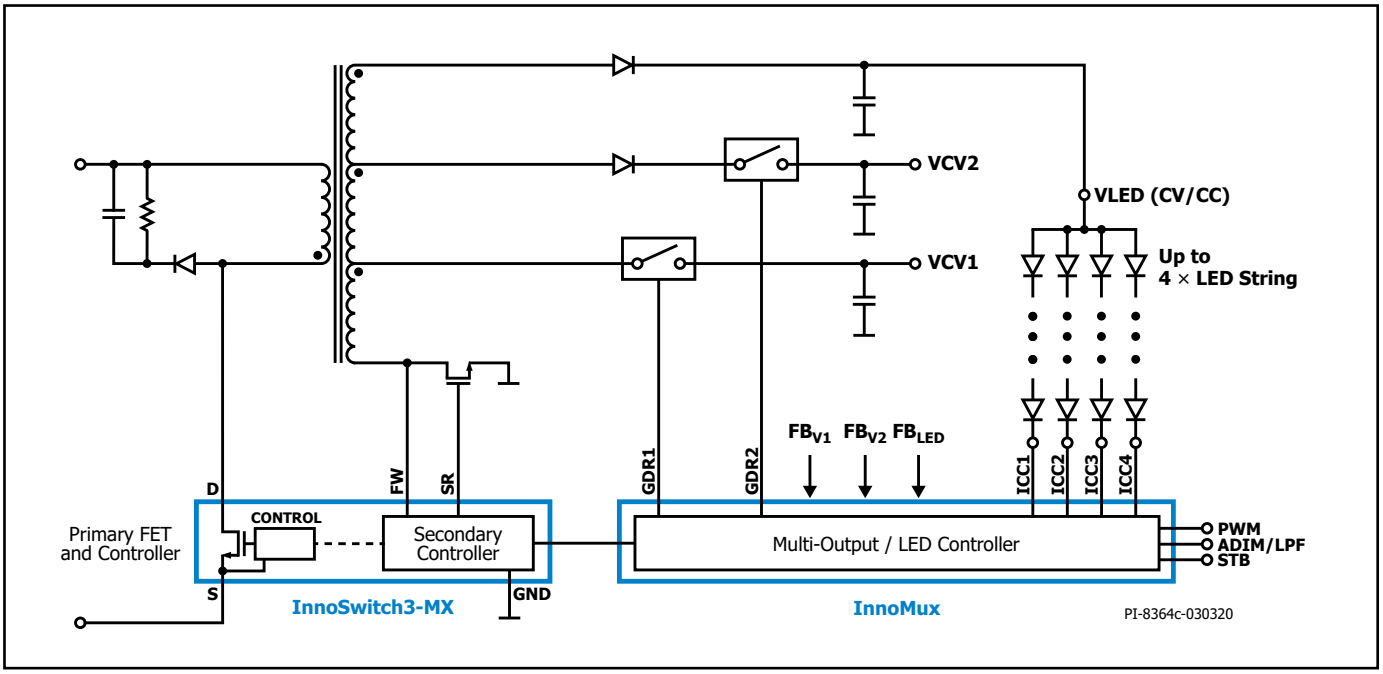


Figure 3. Simplified Schematic for Monitor / TV Application.

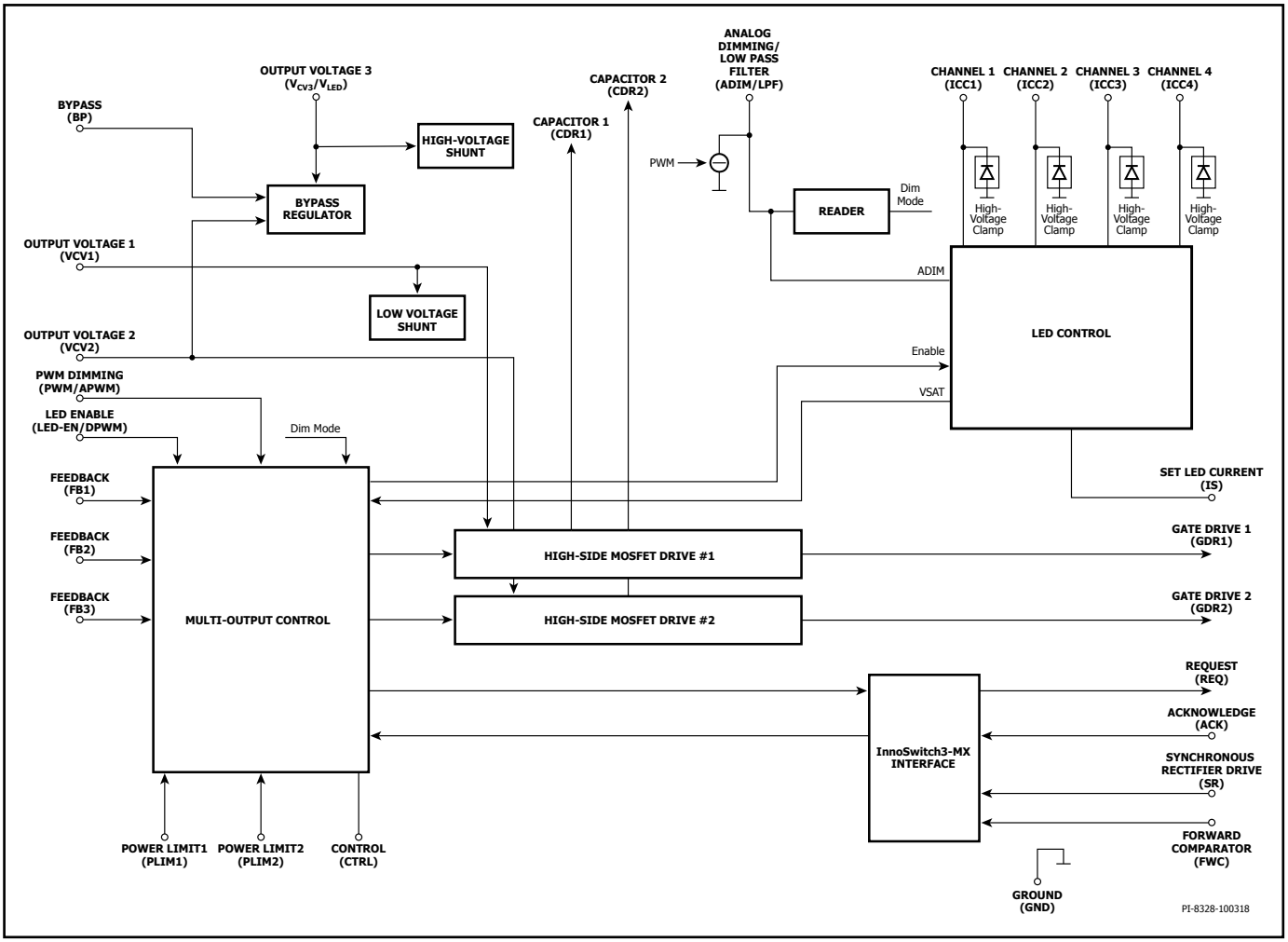


Figure 4. Functional Block Diagram of the InnoMux Controller.

Pin Functional Description

QFN-28 InnoMux Controller

CHANNEL 1 (ICC1) Pin (Pin 1)
LED current regulation channel 1.

CHANNEL 2 (ICC2) Pin (Pin 2)
LED current regulation channel 2.

GROUND (GND) Pin (Pin 3)
Pin 3 must be connected to the exposed pad and the secondary ground.

CHANNEL 3 (ICC3) Pin (Pin 4)
LED current regulation channel 3.

CHANNEL 4 (ICC4) Pin (Pin 5)
LED current regulation channel 4.

GROUND (GND) Pin (Pin 6)
Pin 6 must be connected to the exposed pad and the secondary ground.

SET LED CURRENT (IS) Pin (Pin 7)
Current setting for LED string current.

CONTROL (CTRL) Pin (Pin 8)
Output to control capacitor.

ANALOG DIMMING (ADIM/LPF) Pin (Pin 9)
Analog dimming/low pass filter connection.

PWM DIMMING (PWM/APWM) Pin (Pin 10)
PWM input.

SYNCHRONOUS RECTIFIER (SR) Pin (Pin 11)
SR signal from InnoSwitch3-MX.

FORWARD COMPARATOR (FWC) Pin (Pin 12)
FW comparator signal from InnoSwitch3-MX.

ACKNOWLEDGE (ACK) Pin (Pin 13)
ACK signal from InnoSwitch3-MX.

REQUEST (REQ) Pin (Pin 14)
REQ output to InnoSwitch3-MX.

POWER LIMIT 2 (PLIM2) Pin (Pin 15)
Set power limit for VLED/VCV2.

POWER LIMIT 1 (PLIM1) Pin (Pin 16)
Set power limit for VCV1/VCV2.

GATE DRIVE 2 (GDR2) Pin (Pin 17)
Selection MOSFET gate driver for CV2.

CAPACITOR (CDR2) Pin (Pin 18)
Capacitor for GDR2.

BYPASS (BP) Pin (Pin 19)
BP/VDD regulator output. Also supplies InnoSwitch3-MX.

CAPACITOR (CDR1) Pin (Pin 20)
Capacitor for GDR1.

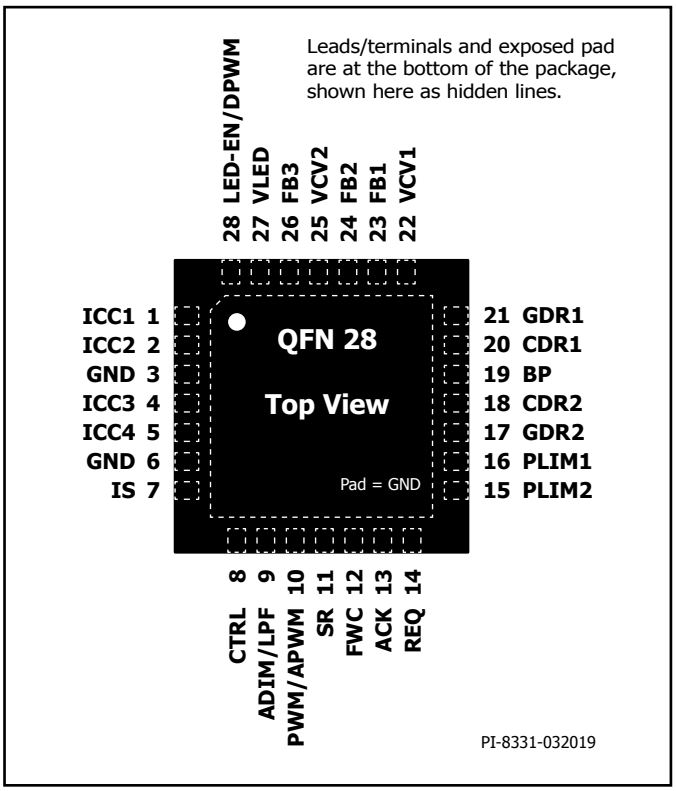


Figure 5. InnoMux QFN-28 Controller Pin Configuration.

GATE DRIVE 1 (GDR1) Pin (Pin 21)
Selection MOSFET gate driver for CV1.

OUTPUT VOLTAGE (VCV1) Pin (Pin 22)
Output voltage connection for CV1 selection MOSFET drive.

FEEDBACK 1 (FB1) Pin (Pin 23)
Feedback input for VCV1 output voltage.

FEEDBACK 2 (FB2) Pin (Pin 24)
Feedback input for VCV2 output voltage.

OUTPUT VOLTAGE (VCV2) Pin (Pin 25)
Output voltage connection for BP regulator and for CV2 selection MOSFET drive.

FEEDBACK 3 (FB3) Pin (Pin 26)
Feedback input for VLED output voltage.

OUTPUT VOLTAGE (VLED) Pin (Pin 27)
Output voltage connection for BP regulator.

LED-EN/DPWM Pin (Pin 28)
LED enable/digital PWM input.

HSOP-28 InnoMux Controller

CHANNEL 3 (ICC3) Pin (Pin 1)
LED current regulation channel 3.

CHANNEL 4 (ICC4) Pin (Pin 2)
LED current regulation channel 4.

SET LED CURRENT (IS) Pin (Pin 3)
Current setting for LED string current.

CONTROL (CTRL) Pin (Pin 4)
Output to control capacitor.

ANALOG DIMMING (ADIM/LPF) Pin (Pin 5)
Analog dimming/low pass filter connection.

PWM DIMMING (PWM/APWM) Pin (Pin 6)
PWM input.

SYNCHRONOUS RECTIFIER (SR) Pin (Pin 7)
SR signal from InnoSwitch3-MX.

GROUND (GND) Pin
All grounds must connect to secondary ground.

FORWARD COMPARATOR (FWC) Pin (Pin 8)
FW comparator signal from InnoSwitch3-MX.

ACKNOWLEDGE (ACK) Pin (Pin 9)
ACK signal from InnoSwitch3-MX.

REQUEST (REQ) Pin (Pin 10)
REQ output to InnoSwitch3-MX.

POWER LIMIT 2 (PLIM2) Pin (Pin 11)
Set power limit for VLED/VCV2.

POWER LIMIT 1 (PLIM1) Pin (Pin 12)
Set power limit for VCV1/VCV2.

GATE DRIVER 2 (GDR2) Pin (Pin 13)
Selection MOSFET gate drive for CV2.

CAPACITOR (CDR2) Pin (Pin 14)
Capacitor for GDR2.

BYPASS (BP) Pin (Pin 15)
BP/VDD regulator output. Also supplies InnoSwitch3-MX.

CAPACITOR (CDR1) Pin (Pin 16)
Capacitor for GDR1.

GATE DRIVE 1 (GDR1) Pin (Pin 17)
Selection MOSFET gate drive for CV1.

OUTPUT VOLTAGE (VCV1) Pin (Pin 18)
Output voltage connection for CV1 selection MOSFET drive.

FEEDBACK 1 (FB1) Pin (Pin 19)
Feedback input for VCV1 output voltage.

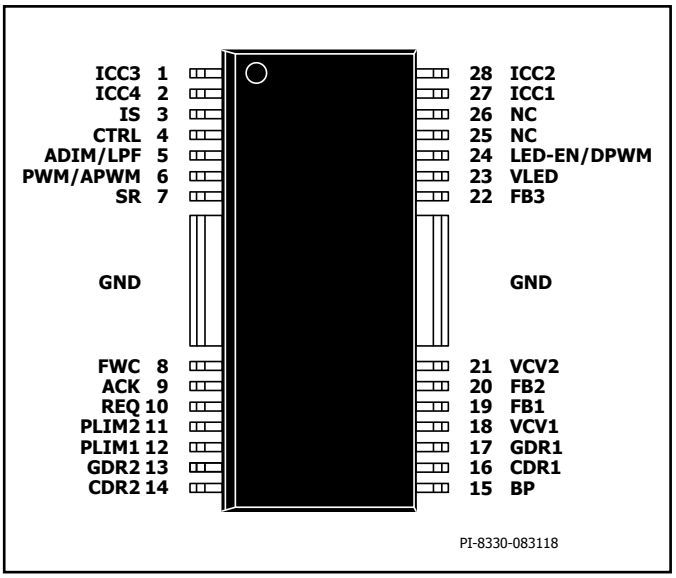


Figure 6. InnoMux HSOP-28 Controller Pin Configuration.

FEEDBACK 2 (FB2) Pin (Pin 20)
Feedback input for VCV2 output voltage.

OUTPUT VOLTAGE (VCV2) Pin (Pin 21)
Output voltage connection for BP regulator and for CV2 selection MOSFET drive.

FEEDBACK 3 (FB3) Pin (Pin 22)
Feedback input for VLED output voltage.

OUTPUT VOLTAGE (VLED) Pin (Pin 23)
Output voltage connection for BP regulator.

LED-EN/DPWM Pin (Pin 24)
LED enable/digital PWM input.

NOT CONNECTED (NC) Pin (Pin 25)
This pin is not connected and should be left floating.

NOT CONNECTED (NC) Pin (Pin 26)
This pin is not connected and should be left floating.

CHANNEL 1 (ICC1) Pin (Pin 27)
LED current regulation channel 1.

CHANNEL 2 (ICC2) Pin (Pin 28)
LED current regulation channel 2.

InnoMux Functional Description

When paired with the InnoSwitch3-MX, the InnoMux combines dual constant voltage output regulation with a four string constant current LED backlight controller.

The InnoMux controller consists of a multi-output controller for regulating the three outputs independently, a BP Regulator for supplying both the InnoMux as well as the paired InnoSwitch3-MX secondary controller, High-Side MOSFET Drivers for directing the energy from the transformer to the appropriate output, Shunts to prevent individual outputs from rising in abnormal loading conditions, Current Sources to drive up to four LED backlight strings, and Readers to determine the value of application configuration resistors.

Block Diagram

BP Regulator

The regulator regulates the BP pin to $V_{BP(REG)}$. The BP regulator will use V_{CV2} as its primary source. During start-up, the regulator will use V_{LED} as long as V_{CV2} is too low (below $V_{CV2(MIN)}$).

It is possible to connect an unregulated supply to V_{CV2} to power the controller in single CV applications. For the controller to function properly, the application designer must make sure that V_{CV2} remains above $V_{CV2(MIN)}$ in all operating conditions after start-up.

A ceramic capacitor on the BP in is recommended. There are no stability requirements on the capacitor; the BP regulator is unconditionally stable.

Multi Output Control

The multi output control regulates each of the two CV outputs and the LED output independently by requesting pulses from the primary based on the FB pin voltages for the three outputs. The transformer energy is then directed to the output that needs the energy on a cycle by cycle basis by turning on the appropriate selection MOSFET in series with either the CV1 or the CV2 output. The transformer shall be designed such that the VOR is increasing from VCV1 to VCV2 to VLED, this guarantees that the current through the VLED diode is negligible when the selection MOSFET for either VCV1 or VCV2 is turned on; only disabling both MOSFETs will direct the energy delivery to the LED output.

Due to the restriction in VOR, the maximum suggested LED output voltage range is about 2:1. A larger range will yield a less optimized design, as the VOR of the CV outputs gets very low. This is further explained in the applications section.

The controller uses a variable frequency control scheme. The CV outputs can run in continuous conduction mode (CCM) during high load. The V_{LED} output will always run discontinuous conduction mode (DCM) to prevent high reverse recovery losses in the high voltage silicon diode for the V_{LED} output.

High-Side MOSFET Drive

The high side selection MOSFETs are driven with a drive voltage 5 V above V_{CV1} for GDR1 and 5V above V_{CV2} for GDR2 using a capacitive drive approach.

The capacitive drive approach benefits from easy level translation by use of capacitor C_{DR}. A regular refresh cycle to top up the charge on C_{DR} is needed when one of the switches has been on for a long time, as the charge on C_{DR} will otherwise slowly leak away. Refresh is also needed during start-up to allow C_{DR} to follow the output voltage when the output is being pulled up. The controller will perform refresh cycles when necessary by turning the selection MOSFET off and then back on.

The default refresh time is $T_{RESFRESH}$, which is doubled to $2 \times T_{RESFRESH}$ during start-up. The longer the refresh time the better but the MOSFET needs to be turned back on before the end of the primary on time. Once the CV outputs are in regulation the refresh time is reduced to $T_{RESFRESH}$. Because the output is no longer changing the refresh is only needed to top up C_{DR} and by reducing the refresh time the risk of the primary on time finishing before the refresh is reduced.

The optimal capacitor value for C_{DR} depends on the gate charge of the selection MOSFET. The selection MOSFET on-level gate voltage is determined by $V_{BP} \times (C_{DR}/(C_G + C_{DR})$, so it is essential that the gate charge (at 5 V gate voltage) is much smaller than the charge in the C_{DR} cap. A typical value for the C_{DR} capacitor is 100nF. For higher C_{DR} capacitor values, the refresh time might be insufficient and the capacitor will not be able to follow the output during start-up. It is therefore important to select low gate-charge devices for the selection MOSFETs to minimise the required C_{DR} capacitor value as well as to minimise energy consumption for driving the MOSFETs.

Shunts

The LV shunt is designed to limit the voltage lift on the V_{CV1} output. Voltage lift on the V_{CV1} output will typically occur due to the lower VOR of the 5 V output. At turn-on of the 5 V selection MOSFET after delivery of a pulse to one of the other outputs, a small amount of energy is delivered to the CV1 output from the higher idle ring voltage.

The LV shunt is turned on when the FB1 voltage exceeds $V_{LVSHUNT}$.

In practical applications it is unlikely for the CV1 output to lift; CV1 output lift typically only occurs when the CV1 output is completely unloaded while the other outputs are running at high output load.

The HV shunt is used to limit the voltage on the V_{LED} rail to the maximum allowed voltage in case of peak-charging of the V_{LED} output when the LED output is not loaded. This peak charging is predominantly caused by leakage in the transformer; the V_{LED} output typically has lowest leakage and thus will receive a small amount of energy from switching cycles that are destined for V_{CV1} or V_{CV2}.

The HV shunt is turned on when the FB3 voltage exceeds $V_{HV(SHUNT)}$.

In case of application problems with overvoltage on V_{LED}, it is possible to implement an additional Zener diode clamp with a small series resistor to dissipate the excess power as the range between $V_{FB3(REG)}$ and $V_{FB3(OVP)}$ is sufficiently large.

Note that the V_{CV2} output does not need a shunt as this output is not susceptible to peak charging or unintended energy delivery.

LED Current Control

Operation

Current sources control the current into the ICC pins.

The maximum current for each current source is $I_{ICC(MAX)}$. The desired (full-scale) current for each of the current sources can be set by a single external current sense resistor R_{LED} (which is connected to the IS pin).

The design of the current sources guarantees that the current in each of the strings is tightly balanced.

Current sources can be paralleled (ganged together) when only one or two strings are used. This will increase the maximum allowed string current.

The current sources accommodate PWM dimming, analog dimming and hybrid dimming. Hybrid dimming is a combination of analog and PWM dimming. Dimming is further described in Led Dimming section.

Output Voltage Regulation for V_{LED} Output

InnoMux keeps the voltage drop over the current sources as low as possible to maintain optimum system efficiency. The output voltage for driving the LED string(s) (V_{LED}) is therefore regulated based on the minimum required voltage drop over the four current sources. The low voltage drop over the current sources is maintained for any LED current by changing the V_{LED} output voltage set point.

When the LEDs are on, the voltage on the C_{CTRL} capacitor is used as set point for the V_{LED} output voltage. The voltage on the capacitor is increased when the voltage drop over anyone of the current sources is less than the target value. Vice versa, the voltage on the cap is reduced when the voltage on all current sources is too high.

The regulation loop is subject to stability criteria and the capacitor has to be chosen accordingly; the optimal capacitor value depends on:

1. The ratio of the LED rail output capacitance (C_{VLED}) to the available current for increasing the V_{LED} rail voltage;
2. The FB3 voltage divider ratio (FB3RATIO=VLED/VFB3).

The minimum capacitance value for the C_{CTRL} capacitor is given by the following formulae; both conditions have to be met:

$$C_{CTRL} \geq \frac{0.3 \times Gm_{CTRL(UP)}}{0.2 \times I_{LED}} \times FB3RATIO \times C_{VLED}$$

$$C_{CTRL} \geq 4 \times Gc_{CTRL(DOWN)} \times FB3RATIO$$

The first formula guarantees that the maximum dV/dt on the V_{LED} voltage rail is larger than the dV/dt on the C_{CTRL} capacitor. The second formula makes sure that the reduction in voltage on the C_{CTRL} capacitor is smaller than the measured voltage error on the V_{LED} rail

For typical designs, 220 nF is a good starting point.

Low Current Clamps

Low-current clamps on each of the I_{CC} outputs are designed to prevent over voltage conditions on the ICC pins when the LEDs are turned off. The maximum current for these clamps is $I_{CCHV(CLAMP)}$. These clamps will limit the voltage on the ICC pins below $V_{HV(CLAMP)}$ in LED off conditions, even when the nominal LED string voltage (V_F) is about 100 V.

InnoSwitch3-MX Interface

The InnoMux to InnoSwitch3-MX interface is a four-wire interface.

The REQ signal indicates a request from the InnoMux controller for a new pulse. Upon reception, InnoSwitch3-MX will then communicate this request to the primary side controller over the integrated flux-link. (Note that the InnoSwitch3-MX will delay the request to the primary when in DCM to achieve QR mode switching.)

The REQ signal is also used to communicate timing for specific events during start-up as well as error conditions to the InnoSwitch3-MX. For this reason, REQ is a multi-level signal. The levels are shown in the table below.

REQ Pin Voltage Level	Condition
REQ < 0.25 × V_{REF}	Initial level at power-up. No pulse requested by InnoMux. InnoSwitch3-MX secondary on stand-by / in primary control mode. InnoSwitch3-MX secondary will start handshake and obtain control when the first pulse is requested.
0.25 × V_{REF} < REQ < 0.5 × V_{REF}	InnoMux indicates measurement window to InnoSwitch3-MX for idle ring frequency measurement. This is a one-off event during stat-up.
0.5 × V_{REF} < REQ < V_{REF}	No pulse requested by InnoMux.
V_{REF} < REQ < 2V_{REF}	Pulse requested by InnoMux. InnoMux will retain the REQ level until the pulse request has been acknowledged (pulse on ACK pin) by InnoSwitch3-MX and a rising edge is observed on the SR pin.
REQ > 2V_{REF}	Output overvoltage indication by InnoMux. InnoSwitch3-MX secondary will signal the primary to latch-off.

The ACK signal indicates that a pulse request has been made by InnoSwitch3-MX secondary to the primary controller (via the flux link). The rising edge of the SR signal (driven by InnoSwitch3-MX) is used byInnoMux to assess when the transformer starts delivering energy to the secondary.

The PCB trace connecting the REQ pins deserves specific attention during layout; it is a high-impedance multi-level analog signal and is sensitive to noise pick-up and layout impedance.

Readers

The (pin-) readers determine the presence and value of the resistors/ capacitors connected to the PLIM and ADIM inputs. These readers are active only directly after start-up and will not update until the next power-up.

Start-Up

During start-up, the InnoSwitch3-MX will run at a fixed frequency and 50% of maximum ILIM. The InnoMux controller will first bring up V_{LED} to $V_{STAYALIVE}$ level, a sufficient level to provide power to the BP regulator or to 20% of the target value, whichever is highest. As soon as the V_{LED} has reached the designated level, the controller will start bringing up V_{CV2} to 20% of the target value and finally the V_{CV1} to 10% of the target value. When all three outputs are at the correct level, the InnoMux controller will take control and bring up V_{CV1} and V_{CV2} simultaneously. The voltage on the control capacitor is slowly increased and is used as the reference for the V_{CV1} and V_{CV2} outputs during pull up. The size of the C_{CTRL} capacitor will affect the rate of rise of the outputs during pull up.

The LEDs will only be enabled after V_{CV1} and V_{CV2} have reached regulation voltage. At this moment, the CV output regulators switch to a fixed internal reference and the VLED output will start using the voltage on C_{CTRL} as its set point.

Figure 7 shows a schematic representation of the start-up process.

LED String Configuration Detection

During pull up of the CV outputs, the controller will also increase the V_{LED} and try to run a small amount of current through the LEDs strings to detect which of the four ICC pins have an LED string attached and whether any of the ICC pins have been connected in parallel in a supported configuration. Unused pins should be connected to GND and will be disabled by the controller.

At start-up, the controller will verify that none of the connected LED strings is short-circuit (the ICC pin connected directly to the V_{LED} supply rail). If one of the strings were short-circuit, the response depends on the maximum LED voltage. For low-voltage LED configurations (up to about 55 V maximum LED string voltage), the affected string will be turned off and the controller will start-up as normal. For high voltage LED configurations, the controller will auto-restart as the short-circuit string could violate the maximum allowed ICC pin voltage. The low-voltage / high-voltage detection is based on the FB3 resistor ratio, which is determined at start-up.

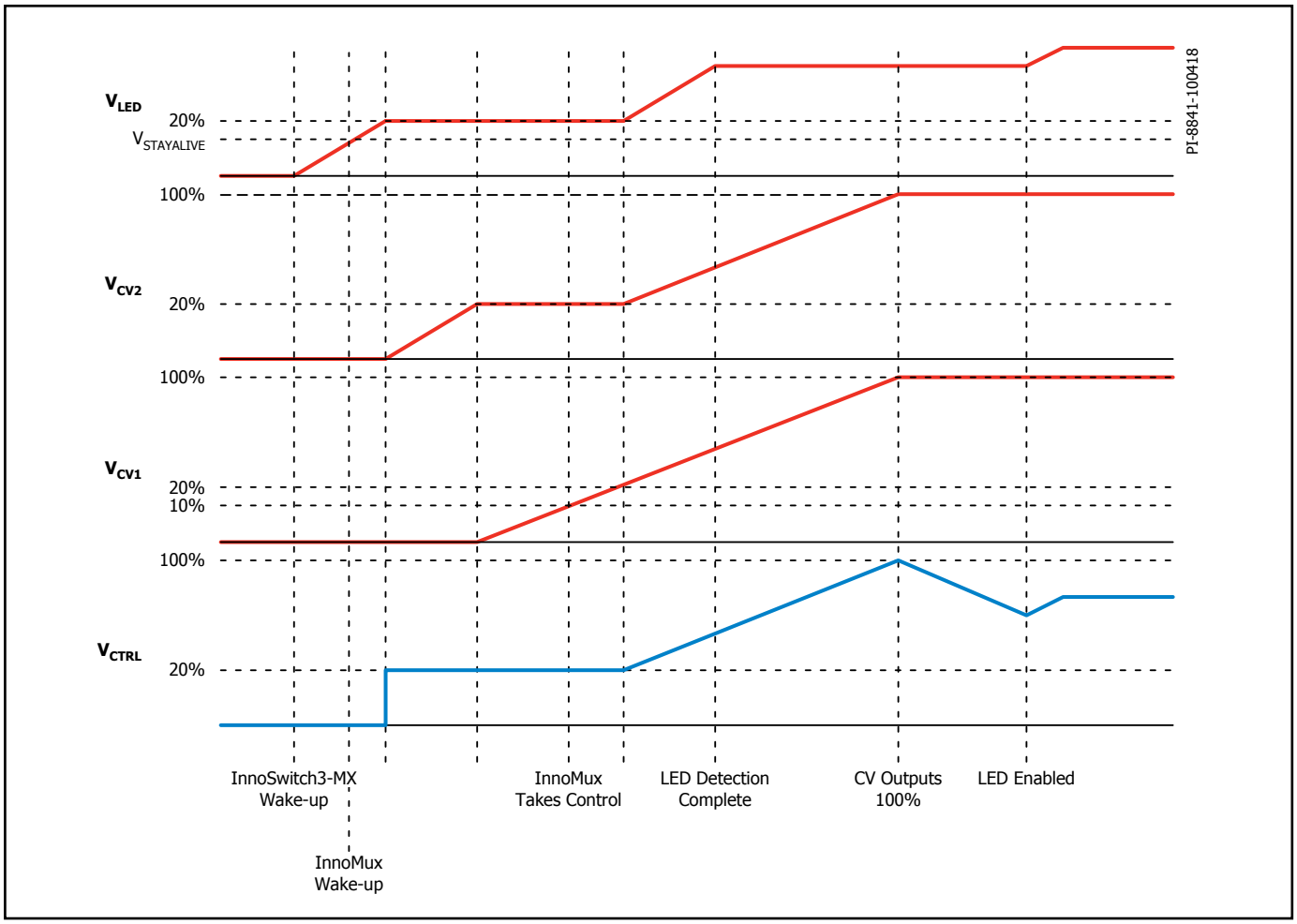


Figure 7. Start-Up Diagram.

LED Dimming

The current through the LED strings can be varied for changing (dimming) the LED brightness.

Three LED dimming modes are supported:
1. PWM only dimming with fixed output current
2. Analog dimming, output current set by an external reference voltage (V_{ADIM})
3. Hybrid dimming: analog dimming and PWM dimming combined.

The first dimming mode only supports PWM dimming. In this mode, the LED current is set by a resistor on the IS pin. The analog dimming mode (second mode) allows reducing the LED current from 100% (as set by R_{LED} on the IS pin) to 0 (minimum current: $I_{CC(MIN)}$) by varying the voltage on the ADIM pin. The third mode is a combination of analog and PWM dimming.

The LED dimming mode is selected at start-up and is determined by the level on the ADIM pin. A pull-up connection / resistor to BP selects the PWM only dimming mode. (The value of the pull-up resistor will then select between normal and sequenced PWM. A low signal level at start-up (ADIM voltage below $V_{ADIM(SEL)}$) will select the analog or the hybrid dimming mode.

After start-up, the dimming mode is fixed and cannot be changed without a power-on reset.

Figure 8 below shows an overview of the available dimming modes in the InnoMux controller.

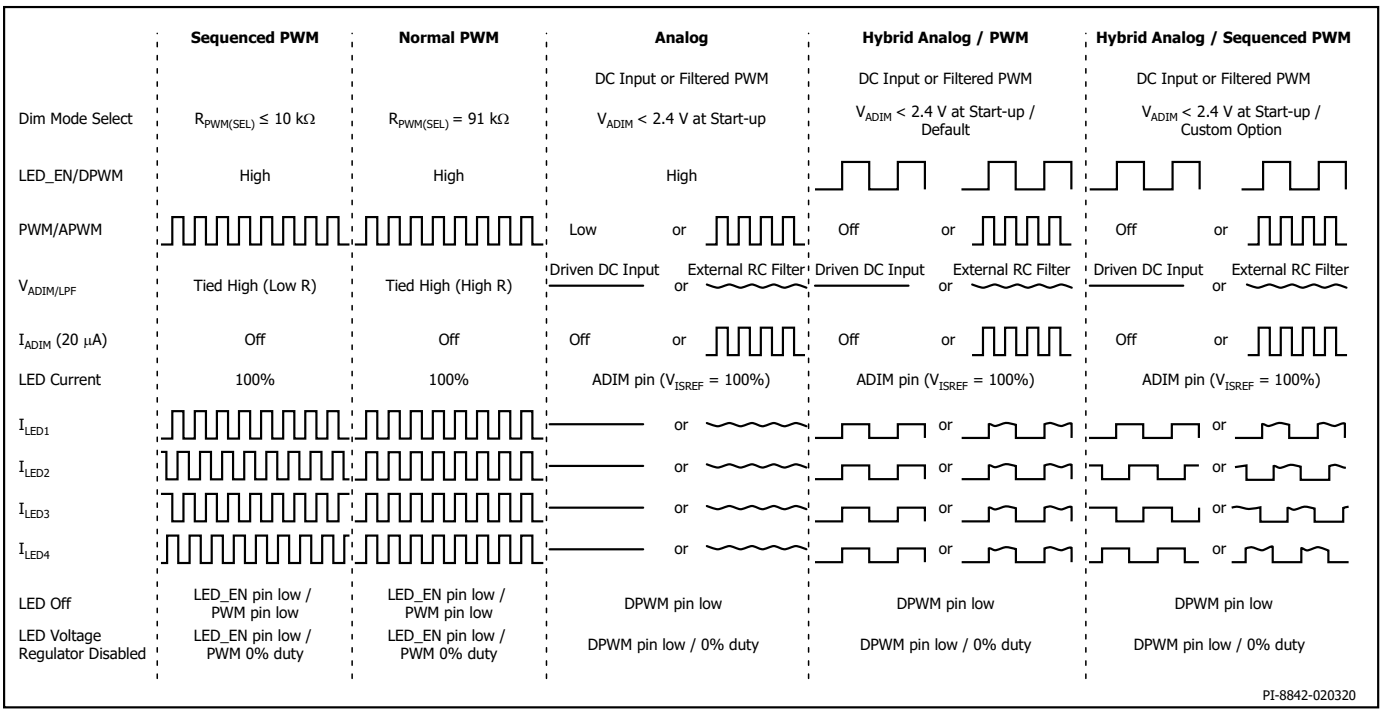


Figure 8. InnoMux Dimming Modes.

PWM Dimming Only

By connecting the ADIM/LPF pin to BP, the LED current (per string) is set by the RLED resistor based on an internal reference ($V_{IS(REF)}$).

$$R_{LED} = V_{IS(REF)} \times \left(\frac{I_{OUT}}{561.56} \right)^{-1.015}$$

The formula shows the relationship between the desired output current and the required value for the current setting resistor.

I_{OUT} is the ICC pin current (for four string operation, the total current equals 4 × I_{OUT}), $V_{IS(REF)}$ is an internally generated reference voltage of 1.5 V. The result gives the resistor value for RLED which sets the current for each of the ICC pins. As the formula is non-linear, the desired ICC pin current must be given in Ampere (A, not mA) and the result is in Ohms (Ω).

Figure 9 shows a graph of R_{LED} vs. LED string current. This graph can be used for estimating the required R_{LED}.

PWM dimming is supported by applying a PWM signal with desired duty cycle to the PWM pin. The allowed PWM frequency range is $PWM_{F(RANGE)}$. Pulling the LED-EN pin low will turn off the LEDs as well as the LED regulator. This is intended for disabling the LEDs during a 'screen-off' mode. Turning off the LED regulator will reduce chip current consumption.

Notes:

- Pulling the PWM pin low to turn the LEDs off is allowed. Keeping the PWM pin low longer than the minimum PWM period will also turn off the LED regulator, independent of the LED-EN signal.
- Pulling LED-EN low will override the state of the PWM signal.

PWM dimming is supported using normal PWM dimming and sequenced (phase shifted) PWM dimming. Normal PWM and sequenced PWM are further explained in the section on PWM dimming (These two PWM dimming modes are also supported in the hybrid dimming mode, see below.)

Figure 11 (page 12) shows the typical connections in this mode for the PWM and LED-EN signals. The $R_{PWM(SEL)}$ pull-up resistor selects between normal and sequenced PWM mode.

Analog and Hybrid Dimming Modes

Analog Dimming

In the analog dimming mode, the voltage on the ADIM/LPF pin determines the LED current. The LED current changes linearly over the V_{ADIM} range. The 100% LED current level (per string) is set by the R_{LED} resistor.

$$R_{LED} = V_{ADIM} \times \left(\frac{I_{OUT}}{561.54} \right)^{-1.015}$$

The formula shows the relationship between the desired output current and the required value for the current setting resistor.

I_{OUT} is the ICC pin current (for four string operation, the total current equals 4 × I_{OUT}), V_{ADIM} is the voltage on the ADIM pin (1.5 V is full scale). The result gives the resistor value for R_{LED} which sets the current for each of the ICC pins. As the formula is non-linear, the desired ICC pin current must be given in Ampere (A, not mA) and the result is in Ohms (Ω).

Figure 9 shows a graph of R_{LED} vs. LED string current at V_{ADIM} = 1.5 V. This graph can be used for estimating the required R_{LED}.

The ADIM pin is normally driven from an external source (e.g. display controller) to set the display brightness.

It is possible to use a PWM signal (A-PWM) to generate the analog dimming reference (V_{ADIM}) for the LED current; the duty cycle on the APWM pin is then accurately converted into an analog dimming reference voltage on the ADIM/LPF pin by a simple external RC low pass filter fed by an on chip current source providing $I_{PWM(LPF)}$.

The low pass filter needs a 75 kΩ resistor to allow regulating up to 100%. The capacitor is typically chosen as 10 nF, but can be changed if a different RC time constant would be desired.

The APWM pin should be tied low when a DC voltage is supplied to the ADIM/LPF pin.

The DPWM pin should be high during analog dimming. Pulling the DPWM pin low will turn off the LEDs and the LED regulator. This is intended for disabling the LEDs during use in a 'screen-off' mode. Reducing the ADIM voltage down to 0 V to turn the LEDs off is not allowed for disabling the LEDs.

Figure 11 (page 12) shows the typical connections in this mode for the DPWM, APWM and analog dimming reference (V_{ADIM}) signals.

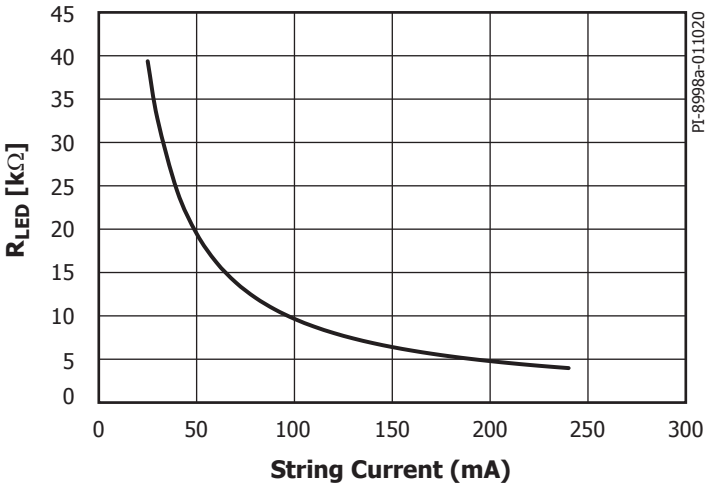


Figure 9. R_{LED} vs. LED String Current for PWM Dimming and at V_{ADIM} = 1.5 V for Analog Dimming.

LED Configuration	Required Phase Shift	Description
1 – 2 – 3 – 4	0°, 90°, 180°, 270°	Four strings. All outputs 90° phase shifted.
1 – 2 – 3	0°, 120°, 240°	Three strings. Outputs 1, 2, and 3 all 120° phase shifted. Output 4 not used.
1 – 3	0°, 180°	Two strings only. Output 3 180° phase shifted with respect to output 1.
1 2 – 34	0°, 180°	Same as above, but now with outputs 1+2 and 3+4 ganged together. Outputs 3 and 4 180° phase shifted with respect to outputs 1 and 2.

Table 2. Sequenced PWM Dimming Options.

Hybrid Dimming

PWM dimming is supported during analog dimming by applying a PWM signal (D-PWM) with desired duty cycle to the DPWM pin. The allowed PWM frequency range is $PWM_{F(RANGE)}$. The LEDs are turned off by pulling the DPWM pin low. Normal PWM is active by default. Sequenced PWM is available as a custom option. (The $R_{PWM(SEL)}$ resistor is not available in this mode.)

Pulling the DPWM pin low longer than the minimum PWM period will turn off the LED regulator, which will reduce chip current consumption in a 'screen-off' mode. Reducing the ADIM voltage down to 0 V to turn the LEDs off is not allowed for disabling the LEDs.

Figure 11 (page 12) shows the typical connections in this mode for the DPWM, APWM and external LED current reference (V_{ADIM}) signals.

PWM Dimming

In PWM dimming, the LED current sources switch rapidly between the set reference current and off, following the digital state of the PWM input.

Two PWM dimming modes are available; normal and sequenced PWM. In PWM dimming, the ADIM/LPF pull-up resistor value selects between normal or sequenced PWM dimming. In hybrid dimming, the selection between normal and sequenced PWM has been preset and cannot be changed by application components.

Normal PWM Dimming Mode

During normal PWM mode dimming, all strings will turn on and off in phase.

Sequenced PWM Dimming Mode

In sequenced PWM mode, the on-periods of the four LED strings are sequenced in time by applying an equal phase shift to each of the strings. The sequenced PWM mode is designed to improve visual performance as well as reduce transient loading on the power supply which will reduce audible noise. Dependent on the LED configuration, the PWM phase shift between channels should be 90°, 120° or 180°. The allowed LED configurations for sequenced PWM diming are shown in Table 2.

The controller will revert to normal PWM dimming if sequenced PWM is selected with an unsupported LED string configuration.

Typical low PWM duty cycle examples for two, three and four strings are shown in Figure 10. It shows the relative timing of the LED currents in two, three and four-channel sequenced PWM dimming operation. The top waveform depicts the incoming PWM signal (PWM/D-PWM).

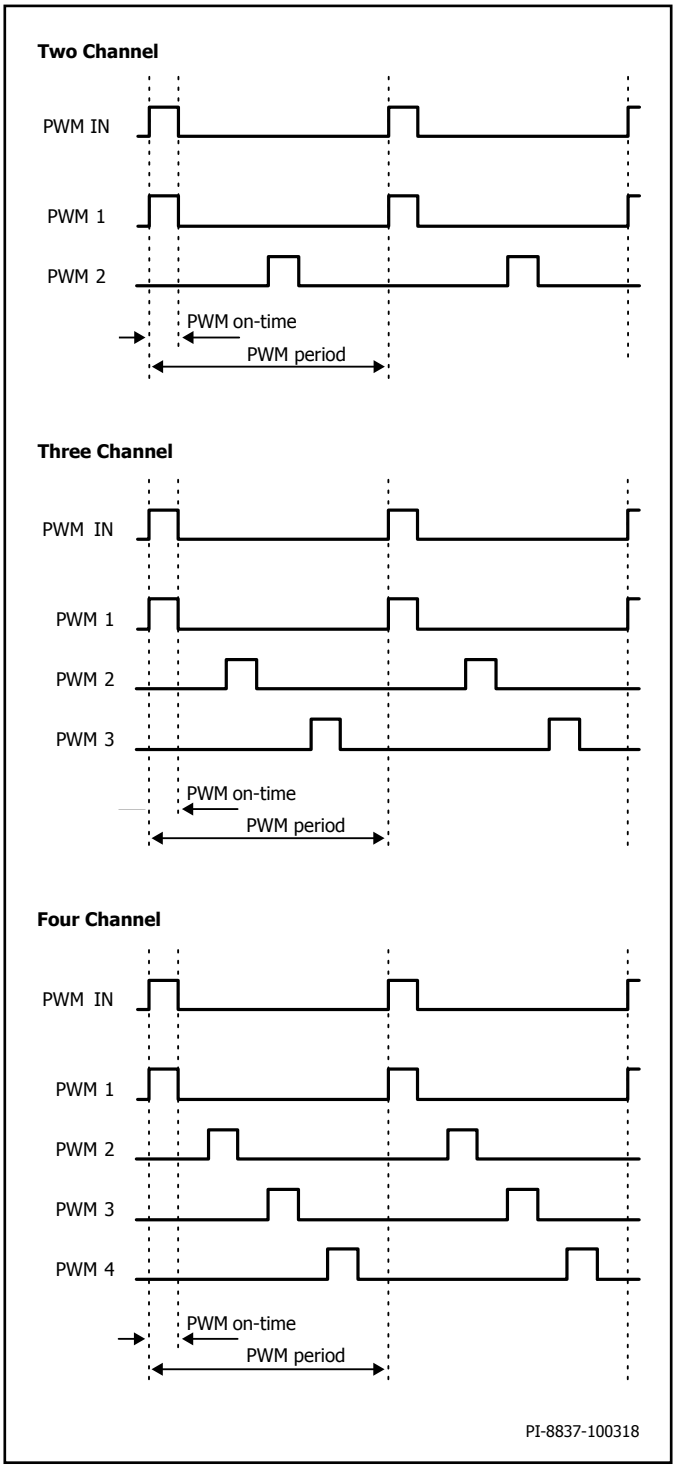
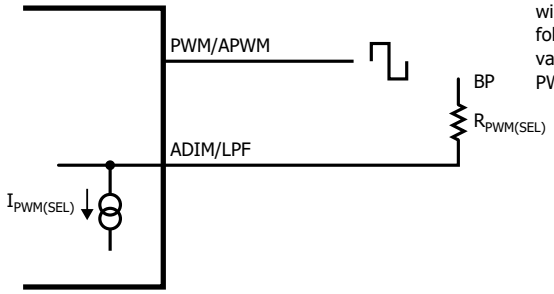


Figure 10. PWM Timing Diagram for Two, Three and Four Channel Sequenced PWM Dimming.

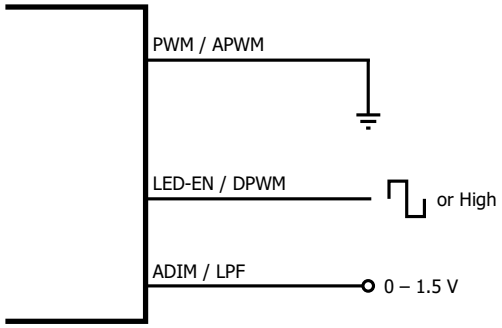
Connection Diagrams for the Various Dimming Options

PWM Dimming;
PWM Mode Selection: normal / sequenced PWM by a resistor



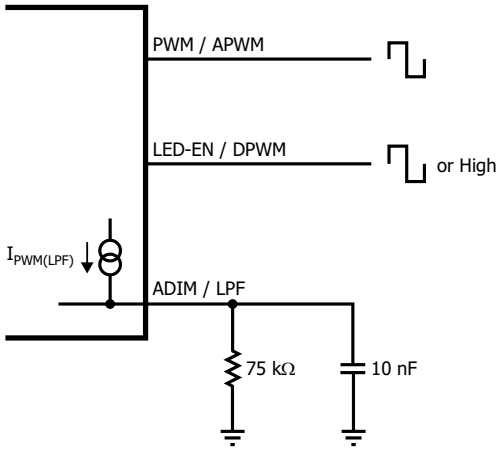
At start-up, a pull-up resistor on the ADIM pin will select PWM dimming. The output current follows the PWM signal. The $R_{PWM(SEL)}$ resistor value selects between Normal and Sequenced PWM.

Analog / Hybrid Dimming;
PWM optional on LED-EN / DPWM pin



At startup, an ADIM voltage below $V_{ADIM(SEL)}$ selects analog / hybrid dimming. The voltage on the ADIM pin sets the LED current; varying the ADIM voltage will allow for analog dimming. The LED-EN / DPWM pin will turn the LEDs on and off and can be driven with a PWM signal for hybrid dimming.

Analog / Hybrid Dimming with Low Pass Filter;
PWM optional on LED-EN / DPM pin



In analog/hybrid dimming mode, the PWM/APWM pin can be driven with a PWM (A–PWM) signal. This will turn the $I_{PWM(LPF)}$ current source on the ADIM/LPF pin on and off. The simple RC filter on the ADIM/LPF (as shown) will convert the PWM duty cycle into an accurate analog level that is then used as the ADIM level for the analog dimming. The LED-EN / DPWM pin will turn the LEDs on and off and can optionally be driven with a second PWM signal (D-PWM) for hybrid dimming.

PI-8838-020320

Figure 11. Connection Diagrams for Dimming Options.

Protection Features and Fault Handling

Overload / Maximum Power Protection and Maximum Power Limit

Maximum Power Protection:
Overload / Short-Circuit Protection
The CV1, CV2 and VLED outputs have a maximum power protection. The simplest part of the protection is to detect whether the output is more than 10% (CV outputs) or more than 1% (V_{LED} output) below set point. If this condition persists for more than 32 switching cycles, then the output is assumed to be overloaded; either the output has a short-circuit or the overall power capability of the power supply has been exceeded and it simply cannot keep the output in regulation.

Maximum Power Limit
The short-circuit fault protection forms an overall power limit but it would allow the full output power to be drawn from a single output without any further protection. Therefore, the power limit function also includes an average frequency limit that has a user selectable level.

The power limit threshold for each of the three outputs is set by the designer using external components on the two PLIM pins. Four setting levels for each output are available.

The power limit measures the average frequency of switching pulses to a specific output. If this frequency is above a preset threshold for a certain amount of time, then a fault is flagged and the controller will auto restart or latch-off.

For calculating the maximum power limit threshold, the frequency for a specific output should be calculated as a fraction of the maximum total output power.

$$f_{LIMIT} = \frac{P_{OUTPUT(MAX)}}{P_{MAX}} \times f_{MAX}$$

$P_{OUTPUT(MAX)}$ Maximum allowed power for this output
P_{MAX} Maximum total output power
f_{MAX} Operating frequency at maximum output power
f_{LIMIT} Calculated maximum frequency for this output

The maximum overload duration is set such that the load is able to draw at least double the nominal power for at least 10 ms, assuming the load is not drawing more power than the power supply is physically capable of delivering.

	CV1 PLIM1	V_{LED} PLIM2
30 kHz	5.1 kΩ	5.1 kΩ
41 kHz	10 kΩ	10 kΩ
56 kHz	22 kΩ	22 kΩ
78 kHz	39 kΩ	39 kΩ

Table 3. CV1 and VLED Power Limit Selection.

The power for CV2 is selected with the presence or absence of capacitors on PLIM1 and PLIM2 as shown in the table below. If there is no CV2 output then no capacitors are needed.

	PLIM1	PLIM2
30 kHz	No Capacitor	No Capacitor
41 kHz	Capacitor	No Capacitor
56 kHz	No Capacitor	Capacitor
78 kHz	Capacitor	Capacitor

Table 4. CV2 Power Limit Selection.

The time constant for the PLIM resistor and capacitor should be chosen as T_{PLIM}. This defines the capacitor value for a given resistor.

Further details on setting the PLIM components can be found in the applications section.

Output OV

Any output reaching the output overvoltage (V_{OV}) threshold will cause a restart or latch-off of the controller. The output OV condition is detected on the respective FB pins for the three outputs.

LED Fault Detection

During operation, the controller will continuously monitor the voltages on the ICC pins. If a large asymmetry between the LED strings (>$V_{ICC(OV)}$) is detected, the shorter string(s) will be disabled to prevent excessive power dissipation in the controller. Any strings that go open-circuit or short-circuit will also be disabled.

LED return short to ground will be detected by the power limit protection, which will force a controller restart. After restart, the affected string will be disabled.

Over-Temperature

The thermal protection circuitry continuously measures the controller temperature. The threshold is set at T_{PROT}. When the temperature rises above T_{PROT}, the InnoMux will disable the LEDs as well as the CV outputs with hysteretic over-temperature protection; the LEDs and CV outputs will remain disabled and the V_{LED} rail will be maintained at $V_{STAYALIVE}$ until the temperature drops below T_{PROT} - T_{HYST}. The controller will restart when the temperature has dropped below this level.

If the temperature at any moment exceeds T_{SD}, the InnoMux will send a latch-off request to the InnoSwitch3-MX.

Fault Handling

When a fault is flagged, the controller will either auto-restart or latch-off.

In the auto-restart condition, the InnoMux will stop requesting switching cycles. This will cause the output rails to collapse. As there will be no further requests, the InnoSwitch3-MX primary will take back control after a pre-defined time-out and restart.

In the latch-off condition, the InnoMux will send a latch-off request to the InnoSwitch3-MX and the primary will latch-off. This condition will persist until the mains input power is cycled.

Absolute Maximum Ratings[1,2]

BP Pin Voltage ..... -0.3 V to 6 V
V_{CV1}, V_{CV2} Pin Voltage..... -0.3 V to 25 V
V_{CV3} / V_{LED} Pin Voltage ..... -0.3 V to 125 V
GDR1, GDR2 Pin Voltage ..... -0.3 V to 30 V
ICC1, ICC2, ICC3, ICC4 Pin Voltage ..... -0.5 V to 65 V
All Other Pins..... -0.3 V to 6 V
Storage Temperatue ..... -65 °C to 150 °C
Operating Junction Temperature[3]..... -40 °C to +150 °C

Notes:
1. All voltages referenced to Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Normally limited by internal circuitry.

Thermal Resistance

Thermal Resistance: HSOP-28 Package
(θ_{JA})..... 58 °C/W[1]
(θ_{JA})..... 50 °C/W[2]
(θ_{JL})..... 15 °C/W[3]
QFN-28 Package
(θ_{JA})..... 69 °C/W[4]
(θ_{JA})..... 50 °C/W[5]

Notes:
1. Single-Layer, 2 oz. Cu. 0.36 sq. in. heat sinking area.
2. Single-Layer, 2 oz. Cu. 1.0 sq. in. heat sinking area.
3. Single-Layer, 2 oz. Cu. 0.36 & 1.0 sq. in. heat sinking area. Thermocouple attached to ground lead shoulder, near to edge of plastic body.
4. Dual-Layer, 2 oz. Cu. 0.36 sq. in. heat sinking area (bottom layer, connected by 9 filled vias).
5. Dual-Layer, 2 oz. Cu. 1.0 sq. in. heat sinking area (bottom layer, connected by 9 filled vias).

Parameter	Symbol	Conditions All Voltages Referenced to GROUND / 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Pin Description and Parameters							
BP Pin		Internal voltage supply for InnoMux and supply for InnoSwitch3-MX					
BP Voltage Regulation	$V_{BP(REG)}$			4.75	5.0	5.25	V
BP Current	I_{BP}	Full load excludes current consumption by InnoSwitch3-MX and selection MOSFET Drivers			18		mA
	BP_{UV}				4.4		V
Standby Supply Current	$I_{SBP(STANDBY)}$				6		mA
VCV1 Pin (See Note B)		Input voltage for CV1 selection MOSFET drive					
	V_{CV1}	V_{CV1} output voltage range		3		22	V
VCV2 Pin (See Note B)		Input voltage for VDD regulator and for CV2 selection MOSFET drive					
	V_{CV2}	V_{CV2} output voltage range		3		22	V
	$V_{CV2(MIN)}$	Minimum V_{CV2} voltage for BP regulator	Standby 25 °C	5.8			V
			Full Load (30 mA)	8.0			
VLED Pin	V_{LED}	V_{LED} output voltage range		20		100	V
	$V_{STAYALIVE}$	Minimum V_{LED} voltage that will always be maintained by the controller			15		V
Gate Drive Pins							
Refresh Pulse Width	$T_{REFRESH}$	$T_{REFRESH}$ is doubled during start-up See Note D			500		ns
GDR1		The GDR1 pin drives the CV1 selection MOSFET					

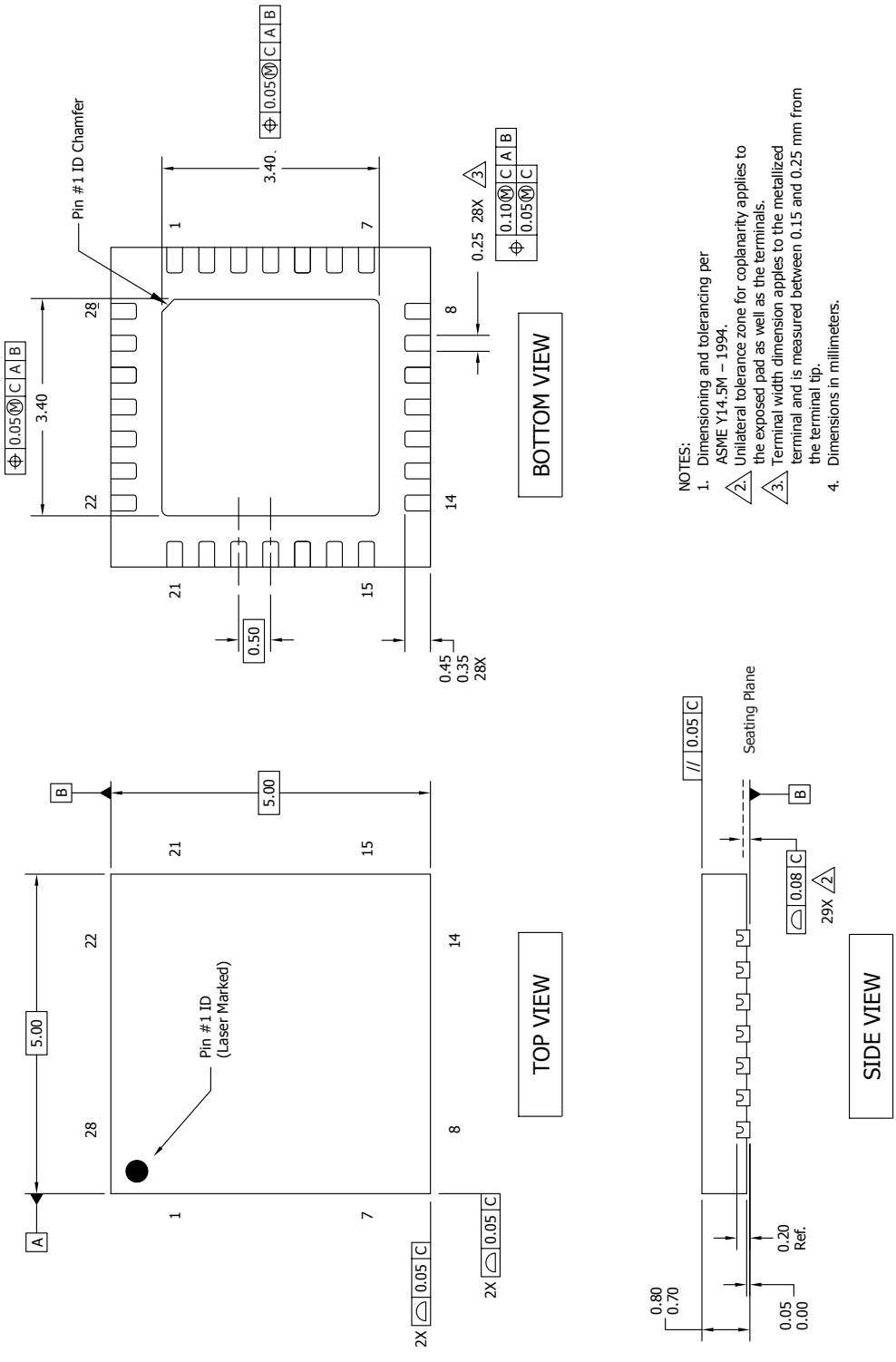
Parameter	Symbol	Conditions All Voltages Referenced to GROUND / 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Gate Drive Pins (cont.)						
GDR1 Output Drive Voltage	V_{DR1}	V_{CV1} + V_{BPREG} (GDR_1 High) V_{CV1} (GDR_1 Low)				
GDR1 Resistance	R_{DR1}	T_J = 125 °C See Note C		30	35	Ω
GDR2		The DR2 pin drives the CV2 selection MOSFET				
GDR2 Output Drive Voltage	V_{DR2}	V_{CV2} + V_{BPREG} (GDR_2 High) V_{CV2} (GDR_2 Low)		V_{CV2}+V_{BPREG} (high) / V_{CV2} (low)		V
GDR2 Resistance	R_{DR2}	T_J = 125 °C See Note C		30	35	Ω
FB/IS Pins						
FB1		FB input for V_{CV1} output voltage				
FB1 Regulation Voltage	$V_{FB1(REG)}$			V_{REF}		
LV Shunt Threshold	$V_{LV(SHUNT)}$			108% of V_{REF}		V
	$I_{CCLV(SHUNT)}$	See Note D	17	20		mA
FB1 Overvoltage	$V_{FB1(OVP)}$			112% of V_{REF}		V
FB2		FB input for V_{CV2} output voltage				
FB2 Regulation Voltage	$V_{FB2(REG)}$			V_{REF}		V
FB2 Overvoltage	$V_{FB2(OVP)}$			112% of V_{REF}		V
FB3		FB input for V_{LED} output voltage				
High-Voltage Shunt Threshold	$V_{HV(SHUNT)}$			108% of V_{REF}		V
	$I_{CCHV(SHUNT)}$	See Note D	8.5	10		mA
FB3 Overvoltage	$V_{FB3(OVP)}$			120% of V_{REF}		V

Parameter	Symbol	Conditions All Voltages Referenced to GROUND / 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
InnoSwitch3-MX Interface Pins						
REQ		Pulse request output Should be connected to the InnoSwitch3-MX REQ input				
ACK		Acknowledge from InnoSwitch3-MX that a request has been issued to the primary-side. Should be connected to the InnoSwitch3-MX ACK output				
FWC		Forward comparator output from InnoSwitch3-MX. Should be connected to the InnoSwitch3-MX FWC output				
SR		SR output from InnoSwitch3-MX. Should be connected to the InnoSwitch3-MX SR output				
LED Regulation Pins						
CTRL Pin		Output to CTRL capacitor				
Maximum Current	$I_{CTRL(POS)}$ $I_{CTRL(NEG)}$			10		µA
	$I_{CTRL(STARTUP)}$			0.125 × I_{CTRL}		A
Regulator Gm (UP)	$Gm_{CTRL(UP)}$	0 V < $V_{ICC(ERROR)}$ < 0.3 V		0.825 × I_{CTRL}		A/V
Regulator (DOWN)	$Gc_{CTRL(DOWN)}$	-0.3 V < $V_{ICC(ERROR)}$ < 0 V		41.25µ × I_{CTRL}		C/V
ICC Pins		Regulator 1-4				
ICC Voltage Protection Limit	$V_{ICC(OV)}$		8		9	V
Minimum ICC Current	$I_{CC(MIN)}$	Per channel		5		mA
Maximum ICC Current	$I_{ICC(MAX)}$	Per channel		240		mA
ICC Channel Matching (See Note A)	Δ100 mA	100 mA Current per string, measured in analog dimming. Equal voltage on all ICC pins. T_J = 25 °C			±3	%
	Δ5 mA	5 mA Current per string, measured in analog dimming. Equal voltage on all ICC pins. T_J = 25 °C			±3	%
ICC Clamp Voltage	$V_{ICC(CLAMP)}$			60	65	V
Maximum ICC Clamp Current	$I_{CCHV(CLAMP)}$		4			µA
LED Control Pins						
LED-EN/DPWM and PWM/APWM Pins	V_{IL}	LED-EN/DPWM and PWM/APWM input from system microcontroller 0 V / 5 V, 3.3 V compliant			1.5	V
	V_{IH}		2.3			
PWM/APWM/DPWM Frequency	$PWM_{F(RANGE)}$	Frequency range	100		27,000	Hz
	$PWM_{D(RANGE)}$	Duty cycle range is Minimum on-time 3 µs	2		100	%
ADIM/PWM Selection Voltage	$V_{ADIM(SEL)}$		2.4		2.5	V

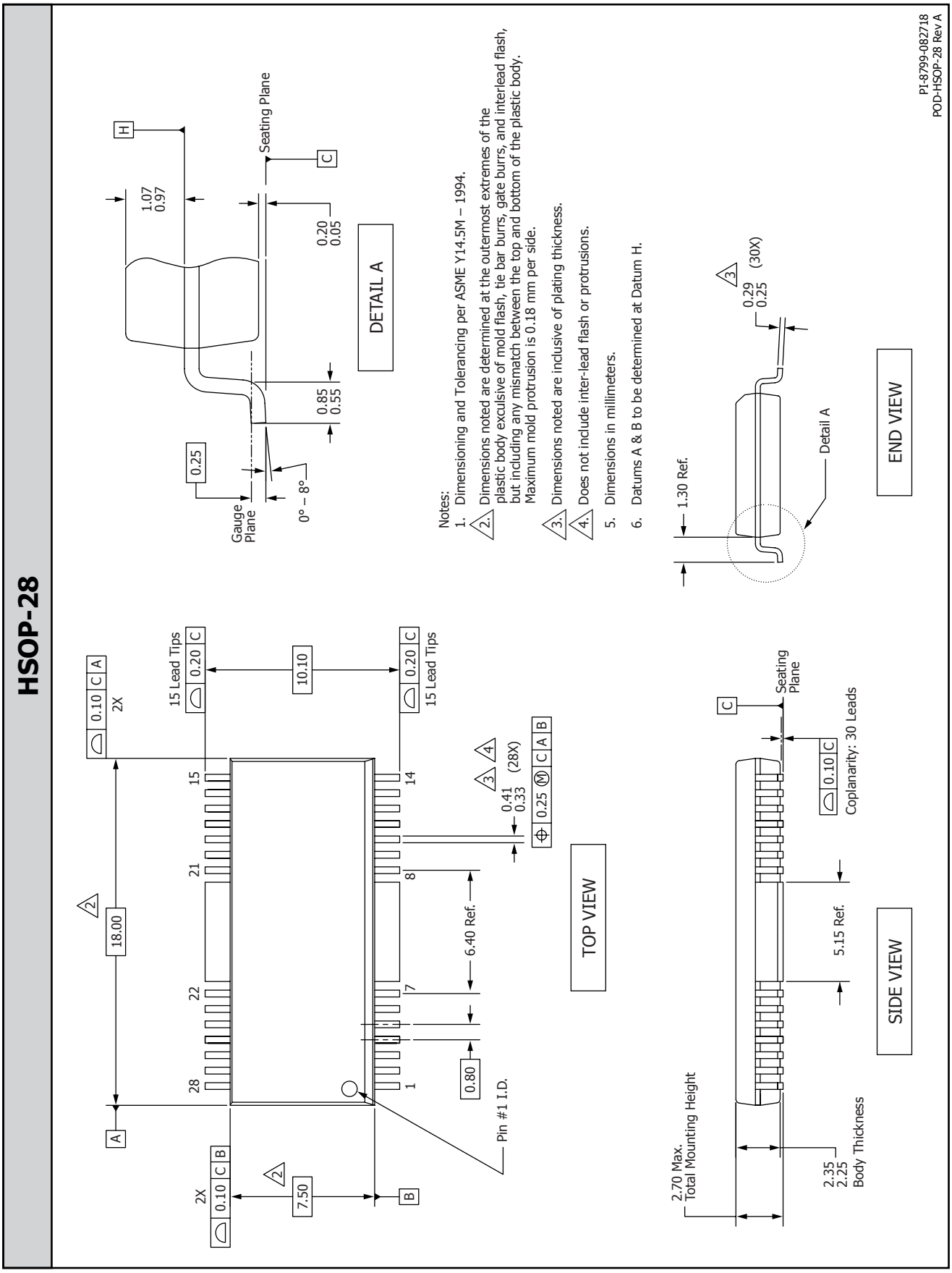
Parameter	Symbol	Conditions All Voltages Referenced to GROUND / 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
LED Control Pins (cont.)						
ADIM/LPF Maximum Voltage	V_{ADIM}	Analog dimming mode: 2% to 100% 2% brightness for V_{ADIM} = 0.03 V 100% brightness for V_{ADIM} = $V_{IS(REF)}$ Note: Minimum output current level is $I_{CC(MIN)}$				
Current Source	$I_{PWM(LPF)}$	T_J = 25 °C	19.6	20.0	20.4	µA
PWM Mode Selection Voltage	$V_{PWM(SEL)}$	$V_{ADIM(SEL)}$ < V_{ADIM} < $V_{PWM(SEL)}$ = Normal PWM V_{ADIM} > $V_{PWM(SEL)}$ = Sequenced PWM	3.8		3.9	V
IS Pin Reference Voltage	$V_{IS(REF)}$	T_J = 25 °C	1.47	1.50	1.53	V
Current Source	$I_{PWM(SEL)}$	Only enabled during start-up		-20		µA
IS Pin Current Gain	$I_{S(RATIO)}$	$I_{S(RATIO)}$ = I_{LED}/I_S I_{LED} = 100 µA T_J = 25 °C I_S = 156 µA V_{ADIM} ≈ 0.72 V	629	642	655	
Other Parameters						
PLIM Pins		Maximum power setting for V_{CV1}, V_{CV2} and V_{LED}				
PLIM Pin RC Time Constant	T_{PLIM}	External RC on P_{LIM} pins	100		250	µs
Reference Voltage	V_{REF}	T_J = 25 °C	1.194	1.218	1.242	V
OTL Protection	T_{PROT}		130	142		°C
OTL Hysteresis	T_{HYST}			67		°C
OTL Shut Down	T_{SD}			150		°C

NOTES:
A. The mismatch is calculated using the following formula: $\Delta = \pm\frac{(I_{MAX} - I_{MIN})}{2 \times I_{AVG}} \times 100\%$
B. V_CV2 must be greater than or equal to V_CV1.
C. This parameter is derived from characterization.
D. This parameter is guaranteed by design.

QFN-28

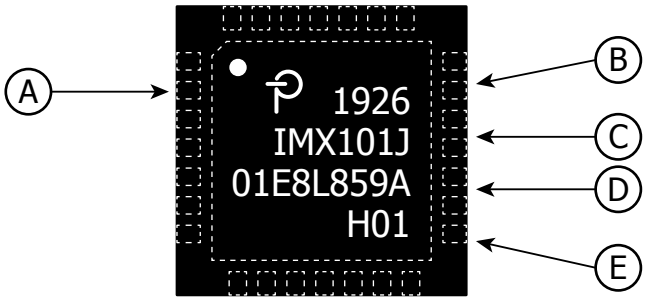

Pin #1 ID Chamfer
3.40
0.05 M C A B
0.50
0.45
0.35
28X
0.25 28X 3
0.10 M C A B
0.05 M C
BOTTOM VIEW
Pin #1 ID
(Laser Marked)
5.00
TOP VIEW
2X 0.05 C
0.08 C
29X 2
Seating Plane
0.80
0.70
0.20
Ref.
0.05
0.00
SIDE VIEW
NOTES:
1. Dimensioning and tolerancing per ASME Y14.5M – 1994.
2. Unilateral tolerance zone for coplanarity applies to the exposed pad as well as the terminals.
3. Terminal width dimension applies to the metallized terminal and is measured between 0.15 and 0.25 mm from the terminal tip.
4. Dimensions in millimeters.
PI-8949-052219
POD-QFN-28 Rev B

HSOP-28


PI-8799-082718
POD-HSOP-28 Rev A
Notes:
1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 mm per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Dimensions in millimeters.
6. Datums A & B to be determined at Datum H.
DETAIL A
Seating Plane
Gauge Plane
0° – 8°
1.07
0.97
0.20
0.05
0.85
0.55
0.25
TOP VIEW
15 Lead Tips
10.10
18.00
6.40 Ref.
0.80
Pin #1 I.D.
7.50
0.41
0.33
(28X)
END VIEW
1.30 Ref.
Detail A
0.29
0.25
(30X)
SIDE VIEW
2.70 Max.
Total Mounting Height
2.35
2.25
Body Thickness
5.15 Ref.
Coplanarity: 30 Leads

PACKAGE MARKING

QFN-28



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Extended Lot Identification Code

PI-9106-011020

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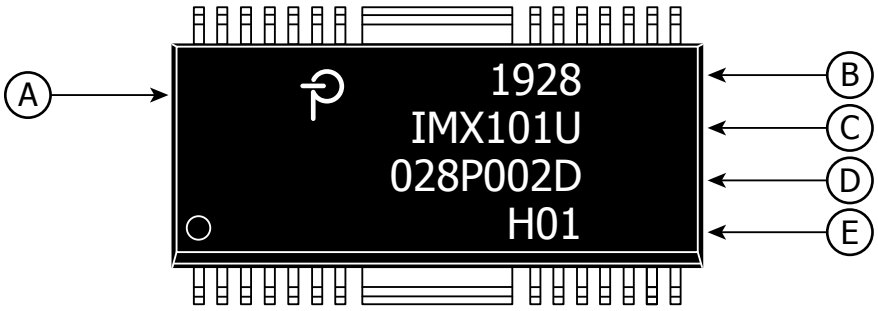
HSOP-28



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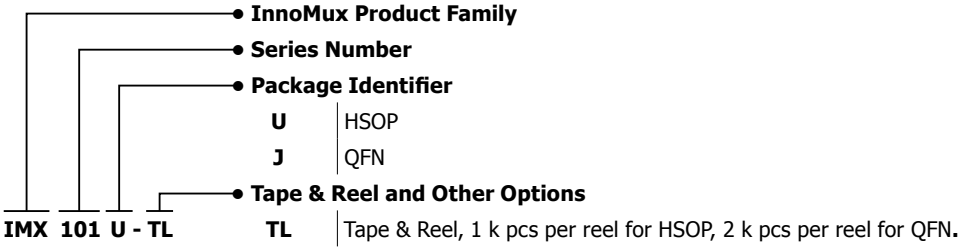
Part Ordering Information



Revision	Notes	Date
B	Code L release.	03/19
C	Code A release.	03/20
D	Added Storage Temperature data to Absolute Maximum Rating table.	11/20

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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