Title	***Reference Design Report for a 1.2 W Non-Isolated, Dual Output Buck / Buck-Derived Power Supply with Configurable Positive or Negative Outputs Using LNK304DN***
Specification	85 – 265 VAC Input, 12 V, 80 mA and 5 V, 50 mA Outputs
Application	Meters
Author	Power Integrations Applications Department
Document Number	RDR-138
Date	November 12, 2007
Revision	1.0

Summary and Features

- Compact, lightweight, low cost, low component count design provides two outputs
- Outputs configurable as both positive or one positive and one negative
- Very good cross regulation
- Integrated safety and reliability features
  - Accurate, auto-recovering, thermal shutdown function maintains safe PCB temperatures under all conditions
  - Auto-restart protects against output short circuits and lost regulation faults
- Meets CISPR-22/EN55022B limits for conducted EMI with >10 dB margin

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Table of Contents

1 Introduction 3
2 Power Supply Specification 4
3 Schematic 5
4 Circuit Description 6
4.1 AC Input Rectification and EMI Filtering 6
4.2 LinkSwitch-TN Device 6
4.3 Output Rectification and Filtering 7
4.4 Feedback Network 7
4.5 Linear Regulator 8
5 PCB Layout 9
6 Bill of Materials 10
7 Performance Data 11
7.1 Efficiency 11
7.1.1 Active Mode CEC Measurement Data 11
7.2 No-load Input Power 13
7.3 Regulation 13
7.3.1 Load and Line 13
7.3.2 Line 15
8 Thermal Performance 16
9 Waveforms 17
9.1 Drain Voltage and Current, Normal Operation 17
9.2 Output Voltage Start-up Profile 17
9.3 Source Voltage and Drain Current Start-up Profile 18
9.4 Load Transient Response (75% to 100% Load Step) 19
9.5 Output Ripple Measurements 21
9.5.1 Ripple Measurement Technique 21
9.5.2 Measurement Results 22
10 Conducted EMI 23
11 Line Surge 24
12 Revision History 25

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing both a buck and a buck-derived power supply utilizing a LNK304DN device that provides two output voltages.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

Figure 1 – Populated Circuit Board Photograph.

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.2	W	
Output						
Output Voltage 1	V_{OUT1}		12		V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$				mV	20 MHz Bandwidth
Output Current 1	I_{OUT1}		80		mA	
Output Voltage 2	V_{OUT2}		5		V	± 5%
Output Ripple Voltage 2	$V_{RIPPLE1}$				mV	20 MHz Bandwidth
Output Current 2	I_{OUT1}		50		mA	
Total Output Power						
Continuous Output Power	P_{OUT}			1.21	W	
Efficiency						
Full Load	η	52.7			%	Measured at P_{OUT} 25 °C
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	η_{CEC}[1]	51.7			%	Per California Energy Commission (CEC) / Energy Star Requirements
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge Differential Mode		1			kV	1.2/50 μs Surge, IEC 61000-4-5, Series Impedance: Differential Mode: 2 Ω
Ambient Temperature	T_{AMB}	0		50	°C	Free Convection, Sea Level

[1] CEC does not apply to this design but data are shown for reference.

3 Schematic

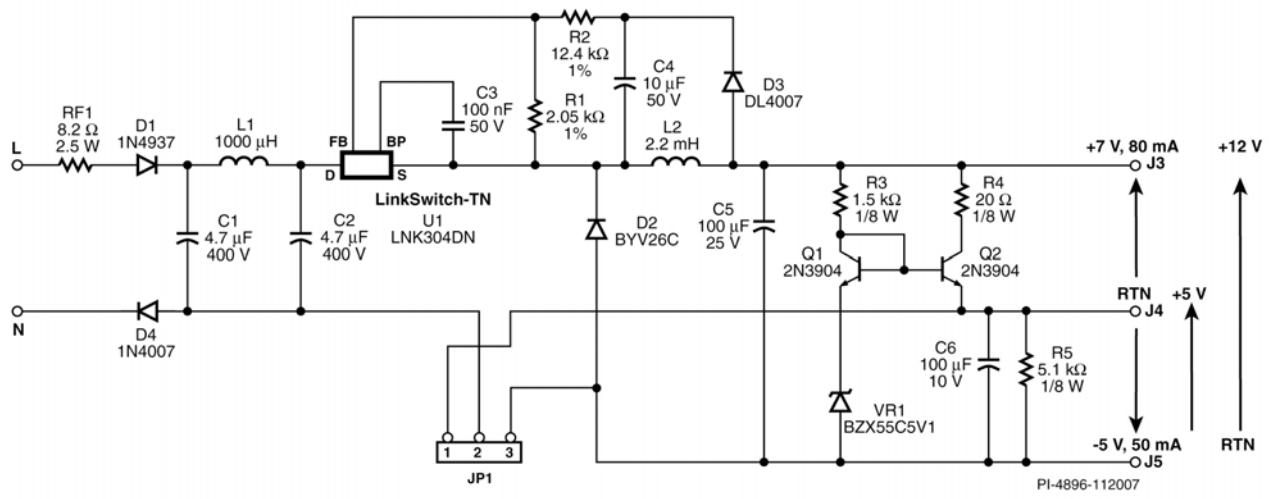

Figure 2 – Schematic.

With respect to RTN (J4), the supply provides outputs of – 5 V & +7 V with pins 1 & 2 of JP1 shorted. When pins 2 & 3 of JP1 are shorted, the supply provides +5 V and +12 V with respect to RTN (J5).

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4 Circuit Description

The power supply described has a jumper that allows for the supply to operate using either the buck topology–enabling the two outputs to be configured as positive outputs with respect to AC neutral–or a buck-derived topology–enabling one of the two outputs to be configured as a negative output with respect to AC neutral. Shorting pins 1 and 2 of JP1 will operate the supply in a buck-derived topology, while shorting pins 2 and 3 will operate the supply in the buck topology. See Figure 1 for an illustration of the two jumper positions.

While in the buck topology, the power supply has a 12 V output capable of delivering 80 mA and a 5 V output capable of 50 mA. If the supply is in the buck-derived topology, it provides a –5 V output when referenced to return and can provide 50 mA of current. The other output can be used to supply 80 mA and a 7 V output when referenced to return, or it can be configured as a floating12 V output.

The data presented in the report were taken using the buck topology with both outputs configured as positive outputs.

4.1 AC Input Rectification and EMI Filtering

The AC input is half-wave rectified by fast recovery diode D1 and general purpose diode D4. The fast recovery diode helps to improve differential mode conducted EMI. A second diode, D4, is placed in the return conductor of the supply to provide EMI noise gating. This helps minimize common mode noise and reduce EMI.

Included in the path of the AC input is a fusible flameproof resistor, RF1. In the event of a catastrophic failure, the failure mechanism of this resistor is open circuit, with no flame or smoke emitted. Additionally, this resistor is wire wound to prevent premature failure due to the inrush currents when AC is applied.

The input stage is completed by capacitors C1 and C2, which provide bulk energy storage. Inductor L1 forms a π-filter with the bulk capacitors, which helps to minimize differential mode conducted EMI.

4.2 LinkSwitch-TN Device

LinkSwitch-TN is a low-cost, full-featured monolithic IC integrating both the control circuitry and high voltage MOSFET switch into the same device. Some of the most prominent features of the device include an On/Off type controller, a maximum switching frequency of 66 kHz, which includes ±4 kHz of frequency jitter to help reduce EMI and a 700 V MOSFET. The LinkSwitch-TN device also includes a number of protection features, including output short-circuit protection, open loop fault protection, MOSFET current limit protection and thermal shutdown with hysteresis. The device is powered from the drain pin with local supply decoupling provided by the 100 nF capacitor C3 connected to the bypass pin (BP) of the LinkSwitch-TN device, U1.

4.3 Output Rectification and Filtering

During U1's conduction time, current through inductor L2 linearly ramps up, delivering energy to the load and to capacitor C5. During U1's on time, the energy from the inductor is also used by the linear regulator circuitry.

During U1's off time, the voltage across inductor L2 changes its polarity in an attempt to maintain current flow and thus forward biases freewheeling diode D2. During D2's conduction time, the energy stored in the inductor is delivered to capacitor C5, the load, and the linear regulator while the current through the inductor ramps downward.

Freewheeling diode D2 provides output rectification and should be an ultrafast type diode, such as UF4005 with a reverse recovery time t_{rr} ≤75 ns (In this case the BYV26C was used to improve efficiency). This is a sufficient reverse recovery time as this design operates in the mostly discontinuous operating mode (MDCM). Slower diodes result in large leading edge current spikes, which will result in prematurely terminated switching cycles due to exceeding the device's internal current limit. This diode should also be able to withstand the maximum DC bus voltage plus an appropriate margin (usually at least 25%).

4.4 Feedback Network

As previously mentioned, the LinkSwitch-TN family of devices uses a simple and efficient On/Off control scheme. The on time of the MOSFET is determined by the output inductor's value, the current limit of the device and the value of the DC bus voltage. This is due to the use of the On/Off control scheme, which turns off the device once the current limit is reached.

The device will therefore reach its internal current limit during every enabled switching cycle. Thus the output voltage is regulated by disabling (skipping) switching cycles. Switching cycles are skipped whenever current in excess of 49 µA is delivered into the feedback (FB) pin.

A feedback signal is derived from the output (the voltage across C5) through a simple voltage divider formed by 1 % tolerance metal film resistors R1 and R2. The input signal to this voltage divider is the voltage on capacitor C4, which closely tracks the output voltage and is charged whenever diode D3 is forward biased.

Diode D3 is necessary to prevent the FB pin from delivering current to the output whenever the MOSFET is conducting, since the FB pin has a voltage of 1.65 V + V_{SOURCE}. The voltage divider does not need to take into account D3's forward voltage drop because, to a first order, D2 and D3's forward voltages are equal, and thus the feedback network tracks the output voltage.

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4.5 Linear Regulator

LinkSwitch-TN regulates the voltage across C5 (J5 to J3) to be 12 V. To create a second regulated output, a linear regulator was used.

The linear regulator acts to keep the voltage at J4 centered such that the voltage from J4 to J5 is 6.9 V (12 V - 5.1 V), and -5.1 V from J4 to J5.

Zener diode VR1 defines the voltage on the emitter of Q2 (via Q1), and therefore J4, to be 5.1 V above the voltage on J5. Should this difference in voltage across J4 and J5 reduce, then the voltage on the base of Q2 rises, increasing collector and load current delivered to the -7 V output (J4 to J5) and maintaining the voltage difference.

Maximum dissipation within the linear regulator occurs when the +5 V (J4 to J5) is fully loaded. At full load of 50 mA, this dissipation can be estimated as
$P_{DQ2} = V_{CEQ2} \times I_{CQ2}$
$P_{DQ2} = 5.9\ V \times 50\ mA = 295\ mW$

Resistor R3 sets the bias current through VR1 to be ~ 4 mA, which also acts as a pre-load for the 12 V output (J5 to J3). For better efficiency and lower no-load consumption, a low test current Zener diode should be used.

An optional pre-load resistor, R5, is placed on the output to maintain better than ±5% voltage regulation on this output. As the transistors Q1 and Q2 are physically close to one another, they provide better thermal tracking by cancelling V_{BE} variations, thereby helping to maintain good regulation.

5 PCB Layout

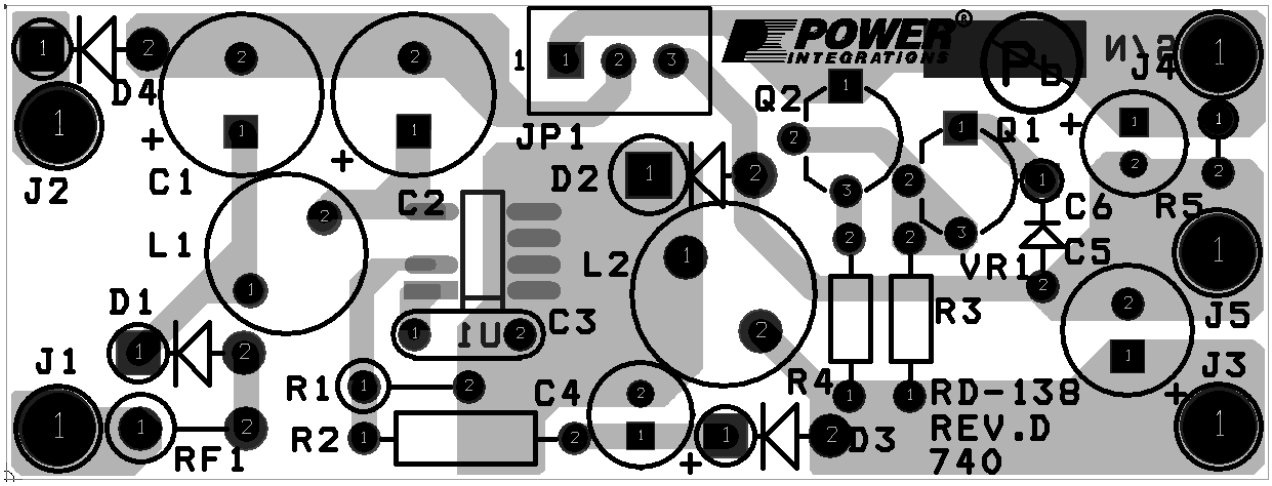

Figure 3 – Printed Circuit Layout.

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6 Bill of Materials

Item	Qty	Ref	Description	Mfg	Mfg Part Number
1	2	C1 C2	4.7 μF, 400 V, Electrolytic, (8 x 11.5)	Taicon Corporation	TAQ2G4R7MK0811MLL3
2	1	C3	100 nF, 50 V, Ceramic, Z5U, .2 Lead Space	Kemet	C317C104M5U5TA
3	1	C4	10 μF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	Nippon Chemi-Con	EKMG500ELL100ME11D
4	1	C5	100 μF, 25 V, Electrolytic, Very Low ESR, 130 mΩ, (6.3 x 11)	Nippon Chemi-Con	EKZE250ELL101MF11D
5	1	C6	100 μF, 10 V, Electrolytic, Very Low ESR, 300 mΩ, (5 x 11)	Nippon Chemi-Con	EKZE100ELL101ME11D
6	1	D1	600 V, 1 A, Fast Recovery Diode, 200 ns, DO-41	Diodes Inc.	1N4937-T
7	1	D2	600 V, 1 A, Ultrafast Recovery, 30 ns, SOD57	Philips	BYV26C
8	2	D3 D4	1000 V, 1 A, Rectifier, DO-41	Vishay	1N4007-E3/54
9	1	J1	Test Point, WHT, THRU-HOLE MOUNT	Keystone	5012
10	2	J2 J5	Test Point, BLK, THRU-HOLE MOUNT	Keystone	5011
11	1	J3	Test Point, RED, THRU-HOLE MOUNT	Keystone	5010
12	1	J4	Test Point, YEL, THRU-HOLE MOUNT	Keystone	5014
13	1	J6	SHUNT, 2 Position, ECON, PHBR 15 AU, BLACK	Amp/Tyco Elect.	382811-6
14	1	JP1	3 Position (1 x 3) header, 0.1 pitch, Vertical	Molex	22-28-4030
15	1	L1	1000 μH, 0.28 A	Tokin	SBC3-102-281
16	1	L2	2.2 mH, 0.27 A	Coilcraft	RFB0810-222L
17	2	Q1 Q2	NPN, Small Signal BJT, 40 V, 0.2 A, TO-92	Micro Commercial Components	2N3904-AP
18	1	R1	2.05 k, 1%, 1/4 W, Metal Film	Yageo	MFR-25FBF-2K05
19	1	R2	12.4 k, 1%, 1/4 W, Metal Film	Yageo	MFR-25FBF-12K4
20	1	R3	1.5 k, 5%, 1/8 W, Carbon Film	Yageo	CFR-12JB-1K5
21	1	R4	20 R, 5%, 1/8 W, Carbon Film	Yageo	CFR-12JB-20R
22	1	R5	5.1 k, 5%, 1/8 W, Carbon Film	Yageo	CFR-12JB-5K1
23	1	RF1	8.2 R, 2.5 W, Fusible/Flame Proof Wire Wound	Vitrohm	CRF253-4 5T 8R2
24	1	U1	LinkSwitch-TN, LNK304DN, SO-8	Power Integrations	LNK304DN
25	1	VR1	5.1 V, 500 mW, 5%, DO-35	Vishay	BZX55C5V1

All Parts shown are RoHS compliant

7 Performance Data

All measurements performed at room temperature, 60 Hz input frequency.

7.1 Efficiency

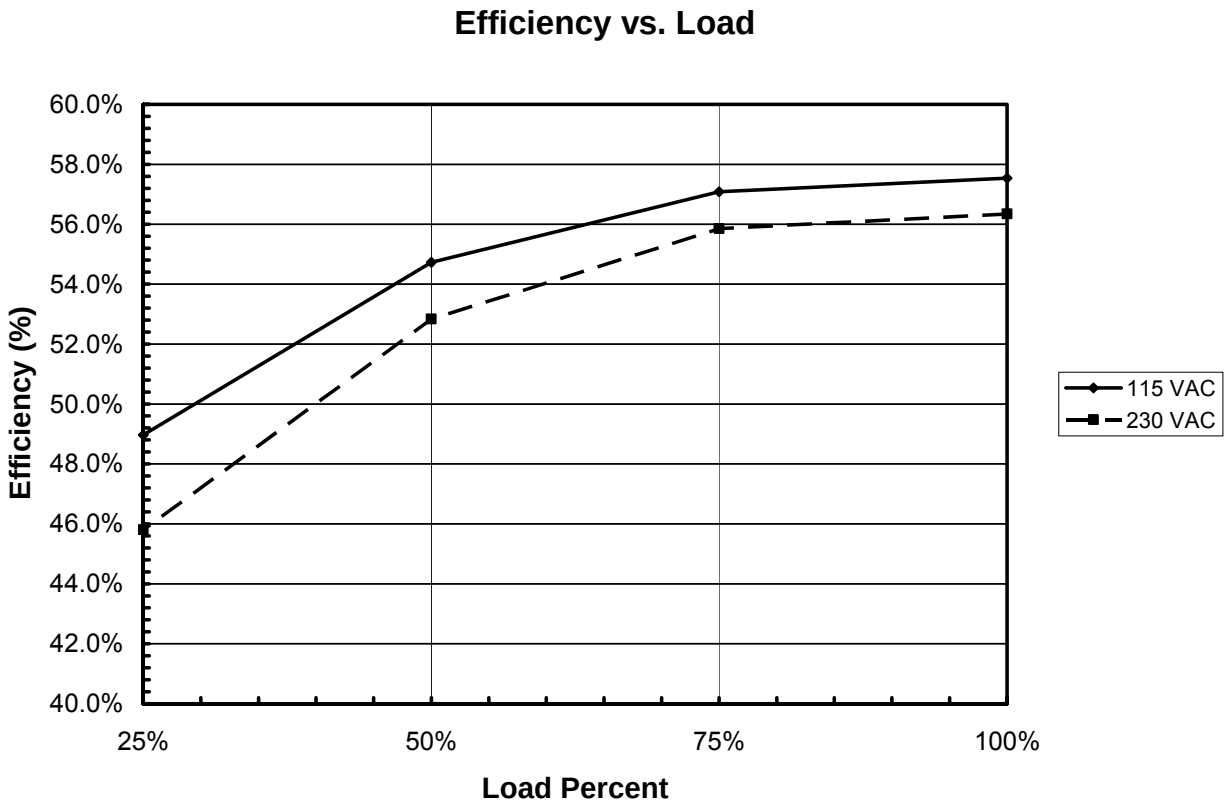

Figure 4 – Efficiency vs. Output Power, Room Temperature, 60 Hz.

7.1.1 Active Mode CEC Measurement Data

All single output adapters, including those provided with products, for sale in California after July 1st, 2008, must meet the California Energy Commission (CEC) requirement for minimum active mode efficiency and no load input power. Minimum active mode efficiency is defined as the average efficiency of 25, 50, 75 and 100% of rated output power with the limit based on the nameplate output power:

Nameplate Output (P_O)	Minimum Efficiency in Active Mode of Operation
< 1 W	$0.50 \times P_O$
≥ 1 W to ≤ 49 W	$0.09 \times \ln(P_O) + 0.50$ [ln = natural log]
> 49 W	0.85

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For adapters that are single input voltage only, the measurement is made at the rated single nominal input voltage (115 VAC or 230 VAC); for universal input adapters, the measurement is made at both nominal input voltages (115 VAC and 230 VAC).

To meet the standard, the measured average efficiency (or efficiencies for universal input supplies) must be greater than or equal to the efficiency specified by the CEC/Energy Star standard.

Percent of Full Load	**Efficiency (%)**	
	115 VAC	**230 VAC**
25	57.5	56.3
50	57.1	55.9
75	54.7	52.8
100	49.0	45.8
Average	54.6	52.7
CEC specified minimum average efficiency (%)	51.7*	

Table 1 – CEC Efficiency Table.

*Although the CEC standard does not apply to this design, the data are provided for reference.

More states within the USA and other countries are adopting this standard. For the latest information, please visit the PI Green Room:

http://www.powerint.com/greenroom/regulations.htm

7.2 No-load Input Power

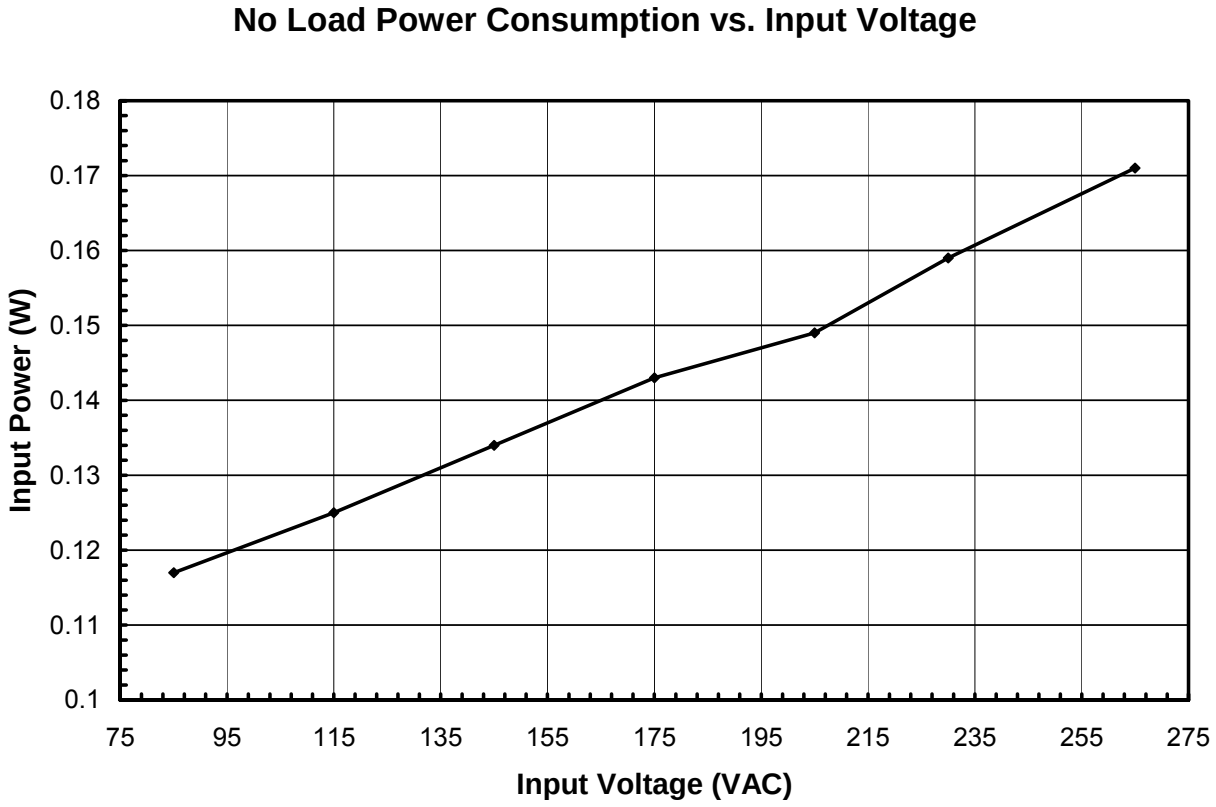

Figure 5 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

7.3 Regulation

7.3.1 Load and Line

5 V Output

The 12 V output was loaded to $I_{O(12VMIN)}$, and the 5 V load current was swept from $I_{O(5VMIN)}$ to $I_{O(5VMAX)}$. This was then repeated while 12 V output was loaded to $I_{O(12VMAX)}$.

12 V Output

The 5 V output was loaded to $I_{O(5VMIN)}$, and the 12 V load current was swept from $I_{O(12VMIN)}$ to $I_{O(12VMAX)}$. This was then repeated while 5 V output was loaded to $I_{O(5VMAX)}$.

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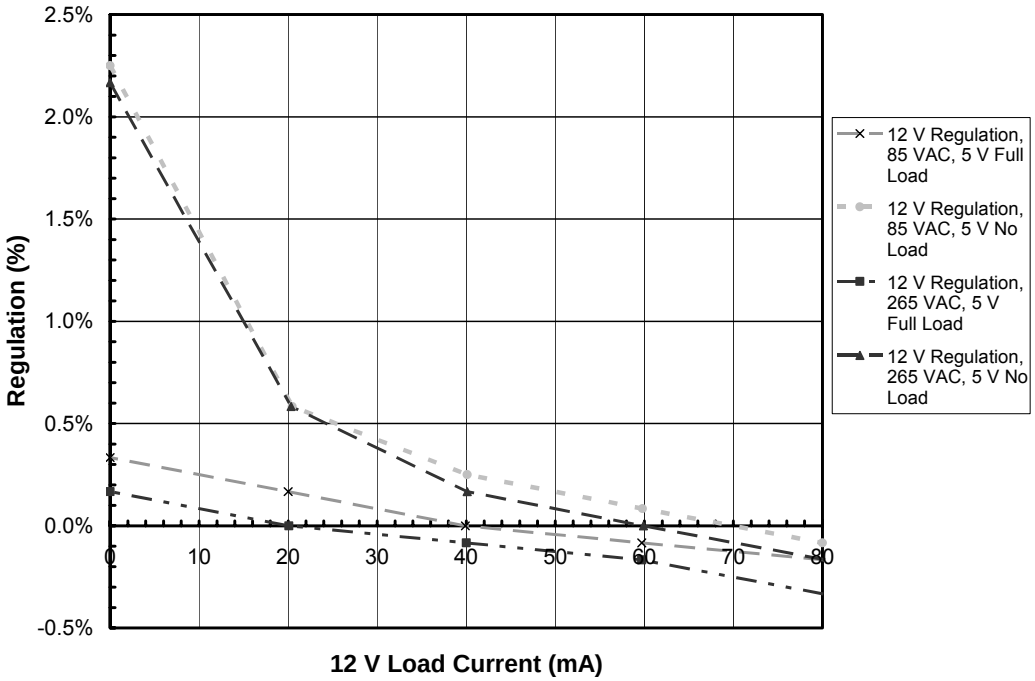

Figure 6 – 12 V Load Line and Load Regulation (5 V Min / Max Load, 85 VAC and 265 VAC), 25 ºC.

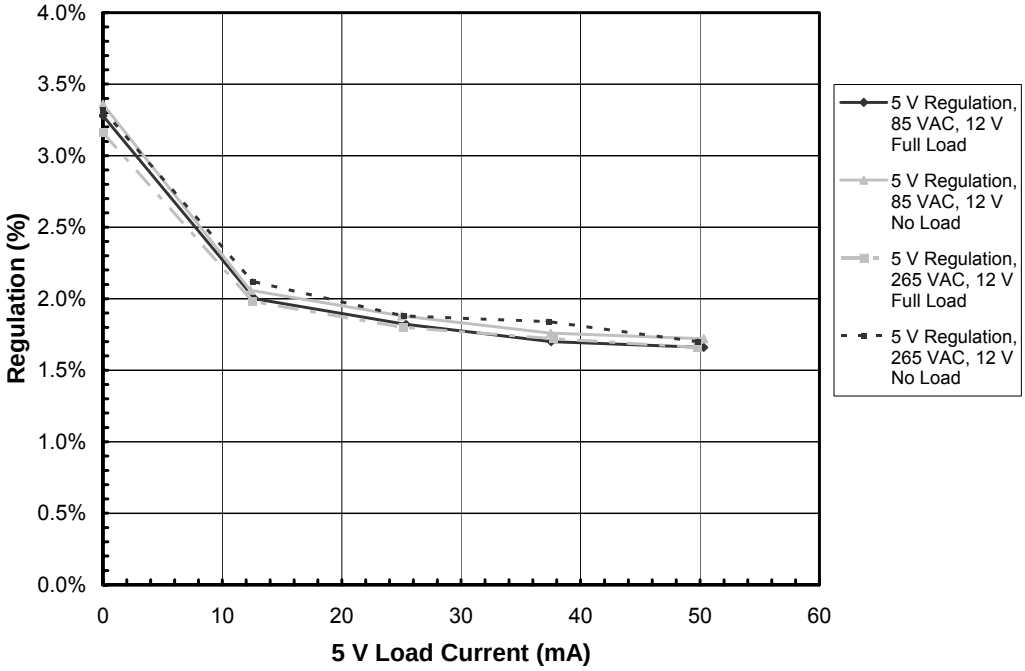

Figure 7 – 5 V Load Line and Load Regulation (12 V Min / Max Load, 85 VAC and 265 VAC), 25 ºC.

7.3.2 Line

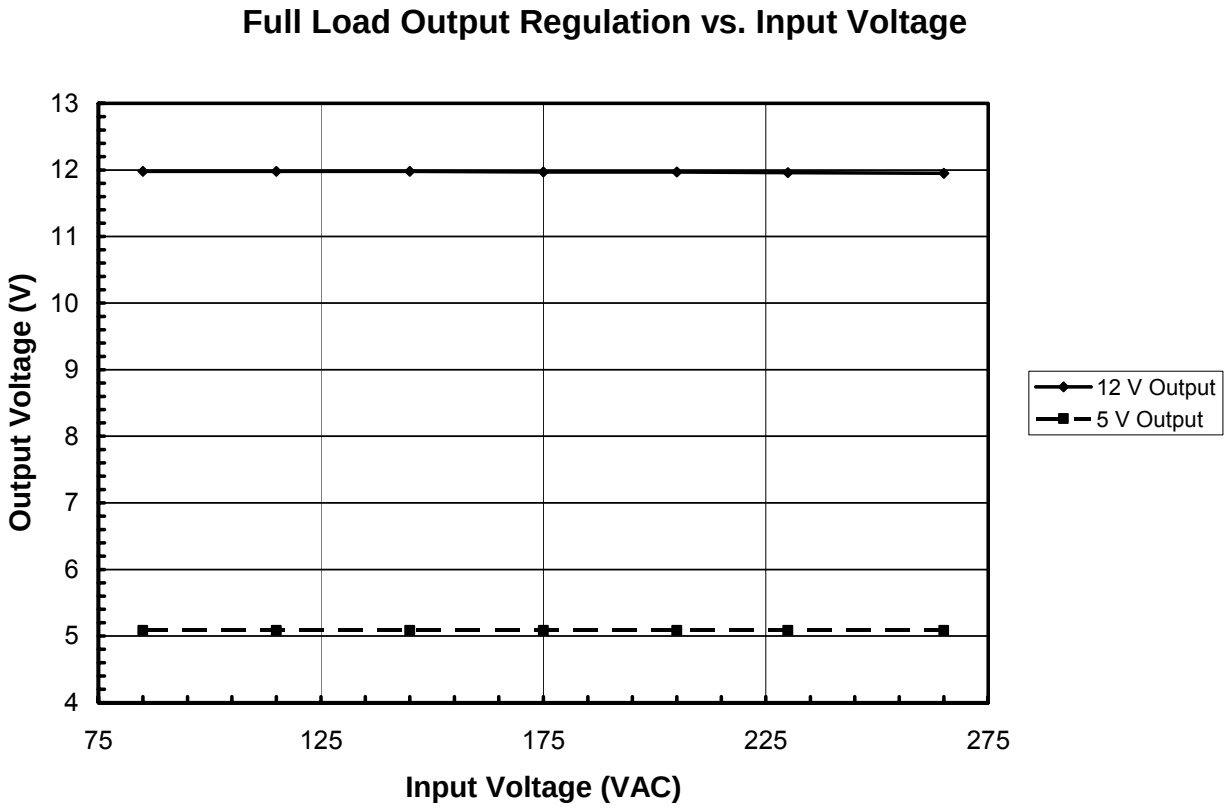

Figure 8 – Line Regulation, Room Temperature, Full Load.

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8 Thermal Performance

Table 2 shows the thermal performance at 50 ºC ambient temperature.

Item	Temperature (°C)	
	86 VAC	265 VAC
Ambient	50	50
Device (U1)	76	81
Anode of Output Diode (D2)	76	80
Collector of Transistor (Q2)	87	90
Output Inductor (L2)	73	76

Table 2 – Thermal Measurements Taken.

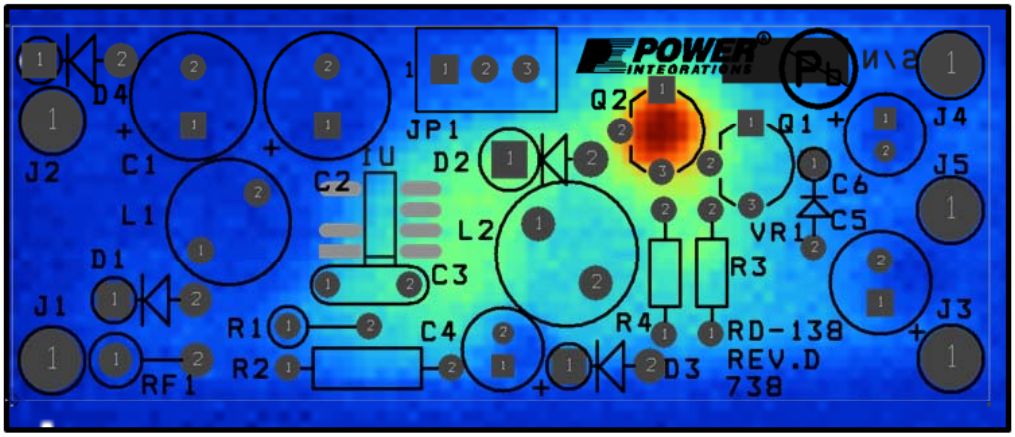

Figure 9 – Top Side Thermal Image.

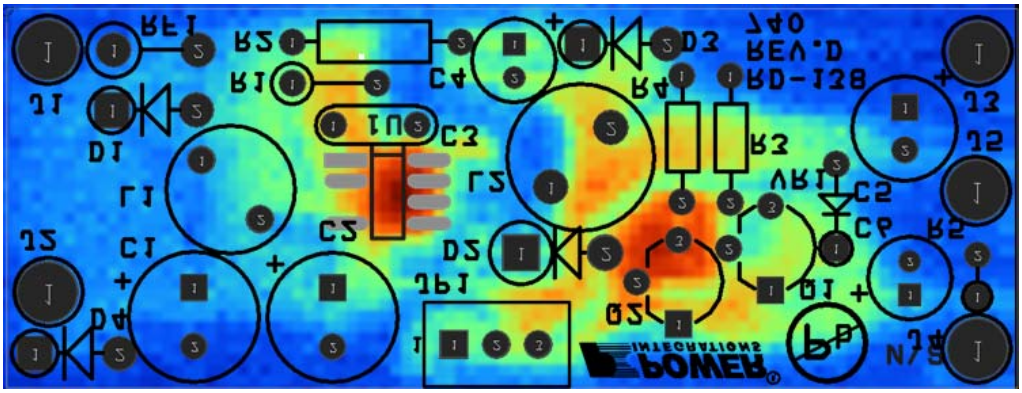

Figure 10 – Bottom Side Thermal Image.

9 Waveforms

9.1 Drain Voltage and Current, Normal Operation

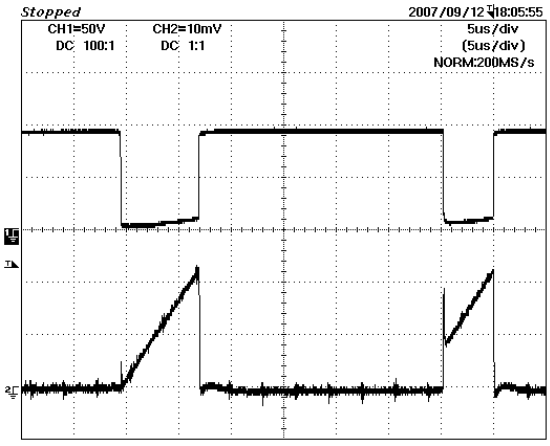

Figure 11 – 85 VAC, V_{DC} To $V_{SOURCE,}$ Full Load.
Upper: V_{SOURCE}, 50 V / div, 5 µs/div.
Lower: I_{DRAIN}, 0.1 A / div.

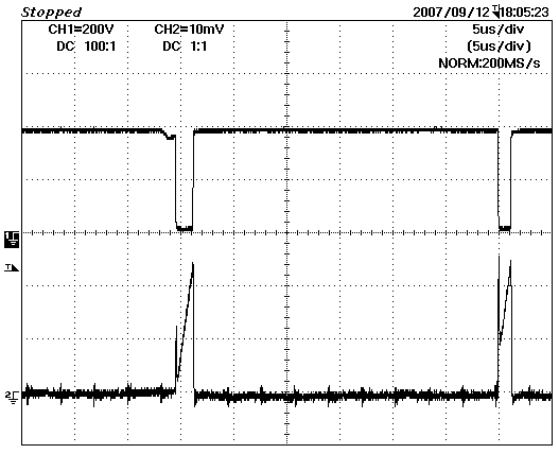

Figure 12 – 265 VAC, V_{DC} To $V_{SOURCE,}$ Full Load.
Upper: V_{SOURCE}, 200 V / div, 5 µs/div.
Lower: I_{DRAIN}, 0.1 A / div.

9.2 Output Voltage Start-up Profile

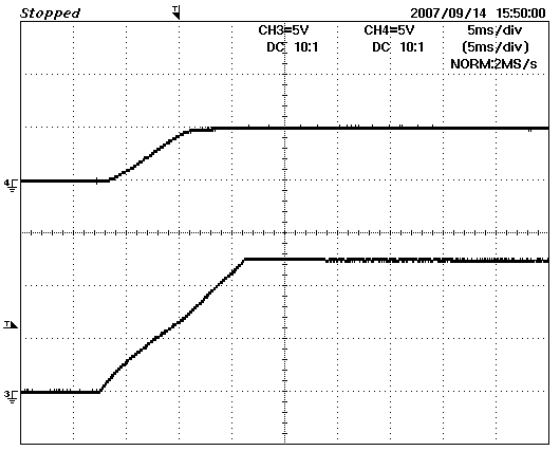

Figure 13 – Start-up Profile, 85 VAC.
Upper: 5 V Output, 5 V / div.
Lower: 12 V Output, 5 V /div.
Time base: 5 ms / div.

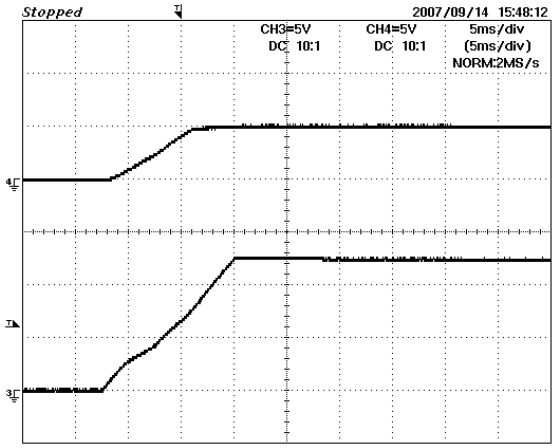

Figure 14 – Start-up Profile, 265 VAC.
Upper: 5 V Output, 5 V / div.
Lower: 12 V Output, 5 V /div.
Time base: 5 ms / div.

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9.3 Source Voltage and Drain Current Start-up Profile

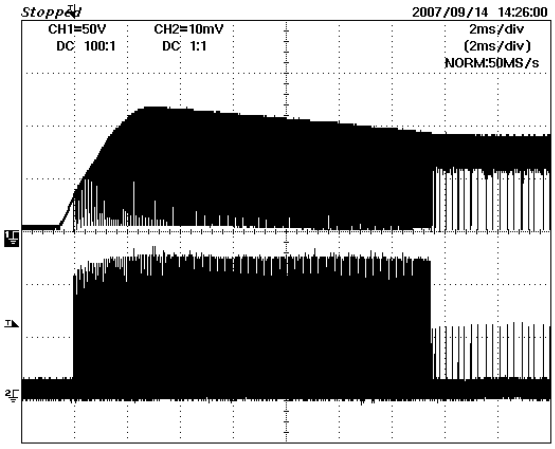

Figure 15 – 85 VAC Input and Maximum Load.
Upper: V_{DC} To V_{SOURCE}, 50 V.
Lower: I_{DRAIN}, 0.2 A / div.
Time base: 2 ms / div.

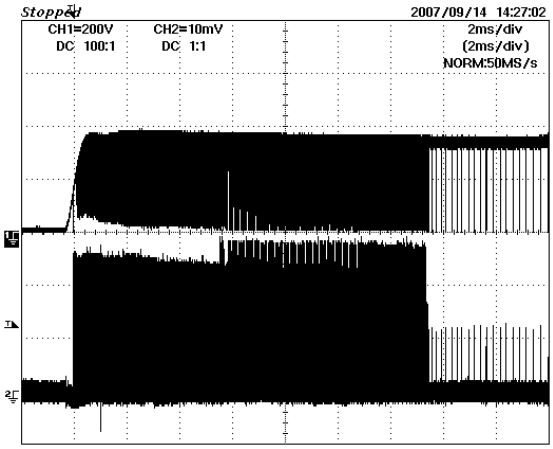

Figure 16 – 265 VAC Input and Maximum Load.
Upper: V_{DC} To V_{SOURCE}, 200 V.
Lower: I_{DRAIN}, 0.2 A / div.

9.4 Load Transient Response (75% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.

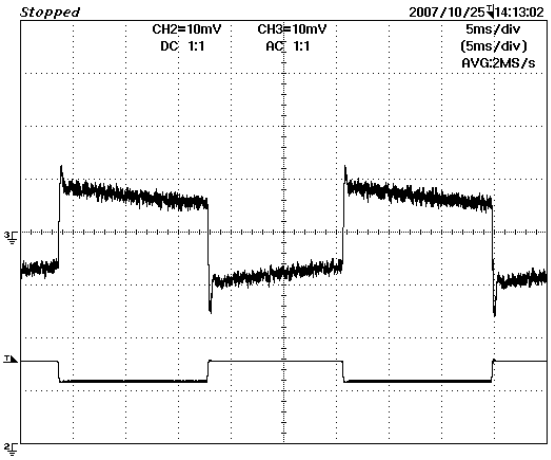

Figure 17 – Transient Response, 85 VAC.
75-100-75% Load Step. On 12 V Output.
Upper: 12 V Output, 10 mV / div.
Lower: 12 V Load Current 50 mA / div.
Timebase: 5 ms / div.

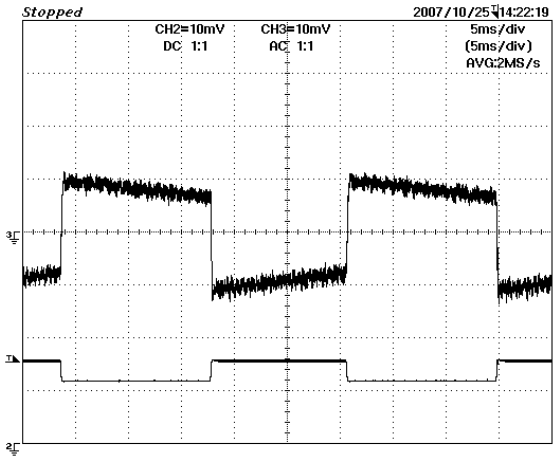

Figure 18 – Transient Response, 265 VAC.
75-100-75% Load Step On 12 V Output.
Upper: 5 V Output, 10 mV / div.
Bottom: 12 V Load Current 50 mA / div.
Timebase: 5 ms / div.

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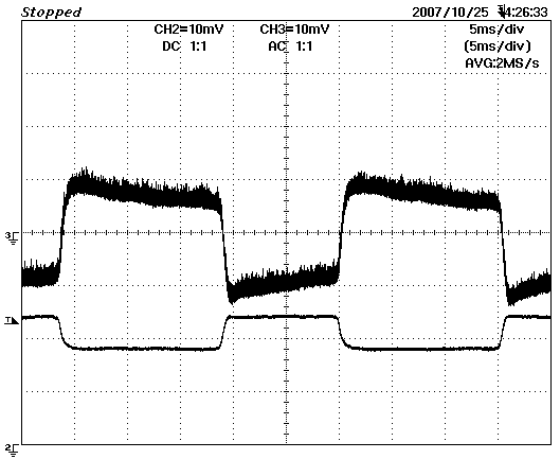

Figure 19 – Transient Response, 85 VAC.
75-100-75% Load Step on 5 V Output.
Upper: 5 V Output, 10 mV / div.
Lower: 5 V Load Current 20 mA / div.
Timebase: 5 ms / div.

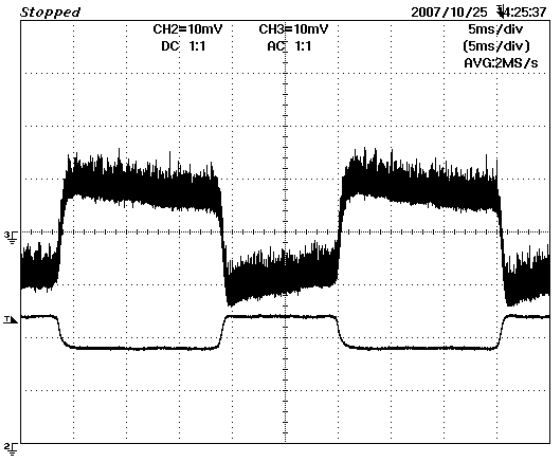

Figure 20 – Transient Response, 265 VAC.
75-100-75% Load Step on 5 V Output.
Upper: 5 V Output, 10 mV / div.
Lower: 5 V Load Current 20 mA / div.
Timebase: 5 ms / div.

9.5 Output Ripple Measurements

9.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 21 and Figure 22.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic type. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

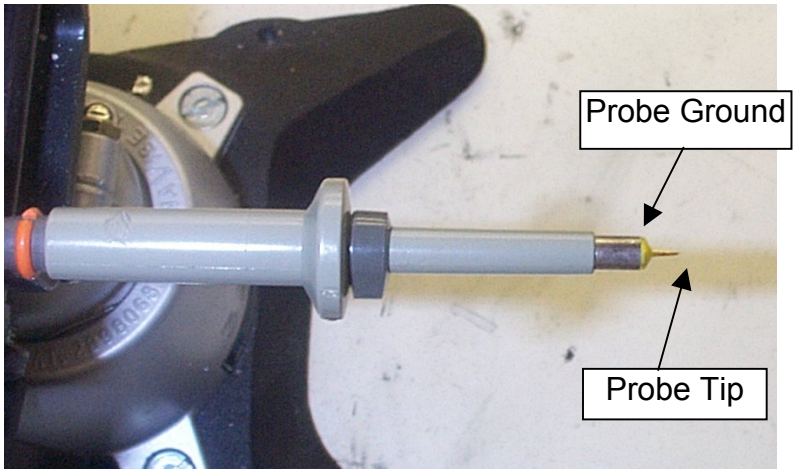

Figure 21 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

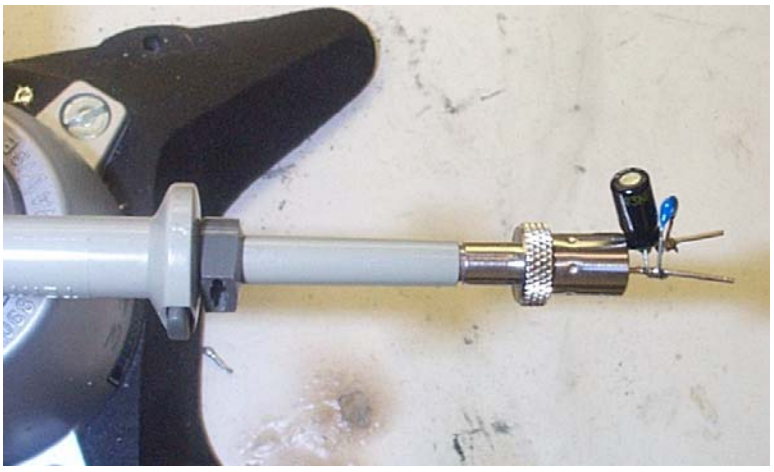

Figure 22 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter.
(Modified with Wires for Ripple Measurement, and Two Parallel Decoupling Capacitors Added)

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9.5.2 Measurement Results

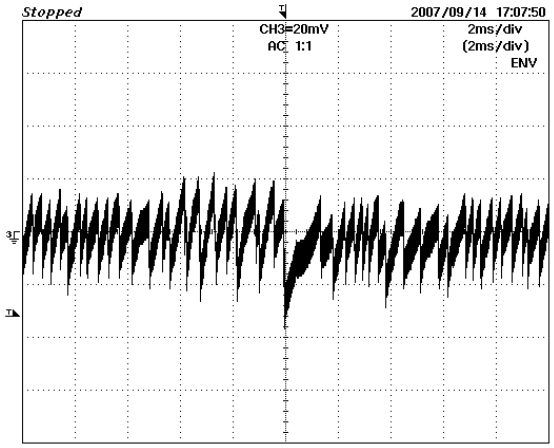

Figure 23 – 12 V Ripple, 85 VAC, Full Load.
20 mV / div, 2 ms / div.

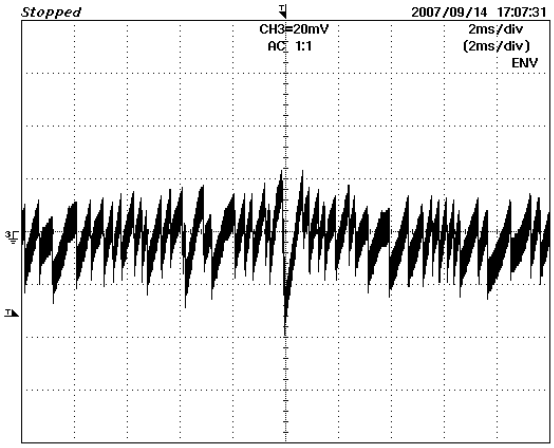

Figure 24 – 12 V Ripple, 265 VAC, Full Load.
20 mV / div, 2 ms / div.

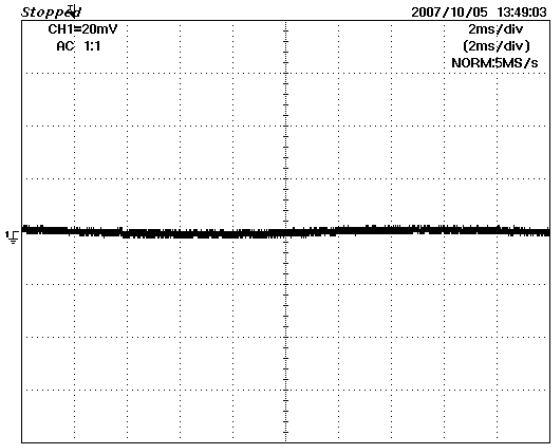

Figure 25 – 5 V Ripple, 85 VAC, Full Load.
2 ms, 20 mV /div.

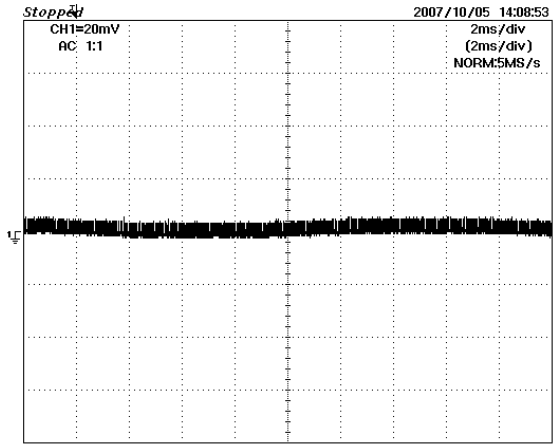

Figure 26 – 5 V Ripple, 265 VAC, Full Load.
2 ms, 20 mV /div.

10 Conducted EMI

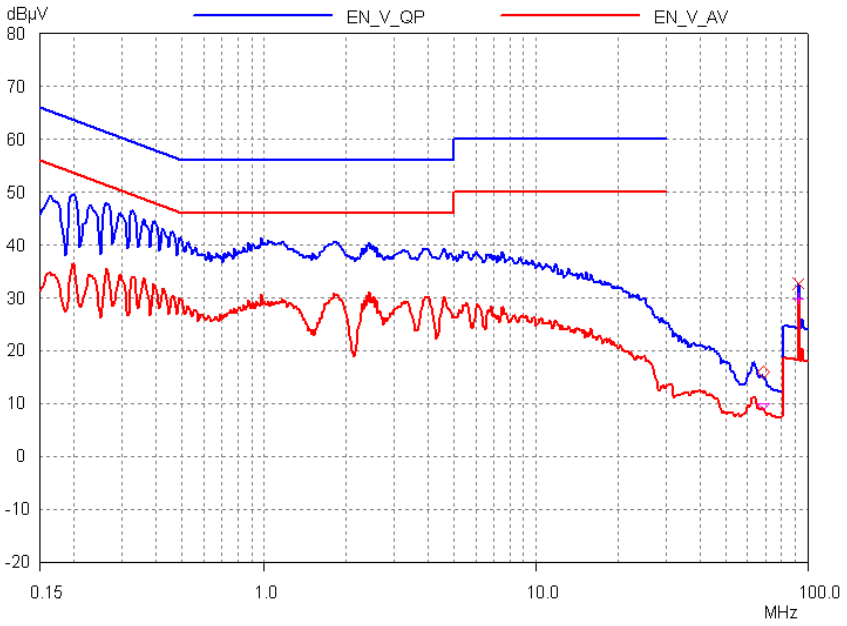

Figure 27 – Worst Case Conducted EMI, Measured at Full Load, 230 VAC Input, 60 Hz, Neutral Conductor, EN55022B Limits Shown.

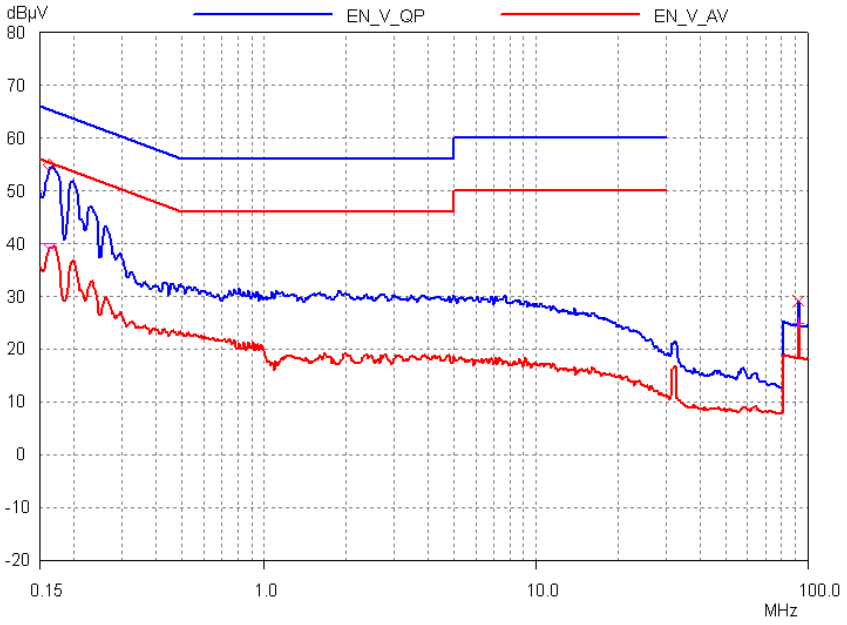

Figure 28 – Worst Case Conducted EMI, Measured at Full Load, 115 VAC Input, 60 Hz, Neutral Conductor, EN55022B Limits Shown.

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11 Line Surge

Differential and Common mode 1.2/50 μs surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load, and operation was verified following each surge event.

Event	Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
1	+1000	230	L to N	90	Pass
2	+1000	230	L to N	90	Pass
3	+1000	230	L to N	90	Pass
4	+1000	230	L to N	90	Pass
5	+1000	230	L to N	90	Pass
6	+1000	230	L to N	90	Pass
7	+1000	230	L to N	90	Pass
8	+1000	230	L to N	90	Pass
9	+1000	230	L to N	90	Pass
10	+1000	230	L to N	90	Pass
1	-1000	230	L to N	270	Pass
2	-1000	230	L to N	270	Pass
3	-1000	230	L to N	270	Pass
4	-1000	230	L to N	270	Pass
5	-1000	230	L to N	270	Pass
6	-1000	230	L to N	270	Pass
7	-1000	230	L to N	270	Pass
8	-1000	230	L to N	270	Pass
9	-1000	230	L to N	270	Pass
10	-1000	230	L to N	270	Pass

Unit passes under all test conditions.

12 Revision History

Date	Author	Revision	Description & changes	Reviewed
12-Nov-07	KM	1.0	Initial Release.	

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Notes

Notes

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