Title	***Reference Design Report for a 12 W Power Supply Using TinySwitch™-4 TNY288PG***
Specification	85 VAC – 265 VAC Input, 12 V, 1 A Output
Application	TinySwitch-4 Reference Design
Author	Applications Engineering Department
Document Number	RDR-399
Date	October 9, 2015
Revision	1.2

Summary and Features

- EcoSmart™ – meets all existing and proposed energy efficiency standards including U.S. DOE EISA2007 (Level VI) and European Commission Code of Conduct (Version 5)
  - No-load consumption <140 mW at 265 VAC (no bias winding required)
  - >83% average active-mode efficiency
- BP/M capacitor value selects power MOSFET current limit for greater design flexibility
- Output overvoltage protection (OVP) using primary bias winding sensed shutdown feature
- Tightly toleranced I^2f parameter (-10%, +12%) reduces system cost
  - Increases MOSFET and magnetics power delivery
  - Reduces overload power, which lowers output diode and capacitor costs
- Integrated TinySwitch-4 Safety/Reliability features
  - Accurate (±5%), auto-recovering, hysteretic thermal shutdown function maintains safe PCB temperatures under all conditions
  - Auto-restart protects against output short-circuit and open loop fault conditions
  - >3.2 mm creepage on package enables reliable operation in high humidity and high pollution environments
- Meets EN550022 and CISPR-22 Class B conducted EMI with >12 dBµV margin
- Meets IEC61000-4-5 Class 3 AC line surge

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Important Note:
Although this board was designed to satisfy safety isolation requirements, it has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the power supply.

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1 Introduction

This report describes a universal input, 12 V, 1 A flyback power supply using a TNY288PG device from the TinySwitch-4 family of ICs. It contains the complete specification of the power supply, a detailed circuit diagram, the entire bill of materials required to build the supply, extensive documentation of the power transformer, along with test data and oscillographs of the most important electrical waveforms. The board provides a number of user configurable options which are designed to demonstrate the features and flexibility of the TinySwitch-4 family. These include easy adjustment of the device current limit for increased output power or higher efficiency operation, and a latched output overvoltage shutdown.

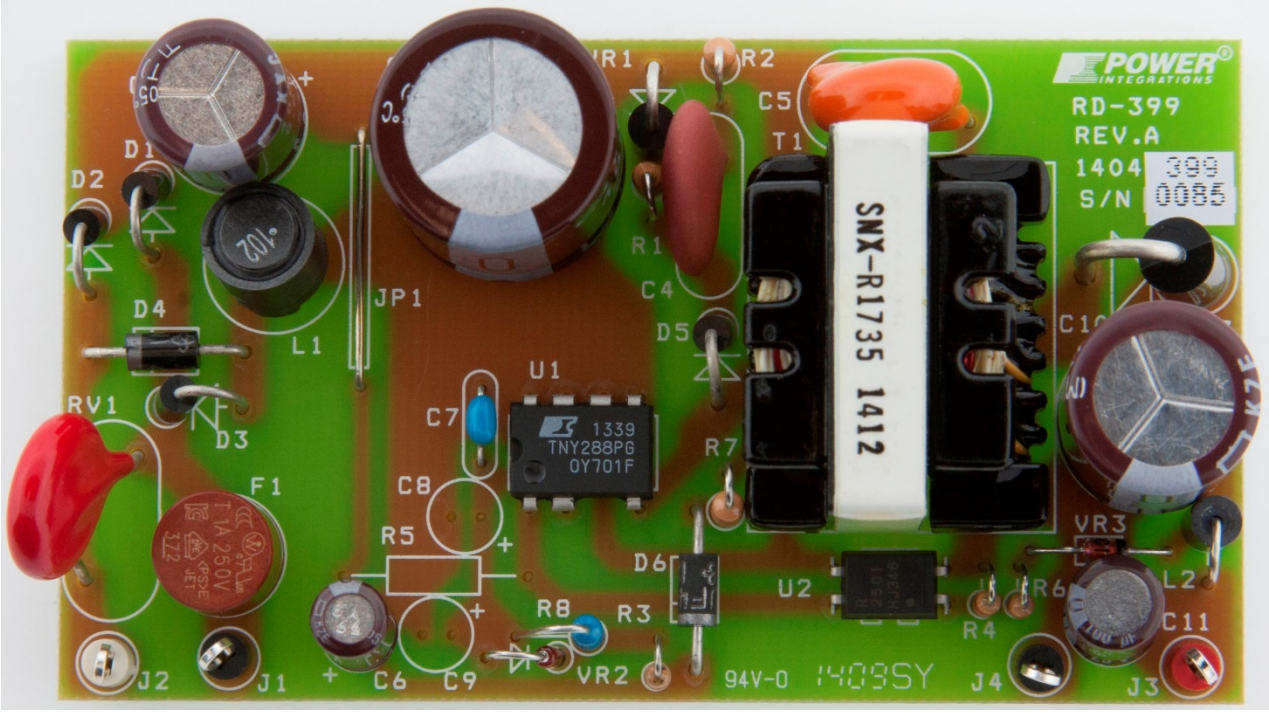

Figure 1 – RD-399 Populated Circuit Board Photograph.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.15	W	w/o UVLO resistor or bias winding
No-load Input Power (230 VAC)				0.025	W	With bias winding support
Output						
Output Voltage	V_{OUT}	11	12	13	V	± 8%
Output Ripple Voltage	V_{RIPPLE}			100	mV	20 MHz bandwidth
Output Current	I_{OUT}	1			A	
Total Output Power						
Continuous Output Power	P_{OUT}	12			W	
Overvoltage Shutdown	V_{OV}	15		18	V	With bias sense
Efficiency						
Full Load	η	84			%	Measured at P_{OUT} 25 °C
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	η_{DOE}	83			%	Per DOE EISA2007 (Level VI) with TNY278 & standard current limit
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge (Differential)		1			kV	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
Surge (Common mode)		2			kV	
Ambient Temperature	T_{AMB}	0		50	°C	Free convection, sea level

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3 Schematic

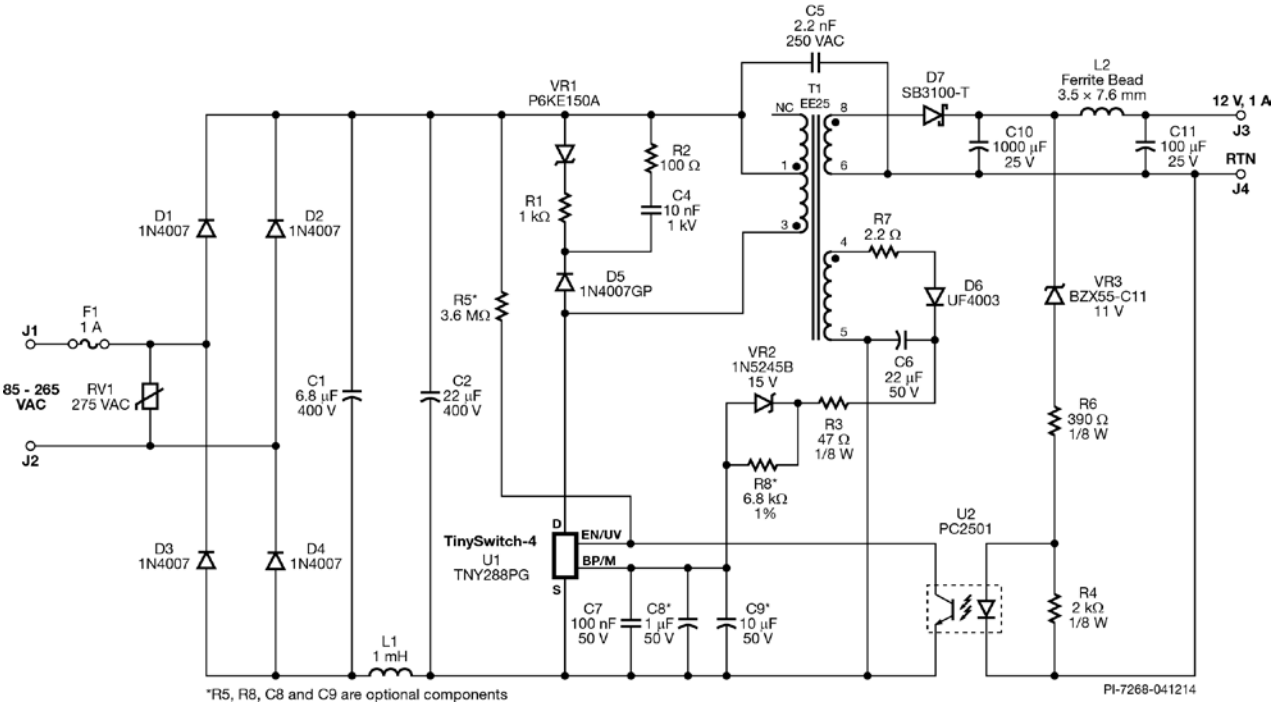

Figure 2 – Schematic.

4 Circuit Description

This circuit is configured as a flyback topology power supply utilizing the TNY288PG. Secondary side constant voltage (CV) regulation is accomplished through optocoupler feedback with a Zener reference.

4.1 Input Rectification and Filtering

The AC input voltage is rectified by input bridge D1 – D4. The rectified DC is then filtered by the bulk storage capacitors C1 and C2. Inductor L1, C1 and C2 form an input pi filter, which attenuates differential mode conducted EMI.

4.2 TNY288PG Operation

The TNY288PG device U1 integrates the power switching device, oscillator, control, startup, and protection functions.

The rectified and filtered input voltage is applied to the primary winding of T1. One side of the power transformer (T1) primary winding is connected to the positive leg of C2, and the other side is connected to the DRAIN (D) pin of U1. At the start of a switching cycle, the controller turns the power MOSFET on and current ramps up in the primary winding, delivering energy from bulk capacitor to transformer. When that current reaches the limit threshold, the controller turns the power MOSFET off. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy is delivered to the output capacitor during flyback time.

When the power MOSFET turns off, the leakage inductance of the transformer induces a voltage spike on the drain node. The amplitude of that spike is limited by an RCD clamp network that consists of D5, C4 and R2. Resistor R2 and R1 not only damp the high frequency leakage ring that occurs when the power MOSFET turns off, but also limit the reverse current through D5 when the power MOSFET turns on. This allows a slow, low-cost, glass passivated diode (with a recovery time of $\leq$2 μs.) to be used for D5. The slow diode also improves conducted EMI and efficiency. Zener diode VR1 defines the lowest voltage across C4 when the average switching frequency is low, preventing the clamp becoming a significant load. This increases light load efficiency and reduces standby input power. As the current through VR1 is limited by R1 a low cost standard Zener may be used in place of the TVS type shown.

Using ON/OFF control, U1 skips switching cycles to regulate the output voltage, based on feedback to its ENABLE/UNDERVOLTAGE (EN/UV) pin. The EN/UV pin current is sampled, just prior to each switching cycle, to determine if that switching cycle should be enabled or disabled. If the EN/UV pin current is <115 μA, the next switching cycle begins, and is terminated when the current through the MOSFET reaches the internal current limit threshold. To evenly spread switching cycles, preventing group pulsing, the EN/UV pin threshold current is modulated between 115 μA and 60 μA based on the state during the

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previous cycle. An internal state machine sets the current limit to one of 4 levels appropriate for the operating conditions, ensuring that the switching frequency remains above the audible range until the transformer flux density is low enough to prevent audible noise. This practically eliminates audible noise when standard dip varnishing of the transformer is used.

4.3 Output Rectification and Filtering

Output rectification is provided by D7. Low ESR capacitor C10 achieves minimum output voltage ripple and noise in a small can size for the rated ripple current specification.

A post filter (ferrite bead L2 and C11) attenuates noise and ripple further to meet the specification.

4.4 Feedback and Output Voltage Regulation

The supply's output voltage regulation set point is set by the voltage that develops across Zener diode VR3, R6 and the LED in optocoupler U2. The value of R4 was calculated to bias VR3 to about 0.5 mA when it goes into reverse avalanche conduction. This ensures that it is operating close to its rated knee current. Resistor R6 limits the maximum current during load transients. The values of R4 and R6 can both be varied slightly to fine-tune the output regulation set point. When the output voltage rises above the set point, the LED in U2 becomes forward biased. On the primary-side, the photo-transistor of U2 turns on and draws current out of the EN/UV pin of U1. Just before the start of each switching cycle, the controller checks the EN/UV pin current. If the current flowing out of the EN/UV pin is greater than 115 μA, that switching cycle will be disabled. As switching cycles are enabled and disabled, the output voltage is kept very close to the regulation set point. For greater output voltage regulation accuracy, a reference IC such as a TL431 can be used in place of VR3.

4.5 Output Overvoltage Shutdown

Overvoltage detection is accomplished by sensing the rectified bias winding voltage. The overvoltage threshold is the sum of VR2 and the BYPASS (BP) pin voltage (15 V + 5.8 V). When an overvoltage condition occurs such that the bias winding output voltage exceeds the threshold voltage, current begins to flow into the BYPASS pin. When this current exceeds 5 mA the internal shutdown circuit in U1 is activated. Reset is accomplished by removing input power and allowing the BYPASS pin voltage to drop below 2 V. Resistors R7 and R3 provide additional filtering of the bias voltage, with R3 also limiting the maximum current into the BYPASS pin in an OV condition

4.6 EMI Design Aspects

In addition to the simple input π filter (C1, L1 and C2) for differential mode EMI, this design makes use of shielding techniques in the transformer to reduce common mode EMI displacement currents. Resistor R2 and C4 are added to act as a damping network

to reduce high frequency transformer ringing. These techniques combined with the frequency jitter of TNY288PG gives excellent conducted and radiated EMI performance.

4.7 Peak Primary Current Limit Selection

The schematic shows three possible values for the capacitor connected to the BP/M pin, C7, C8 and C9. These different capacitor values can be used to exercise the current limit selection feature of the TinySwitch-4 family.

This feature allows the designer to select the current limit appropriate for the application.

- Nominal current limit is selected with a 0.1 μF BP/M pin capacitor and is the normal choice for typical enclosed adapter applications.
- When a 1 μF BP/M pin capacitor is used, the current limit is reduced offering reduced RMS device currents and therefore improved efficiency, at the expense of maximum power capability.
- If a 10 μF BP/M pin capacitor is used, the current limit is increased above nominal, extending the power capability for applications requiring higher power where the thermal conditions allow.

The RD-399 demonstration board comes with a 0.1 μF capacitor installed as C7, which causes U1 to select the standard current limit specified in the TinySwitch-4 data sheet. If C7 were replaced by a 1 μF capacitor (C8 in the BOM, Section 6), the current limit of U1 will be the same as the standard current limit for a TNY287PG device. If a 10 μF capacitor is installed, the current limit of U1 will be the same as the standard current limit for a TNY289PG device. The flexibility of this option enables the designer to do three things. First, it allows to measure the effect of switching to an adjacent device without actually removing and replacing the IC. Second, it allows a larger device to be used with a lower current limit, for higher efficiency. Third, it allows a smaller device to be used with a higher current limit in a design when higher power is not required on a continual basis, which effectively lowers the cost of the supply.

4.8 Undervoltage Lockout

The RD-399 circuit board has a location where an optional undervoltage (UV) lockout detection resistor (R5) can be installed. When installed, MOSFET switching is disabled at start-up until current into the EN/UV pin exceeds 25 μA. This allows the designer to set the input voltage at which MOSFET switching will be enabled by choosing the value of R5. For example, a value of 3.6 MΩ requires an input voltage of 65 VAC (92 VDC across C2) before the current into the EN/UV pin exceeds 25 μA. The UV detect function also prevents the output of the power supply from glitching (trying to restart) after output regulation is lost (during shutdown), by disabling MOSFET switching until the input voltage rises above the undervoltage lockout threshold.

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5 PCB Layout

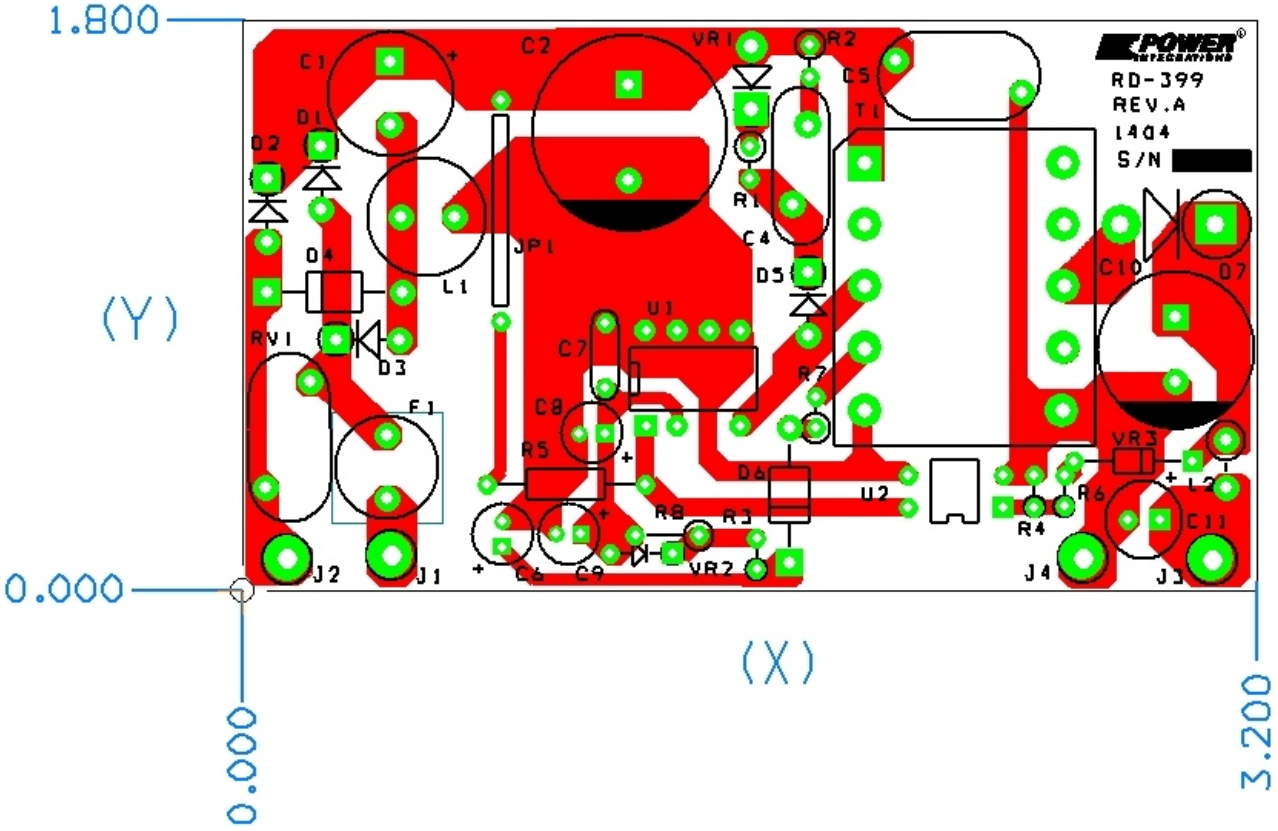

Figure 3 – Printed Circuit Board Layout (3.2 × 1.8 Inches).

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	6.8 µF, 400 V, Electrolytic, (10 x 16),	EKXG401ELL6R8MJ16S	Nippon Chemi-Con
2	1	C2	22 µF, 400 V, Electrolytic, Low ESR, 901 mΩ, (16 x 20)	EKMX401ELL220ML20S	Nippon Chemi-Con
3	1	C4	10 nF, 1 kV, Disc Ceramic	562R5HKMS10	Vishay
4	1	C5	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
5	1	C6	22 µF, 50 V, Electrolytic, Very Low ESR, 340 mΩ, (5 x 11)	EKZE500ELL220ME11D	Nippon Chemi-Con
6	1	C7	100 nF, 50 V, Ceramic, X7R	RPER71H104K2K1A03B	Murata
7	1	C8*	1 µF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG500ELL1R0ME11D	Nippon Chemi-Con
8	1	C9	10 µF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG500ELL100ME11D	Nippon Chemi-Con
9	1	C10	1000 µF, 25 V, Electrolytic, Very Low ESR, 21 mΩ, (12.5 x 20)	EKZE250ELL102MK20S	Nippon Chemi-Con
10	1	C11	100 µF, 25 V, Electrolytic, Very Low ESR, 130 mΩ, (6.3 x 11)	EKZE250ELL101MF11D	Nippon Chemi-Con
11	4	D1 D2 D3 D4	1N4007, 1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
12	1	D5	1N4007GP, 1000 V, 1 A, Rectifier, Glass Passivated, 2 us, DO-41	1N4007GP	Vishay
13	1	D6	200 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	UF4003-E3	Vishay
14	1	D7	100 V, 3 A, Schottky, DO-201AD	SB3100DICT-ND	Diodes, Inc.
15	1	F1	1 A, 250 V, Slow, TR5	37211000411	Wickman
16	2	J1 J4	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
17	1	J2	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
18	1	J3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
19	1	JP1	Wire Jumper, Non insulated, 22 AWG, 0.7 in	298	Alpha
20	1	L1	1 mH, 350 m A	744731102	Wurth
21	1	L2	3.5 mm x 7.6 mm, 75 Ohms at 25 MHz, 22 AWG hole, Ferrite Bead	2743004112	Fair-Rite
22	1	R1	1 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-1K0	Yageo
23	1	R2	100 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-100R	Yageo
24	1	R3	47 Ω, 5%, 1/8 W, Carbon Film	CF18JT47R0	Stackpole
25	1	R4	2 kΩ, 5%, 1/8 W, Carbon Film	CF18JT2K00	Stackpole
26	1	R5*	3.6 M, 5%, 1/4 W, Carbon Film	CFR-25JB-3M6	Yageo
27	1	R6	390 Ω, 5%, 1/8 W, Carbon Film	CF18JT390R	Stackpole
28	1	R7	2.2 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-2R2	Yageo
29	1	R8*	6.81 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-6K81	Yageo
30	1	RV1	275 V, 45 J, 10 mm, RADIAL	V275LA10P	Littlefuse
31	1	T1	Bobbin, 10 Pins, Vertical Transformer Transformer	YW-360-02B SNX-R1735 PNY-28812	Yih-Hwa Enterprises Santronics USA Premier Magnetics
32	1	U1	TinySwitch-4, DIP-8C	TNY288PG	Power Integrations
33	1	U2	Optocoupler, 80 V, CTR 80-160%, 4-DIP	PS2501-1-H-A	CEL
34	1	VR1	150 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE150A	LittlleFuse
35	1	VR2	15 V, 5%, 500 mW, DO-35	1N5245B-T	Diodes, Inc.
36	1	VR3	11 V, 500 mW, 5%, DO-35	BZX55C11	Vishay

*Optional components

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7 Transformer Specification

7.1 Electrical Diagram

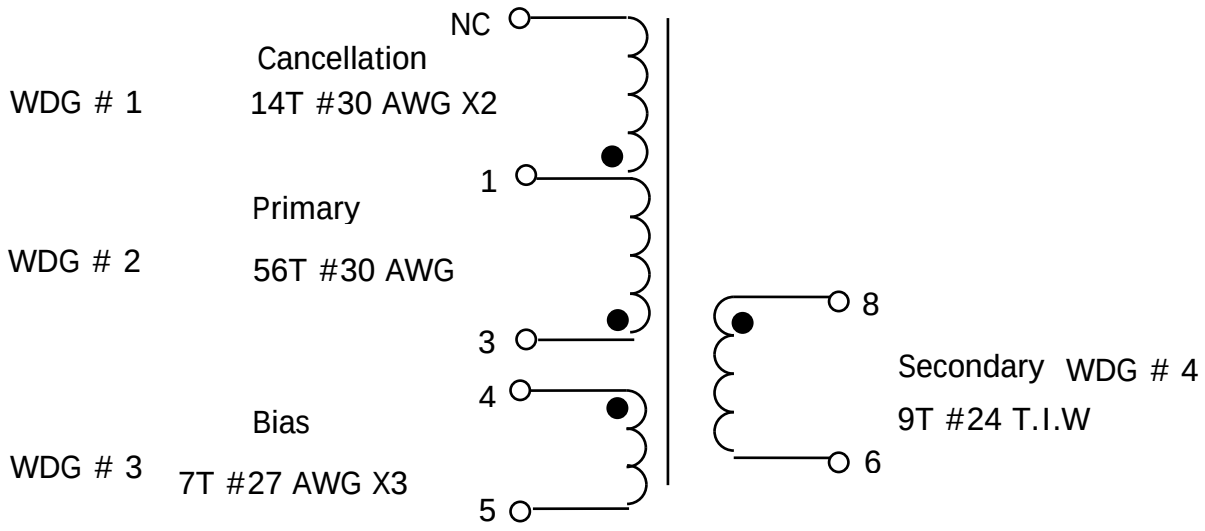

Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-5 to pins 6-10.	3000 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 $V_{RMS.}$	1189 µH ±10%
Resonant Frequency	Pins 1-3, all other windings open.	500 kHz (Min.)
Primary Leakage Inductance	Pins 1-3, with pins 6-8 shorted, measured at 100 kHz, 0.4 $V_{RMS.}$	50 µH (Max.)

7.3 Material List

Item	Description
[1]	Core: PC40EE25-Z, TDK or equivalent Gapped for A_L of 379.1 nH/$T^{2.}$
[2]	Bobbin: EE25, Vertical, 10 pin – Yih-Hwa part # YW-360-02B.
[3]	Magnet Wire: #30 AWG.
[4]	Magnet Wire: #27 AWG.
[5]	Triple Insulated Wire: #24 AWG.
[6]	Tape: 3M # 44 Polyester web. 2.0 mm wide.
[7]	Tape: 3M 1298 Polyester Film, 2.0 mils thick, 8.6 mm wide.
[8]	Tape: 3M 1298 Polyester Film, 2.0 mils thick, 10.7 mm wide.
[9]	Tape: 3M 1298 Polyester Film, 2.0 mils thick, 4.0 mm wide.
[10]	Varnish (applied by dipping only, not vacuum impregnation).

7.4 Transformer Build Diagram

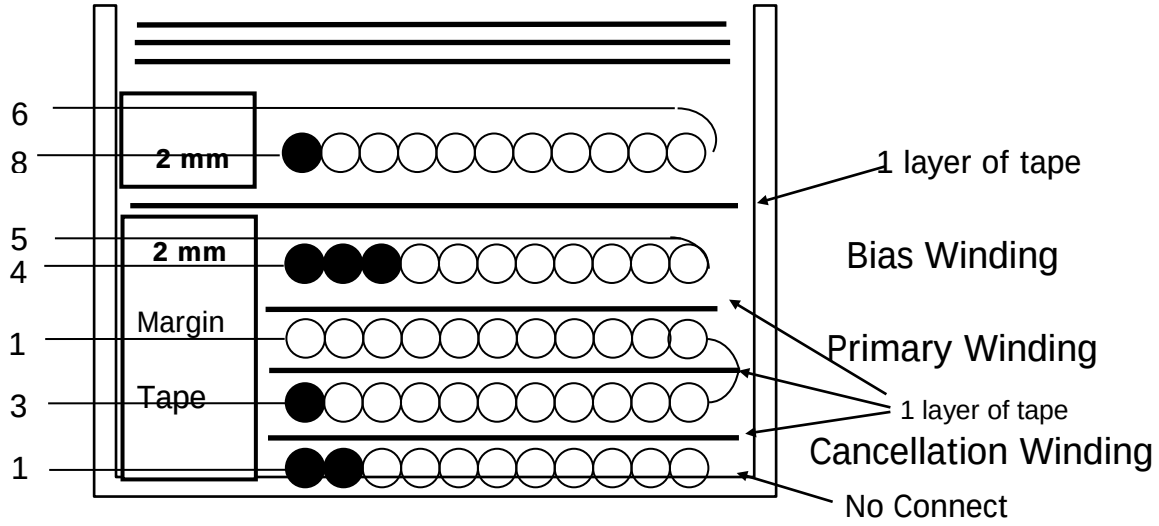

Figure 5 – Transformer Build Diagram.

7.5 Transformer Construction

Bobbin Set-Up Orientation	Set up the bobbin with its pins oriented to the left hand side.
Margin Tape	Apply 2.0 mm margin at the pin side of bobbin using item [6]. Match combined height of shield, primary, and bias windings.
WD1 Cancellation Winding	Start at pin 1. Wind 14 bifilar turns of item [3] from left to right. Wind with tight tension across entire bobbin evenly. Cut the ends of the bifilar and leave floating.
Insulation	1 layer of tape [7] for insulation.
WD #2 Primary Winding	Start at pin 3. Wind 28 turns of item [3] from left to right. Apply 1 layer of tape [7] for insulation. Wind another 28 turns from right to left. Wind with tight tension across entire bobbin evenly. Finish at pin 1.
Insulation	1 layer of tape [7] for insulation.
WD #3 Bias Winding	Start at pin 4, wind 7 trifilar turns of item [4]. Wind from left to right with tight tension. Wind uniformly, in a single layer across entire width of bobbin. Finish on pin 5.
Insulation	1 layer of tape [8] for insulation.
Margin Tape	Apply 2.0 mm margin at the pin side of bobbin using item [6]. Match combined height of secondary windings.
WD #4 Secondary Winding	Start at pin 8, wind 9 turns of item [5] from left to right. Wind uniformly, in a single layer across entire bobbin evenly. Finish on pin 6.
Outer Insulation	3 layers of tape [8] for insulation.
Core Assembly	Assemble and secure core halves using item [1] and item [9].
Varnish	Dip varnish using item [10] (do not vacuum impregnate).

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8 Transformer Design Spreadsheet

ACDC_TinySwitch-4_121812; Rev.1.1; Copyright Power Integrations 2012	INPUT	INFO	OUTPUT	UNIT	ACDC_TinySwitch-4_121812_Rev1-1.xls; TinySwitch-4 Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85		85	Volts	Minimum AC Input Voltage
VACMAX	265		265	Volts	Maximum AC Input Voltage
fL	50		50	Hertz	AC Mains Frequency
VO	12.00		12.00	Volts	Output Voltage (at continuous power)
IO	1.07		1.07	Amps	Power Supply Output Current (corresponding to peak power)
Power			12.84	Watts	Continuous Output Power
n	0.80		0.80		Efficiency Estimate at output terminals. Under 0.7 if no better data available
Z	0.50		0.50		Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC	2.77		2.77	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	28.80		28.8	uFarads	Input Capacitance
ENTER TinySwitch-4 VARIABLES					
TinySwitch-4	**TNY288P**		**TNY288P**		User-defined TinySwitch-4
Chose Configuration	**STD**		Standard Current Limit		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.512	Amps	Minimum Current Limit
ILIMITTYP			0.550	Amps	Typical Current Limit
ILIMITMAX			0.588	Amps	Maximum Current Limit
fSmin			124000	Hertz	Minimum Device Switching Frequency
I^2fmin			35.937	A^2kHz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	79.00		79	Volts	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10	Volts	TinySwitch-4 on-state Drain to Source Voltage
VD			0.7	Volts	Output Winding Diode Forward Voltage Drop
KP			0.51		Ripple to Peak Current Ratio (KP < 6)
KP_TRANSIENT			0.27		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB	10.00		10.00	Volts	Bias Winding Voltage
VDB			0.70	Volts	Bias Winding Diode Forward Voltage Drop
NB			7.09		Bias Winding Number of Turns
VZOV			16.00	Volts	Over Voltage Protection zener diode voltage.
UVLO VARIABLES					
V_UV_TARGET			87.94	Volts	Target DC under-voltage threshold, above which the power supply with start
V_UV_ACTUAL			84.70	Volts	Typical DC start-up voltage based on standard value of RUV_ACTUAL
RUV_IDEAL			3.43	Mohms	Calculated value for UV Lockout resistor
RUV_ACTUAL			3.30	Mohms	Closest standard value of resistor to RUV_IDEAL
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EE25**		**EE25**		Enter Transformer Core
Core		EE25		P/N:	PC40EE25-Z
Custom core				P/N:	EE25_BOBBIN

AE			0.404	cm^2	Core Effective Cross Sectional Area
LE			7.34	cm	Core Effective Path Length
AL			1420	nH/T^2	Ungapped Core Effective Inductance
BW			10.2	mm	Bobbin Physical Winding Width
M	1.00		1	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2.00		2		Number of Primary Layers
NS	9		9		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			80	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.53		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.23	Amps	Average Primary Current
IP			0.51	Amps	Minimum Peak Primary Current
IR			0.26	Amps	Primary Ripple Current
IRMS			0.33	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1189	uHenries	Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 1069 uH
LP_TOLERANCE	10.00		10	%	Primary inductance tolerance
NP			56		Primary Winding Number of Turns
ALG			379	nH/T^2	Gapped Core Effective Inductance
BM			3090	Gauss	Maximum Operating Flux Density, BM<3100 is recommended
BAC			783	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			2053		Relative Permeability of Ungapped Core
LG		Warning	0.10	mm	!!! INCREASE GAP>>0.1. Increase NS, increase VOR,bigger Core
BWE			16.4	mm	Effective Bobbin Width
OD			0.29	mm	Maximum Primary Wire Diameter including insulation
INS			0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.24	mm	Bare conductor diameter
AWG			31	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			81	Cmils	Bare conductor effective area in circular mils
CMA			248	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			3.18	Amps	Peak Secondary Current
ISRMS			1.91	Amps	Secondary RMS Current
IRIPPLE			1.58	Amps	Output Capacitor RMS Ripple Current
CMS			381	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			24	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			561	Volts	Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance)
PIVS			72	Volts	Output Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					

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VO1			12	Volts	Main Output Voltage (if unused, defaults to single output design)
IO1			1.070	Amps	Output DC Current
PO1			12.84	Watts	Output Power
VD1			0.7	Volts	Output Diode Forward Voltage Drop
NS1			9.00		Output Winding Number of Turns
ISRMS1			1.907	Amps	Output Winding RMS Current
IRIPPLE1			1.58	Amps	Output Capacitor RMS Ripple Current
PIVS1			72	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			1N5820, SB320		Recommended Diodes for this output
CMS1			381	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			24	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.51	mm	Minimum Bare Conductor Diameter
ODS1			0.91	mm	Maximum Outside Diameter for Triple Insulated Wire

Note: Warning shown for gap size should be ignored. It is the result of rounding of the parameter.

9 Performance Data

The ON/OFF control scheme employed by TinySwitch-4 yields virtually constant efficiency across the 25% to 100% load range required for compliance with worldwide energy efficiency standards for external power supplies (EPS). Even at loads below 10% of the supply's full rated output power, efficiency remains above 70%, providing excellent standby performance for applications that require it. This performance is automatic with ON/OFF control. There are no special burst modes that require the designer to consider specific thresholds within the load range in order to achieve compliance with global energy efficiency standards.

All measurements performed at room temperature, 60 Hz input frequency.

9.1 Efficiency

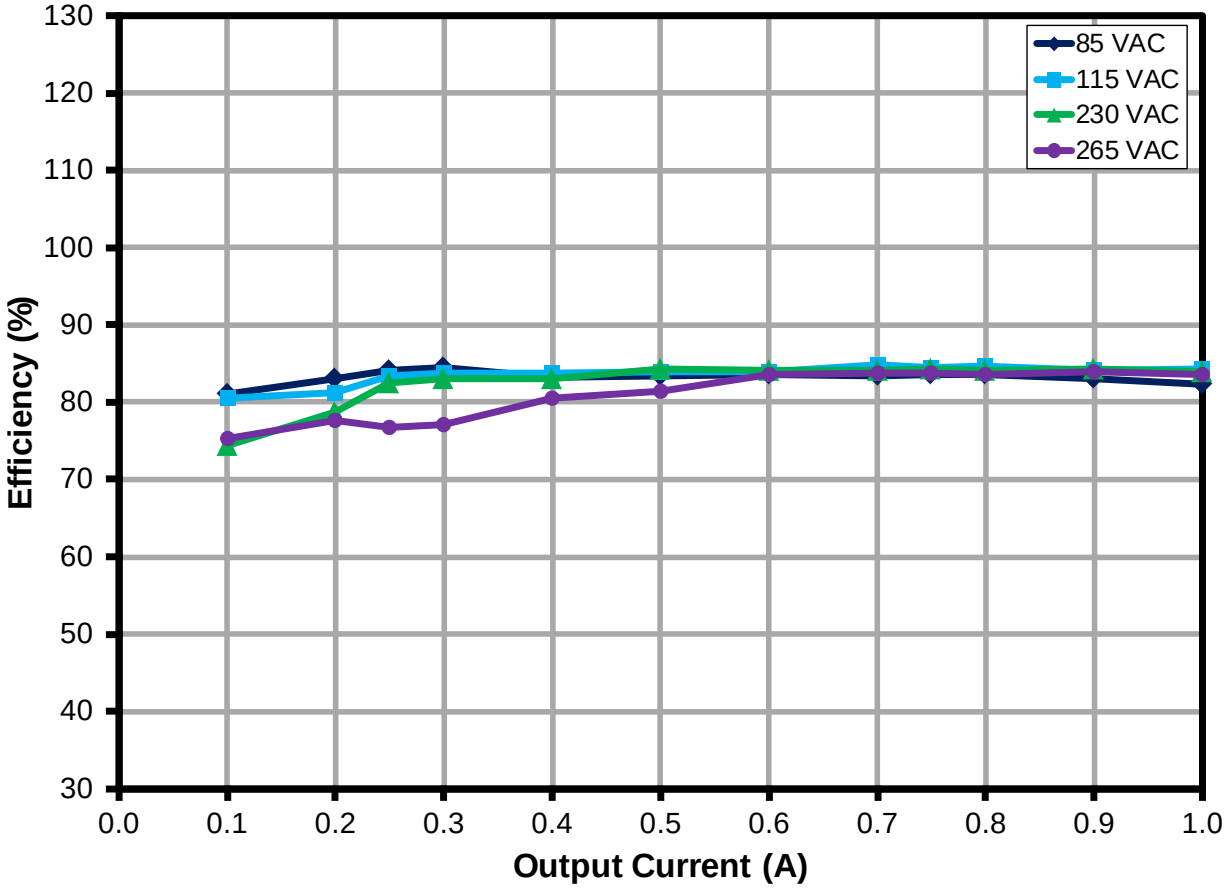

Figure 6 – Efficiency vs. Output Current, Room Temperature, 60 Hz.

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9.2 Active Mode Measurement Data

As this design could be used for an external power supply (vs internal) the efficiency requirements for the two toughest external power supply standards (in effect at time of writing) are shown blow.

This design meets both the U.S. DOE EISA2007 (Level VI) and European Code of Conduct (Version 5) limits.

For other standard and the latest, up-to-date information on energy efficiency regulations, please visit the PI Green Room, at:
http://www.powerint.com/greenroom/regulations.htm

Measured Performance				**Standards**			
		V_{IN} (VAC)		**EISA2007**		**EC CoC (v5)**	
		115	230	2016 Direct operation	2016 Indirect operation	2014 Tier 1	2016 Tier 2
		Efficiency (%)		Efficiency (%)			
Percent of Full Load	10	80.5	82			70	73
	25	83.5	82.6				
	50	83.9	84.3				
	75	84.4	84.3				
	100	84.4	84				
	Ave	**84**	**84**	83	72	80	83
No-Load Input Power† (mW)		**70 (22)**	**125 (24)**	100	500	150	75
		Compliant		Y	Y	Y	Y

† Numbers in parenthesis with IC supplied from optional bias winding.

9.3 No-Load Input Power (R8 Not Installed: No Bias Winding Supplementation)

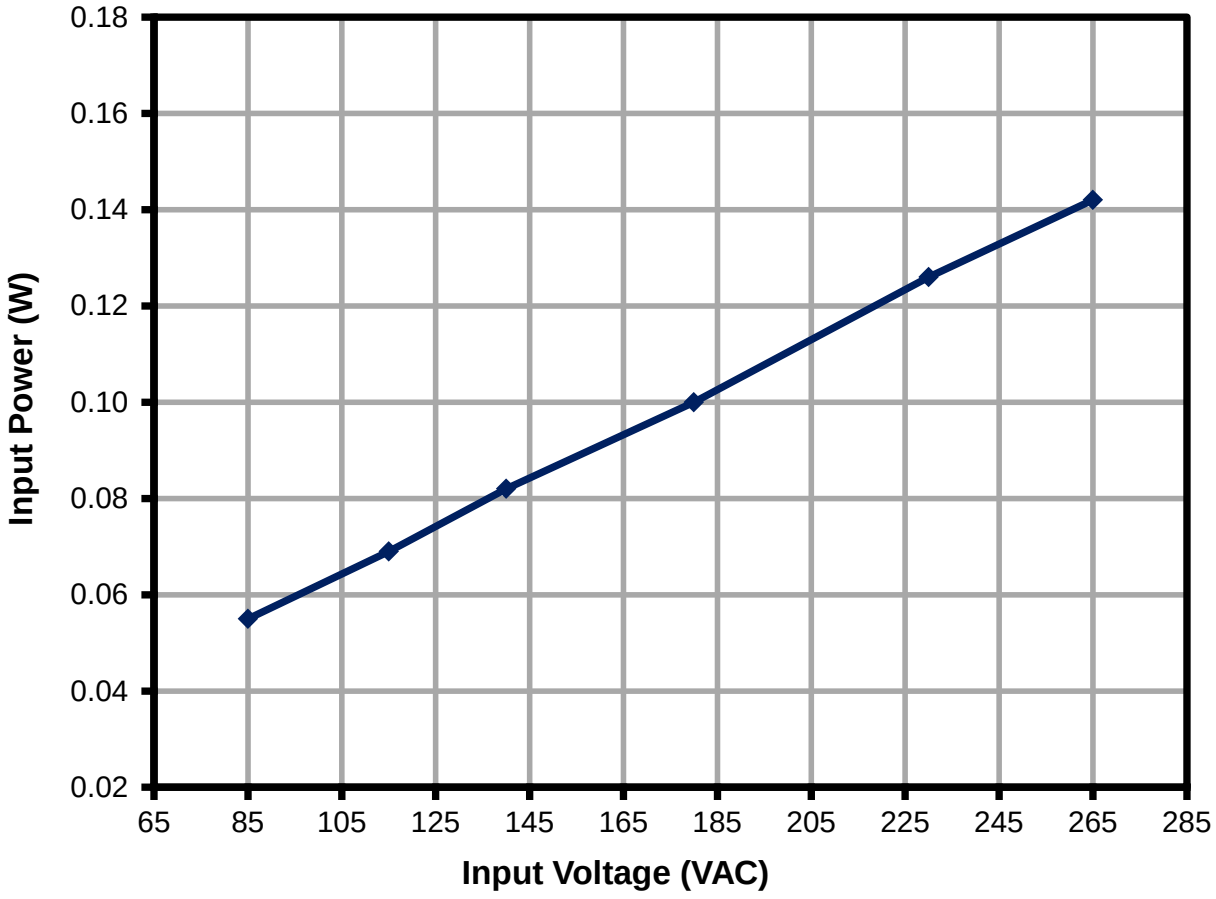

Figure 7 – No-load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

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9.4 No-Load Input Power (with R8 and IC supplied from bias winding)

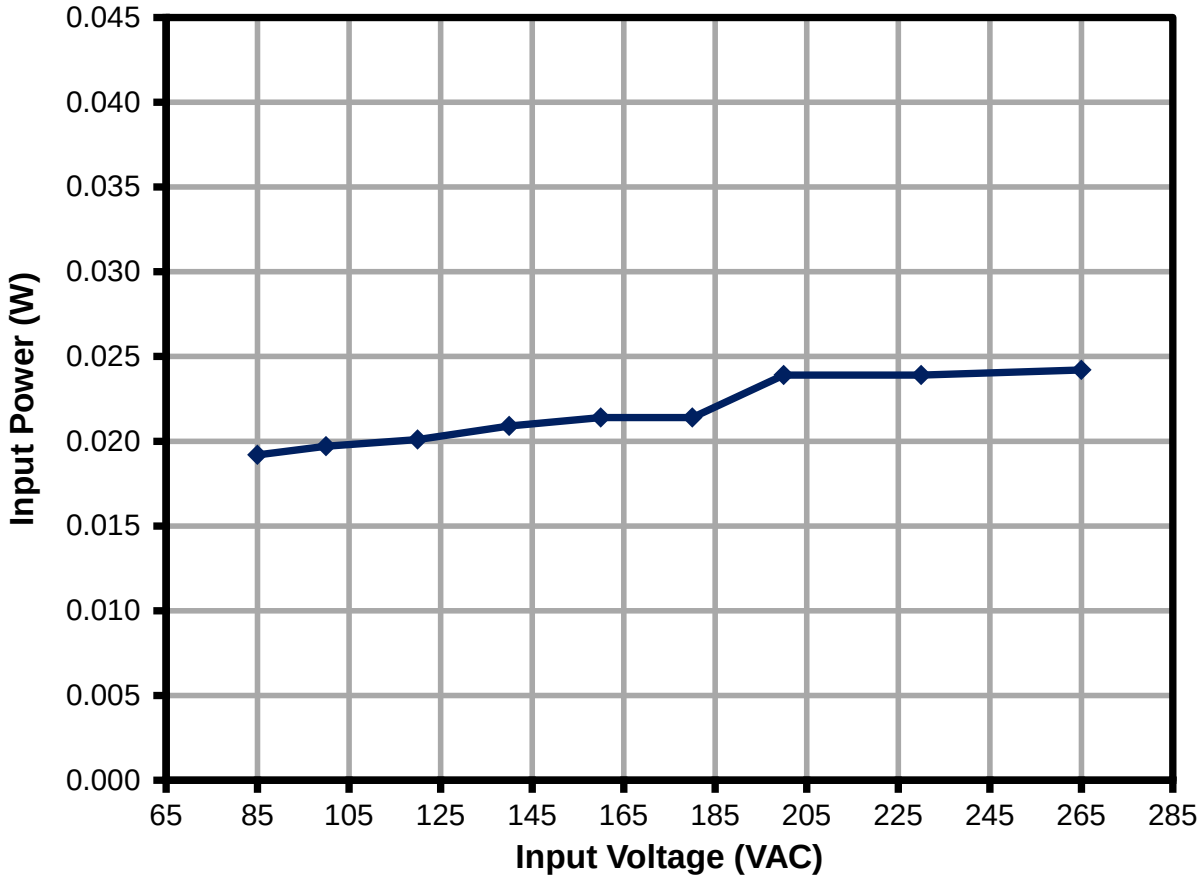

Figure 8 – No-load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz, with Bias Winding.

9.5 Available Standby Output Power

The chart below shows the available output power versus line voltage at input power consumption levels of 1, 2 and 3 watts (respectively). Again, this performance illustrates the value of ON/OFF control, as it automatically maintains a high efficiency, even during very light loading. This simplifies complying with standby requirements that specify that a fair amount of power be available to the load at low input power consumption levels. The TinySwitch-4 ON/OFF control scheme maximizes the amount of output power available to the load in standby operation when the allowable input power is fixed at a low value. This simplifies the design of products such as printers, set-top boxes, DVD players, etc. that must meet stringent standby power consumption requirements.

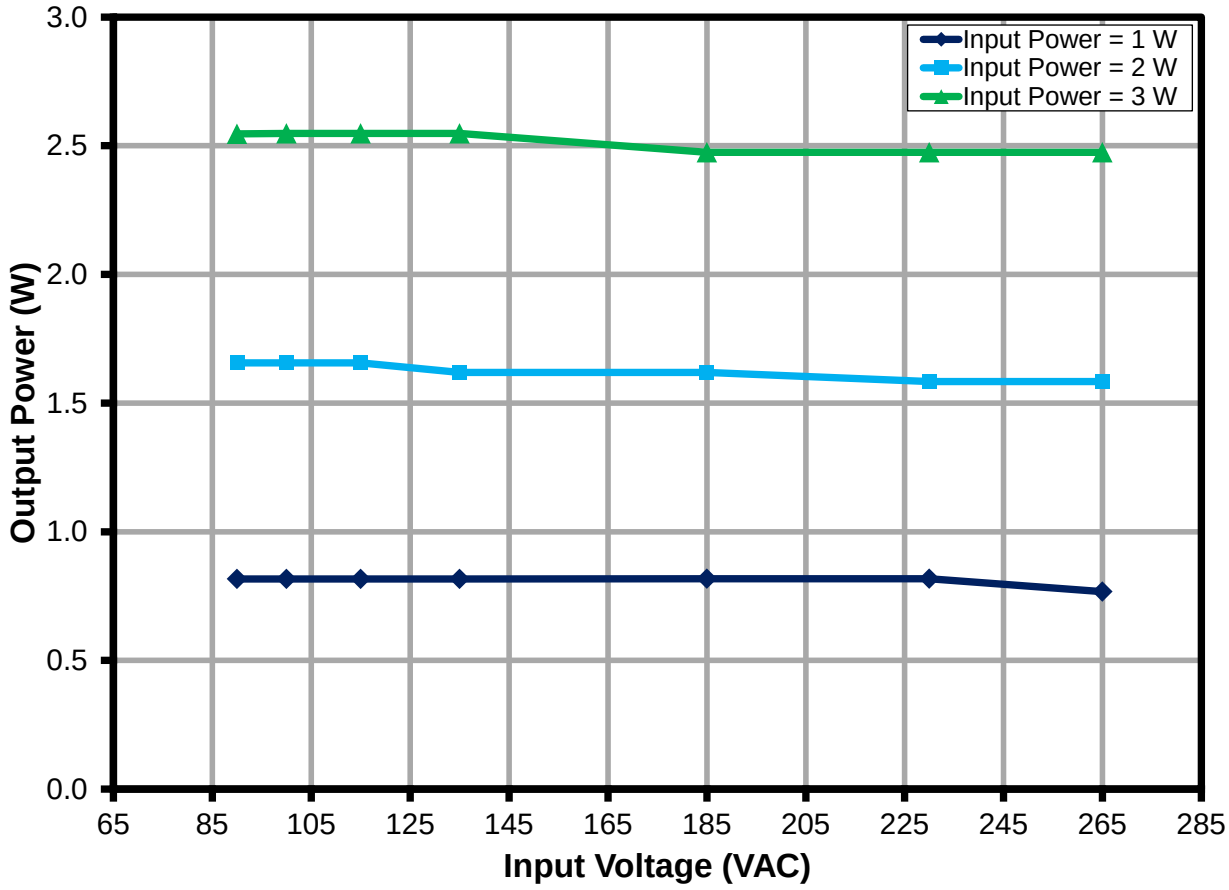

Figure 9 – Available Output Power for 1 W, 2 W and 3 W of Input Power.

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9.6 Regulation

9.6.1 Load and Line

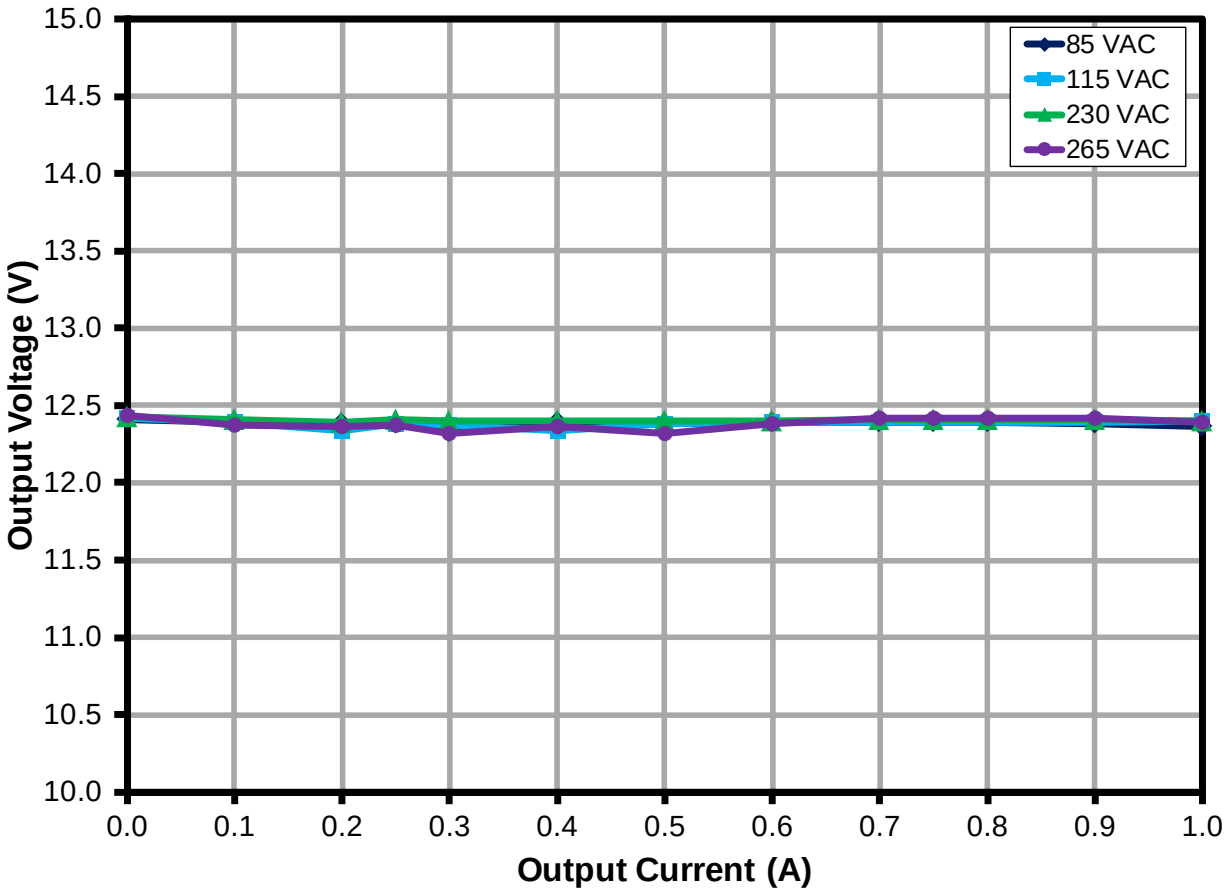

Figure 10 – Load and Line Regulation, Room Temperature.

10 Thermal Performance

Temperature measurements of key components were taken using T-type thermocouples. The thermocouples were soldered directly to a SOURCE pin of the TNY288PG device and to the cathode of the output rectifier. The thermocouples were glued to the output capacitor and to the external core and winding surfaces of transformer T1.

The unit was sealed inside a large box to eliminate any air currents. The box was placed inside a thermal chamber. The ambient temperature within the large box was raised to 50 °C. The unit was then operated at full load and the temperature measurements were taken after they stabilized for 1 hour at 50 °C.

Temperature (°C)		
Item	**85 VAC**	**265 VAC**
Ambient	50*	50*
TNY288PG (U1)	83.9	80.9
Transformer Core(T1)	68	71.1
Transformer Winding (T1)	72.3	72.9
Output Rectifier (D7)	79.7	79.5
Output Capacitor (C10)	60.2	60.2

*To simulate operation inside sealed enclosure at 40 °C external ambient.

These results show that all key components have an acceptable rise in temperature.

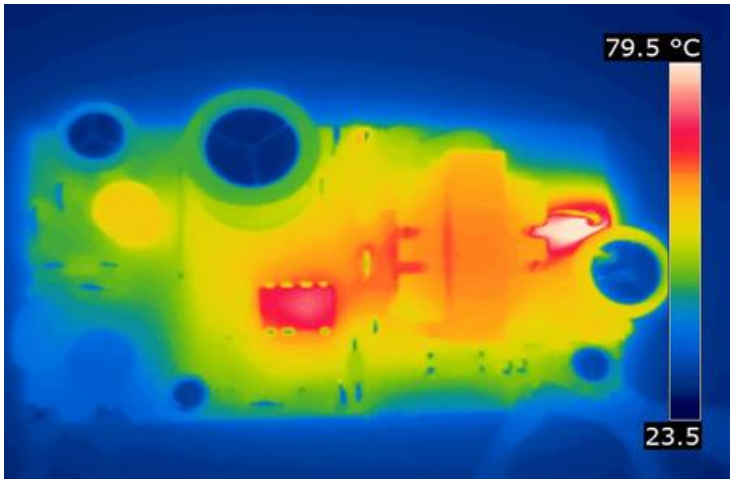

Figure 11 – Infrared Thermograph of Open Frame Operation, at Room Temperature.
85 VAC, 12 W Load, 22 °C Ambient.

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11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

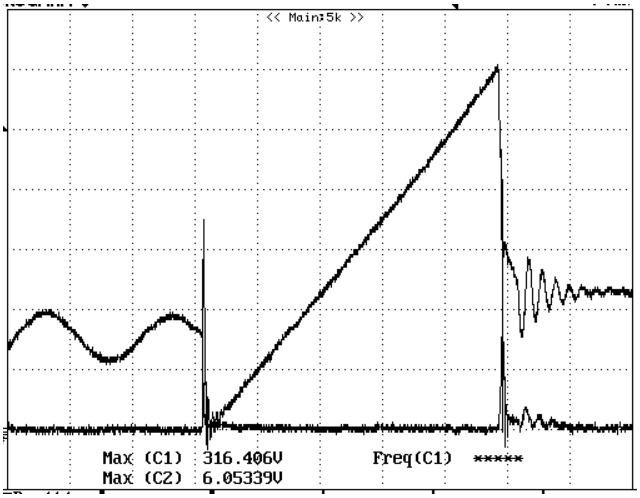

Figure 12 – 115 VAC, Full Load.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 50 V, 500 ns / div.

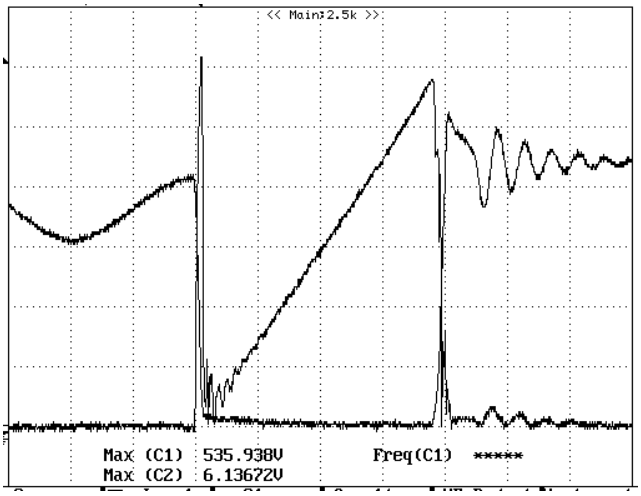

Figure 13 – 230 VAC, Full Load.
Upper: I_{DRAIN}, 0.1 A / div.
Lower: V_{DRAIN}, 100 V / div.

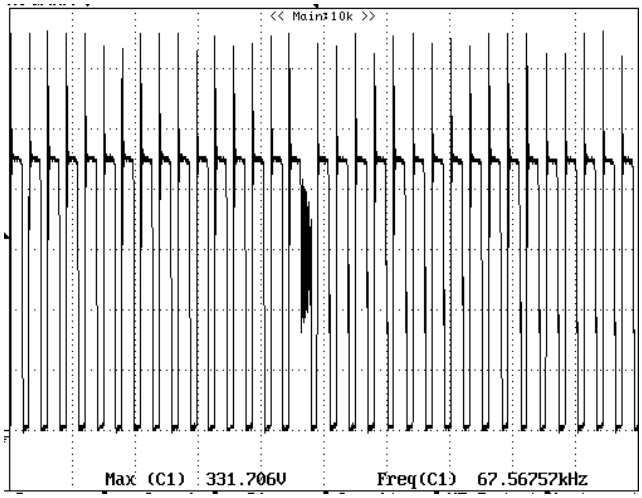

Figure 14 – 115 VAC, Full Load.
V_{DRAIN}, 50 V, 20 µs / div.

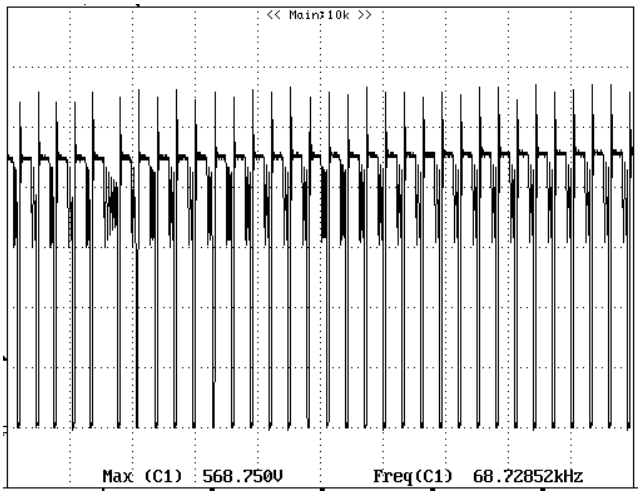

Figure 15 – 230 VAC, Full Load.
V_{DRAIN}, 100 V, 20 µs / div.

11.2 Output Voltage Start-Up Profile

Start-up into full resistive load and no-load were both verified. A 12 Ω resistor was used for the load, to maintain 1 A under steady-state conditions.

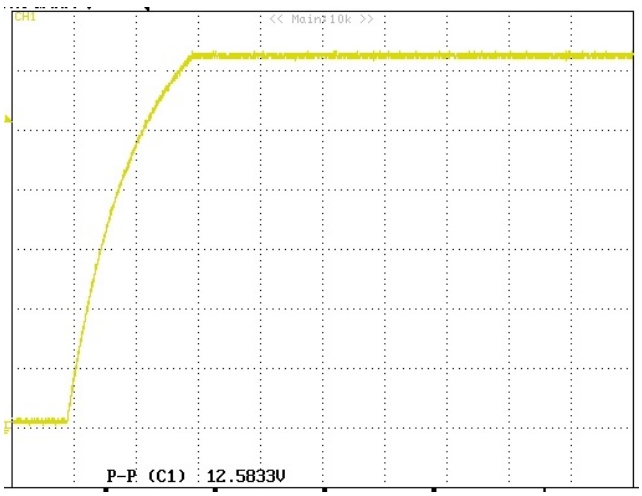

Figure 16 – Start-Up Profile, 115 VAC.
Fast trace is No-load Rise Time.
Slower Trace is Maximum Load (12 Ω)
2 V, 5 ms / div.

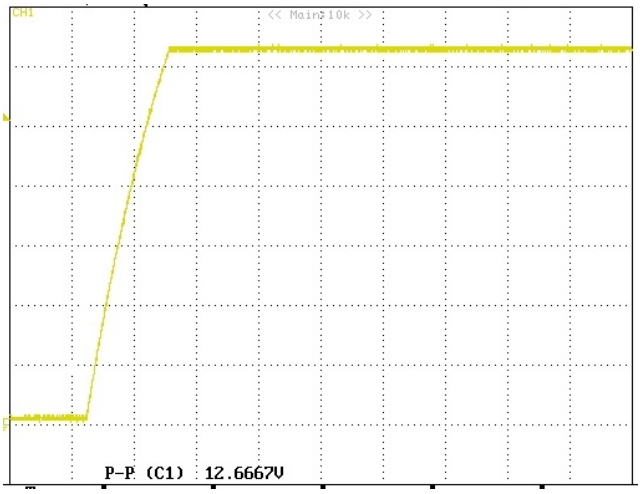

Figure 17 – Start-Up Profile, 230 VAC.
Fast trace is No-load Rise Time.
Slower Trace is Maximum Load (12 Ω)
2 V, 5 ms / div.

11.3 Drain Voltage and Current Start-Up Profile

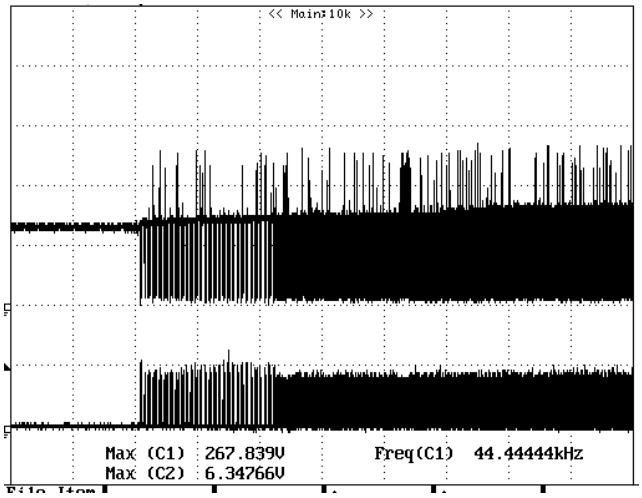

Figure 18 – 90 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 100 V & 100 µs / div.
Lower: I_{DRAIN}, 0.5 A / div.

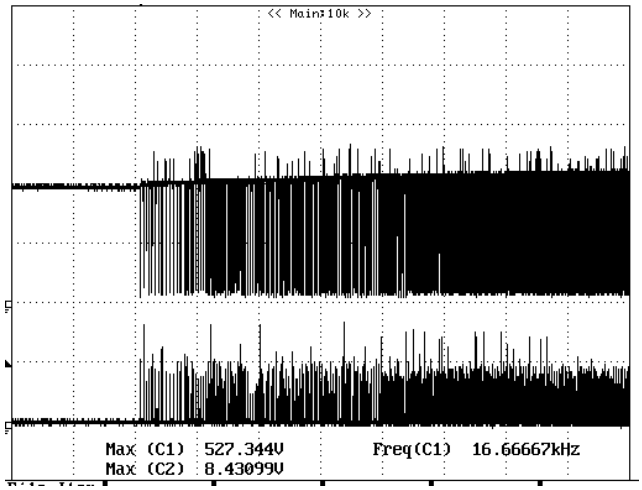

Figure 19 – 265 VAC Input and Maximum Load.
Upper: V_{DRAIN}, 200 V & 100 µs / div.
Lower: I_{DRAIN}, 0.5 A / div.

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11.4 Load Transient Response (50% to 100% Load Step)

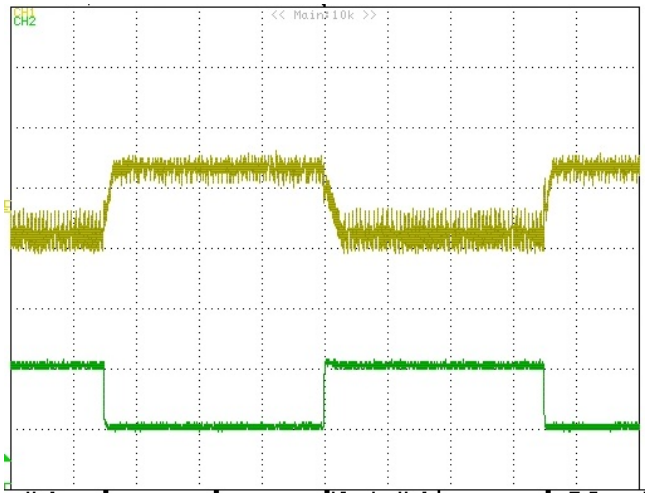

Figure 20 – Transient Response, 115 VAC, 50-100-50% Load Step.
Upper: V_{OUT} 50 mV / div.
Lower: I_{OUT} 0.5 A, 1 ms / div.

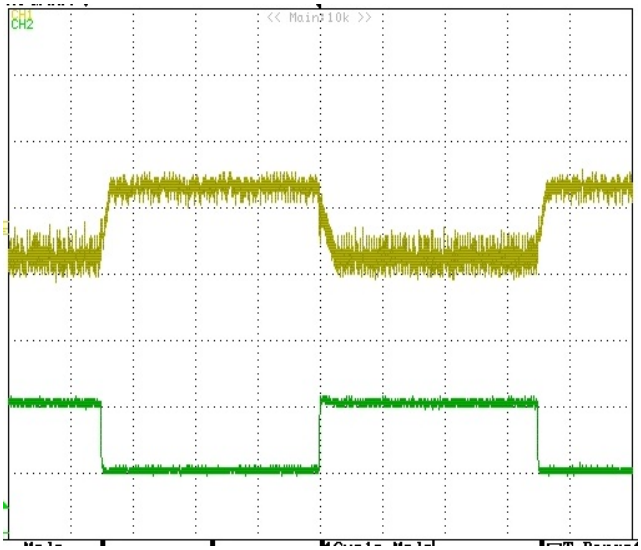

Figure 21 – Transient Response, 230 VAC, 50-100-50% Load Step.
Upper: V_{OUT} 50 mV / div.
Lower: I_{OUT} 0.5 A, 1 ms / div.

11.5 Output Ripple Measurements

11.5.1 Ripple Measurement Technique

A modified oscilloscope test probe was used to take output ripple measurements, in order to reduce the pickup of spurious signals. Using the probe adapter pictured in Figure 22, the output ripple was measured with a 1 μF electrolytic, and a 0.1 μF ceramic capacitor connected as shown.

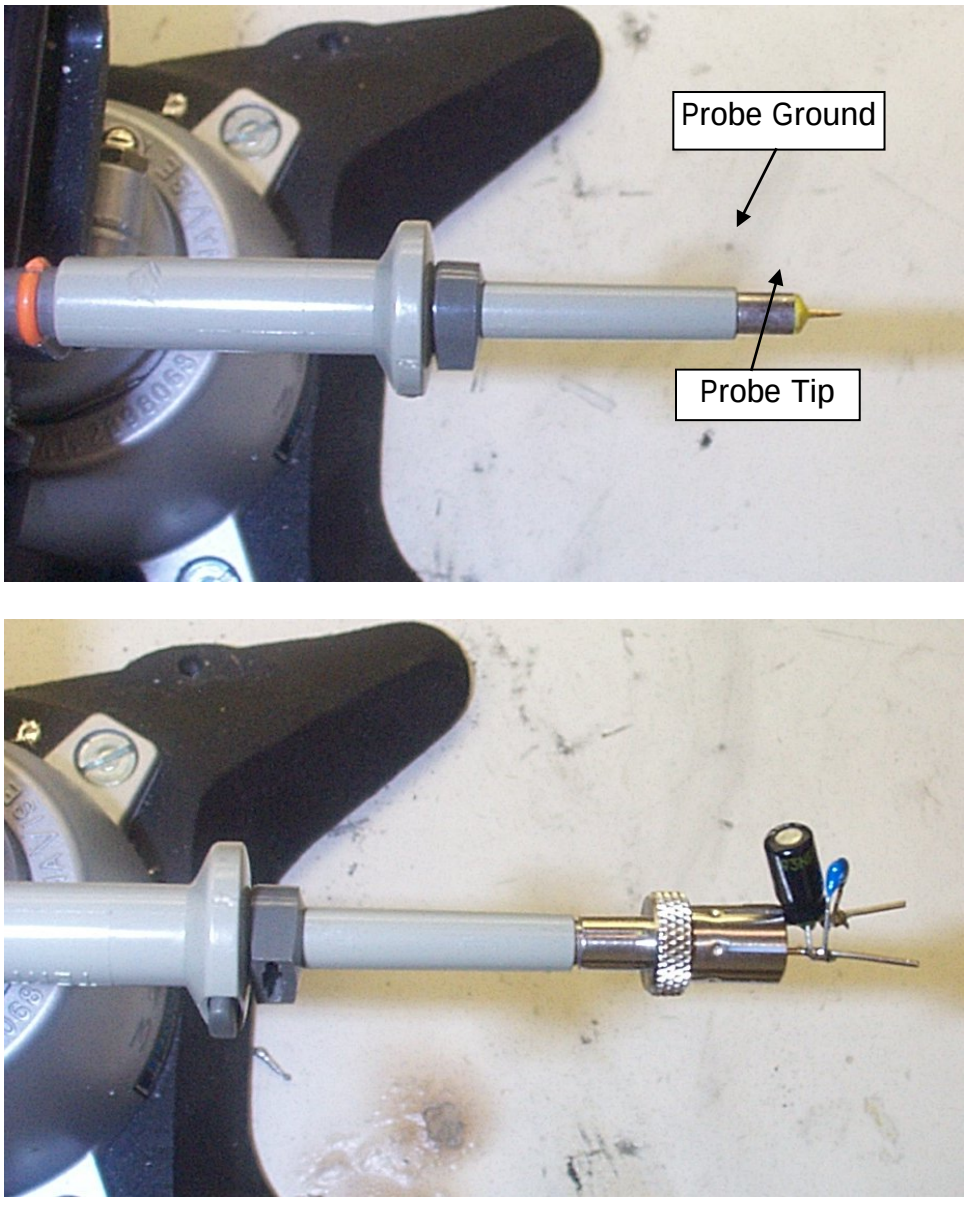

Figure 22 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

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11.5.2 Measurement Results

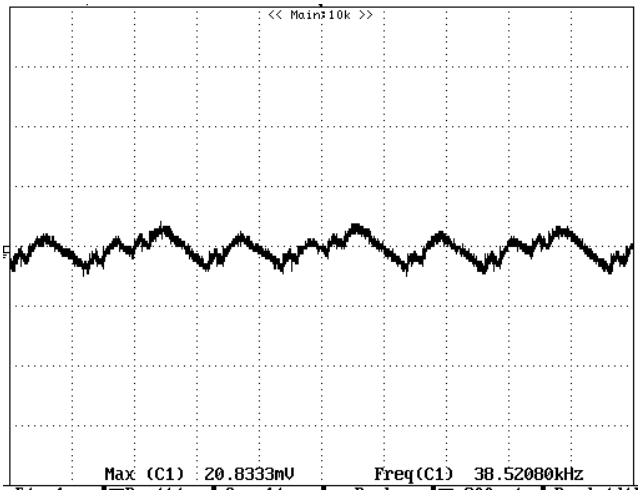

Figure 23 – Ripple, 85 VAC, Full Load.
20 μs, 50 mV / div.

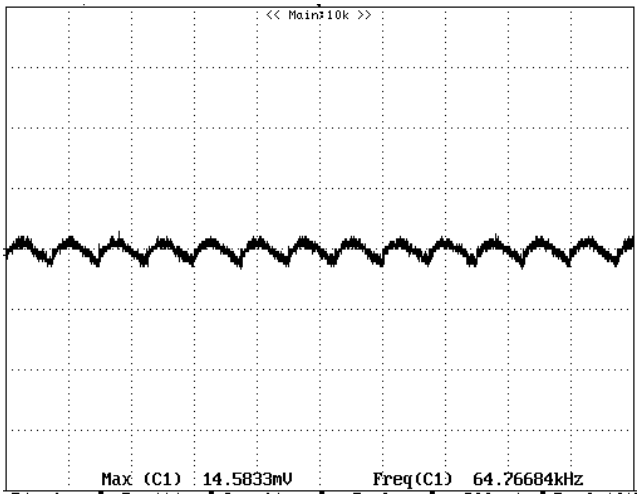

Figure 24 – Ripple, 115 VAC, Full Load.
20 μs, 50 mV / div.

11.6 Overvoltage Shutdown

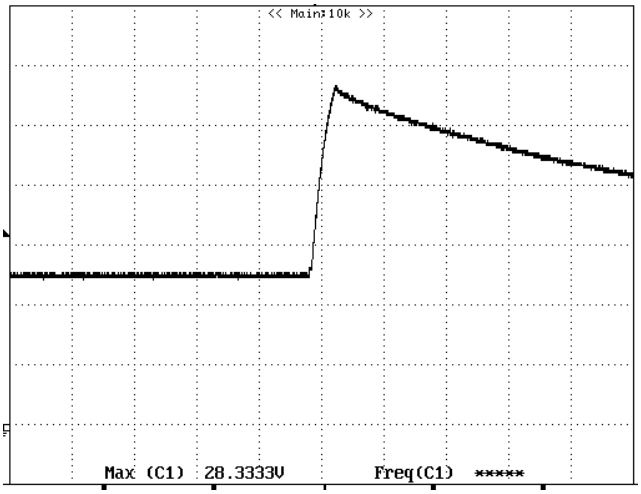

Figure 25 – Overvoltage Shutdown.
265 VAC, No Load.
50 ms, 5 V / div.

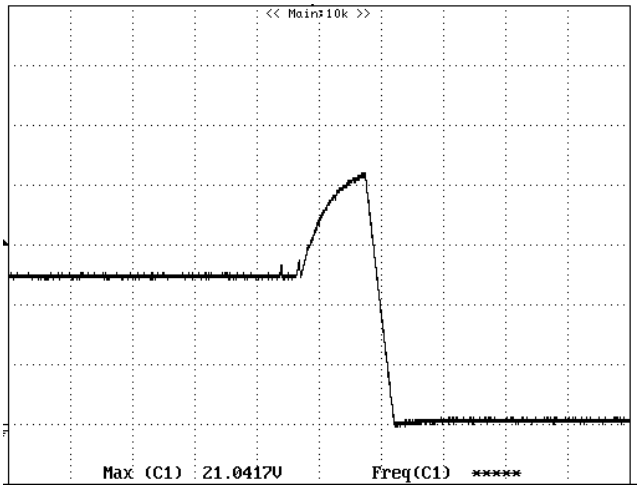

Figure 26 – Overvoltage Shutdown.
265 VAC, Full Load.
50 ms, 5 V / div.

12 Line Surge

Differential input line surge (1.2/50 μs) testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

Surge Voltage	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
1 kV Differential	90	2	10	PASS
2 kV Common Mode	90	12	10	PASS

Unit passed under all test conditions.

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13 Conducted EMI

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load (12 V, 1 A). Measurements were taken with an Artificial Hand connected and a floating DC output load resistor. A DC output cable was included.

Composite EN55022B / CISPR22B conducted limits are shown. In all cases there was excellent (>10 dB) margin.

13.1 115 VAC, Full Load

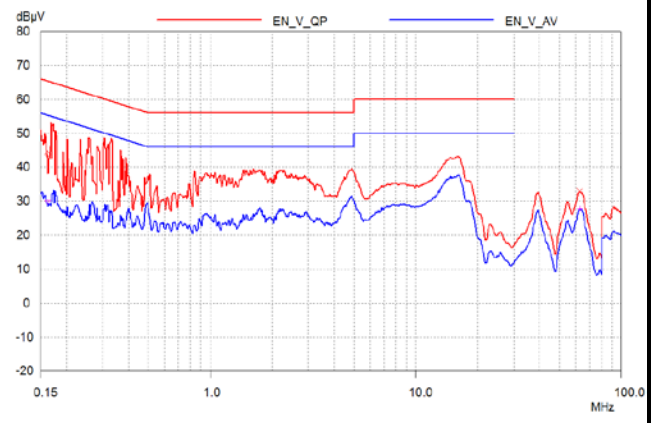
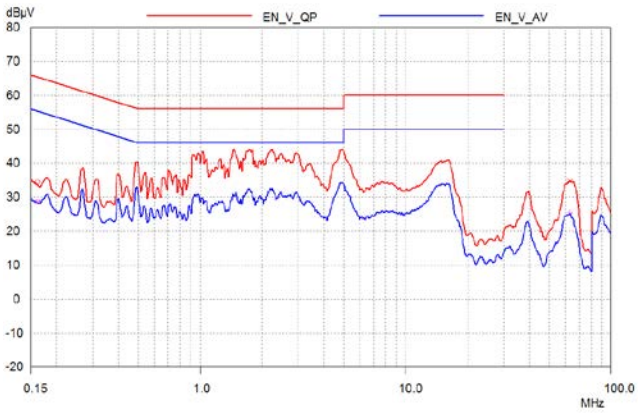
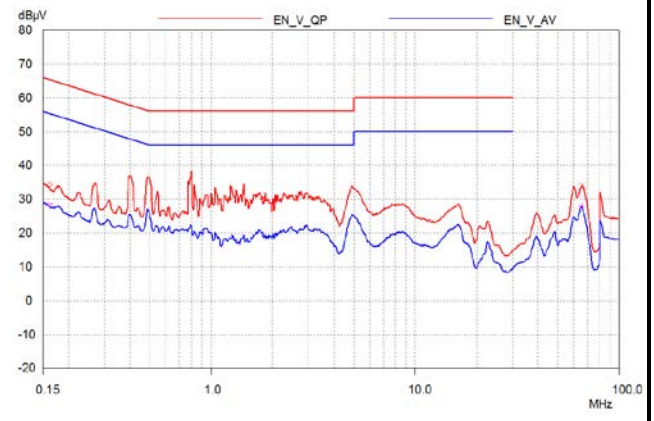
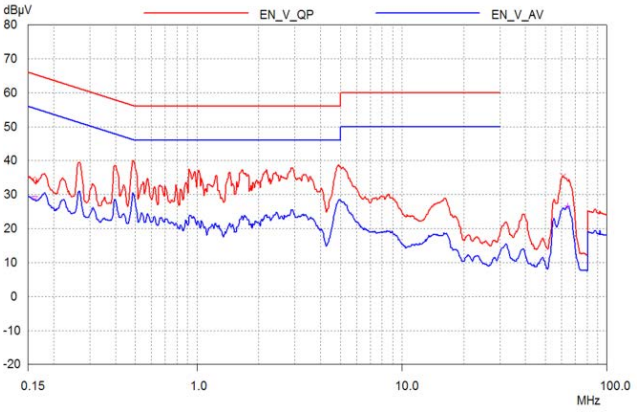
Line	Neutral
	
Artificial Hand Connected to Output Return.	Artificial Hand Connected to Output Return.
	
Output Floating.	Output Floating.

Figure 27 – Conducted EMI at 115 VAC.

13.2 230 VAC, Full Load

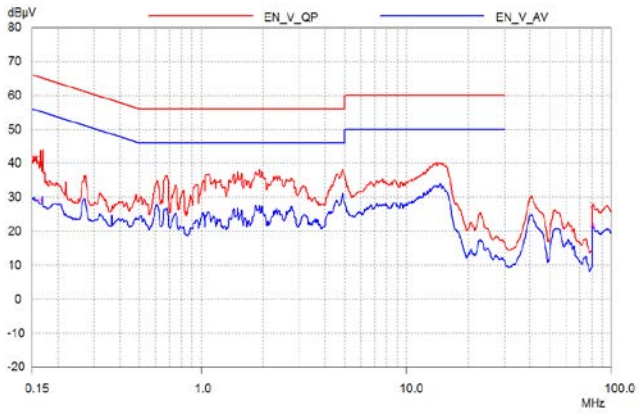
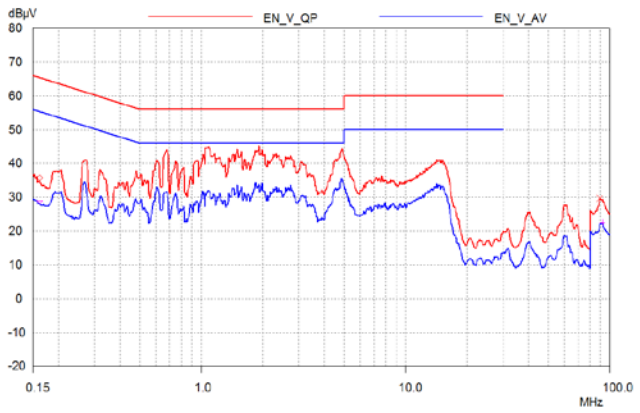
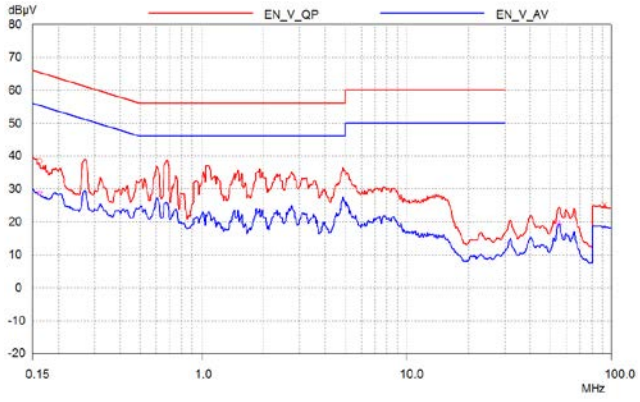
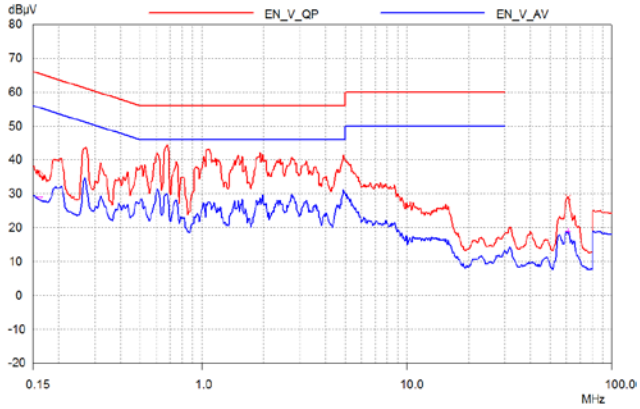
Line	Neutral
 Artificial Hand Connected to Output Return.	 Artificial Hand Connected to Output Return.
 Output Floating.	 Output Floating.

Figure 28 – Conducted EMI at 230 VAC.

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14 Audible Noise

An open-frame (no enclosure) unit was tested with an audio precision analyzer, using a microphone positioned one inch from the core of transformer T1. The test was done with the unit in an acoustically isolated and dampened chamber. The load was adjusted until a maximum reading was obtained.

35 dBrA is considered the acceptable limit for frequencies below 18 kHz. An enclosure will typically further reduce measurable acoustic noise levels by an additional 10 dBrA.

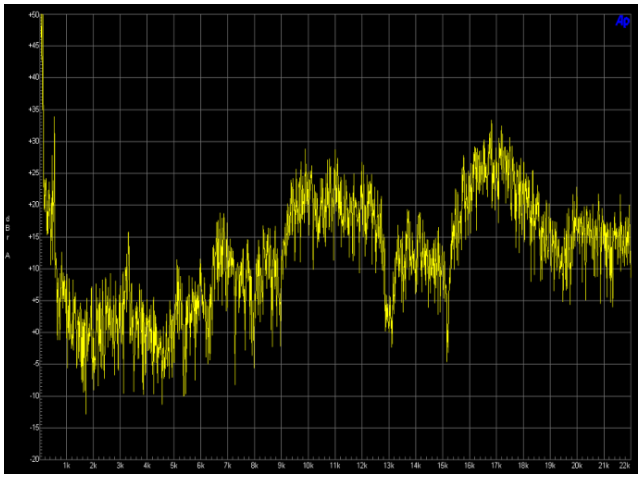

Figure 29 – Audible Noise V_{IN} = 120 VAC; I_{OUT} = 350 mA.

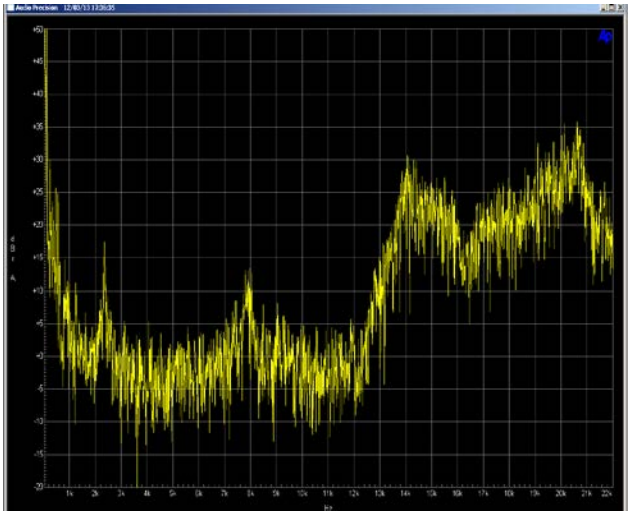

Figure 30 – Audible Noise V_{IN} = 120 VAC; I_{OUT} = 860 mA.

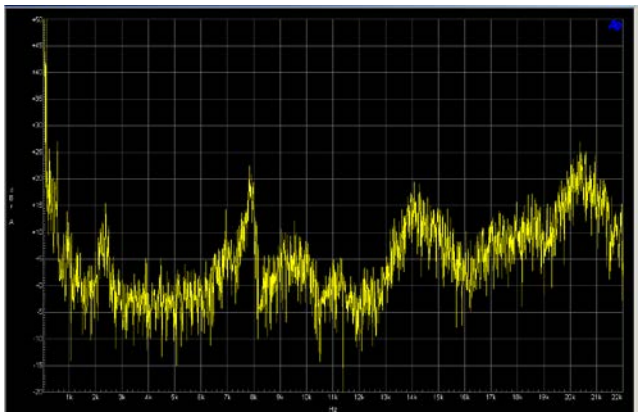

Figure 31 – Audible Noise V_{IN} = 230 VAC; I_{OUT} =930 mA.

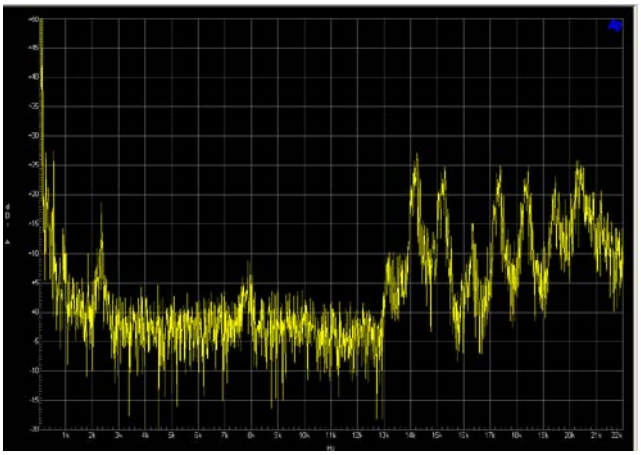

Figure 32 – Audible Noise V_{IN} = 230 VAC; I_{OUT} =880 mA.

15 Extended and Reduced Current Limit (I_{LIMIT}) Operation

Capacitors (C8 and C9 on the BOM in Section 6) can be added to the board to try out the $I_{LIMIT+1}$ and $I_{LIMIT-1}$ operation of TNY288PG. When C7 (0.1 μF) is replaced with a 10 μF capacitor (C9), the TNY288PG will operate in the $I_{LIMIT+1}$ mode, which increases the maximum primary current limit from the standard maximum limit of 0.55 A to 0.65 A (equal to that of a TNY289PG). This allows a TNY288PG to deliver from 15% to 25% more output power (depending on the output voltage and current).

CAUTION: Because RD-399 was designed for standard I_{LIMIT} operation, It should not be loaded with more than 1.25 A at an elevated temperature for very long (a few minutes) when verifying the performance of TNY288PG in the $I_{LIMIT+1}$ mode, since the other power components (transformer, input bulk capacitors, output diode, output capacitors and primary clamp network) are not sized for sustained operation at more than 12 W.

When C7 is replaced with a 1 μF capacitor (C8), the TNY288PG will operate in the $I_{LIMIT-1}$ mode, which reduces the maximum current limit from the standard maximum limit of 0.55 A to 0.45 A (equal to that of a TNY277PG). Although this reduces the maximum output power that the supply can deliver, it typically will increase the efficiency, especially at lower output power levels. To take the fullest advantage of the increase in efficiency that can be obtained from $I_{LIMIT-1}$ operation, the power transformer would need to be redesigned slightly.

16 TNY287PG and TNY289PG Operation in RD-399

A TNY287PG device used in the $I_{LIMIT+1}$ mode (a 10 μF installed in place of C7) will work in the RD-399 reference board, and deliver output power equal to that of a TNY288PG device. This flexibility allows a design engineer the option of using a lower cost part in applications with less demanding thermal requirements.

A TNY289PG device used in the $I_{LIMIT-1}$ mode (a 1 μF installed in place of C7) will deliver the same output power as a TNY288PG in the standard I_{LIMIT} configuration. This can improve efficiency and lower the temperature rise of the device, which can give greater thermal margin to a design that must operate in high ambient temperature environments.

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17 OVP Operation Verification

While the RD-399 is in normal operation, monitor the output with a storage oscilloscope. To cause an overvoltage condition to occur, short-circuit the optocoupler LED (as shown below) to open the feedback control loop. The oscilloscope will capture the output voltage rising until the increasing voltage across VR2 causes it to conduct, and the TNY288PG device latches off. To reset the OVP latch, the AC input power must be removed long enough to allow the input bulk capacitors to fully discharge.

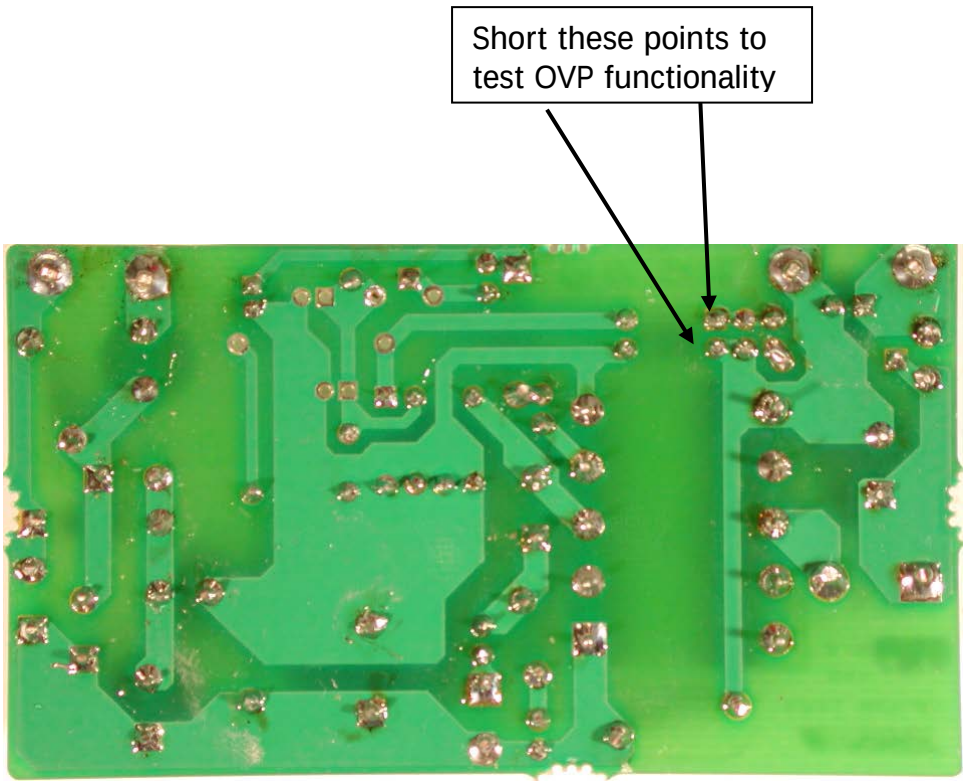

Figure 33 – Point on PCB to Apply Short-Circuit to Trigger OV Shutdown.

18 Revision History

Date	Author	Revision	Description an Changes	Approved
02-Jul-14	RJ	1.1	Initial Release	Apps & Mktg
09-Oct-15	KM	1.2	Updated Brand Style and added Transformer Supplier	

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