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|------------------------|---|
| Title | <i>Reference Design Report for a 10 W CV/CC USB Charger using InnoSwitch™-CH INN2023K</i> |
| Specification | 85 VAC – 264 VAC Input; 5 V, 2 A Output (end of USB Cable) |
| Application | Cell Phone / USB Charger |
| Author | Applications Engineering Department |
| Document Number | RDR-420 |
| Date | April 20, 2015 |
| Revision | 1.1 |

Summary and Features

- InnoSwitch-CH - Industry first AC/DC ICs with isolated, safety rated integrated feedback
- All the benefits of secondary side control with the simplicity of primary side regulation
 - $\pm 3\%$ CV, $\pm 5\%$ CC regulation
 - Insensitive to transformer variation
 - Transient response independent of load timing
 - Smaller, lower cost output capacitors
 - < 10 mW no-load input power
 - Cable voltage drop compensation
- Built in synchronous rectification for high efficiency

PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com. Power Integrations grants its customers a license under certain patent rights as set forth at <http://www.powerint.com/ip.htm>.

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Important Note:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

This document is an engineering report describing a 2 A, 5.0 V USB charger utilizing a device from the InnoSwitch-CH family of ICs. This design is intended to show the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

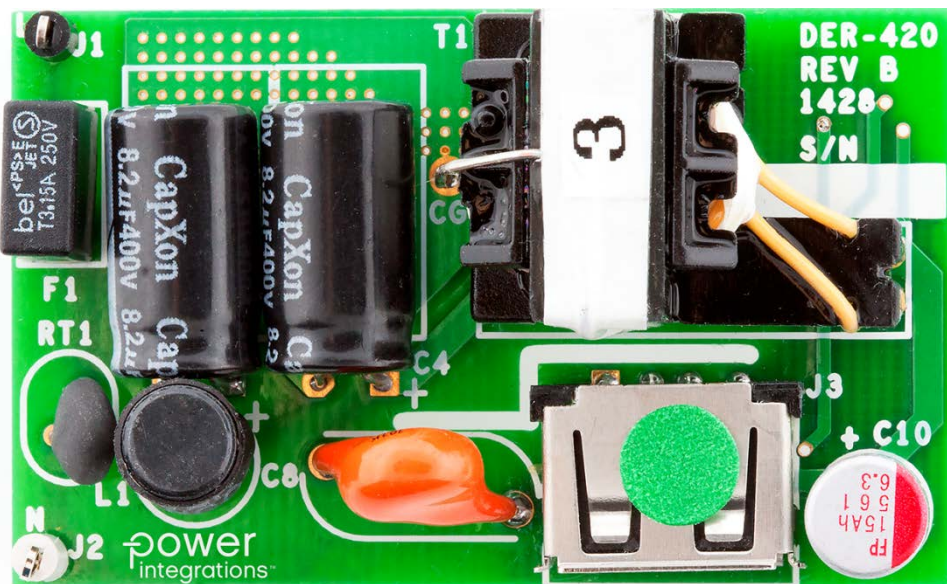


Figure 1 – Populated Circuit Board Photograph, Top.

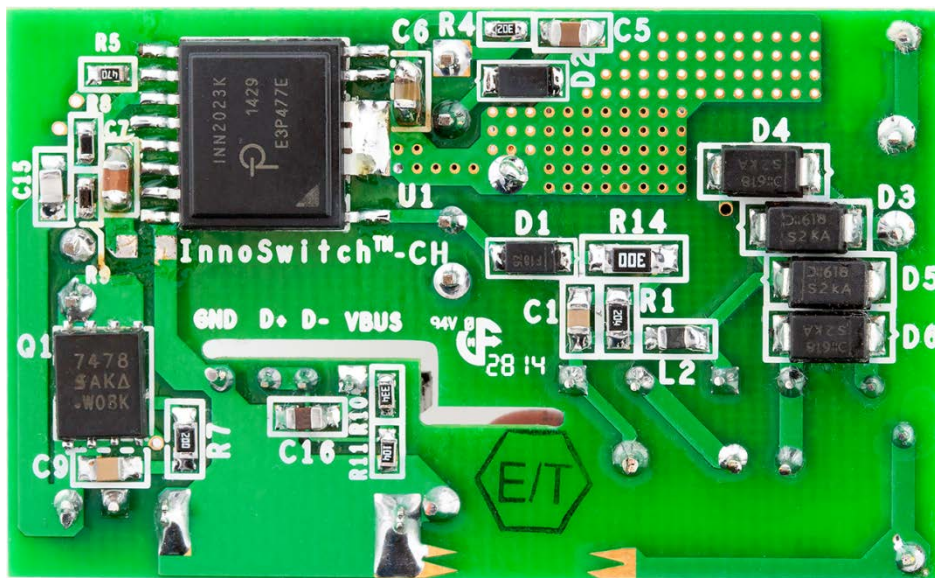


Figure 2 – Populated Circuit Board Photograph, Bottom.



2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

| Description | Symbol | Min | Typ | Max | Units | Comment |
|---------------------------|-------------------|-----------------------|-------|------|--------------------|---|
| Input | | | | | | |
| Voltage | V_{IN} | 85 | | 265 | VAC | 2 Wire – no P.E. |
| Frequency | f_{LINE} | 50 | 50/60 | 64 | Hz | |
| No-load Input Power | | | | 10 | mW | 230 VAC |
| Output | | | | | | |
| Output Voltage | V_{OUT} | 4.75 | 5.0 | 5.25 | V | 0.35 V cable resistance drop |
| Transient Output Voltage | $V_{OUT(T)}$ | 4.2 | | 5.5 | V | 0 A - 2 A - 0 A load step end of cable |
| Output Ripple Voltage | V_{RIPPLE} | | | 150 | mV | At the end of the output cable |
| Output Cable Compensation | V_{CBL} | 250 | 300 | 350 | mV | At 2 A output current |
| Output Current CC point | I_{OUT} | 2 | | 2.5 | A | |
| Auto-Restart Voltage | V_{AR} | 2 | | 3.5 | V | At end of cable |
| Turn on Rise Time | t_R | | | 20 | ms | |
| Rated Output Power | P_{OUT} | | 10 | | W | |
| Efficiency | | | | | | |
| Average | $\eta_{AVE[BRD]}$ | 84 | | | % | Measured at USB socket |
| 25%, 50%, 75%, and 100% | $\eta_{AVE[CBL]}$ | 80 | | | % | With 0.38 V cable resistance drop |
| 10% | $\eta_{10\%}$ | 79 | | | % | |
| Environmental | | | | | | |
| Output Cable Impedance | R_{CBL} | | 190 | | m Ω | |
| Conducted EMI | | | | | | Resistive load, 6 dB Margin |
| Safety | | | | | | 6 dB Margin |
| Audible noise | | | | 25 | dB | Designed to meet |
| Line Surge | | | | | | Measured at 3 cm |
| Common mode (L1/L2-PE) | | | | 6 | kV | Ring Wave, Common Mode: 12 Ω |
| ESD | | ± 16.5 ± 8 | | | kV kV | Contact Air discharge No degradation in performance |
| Ambient Temperature | T_{AMB} | 0 | | 40 | $^{\circ}\text{C}$ | Free convection, sea level in sealed enclosure |

3 Schematic

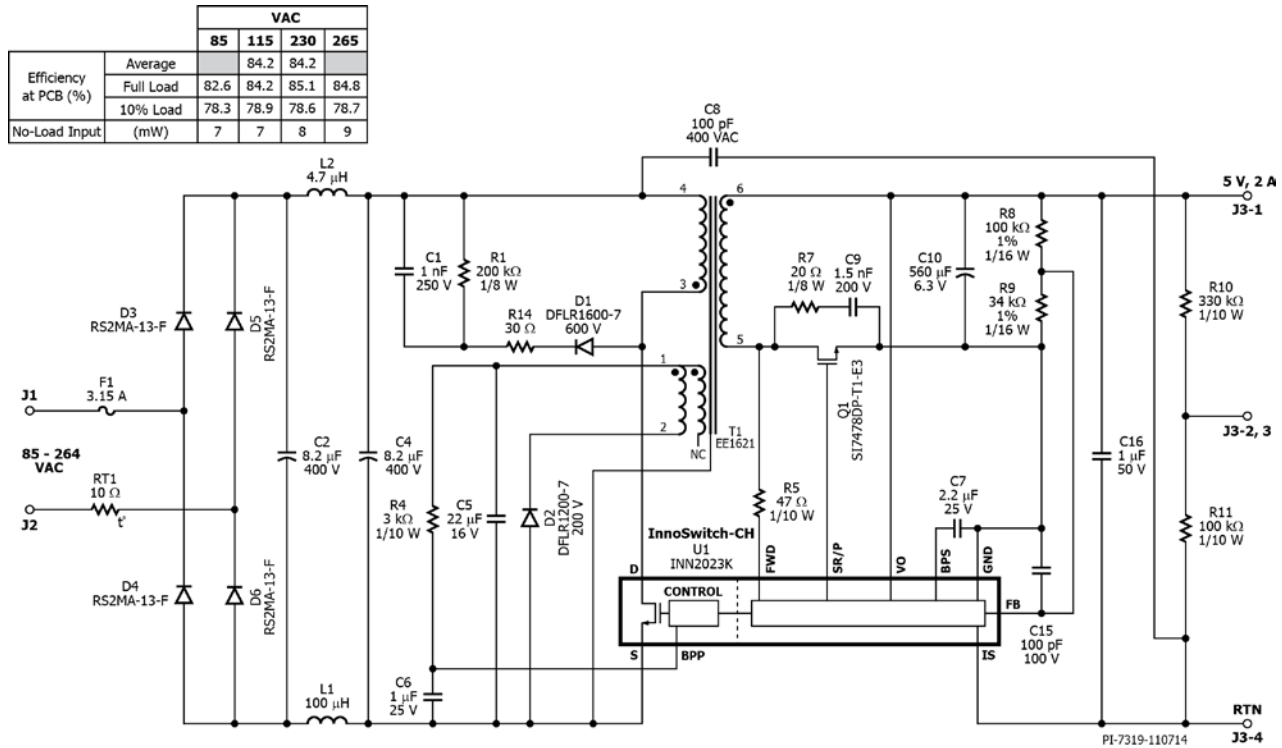


Figure 3 – Schematic.

4 Circuit Description

4.1 Input EMI Filtering

Fuse F1 provides protection against catastrophic failure of components on the primary side.

An inrush limiting thermistor (RT1) was necessary due to the low surge current rating of the rectifier diodes (D1-D4) and the relatively high value and therefore low impedance of the bulk storage capacitors C2 and C4.

Physically small diodes were selected for D1-D4 due to the limited space, specifically height from PCB to case.

Capacitor C2 and C4 provide filtering of the rectified AC input and together with L1 and L2 form a π (pi) filter to attenuate differential mode EMI. A low value Y capacitor (C8) reduces common mode EMI.

4.1 InnoSwitch-CH IC Primary

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 650 V power MOSFET inside the InnoSwitch-CH IC (U1).

A low cost RCD clamp formed by D1, R1, R14 and C1 limits the peak drain voltage due to the effects of transformer and output trace inductance.

The IC is self-starting, using an internal high voltage current source to charge the BPP pin capacitor (C6) when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding, rectified and filtered (D2 and C5) and fed in the BPP pin via a current limiting resistor R4.

Output regulation is achieved using On/Off control, the number of enabled switching cycles are adjusted based on the output load. At high load most switching cycles are enabled, and at light load or no-load most cycled are disabled or skipped. Once a cycle is enabled, the power MOSFET remain on until the primary current ramps to the device current limit for the specific operating state. There are four operating states (current limits) arrange such that the frequency content of the primary current switching pattern remains out of the audible range until at light load where the transformer flux density and therefore audible noise generation is at a very low level.

4.2 *InnoSwitch-CH IC Secondary*

The secondary side of the InnoSwitch-CH provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

The secondary of the transformer is rectified by Q1 and filtered by C10. High frequency ringing during switching transients that would otherwise create high voltage across Q1 and radiated EMI is reduced via snubber components R7 and C9.

To reduce dissipation synchronous rectification (SR) is provided by Q1. The gate of Q1 is turned on based on the winding voltage sensed via R5 and the FWD pin of the IC. In continuous conduction mode operation the power MOSFET is turned off just prior to the secondary side commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold. Secondary side control of the primary side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR/P pin.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. During CV operation the output voltage powers the device, fed into the VO pin.

During CC operation, when the output voltage falls the device will power itself from the secondary winding directly. During the on-time of the primary side MOSFET the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C7 via R5 and an internal regulator. The unit enters auto-restart when the sensed output voltage is lower than 3 V.

Output current is sensed internally between the IS and GND pins with a threshold of 35 mV to minimize losses. Once the internal current sense threshold is exceeded, the device adjusts the number of enabled switching cycles to maintain a fixed output current.

Below the CC threshold the device operates in constant voltage mode. The output voltage is sensed via resistor divider R8 and R9 operation with a reference voltage of 1.265 V on the FB pin when at the regulation output voltage.



5 PCB Layout

PCB copper thickness is 2 oz (2.8 mils / 70 μm) unless otherwise stated

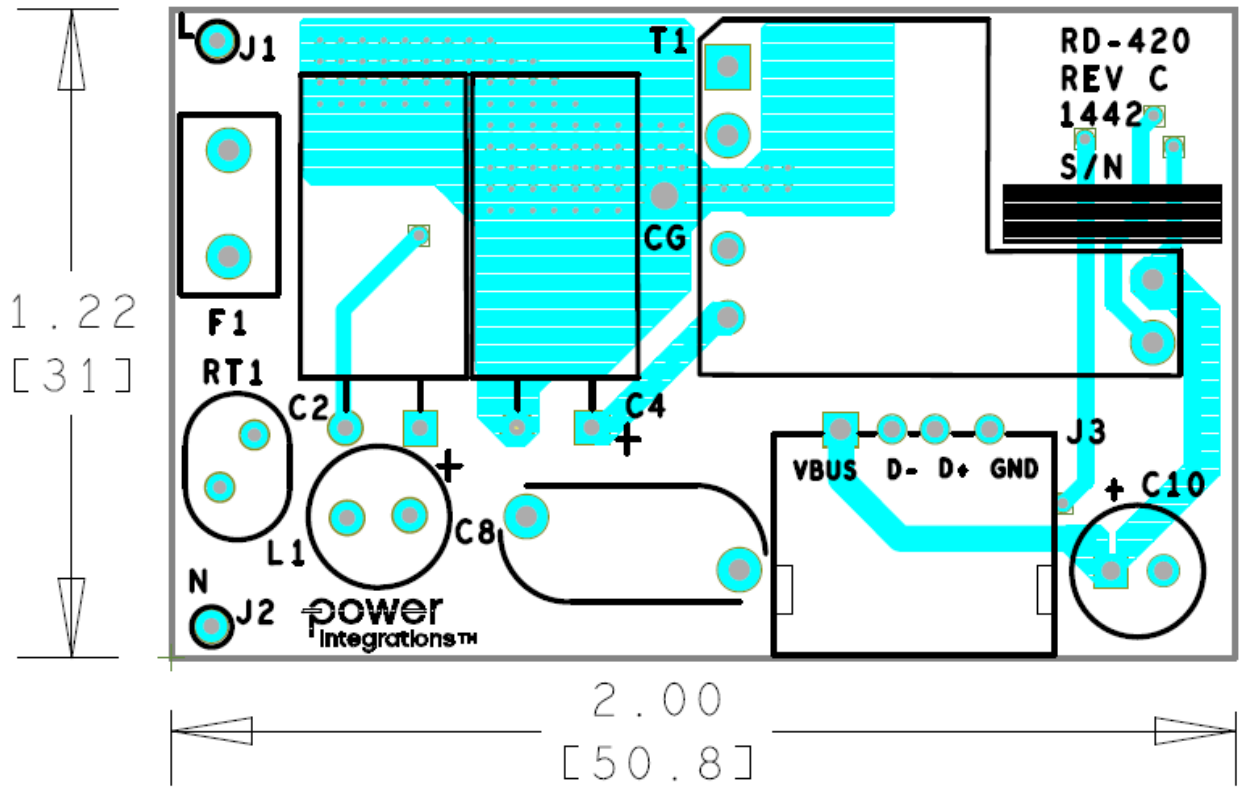


Figure 4 – Printed Circuit Layout, Top.



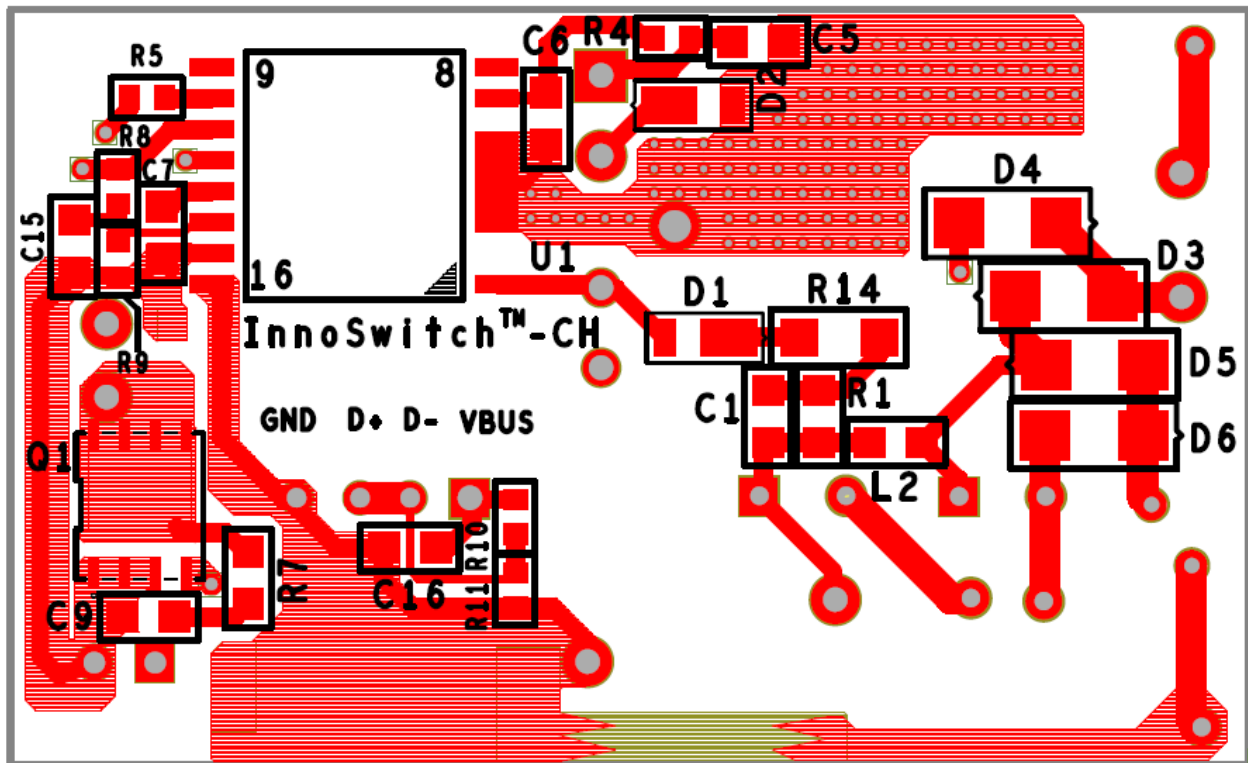


Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

| Item | Qty | Ref Des | Description | Mfg Part Number | Mfg |
|------|-----|----------------|--|-------------------------|---------------------------------|
| 1 | 1 | C1 | 1 nF, 250 V, Ceramic, X7R, 0805 | GRM21AR72E102KW01D | Murata |
| 2 | 2 | C2 C4 | 8.2 μ F, 400 V, Electrolytic, (8 x 14) 8.2 μ F, 400 V, Electrolytic, (8 x 14), Alternate part | 400AX8.2M8X16 | Capxon Rubycon |
| 3 | 1 | C5 | 22 μ F, 16 V, Ceramic, X5R, 0805 | C2012X5R1C226K | TDK |
| 4 | 1 | C6 | 1 μ F, 25 V, Ceramic, X5R, 0805 | C2012X5R1E105K | TDK |
| 5 | 1 | C7 | 2.2 μ F, 25 V, Ceramic, X7R, 0805 | C2012X7R1E225M | TDK |
| 6 | 1 | C8 | 100 pF, Ceramic, Y1 | 440LT10-R | Vishay |
| 7 | 1 | C9 | 1.5 nF, 200 V, 10%, Ceramic, X7R, 0805 | 08052C152KAT2A | AVX |
| 8 | 1 | C10 | 560 μ F, 6.3 V, Al Organic Polymer, Gen. Purpose, 20% | RS80J561MDN1JT | Nichicon |
| 9 | 1 | C15 | 100 pF 100 V 10 % X7R 0805 | 08051C101JAT2A | AVX |
| 10 | 1 | C16 | 1 μ F, 50 V, Ceramic, X5R, 0805 | 08055D105KAT2A | AVX |
| 11 | 1 | D1 | 600 V, 1 A, Rectifier, Glass Passivated, POWERDI123 | DFLR1600-7 | Diodes, Inc. |
| 12 | 1 | D2 | 200 V, 1 A, Rectifier, Glass Passivated, POWERDI123 | DFLR1200-7 | Diodes, Inc. |
| 13 | 4 | D3 D4 D5 D6 | 800 V, 1.5 A, Gen Purpose, SMA 800 V, 1.5 A, Gen Purpose, SMA, Alternate part | S2KA-13-F RS2MA-13-F | Diodes, Inc. Diodes, Inc. |
| 14 | 1 | F1 | 3.15 A, 250 V, Slow, RST | 507-1181 | Belfuse |
| 15 | 1 | J1 | Test Point, BLK, Miniature THRU-HOLE MOUNT | 5001K-ND | Keystone |
| 16 | 1 | J2 | Test Point, WHT, Miniature THRU-HOLE MOUNT | 5002K-ND | Keystone |
| 17 | 1 | J3 | Connector USB Female Type A | USB-AF-DIP-094-H | GOLDCONN |
| 18 | 1 | L1 | 100 μ H, 0.490 A, 20% | RL-5480-2-100 | Renco |
| 19 | 1 | L2 | 4.7 μ H, 600 mA SMD INDUCTOR, MULTILAYER | MLZ2012N4R7LT000 | TDK |
| 20 | 1 | Q1 | 60 V, 15 A, N-Channel, PowerPAK SO-8 | SI7478DP-T1-E3 | Vishay |
| 21 | 1 | R1 | 200 k Ω , 5%, 1/8 W, Thick Film, 0805 | ERJ-6GEYJ204V | Panasonic |
| 22 | 1 | R4 | 3 k Ω , 5%, 1/10 W, Thick Film, 0603 | ERJ-3GEYJ302V | Panasonic |
| 23 | 1 | R5 | 47 Ω , 5%, 1/10 W, Thick Film, 0603 | ERJ-3GEYJ470V | Panasonic |
| 24 | 1 | R7 | 20 Ω , 5%, 1/8 W, Thick Film, 0805 | ERJ-6GEYJ200V | Panasonic |
| 25 | 1 | R8 | 100 k Ω , 1%, 1/16 W, Thick Film, 0603 | ERJ-3KEF1003V | Panasonic |
| 26 | 1 | R9 | 34 k Ω , 1%, 1/16 W, Thick Film, 0603 | ERJ-3KEF3402V | Panasonic |
| 27 | 1 | R10 | 330 k Ω , 5%, 1/10 W, Thick Film, 0603 | ERJ-3GEYJ334V | Panasonic |
| 28 | 1 | R11 | 100 k Ω , 5%, 1/10 W, Thick Film, 0603 | ERJ-3GEYJ104V | Panasonic |
| 29 | 1 | R14 | 30 Ω , 5%, 1/4 W, Thick Film, 1206 | ERJ-8GEYJ300V | Panasonic |
| 30 | 1 | RT1 | NTC Thermistor, 10 Ohms, 0.7 A | MF72-010D5 | Cantherm |
| 31 | 1 | T1 | Custom (see transformer section for material set) | SNX-R1776 TSD-3517 | Santronics Premier Magnetics |
| 32 | 1 | U1 | InnoSwitch-CH IC eSOP-R16B | INN2023K | Power Integrations |

7 Transformer Specification

7.1 Electrical Diagram

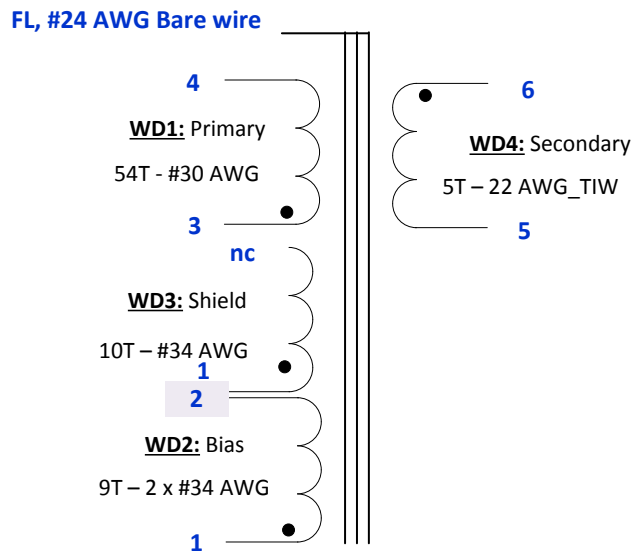


Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

| | | |
|-----------------------------------|--|----------------|
| Primary Inductance | Pins 3-4, all other windings open, measured at 100 kHz, 0.4 V _{RMS} . | 546 μH ±5% |
| Resonant Frequency | Pins 3-4, all other windings open. | 1200 kHz (min) |
| Primary Leakage Inductance | Pins 3-4, with pins 5-6 shorted, measured at 100 kHz, 0.4 V _{RMS} . | 25 μH (max) |

7.3 Materials

| Item | Description |
|------|--|
| [1] | Core: EE1621; PC-40 or equivalent. |
| [2] | Bobbin: EE1621-Vertical – 8 pins (4/4) Shen Zhen Xin Yu Jia Technology Ltd. |
| [3] | Magnet Wire: #30 AWG, double coated. |
| [4] | Magnet Wire: #34 AWG, double coated. |
| [5] | Magnet Wire: #22 AWG, Triple Insulated Wire. |
| [6] | Tape: 3M 1298 Polyester Film, 2 mil thick, 5.5 mm wide. |
| [7] | Epoxy: Devcon, 5 Minute Epoxy, No. 14210; or equivalent. |
| [8] | Bus wire: #24 AWG, Belden Electronics Div; or equivalent. |
| [9] | Varnish: Dolph BC-359. |

7.4 Transformer Build Diagram

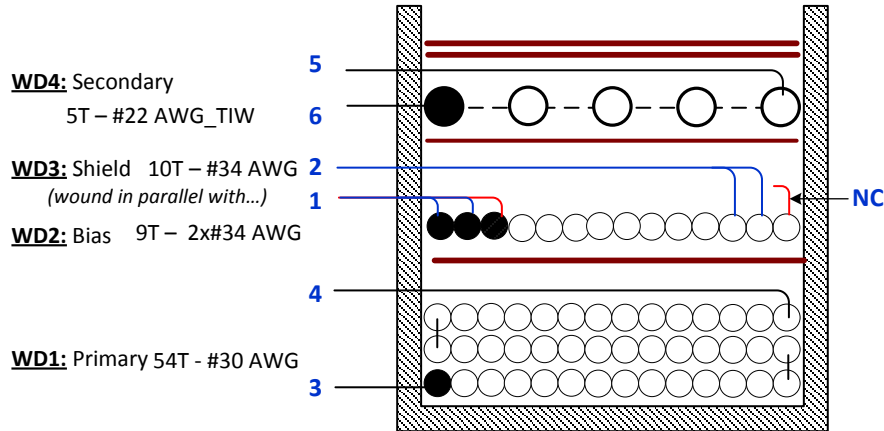
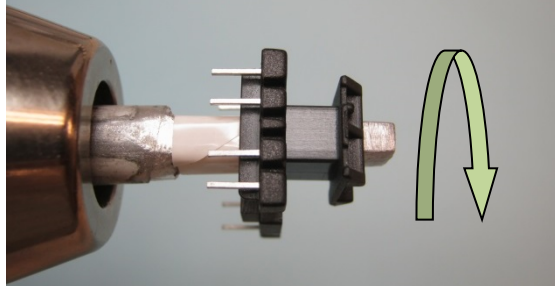
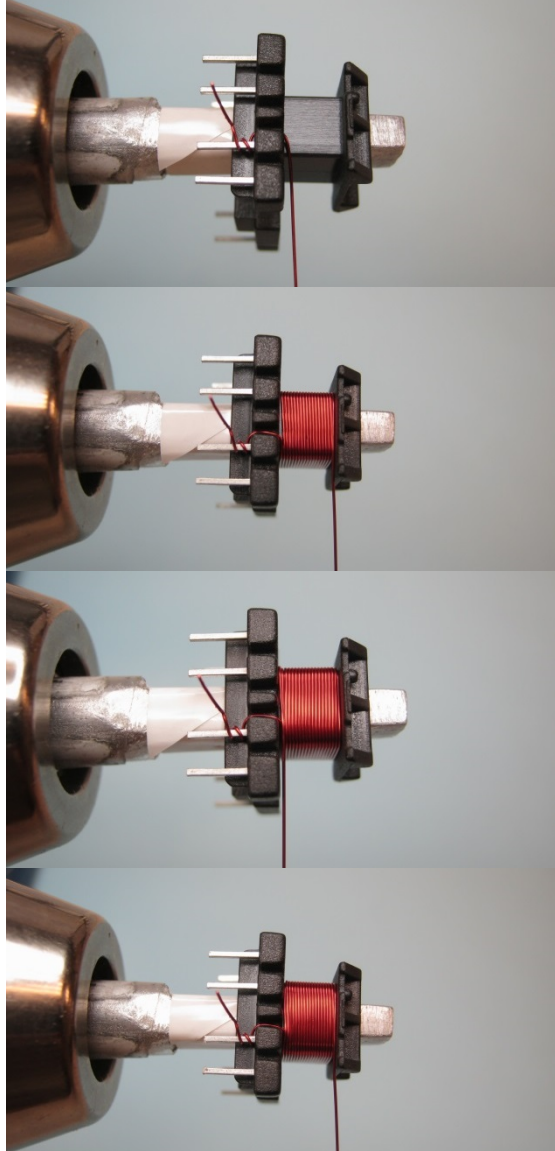


Figure 7 – Transformer Build Diagram.

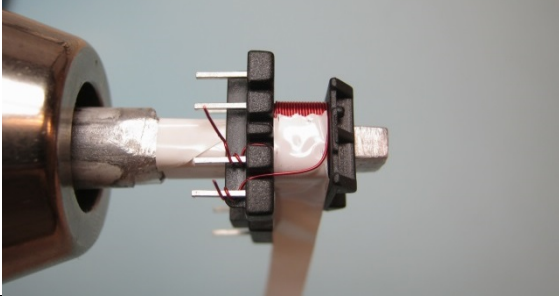
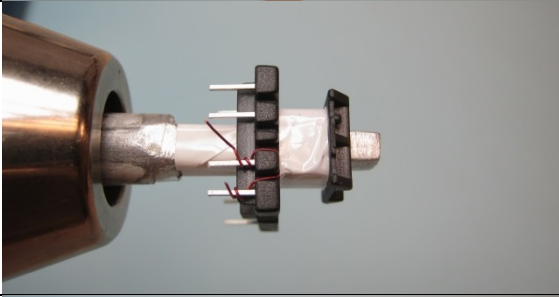
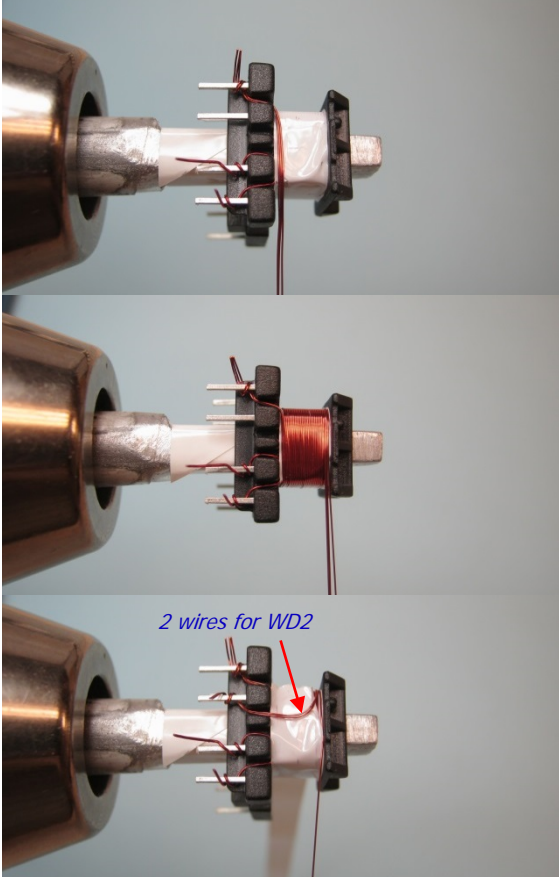
7.5 Transformer Instructions

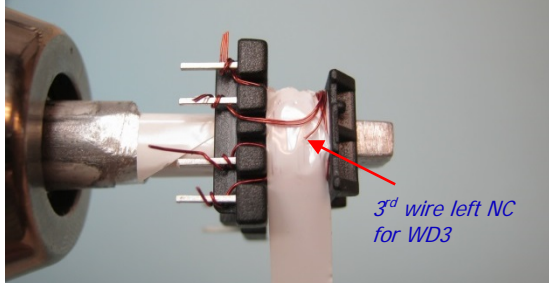
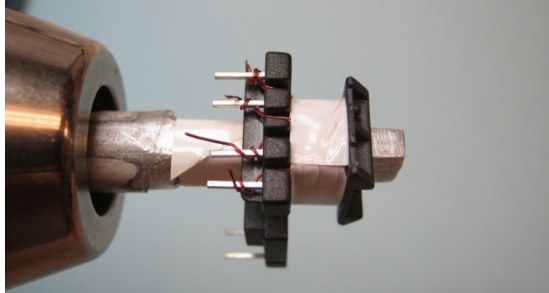
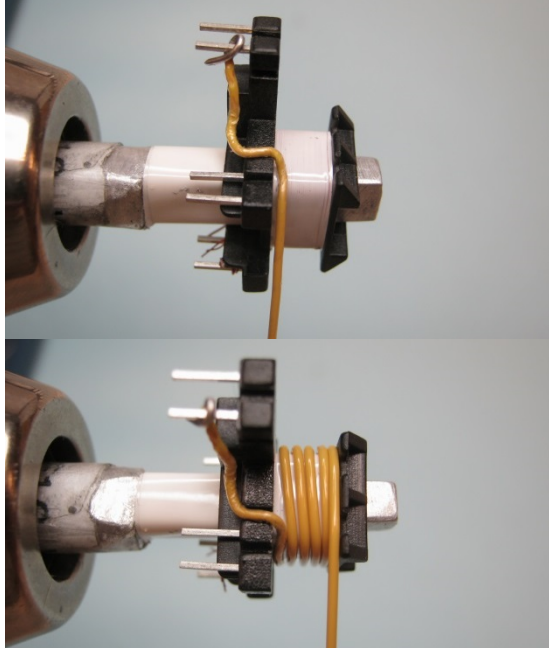
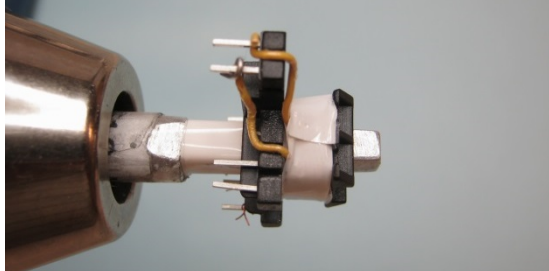
| | |
|--|--|
| Winding Preparation | For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction. |
| WD1 Primary | Start at pin 3, wind 54 turns wire item [2] in 3 layers (18T/layer) with tight tension. At the last turn bring the wire back to the left and finish at pin 4. |
| Insulation | 1 layer of tape [6] for insulation. |
| WD2 & WD3 Bias & Shield | Use 3 wires item [4], start at pin 1, and wind 9 turns from left to right. At the last turn, bring 2 wires to the left to terminate at pin 2 for WD2. Then continue winding on the 3 rd wire 1 more turn and left no-connect for WD3. |
| Insulation | 1 layer of tape [6] for insulation. |
| WD4 Secondary | Start at pin 6, wind 5 turns wire item [5], spread wire evenly. At the last turn bring the wire back to the left and finish at pin 5. |
| Insulation | 2 Layer of tape [6] to secure the windings. |
| Finish | Gap core halves for 546 μ H inductance. Place epoxy item [7] onto both center legs of core halves, (see illustration below). Wrap core halves and bus wire item [8] with tape, (see illustration below). Varnish with item [9]. |

7.6 Transformer Illustrations

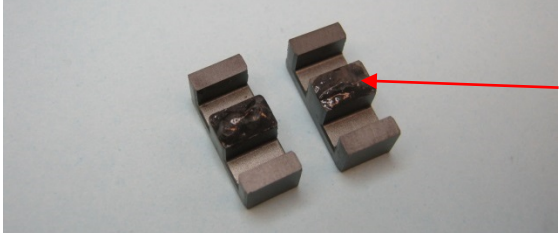
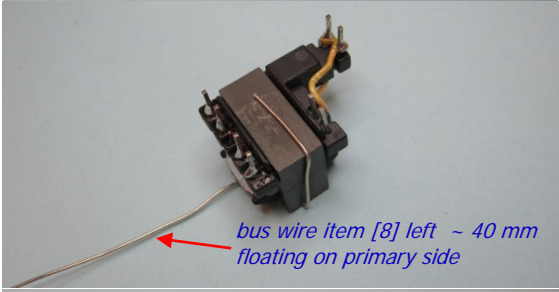
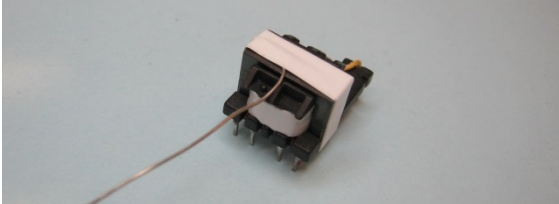
| | | |
|-----------------------------------|---|--|
| <p>Winding Preparation</p> |  | <p>For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.</p> |
| <p>WD1 Primary</p> |  | <p>Start at pin 3, wind 54 turns wire item [2] in 3 layers (18T/layer) with tight tension. At the last turn bring the wire back to the left and finish at pin 4.</p> |



| | | |
|---|---|--|
| |  | |
| <p>Insulation</p> |  | <p>1 layer of tape [6] for insulation.</p> |
| <p>WD2 & WD3 Bias & Shield</p> |  <p style="color: blue; font-size: small;">2 wires for WD2</p> | <p>Use 3 wires item [4], start at pin 1, and wind 9 turns from left to right. At the last turn, bring 2 wires to the left to terminate at pin 2 for WD2. Then continue winding on the 3rd wire 1 more turn and left no-connect for WD3.</p> |

| | | |
|---------------------------------|--|--|
| |  | |
| <p>Insulation</p> |  | <p>1 layer of tape [6] for insulation.</p> |
| <p>WD4 Secondary</p> |  | <p>Start at pin 6, wind 5 turns wire item [5], spread wire evenly. At the last turn bring the wire back to the left and finish at pin 5.</p> |
| <p>Insulation</p> |  | <p>2 layer of tape [6] to secure the windings.</p> |



| | | |
|----------------------|---|--|
| <p>Finish</p> |  <p>A photograph showing two dark-colored core halves. Each half has a small, dark, rectangular epoxy component applied to its center leg. A red arrow points from the right half towards the text on the right.</p> | <p>Gap core halves for 546 μH inductance. Place epoxy item [7] onto both center legs of core halves, (see illustration beside).</p> |
| |  <p>A photograph of the core assembly with a bus wire attached. The wire is connected to the primary side. A red arrow points to the wire with the text: "bus wire item [8] left ~ 40 mm floating on primary side".</p> | |
| |  <p>A photograph of the completed core assembly, now wrapped in white tape. The bus wire is still attached.</p> | <p>Wrap core halves and bus wire item [8] with tape, (see illustration below). Varnish with item [9].</p> |

8 Transformer Design Spreadsheet

| ACDC_InnoSwitch-CH_101614; Rev.2.0; Copyright Power Integrations 2014 | INPUT | INFO | OUTPUT | UNIT | ACDC_InnoSwitch_101614_Rev2-0; InnoSwitch-CH Continuous/Discontinuous Flyback Transformer Design Spreadsheet |
|---|---------|------|-------------------------|--------------------|--|
| ENTER APPLICATION VARIABLES | | | | | |
| VACMIN | | | 85 | V | Minimum AC Input Voltage |
| VACMAX | | | 265 | V | Maximum AC Input Voltage |
| fL | | | 50 | Hz | AC Mains Frequency |
| VO | 5.00 | | 5.00 | V | Output Voltage (continuous power at the end of the cable) |
| IO | 2.00 | | 2.00 | A | Power Supply Output Current (corresponding to peak power) |
| Power | | | 10.6 | W | Continuous Output Power, including cable drop compensation |
| n | 0.82 | | 0.82 | | Efficiency Estimate at output terminals. Use 0.8 if no better data available |
| Z | | | 0.50 | | Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available |
| tC | | | 3.00 | mSeconds | Bridge Rectifier Conduction Time Estimate |
| CIN | 16.40 | Info | 16.40 | uFarad | !!! Input capacitor is too small. Recommended to increase CIN above 19.05 uF to ensure VMIN>70 V |
| ENTER InnoSwitch VARIABLES | | | | | |
| InnoSwitch-CH | INN20x3 | | INN20x3 | | User defined InnoSwitch |
| Cable drop compensation | 6% | | 6% | | Select Cable Drop Compensation option |
| Complete Part Number | | | INN2023K | | Final part number including package |
| Chose Configuration | INC | | Increased Current Limit | | Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications) |
| ILIMITMIN | | | 0.682 | A | Minimum Current Limit |
| ILIMITTYP | | | 0.75 | A | Typical Current Limit |
| ILIMITMAX | | | 0.818 | A | Maximum Current Limit |
| fSmin | | | 93000 | Hz | Minimum Device Switching Frequency |
| I ² fmin | | | 47.25 | A ² kHz | Worst case I ² F parameter across the temperature range |
| VOR | 58 | | 58 | V | Reflected Output Voltage (VOR ≤ 100 V Recommended) |
| VDS | | | 5.00 | V | InnoSwitch on-state Drain to Source Voltage |
| KP | | | 0.80 | | Ripple to Peak Current Ratio at Vmin, assuming ILIMITMIN, and I2FMIN (KP < 6) |
| KP_TRANSIENT | | | 0.46 | | Worst case transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25 |
| ENTER BIAS WINDING VARIABLES | | | | | |
| VB | | | 10.00 | V | Bias Winding Voltage |
| VDB | | | 0.70 | V | Bias Winding Diode Forward Voltage Drop |
| NB | | | 9.32 | V | Bias Winding Number of Turns |
| PIVB | | | 102.59 | V | Bias winding peak reverse voltage at VACmax and assuming VB*1.2 |
| ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES | | | | | |
| Core Type | Custom | | Custom | | Enter Transformer Core |
| Core | EE1621 | | EE1621 | | Enter core part number, if necessary |
| Bobbin | | | 0 | | Enter bobbin part number, if necessary |
| AE | 0.325 | | 0.325 | cm ² | Core Effective Cross Sectional Area |



| | | | | | |
|--|------|---------|-------|-------------------|--|
| LE | 3.93 | | 3.93 | cm | Core Effective Path Length |
| AL | 2800 | | 2800 | nH/T ² | Ungapped Core Effective Inductance |
| BW | 5.40 | | 5.40 | mm | Bobbin Physical Winding Width |
| M | | | 0.00 | mm | Safety Margin Width (Half the Primary to Secondary Creepage Distance) |
| L | 3 | | 3 | | Number of Primary Layers |
| NS | 5 | | 5 | | Number of Secondary Turns |
| DC INPUT VOLTAGE PARAMETERS | | | | | |
| VMIN | 62 | Warning | 62 | V | !!! Minimum DC Input Voltage < 70 Volts. Increase VACMIN or increase CIN |
| VMAX | | | 375 | V | Maximum DC Input Voltage |
| CURRENT WAVEFORM SHAPE PARAMETERS | | | | | |
| DMAX | | | 0.50 | | Duty Ratio at full load, minimum primary inductance and minimum input voltage |
| I AVG | | | 0.21 | A | Average Primary Current |
| IP | | | 0.682 | A | Peak Primary Current assuming I LIMITMIN |
| IR | | | 0.546 | A | Primary Ripple Current assuming I LIMITMIN, and L PMIN |
| IRMS | | | 0.31 | A | Primary RMS Current, assuming I LIMITMIN, and L PMIN |
| TRANSFORMER PRIMARY DESIGN PARAMETERS | | | | | |
| LP | | | 546 | uHenry | Typical Primary Inductance. +/- 5% to ensure a minimum primary inductance of 518 uH |
| LP_TOLERANCE | 5.0 | | 5.0 | % | Primary inductance tolerance |
| NP | | | 54 | | Primary Winding Number of Turns |
| ALG | | | 187 | nH/T ² | Gapped Core Effective Inductance |
| BM | | | 2868 | Gauss | Maximum Operating Flux Density, BM<3000 is recommended |
| BAC | | | 1147 | Gauss | AC Flux Density for Core Loss Curves (0.5 X Peak to Peak) |
| ur | | | 2694 | | Relative Permeability of Ungapped Core |
| LG | | | 0.20 | mm | Gap Length (Lg > 0.1 mm) |
| BWE | | | 16.2 | mm | Effective Bobbin Width |
| OD | | | 0.30 | mm | Maximum Primary Wire Diameter including insulation |
| INS | | | 0.05 | mm | Estimated Total Insulation Thickness (= 2 * film thickness) |
| DIA | | | 0.25 | mm | Bare conductor diameter |
| AWG | | | 31 | AWG | Primary Wire Gauge (Rounded to next smaller standard AWG value) |
| CM | | | 81 | Cmils | Bare conductor effective area in circular mils |
| CMA | | | 259 | Cmils/Amp | Primary Winding Current Capacity (200 < CMA < 500) |
| TRANSFORMER SECONDARY DESIGN PARAMETERS | | | | | |
| Lumped parameters | | | | | |
| ISP | | | 7.37 | A | Peak Secondary Current, assuming I LIMITMIN |
| ISRMS | | | 3.33 | A | Secondary RMS Current |
| IRIPPLE | | | 2.67 | A | Output Capacitor RMS Ripple Current |
| CMS | | | 667 | Cmils | Secondary Bare Conductor minimum circular mils |
| AWGS | | | 21 | AWG | Secondary Wire Gauge (Rounded up to next larger standard AWG value) |
| VOLTAGE STRESS PARAMETERS | | | | | |
| VDRAIN | | | 517 | V | Maximum Drain Voltage Estimate |
| PIVS | | | 54 | V | Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05 |
| TRANSFORMER SECONDARY DESIGN PARAMETERS | | | | | |
| 1st output | | | | | |
| VO1 | | | 5.30 | V | Main Output Voltage directly after output rectifier |

| | | | | | |
|--------------------|--|--|--------|-------|--|
| IO1 | | | 2.00 | A | Output DC Current |
| PO1 | | | 10.60 | W | Output Power |
| VD1 | | | 0.06 | V | Output Synchronous Rectification FET Forward Voltage Drop |
| NS1 | | | 5.00 | Turns | Output Winding Number of Turns |
| ISRMS1 | | | 3.33 | A | Output Winding RMS Current |
| IRIPPLE1 | | | 2.67 | A | Output Capacitor RMS Ripple Current |
| PIVS1 | | | 54 | V | Output Rectifier Maximum Peak Inverse Voltage, assuming the primary has a Voltage spike 40% above VMAX and VO*1.05 |
| Recommended MOSFET | | | QM6006 | | Recommended SR FET for this output |
| RDSON_HOT | | | 0.027 | Ohm | RDSon at 100C |
| VRATED | | | 60 | V | Rated voltage of selected SR FET |
| CMS1 | | | 667 | Cmils | Output Winding Bare Conductor minimum circular mils |
| AWGS1 | | | 21 | AWG | Wire Gauge (Rounded up to next larger standard AWG value) |
| DIAS1 | | | 0.73 | mm | Minimum Bare Conductor Diameter |
| ODS1 | | | 1.08 | mm | Maximum Outside Diameter for Triple Insulated Wire |



9 Performance Data

All measurements performed with external room ambient temperature and 60 Hz input for 115 VAC range and 50 Hz for 230 VAC input range.

9.1 Active Mode Efficiency (at USB Socket) vs. Line

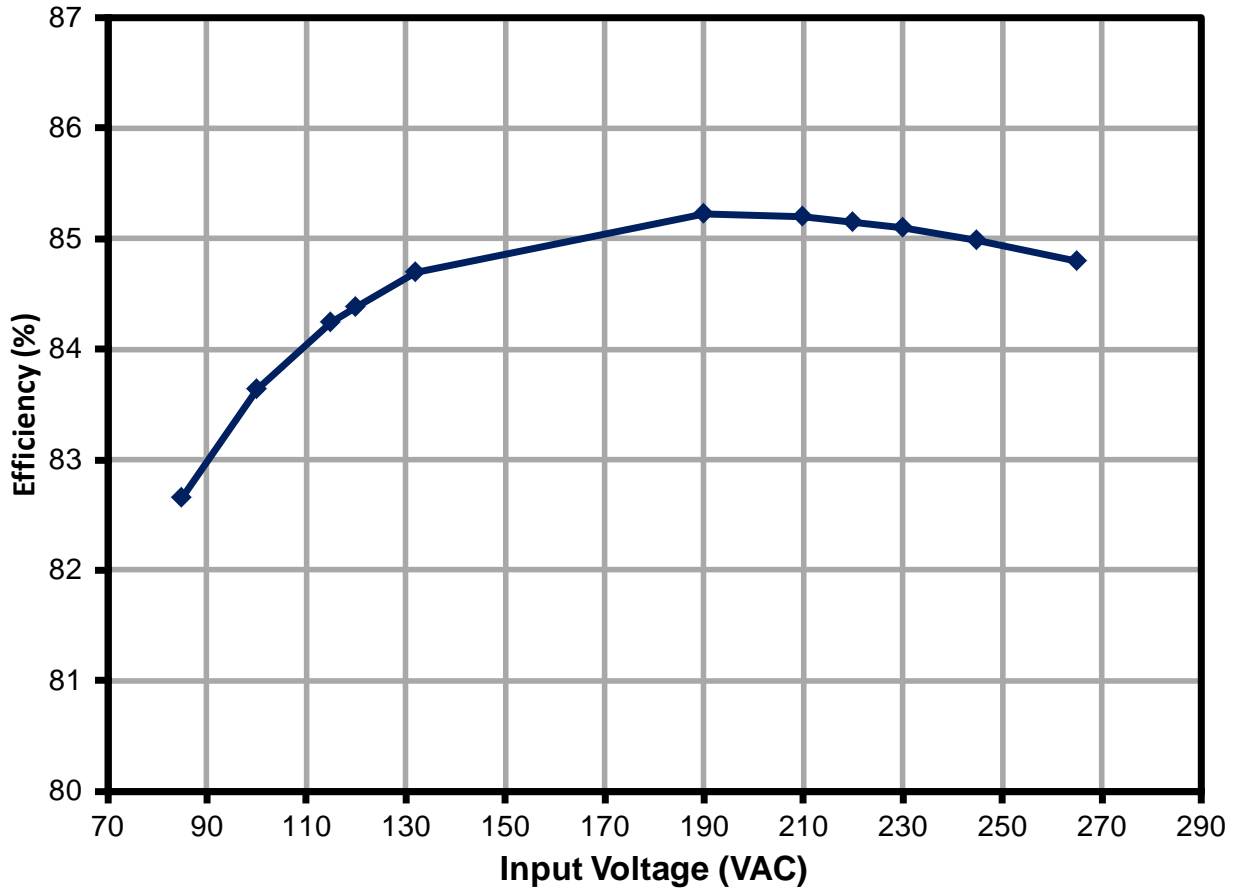


Figure 8 – Efficiency vs Line Voltage, Room Temperature



9.2 Active Mode Efficiency (at USB Socket) vs. Load

9.2.1 Efficiency without Schottky Diode in Parallel with Q1, SR FET

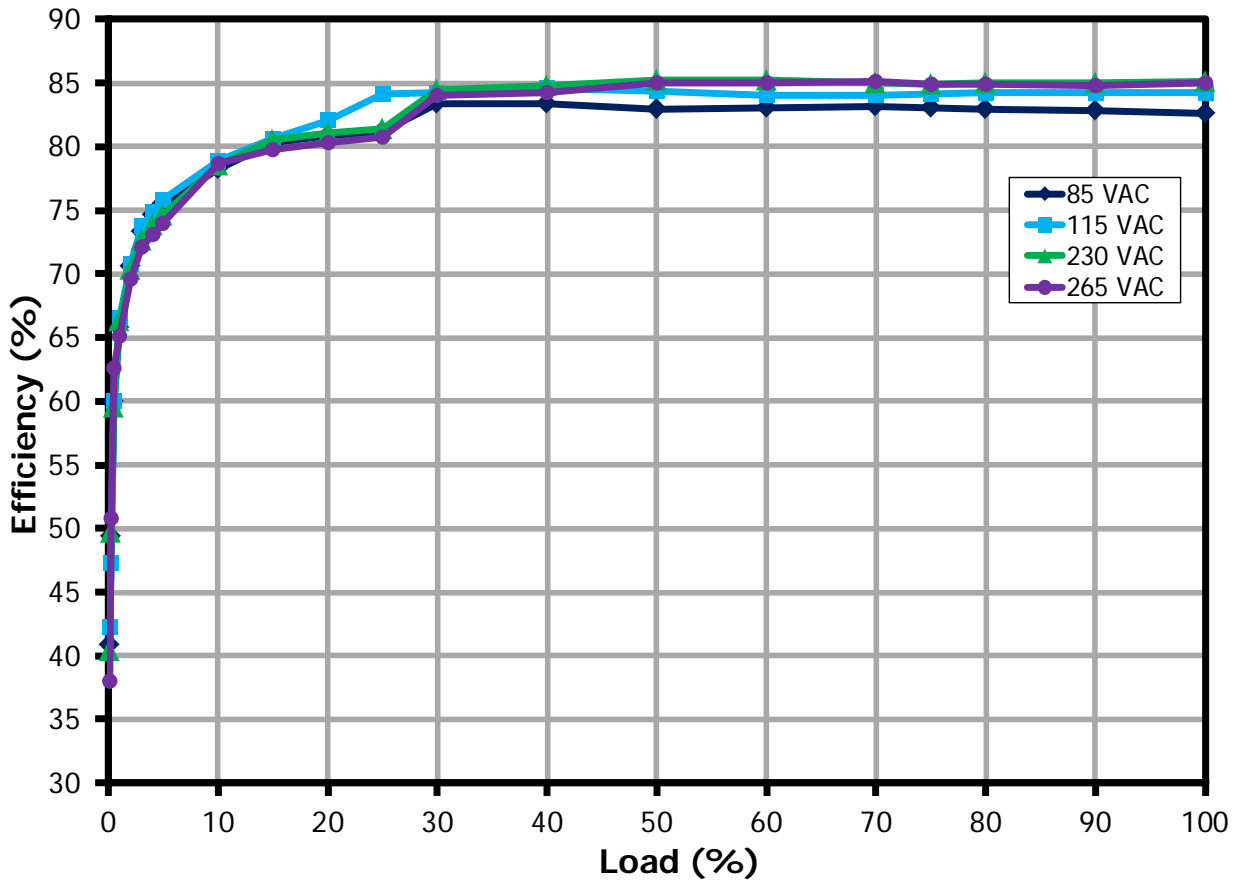


Figure 9 – Efficiency vs Load, Room Ambient

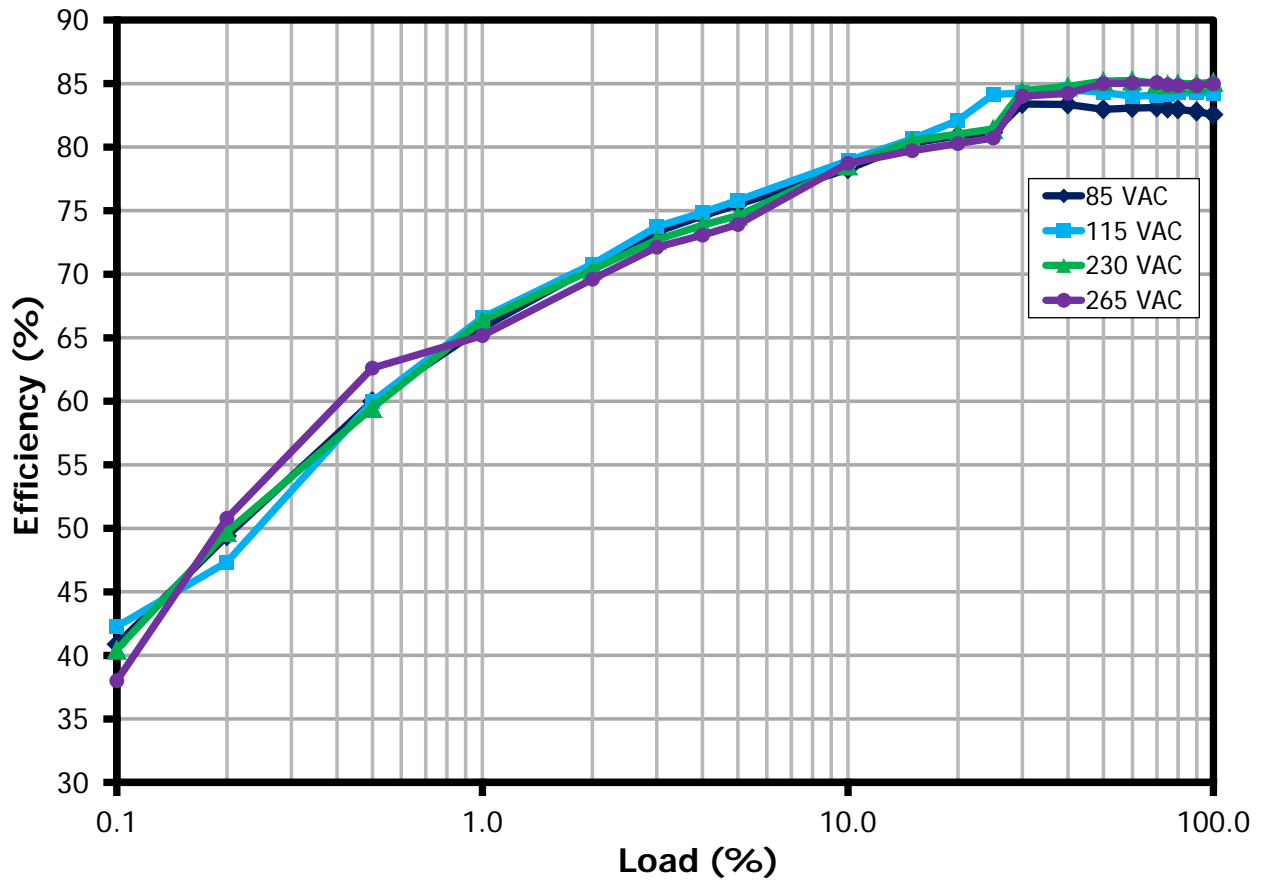


Figure 10 - Efficiency vs Load (log scale to demonstrate light load performance)



9.2.2 Efficiency with a Schottky Diode, SS16, in Parallel with Q1, SR FET

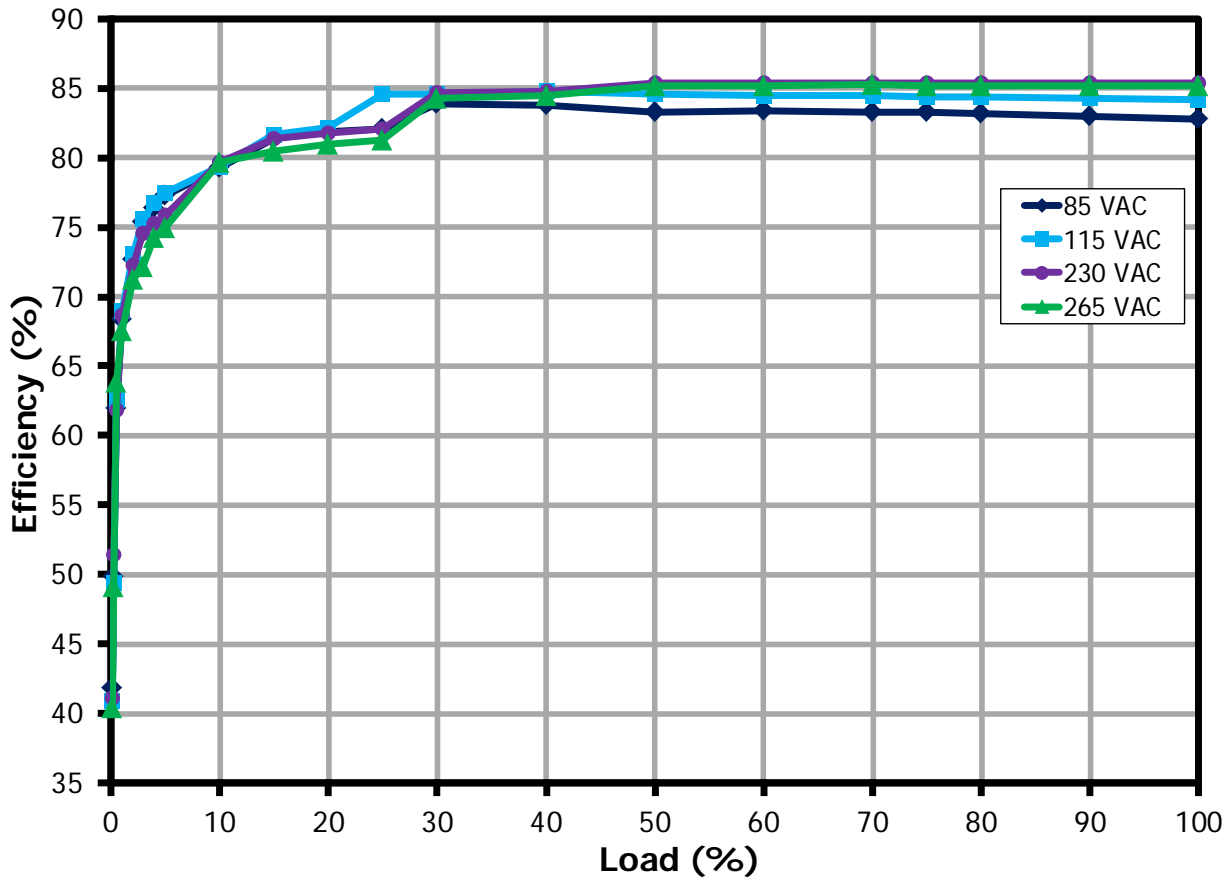


Figure 11 – Efficiency vs Load, Room Temperature, 60 Hz.

9.3 *No-Load Input Power*

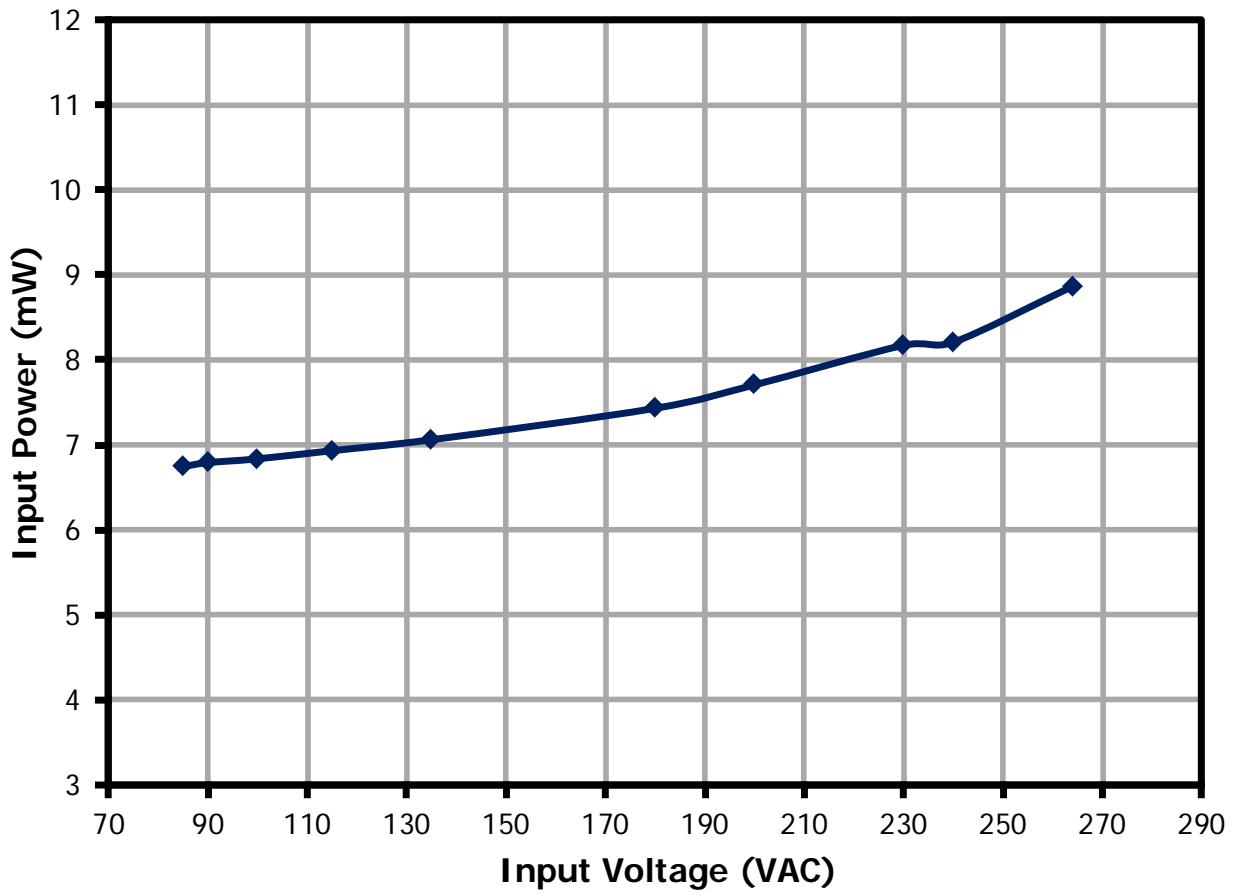


Figure 12 – No Load Input Power vs. Input Line Voltage, Room Temperature.



9.4 Average Efficiency (at USB Socket)

9.4.1 Efficiency Requirements

| Test | Average | Average | Average | Average | 10% Load | 10% Load |
|-----------|---------------|--------------|---------------|---------------|---------------|---------------|
| Model | <6 V Voltage | <6 V Voltage | <6 V Voltage | <6 V Voltage | <6 V Voltage | <6 V Voltage |
| Effective | Now | 2016 | Now | 2016 | Now | 2016 |
| Power [W] | Energy Star 2 | New IESA2007 | CoC v5 Tier 1 | CoC v5 Tier 2 | CoC v5 Tier 1 | CoC v5 Tier 2 |
| 10 | 74.2% | 78.7% | 76.0% | 79.0% | 66.6% | 69.7% |

9.4.2 Average Efficiency at 115 VAC Input

9.4.2.1 No Schottky Diode in Parallel with Q1, SR FET

| Load (%) | V _{IN} (V _{RMS}) | I _{IN} (A _{RMS}) | P _{IN} (W) | PF | %ATHD | V _{OUT} (V _{DC}) | I _{OUT} (A _{DC}) | P _{OUT} (W) | Efficiency (%) | Average Efficiency (%) |
|----------|-------------------------------------|-------------------------------------|---------------------|-------|-------|-------------------------------------|-------------------------------------|----------------------|----------------|------------------------|
| 100 | 114.98 | 0.19 | 12.473 | 0.566 | 131 | 5.2575 | 1.999 | 10.509 | 84.26 | |
| 75 | 114.98 | 0.15 | 9.255 | 0.542 | 144.4 | 5.1950 | 1.499 | 7.789 | 84.16 | |
| 50 | 114.99 | 0.10 | 6.078 | 0.505 | 163.5 | 5.1300 | 0.999 | 5.124 | 84.30 | |
| 25 | 114.99 | 0.06 | 3.001 | 0.449 | 194.8 | 5.0550 | 0.500 | 2.525 | 84.14 | 84.21 |
| 10 | 114.99 | 0.03 | 1.266 | 0.392 | 231.7 | 5.0100 | 0.199 | 0.999 | 78.94 | |

9.4.2.2 Schottky Diode, SS16, in Parallel with Q1, SR FET

| Load (%) | V _{IN} (V _{RMS}) | I _{IN} (A _{RMS}) | P _{IN} (W) | PF | %ATHD | V _{OUT} (V _{DC}) | I _{OUT} (A _{DC}) | P _{OUT} (W) | Efficiency (%) | Average Efficiency (%) |
|----------|-------------------------------------|-------------------------------------|---------------------|-------|-------|-------------------------------------|-------------------------------------|----------------------|----------------|------------------------|
| 100 | 114.98 | 0.19 | 12.492 | 0.572 | 129.4 | 5.2588 | 1.999 | 10.511 | 84.15 | |
| 75 | 114.99 | 0.15 | 9.230 | 0.544 | 143.5 | 5.1963 | 1.499 | 7.791 | 84.41 | |
| 50 | 114.99 | 0.10 | 6.060 | 0.508 | 162.6 | 5.1325 | 0.999 | 5.125 | 84.58 | |
| 25 | 114.99 | 0.06 | 2.987 | 0.452 | 193.4 | 5.0563 | 0.500 | 2.526 | 84.55 | 84.42 |
| 10 | 114.99 | 0.03 | 1.259 | 0.392 | 231.1 | 5.0113 | 0.199 | 0.999 | 79.36 | |

9.4.3 Average Efficiency at 230 VAC Input

9.4.3.1 No Schottky Diode in Parallel with Q1, SR FET

| Load (%) | V _{IN} (V _{RMS}) | I _{IN} (A _{RMS}) | P _{IN} (W) | PF | %ATHD | V _{OUT} (V _{DC}) | I _{OUT} (A _{DC}) | P _{OUT} (W) | Efficiency (%) | Average Efficiency (%) |
|-----------|-------------------------------------|-------------------------------------|---------------------|-------|-------|-------------------------------------|-------------------------------------|----------------------|----------------|------------------------|
| 100 | 230.04 | 0.12 | 12.364 | 0.450 | 195.1 | 5.2663 | 1.999 | 10.527 | 85.14 | |
| 75 | 230.04 | 0.09 | 9.179 | 0.426 | 209.4 | 5.2000 | 1.499 | 7.797 | 84.94 | |
| 50 | 230.04 | 0.07 | 6.021 | 0.397 | 228.4 | 5.1363 | 0.999 | 5.130 | 85.20 | |
| 25 | 230.04 | 0.04 | 3.097 | 0.358 | 258.7 | 5.0488 | 0.500 | 2.522 | 81.43 | 84.18 |
| 10 | 230.04 | 0.02 | 1.273 | 0.312 | 300.9 | 5.0150 | 0.199 | 1.000 | 78.56 | |

9.4.3.2 Schottky Diode, SS16, in Parallel with Q1, SR FET

| Load (%) | V _{IN} (V _{RMS}) | I _{IN} (A _{RMS}) | P _{IN} (W) | PF | %ATHD | V _{OUT} (V _{DC}) | I _{OUT} (A _{DC}) | P _{OUT} (W) | Efficiency (%) | Average Efficiency (%) |
|-----------|-------------------------------------|-------------------------------------|---------------------|-------|-------|-------------------------------------|-------------------------------------|----------------------|----------------|------------------------|
| 100 | 230.04 | 0.12 | 12.329 | 0.449 | 195.6 | 5.2663 | 1.999 | 10.527 | 85.38 | |
| 75 | 230.04 | 0.09 | 9.133 | 0.425 | 210 | 5.2000 | 1.499 | 7.796 | 85.36 | |
| 50 | 230.04 | 0.07 | 6.007 | 0.397 | 229.2 | 5.1363 | 0.999 | 5.129 | 85.39 | |
| 25 | 230.04 | 0.04 | 3.073 | 0.357 | 259.5 | 5.0488 | 0.500 | 2.522 | 82.06 | 84.55 |
| 10 | 230.04 | 0.02 | 1.255 | 0.312 | 301.7 | 5.0150 | 0.199 | 1.000 | 79.68 | |

9.5 CV/CC Regulation Measured at the End of Cable

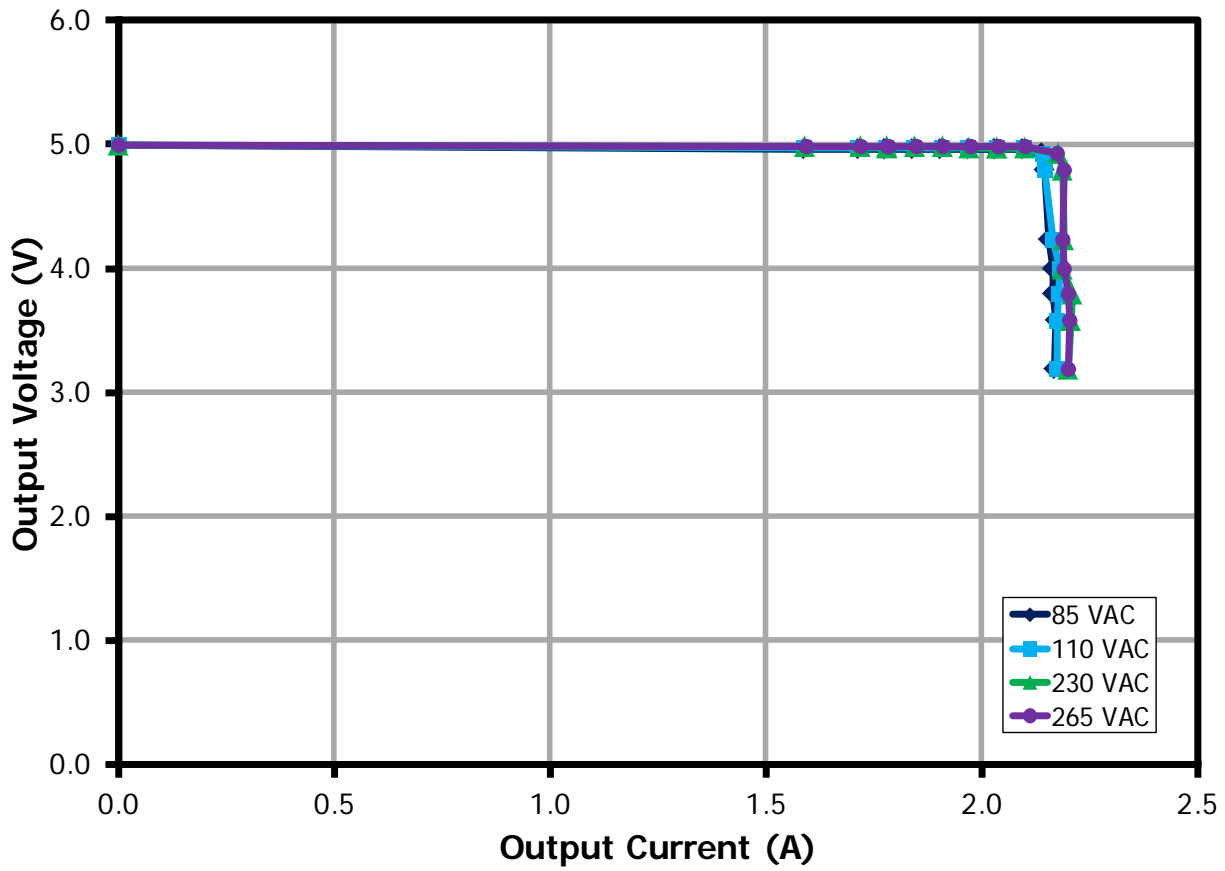


Figure 13 – Output Voltage vs, Output current, Room Temperature.



10 Open Case Thermal Performance

Room ambient.

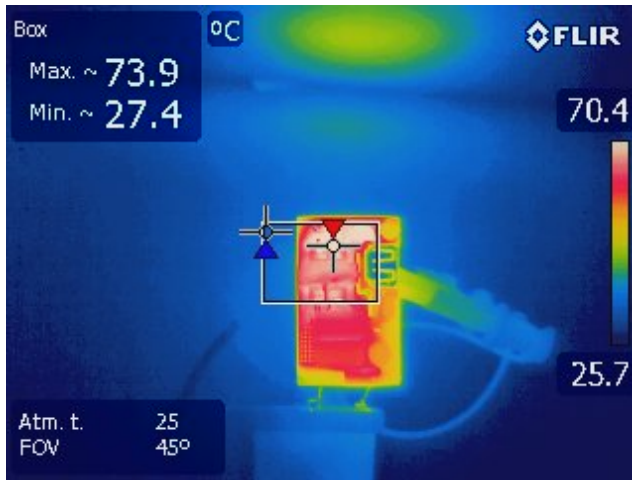


Figure 14 – Transformer Side.
85 VAC, 2 A Load.
Ambient = 26.3 °C.

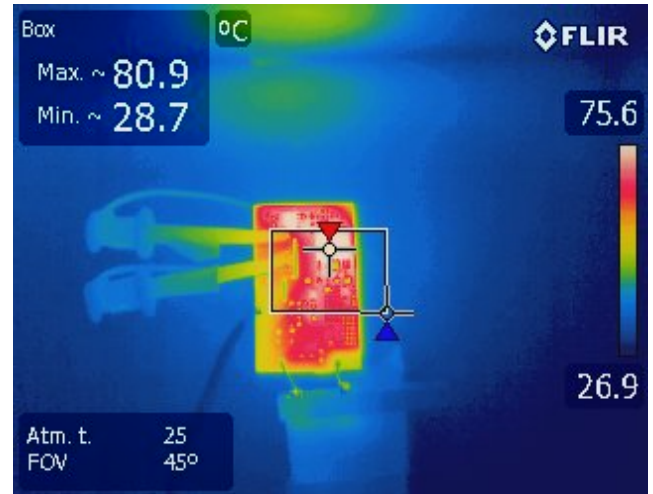


Figure 15 – InnoSwitch-CH Side.
85 VAC, 2 A Load.
Ambient = 27 °C.

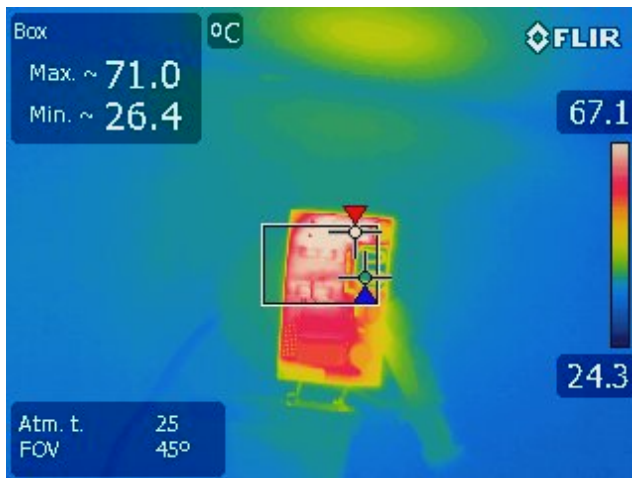


Figure 16 – Transformer Side.
110 VAC, 2 A Load.
Ambient = 26.2 °C.

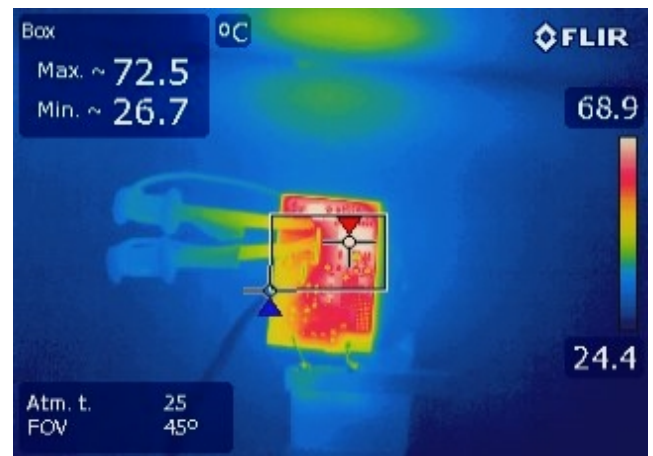


Figure 17 – InnoSwitch-CH Side.
110 VAC, 2 A Load.
Ambient = 25 °C.

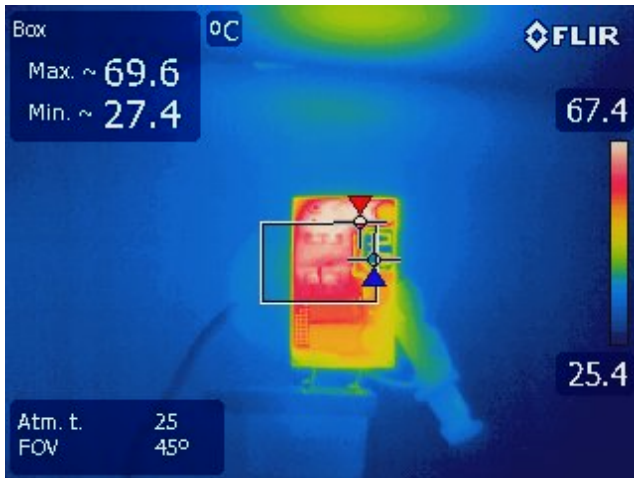


Figure 18 – Transformer Side.
230 VAC, 2 A Load.
Ambient = 26.5 °C.

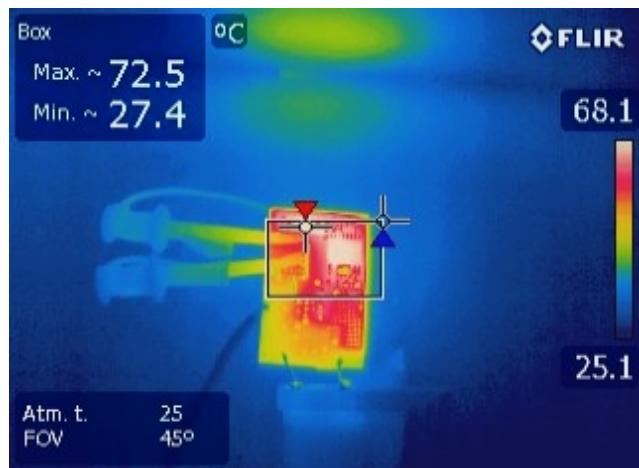


Figure 19 – InnoSwitch-CH Side.
230 VAC, 2 A Load.
Ambient = 25.4 °C.

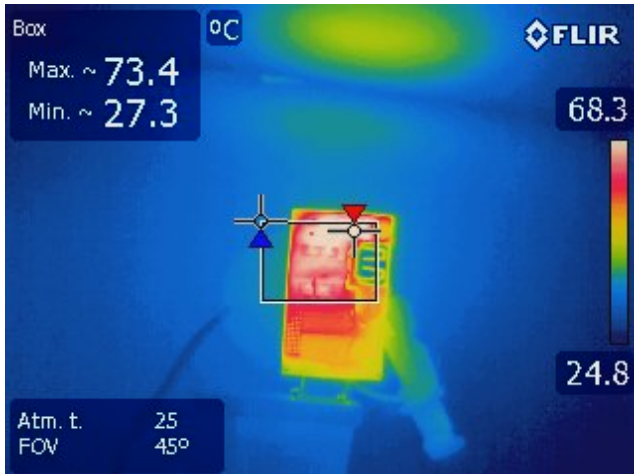


Figure 20 – Transformer Side.
265 VAC, 2 A Load.
Ambient = 26.5 °C.

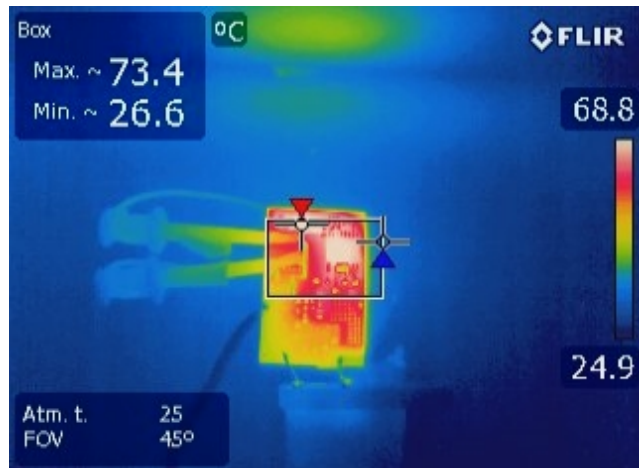


Figure 21 – InnoSwitch-CH Side.
265 VAC, 2 A Load.
Ambient = 25.3 °C.

11 Waveforms

11.1 Load Transient Response (end of cable)

Results were measured with 47 μF at end of cable which is the typical specified measurement condition for mobile phone chargers.

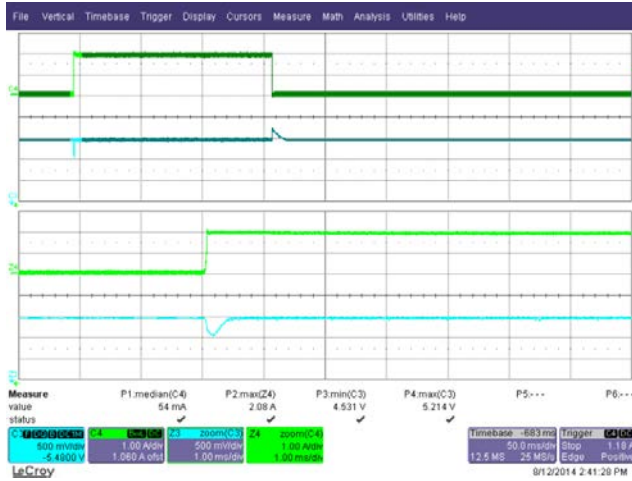


Figure 22 – Transient Response ($4.5 V_{MIN}$).
85 VAC, 0-2 A Load Step.
Upper: I_{LOAD} , 1 A / div.
Lower: V_{OUT} , 500 mV, 50 ms / div.

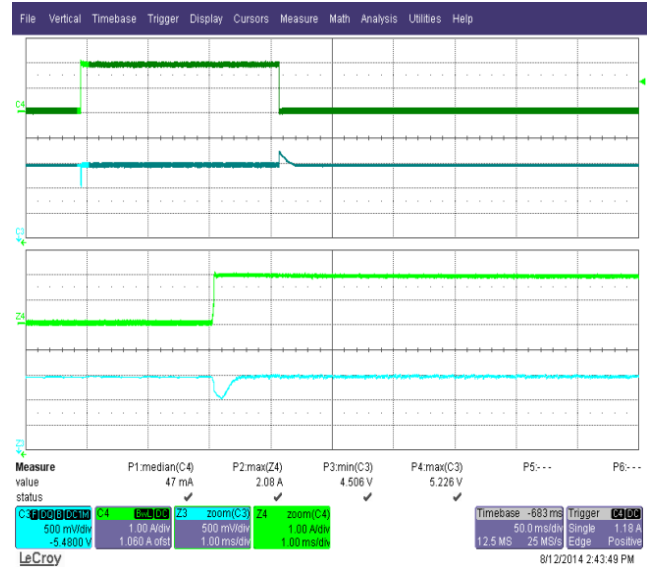


Figure 23 – Transient Response ($4.5 V_{MIN}$).
110 VAC, 0-2 A Load Step.
Upper: I_{LOAD} , 1 A / div.
Lower: V_{OUT} , 500 mV, 50 ms / div.

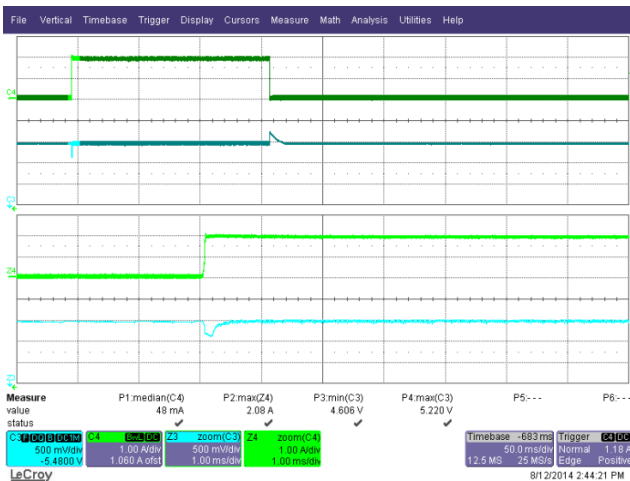


Figure 24 – Transient Response ($4.6 V_{MIN}$).
230 VAC, 0-2 A Load Step.
Upper: I_{LOAD} , 1 A / div.
Lower: V_{OUT} , 500 mV, 50 ms / div.

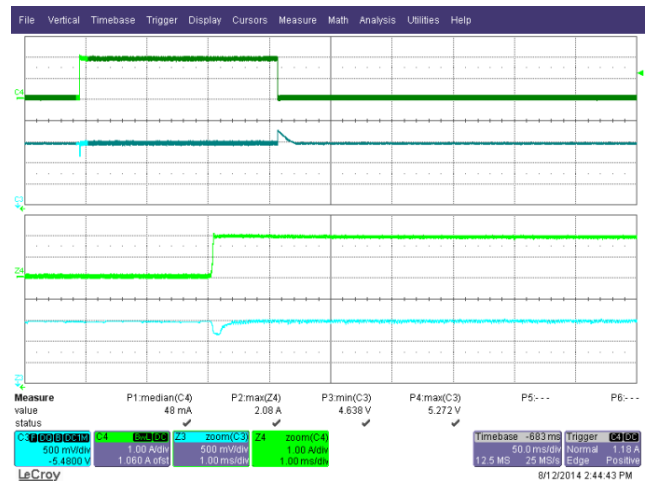


Figure 25 – Transient Response ($4.6 V_{MIN}$).
265 VAC, 0-2 A Load Step.
Upper: I_{LOAD} , 1 A / div.
Lower: V_{OUT} , 500 mV, 50 ms / div.

11.2 Load Transient Response (at USB Socket)

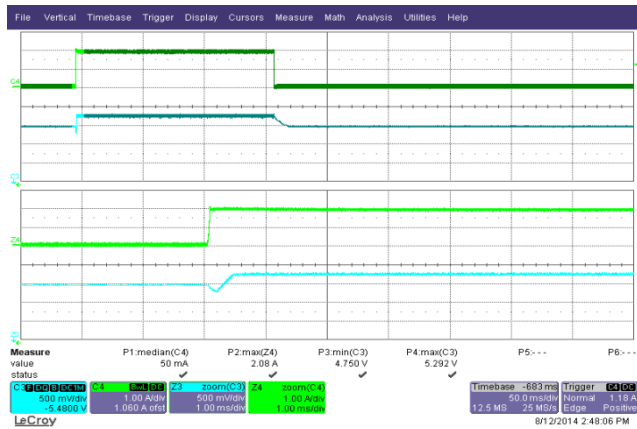


Figure 26 – Transient Response (4.75 V_{MIN}).
85 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

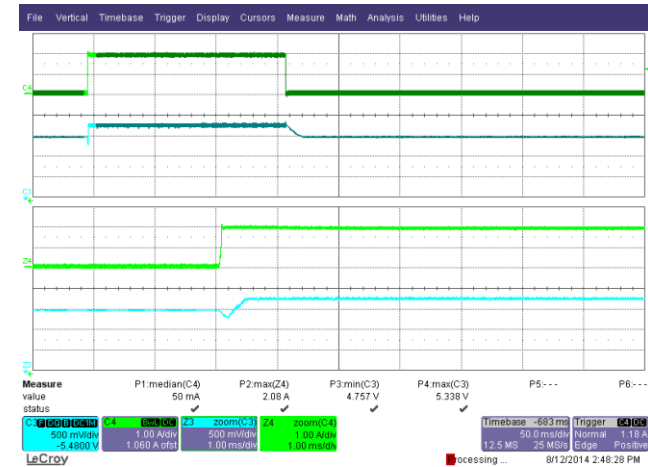


Figure 27 – Transient Response (4.75 V_{MIN}).
110 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

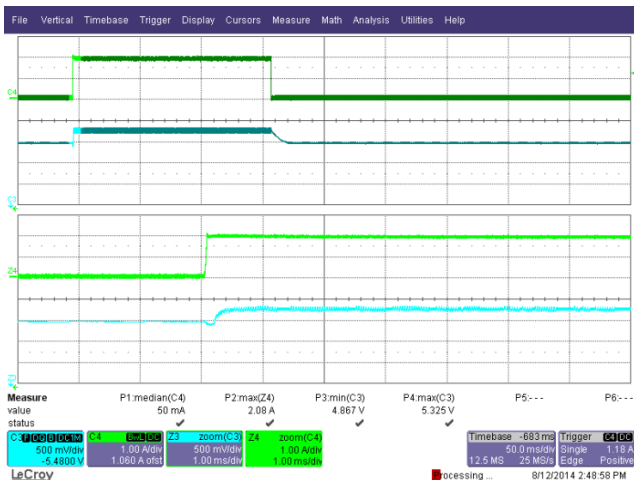


Figure 28 – Transient Response (4.85 V_{MIN}).
230 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

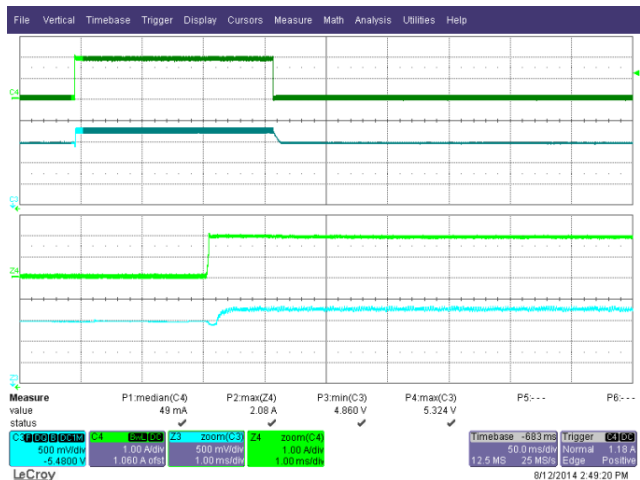


Figure 29 – Transient Response (4.86 V_{MIN}).
265 VAC, 0-2 A Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 500 mV, 50 ms / div.

11.3 Switching Waveforms

11.3.1 InnoSwitch-CH Waveforms

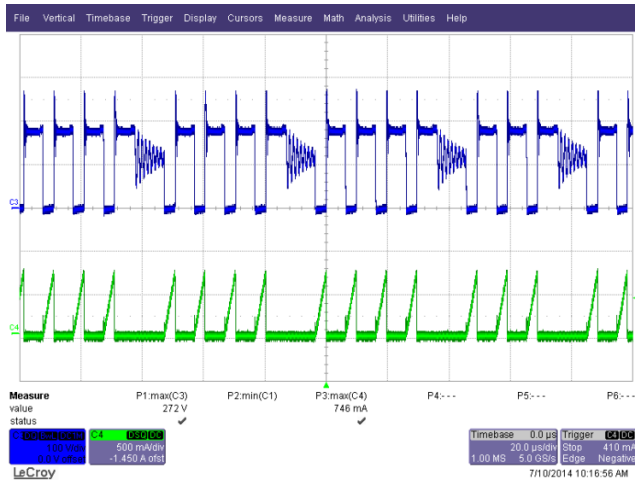


Figure 30 – Drain Voltage and Current Waveforms.
 85 VAC, 2 A load,
 Lower: I_{DRAIN} , 500 mA / div.
 Upper: V_{DRAIN} , 100 V, 20 μ s / div.

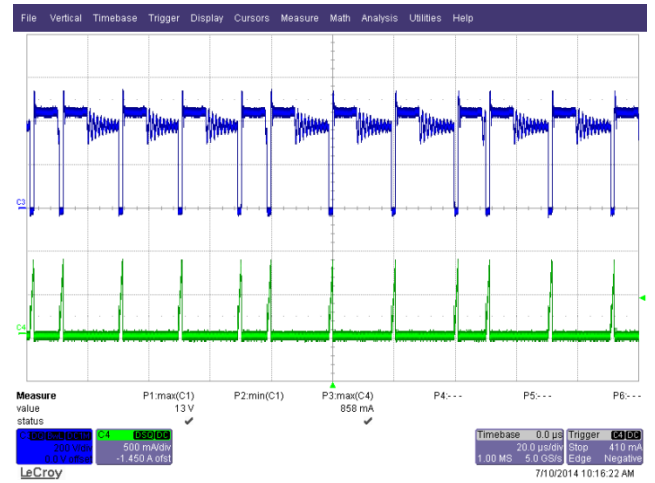


Figure 31 – Drain Voltage and Current Waveforms.
 265 VAC, 2 A Load, 545 V_{MAX} .
 Lower: I_{DRAIN} , 500 mA / div.
 Upper: V_{DRAIN} , 200 V, 20 μ s / div.

11.3.2 SR FET Waveforms

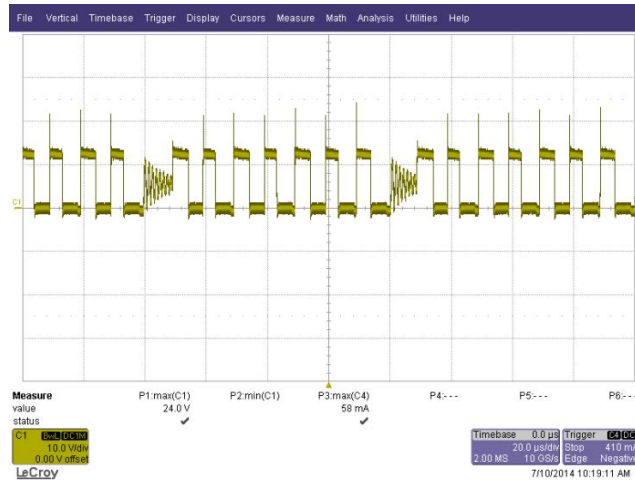


Figure 32 – SR FET Voltage Waveforms.
 85 VAC Input, 2 A Load.
 V_{DRAIN} , 10 V, 20 μ s / div.

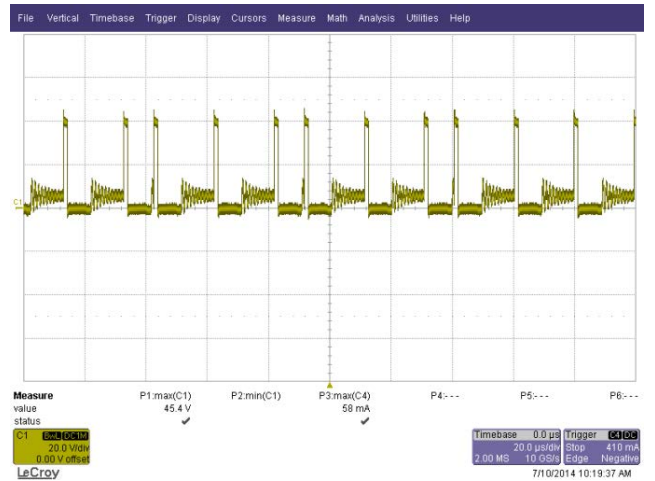


Figure 33 – SR FET Voltage Waveforms.
 265 VAC Input, 2 A Load.
 V_{DRAIN} , 20 V, 20 μ s / div. (45.4 V_{MAX}).



11.4 Output Ripple Measurements

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF /50 V ceramic type and one (1) 47 μF /50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

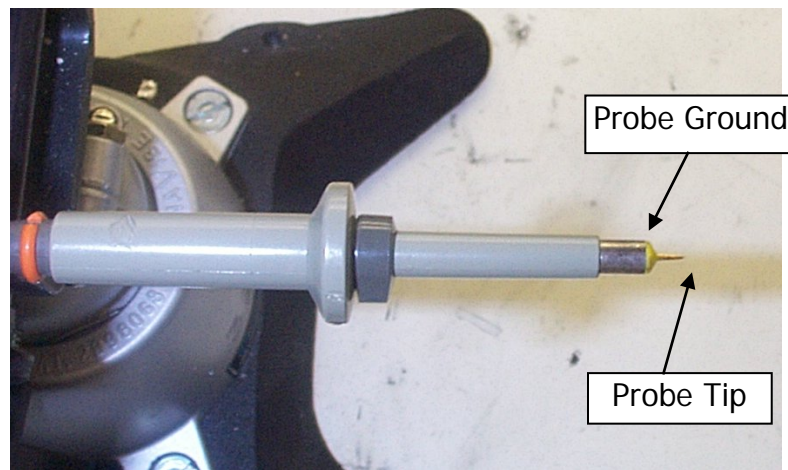


Figure 34 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)



Figure 35 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

11.4.2 Measurement Results

Measured at the end of cable.

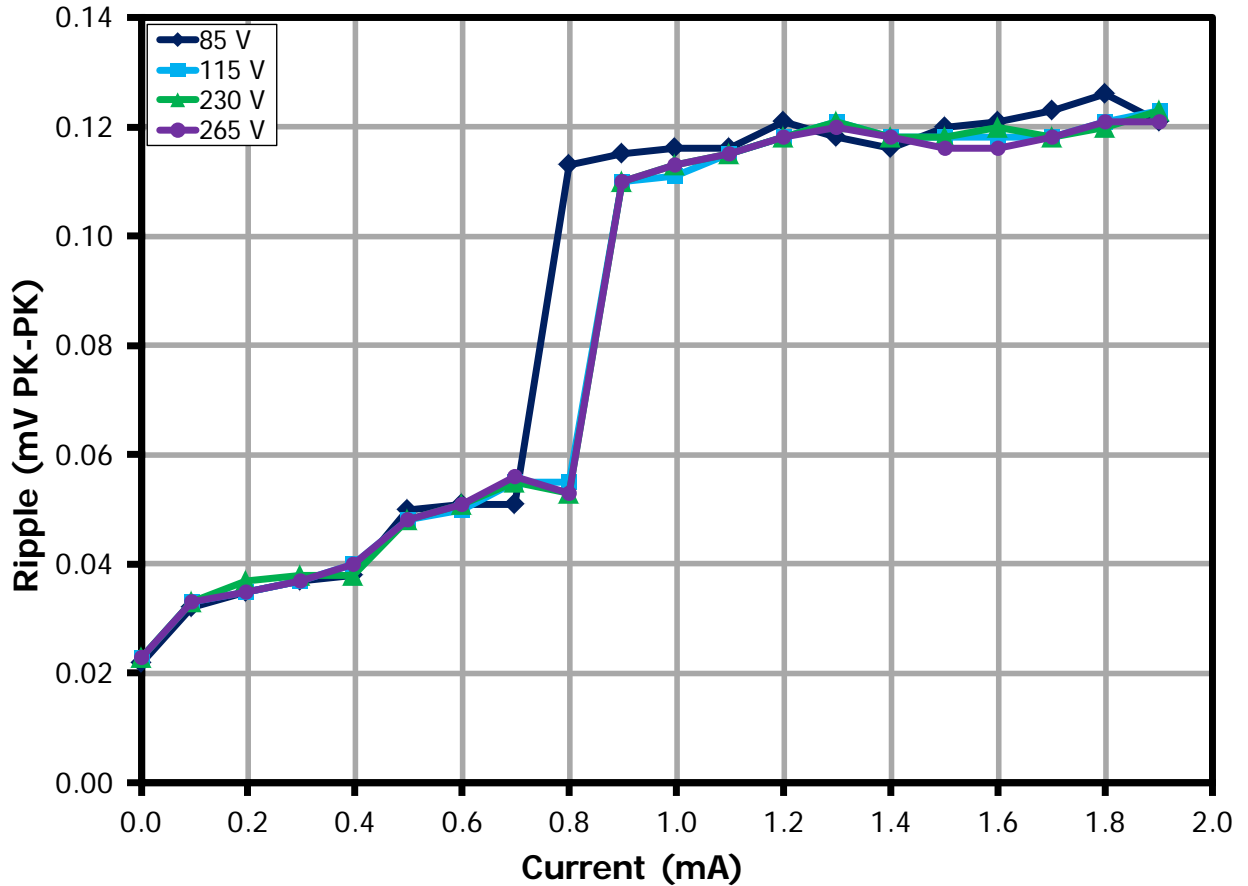


Figure 36 – Output Ripple Voltage.

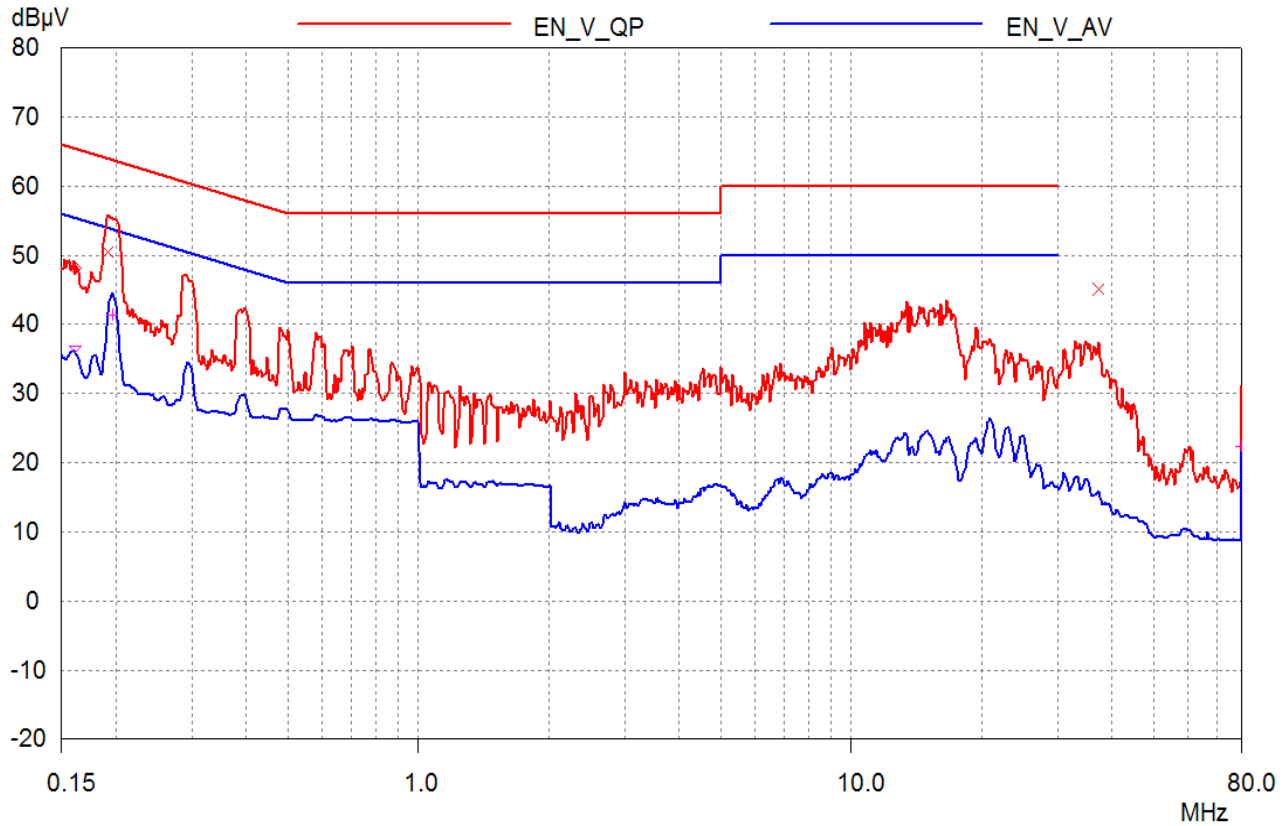
| 85 V RIPPLE (V _{PK-PK}) | 115 V RIPPLE (V _{PK-PK}) | 230 V RIPPLE (V _{PK-PK}) | 265 V RIPPLE (V _{PK-PK}) |
|--------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|
| 0.126 | 0.123 | 0.123 | 0.121 |



12 Conductive EMI

12.1 2 A Resistive Load, Floating Output (PK / AV)

After running 5 minutes.



| Freq (MHz) | QP | Limit | Margin |
|------------|-------|-------|--------|
| 0.19 | 50.48 | 63.95 | 13.47 |

Figure 37 – Floating Ground EMI at 115 VAC.

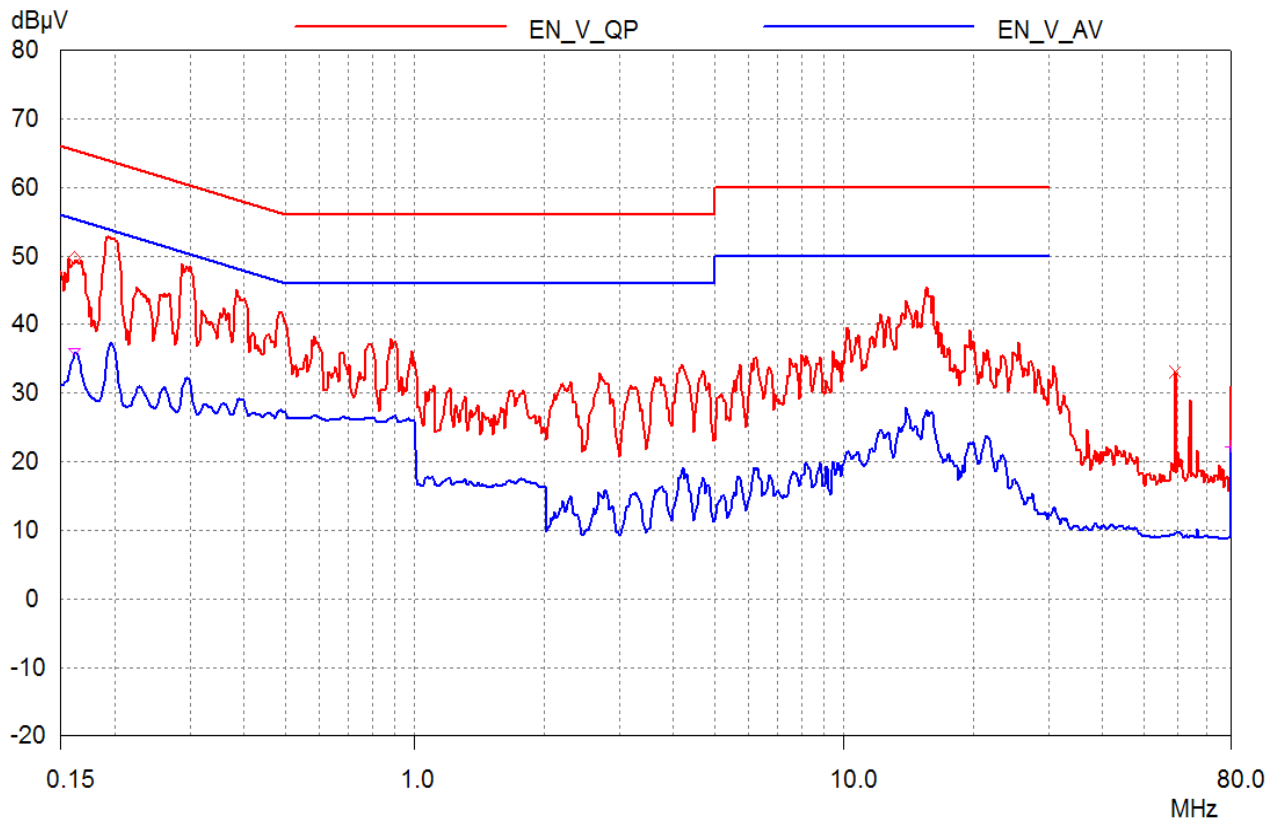
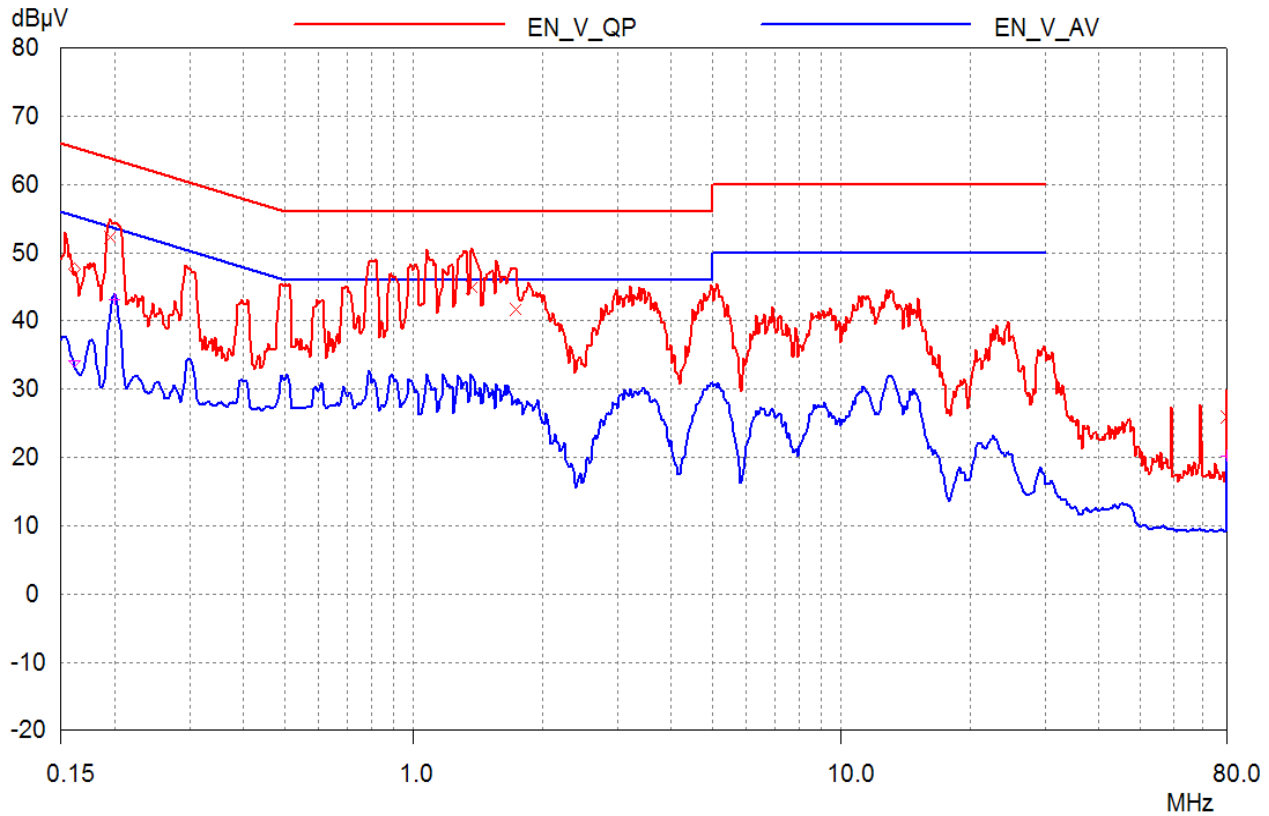


Figure 38 – Floating Ground at 230 VAC.



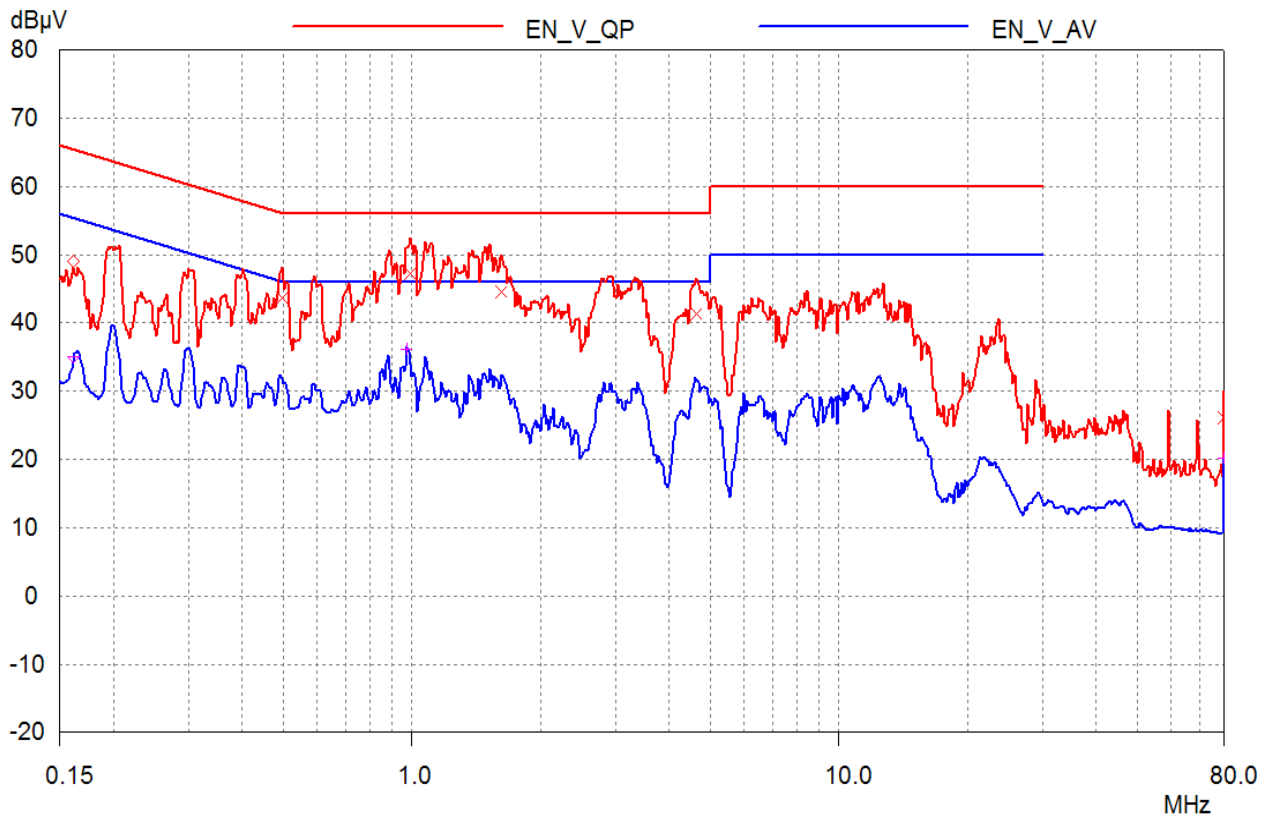
12.2 2 A Resistive Load, Artificial Hand Ground (PK / AV)



| FREQ (MHZ) | QP | LIMIT | MARGIN |
|------------|-------|-------|--------|
| 0.20 | 52.26 | 63.82 | 11.56 |
| 1.37 | 44.97 | 56 | 11.03 |
| 1.73 | 41.65 | 56 | 14.35 |

Figure 39 – Artificial Ground at 115 VAC.





| FREQ (MHZ) | QP | LIMIT | MARGIN |
|------------|-------|-------|--------|
| 0.50 | 43.6 | 56.07 | 12.47 |
| 0.99 | 47.3 | 56 | 8.7 |
| 1.62 | 44.51 | 56 | 11.49 |
| 4.65 | 41.37 | 56 | 14.63 |

Figure 40 – Artificial Ground at 230 VAC.



12.3 Smartphone with Monitor Set-up (HDMI) (QP / AV)

Phone is connected to charger and LCD monitor. The monitor connection increases capacitance to earth ground.

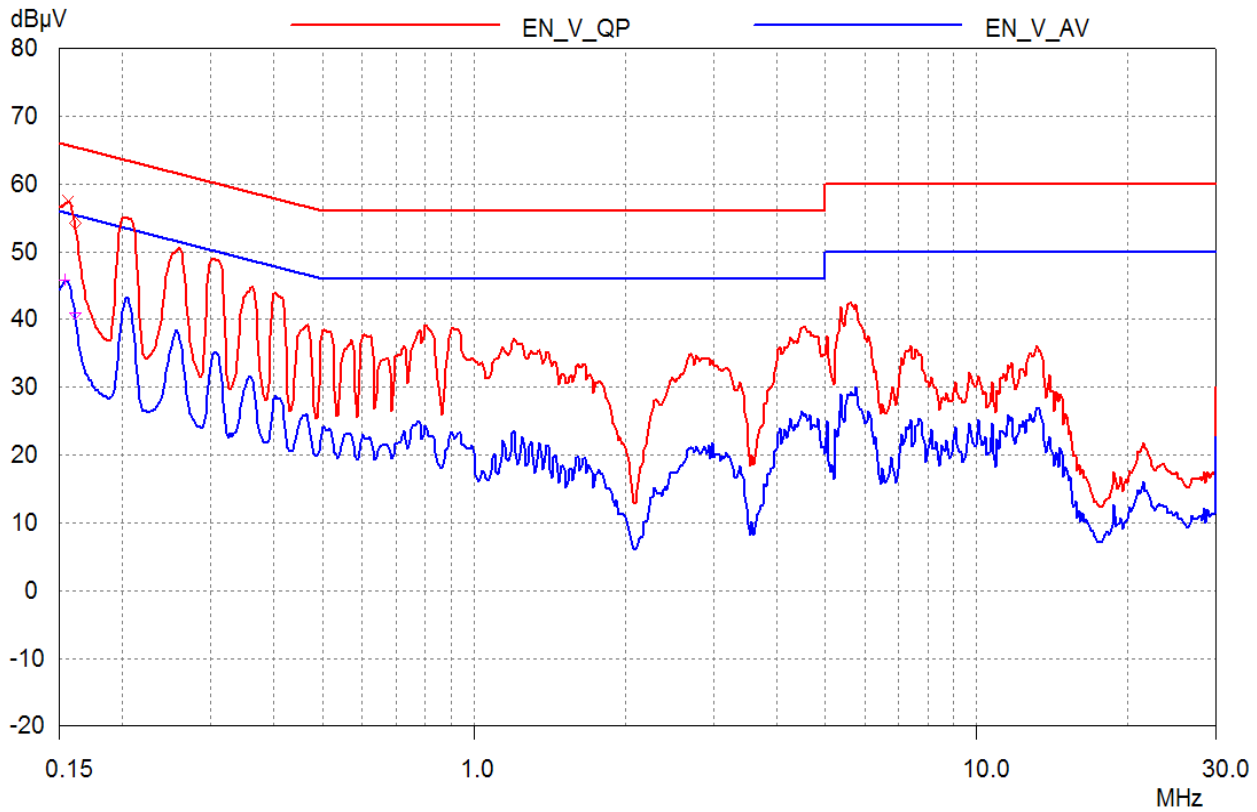


Figure 41 – HDMI at 115 VAC.



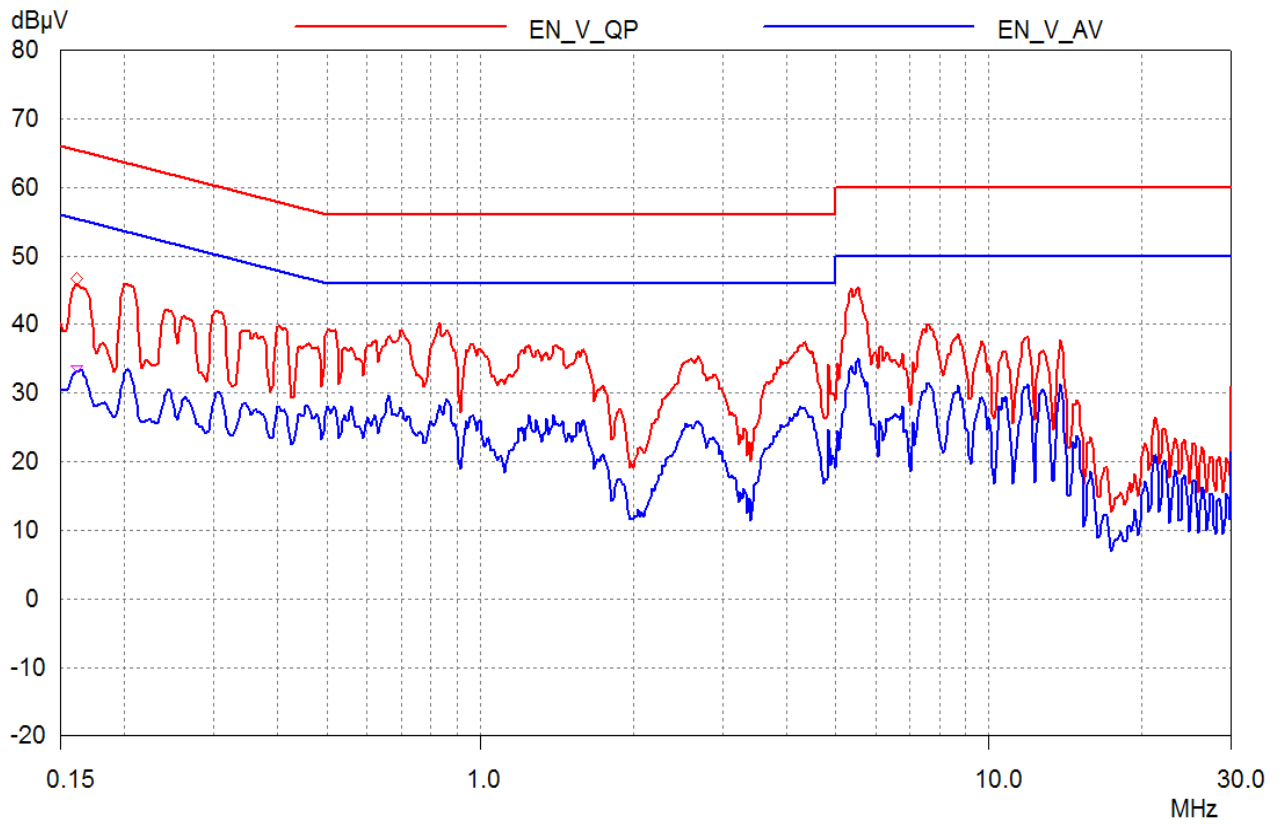


Figure 42 – HDMI at 230 VAC.



13 Radiative EMI

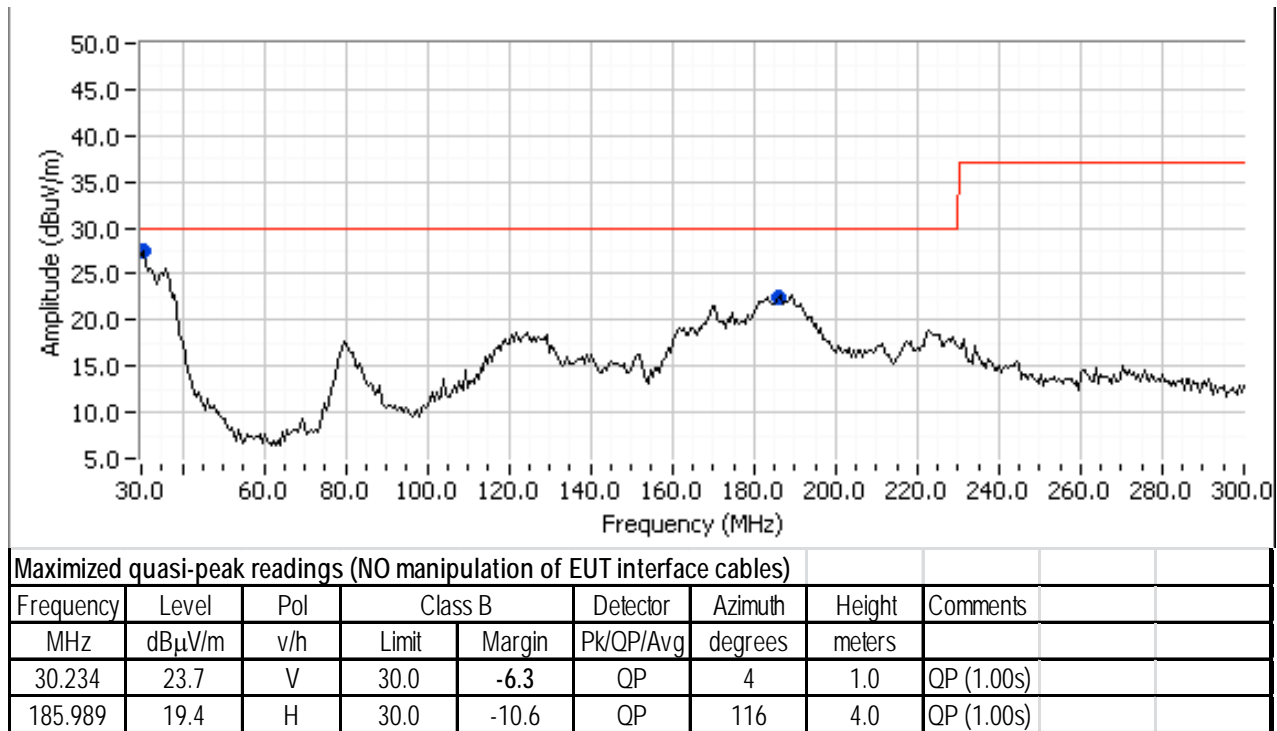


Figure 43 – Radiation at 110 VAC.



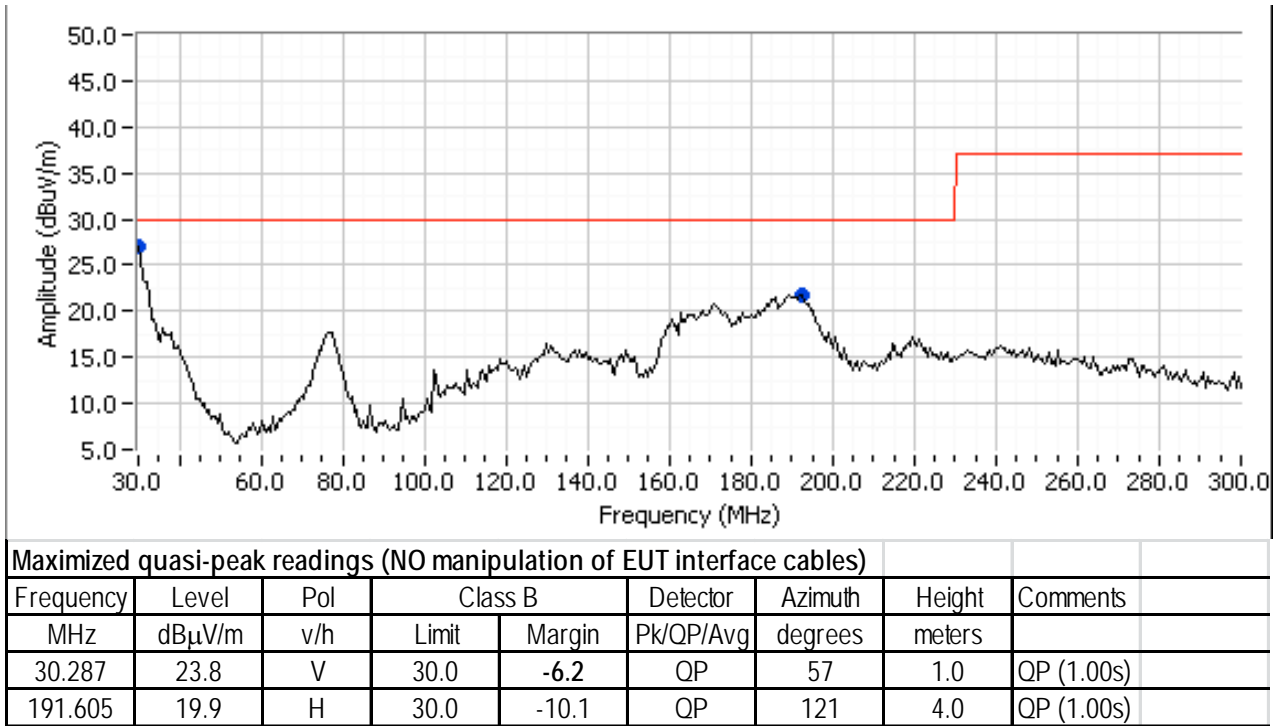


Figure 44 – Radiation at 230 VAC.



14 Audible Noise

Test performed inside case with microphone placed 3 mm from case surface on long side of case, transformer facing towards microphone.

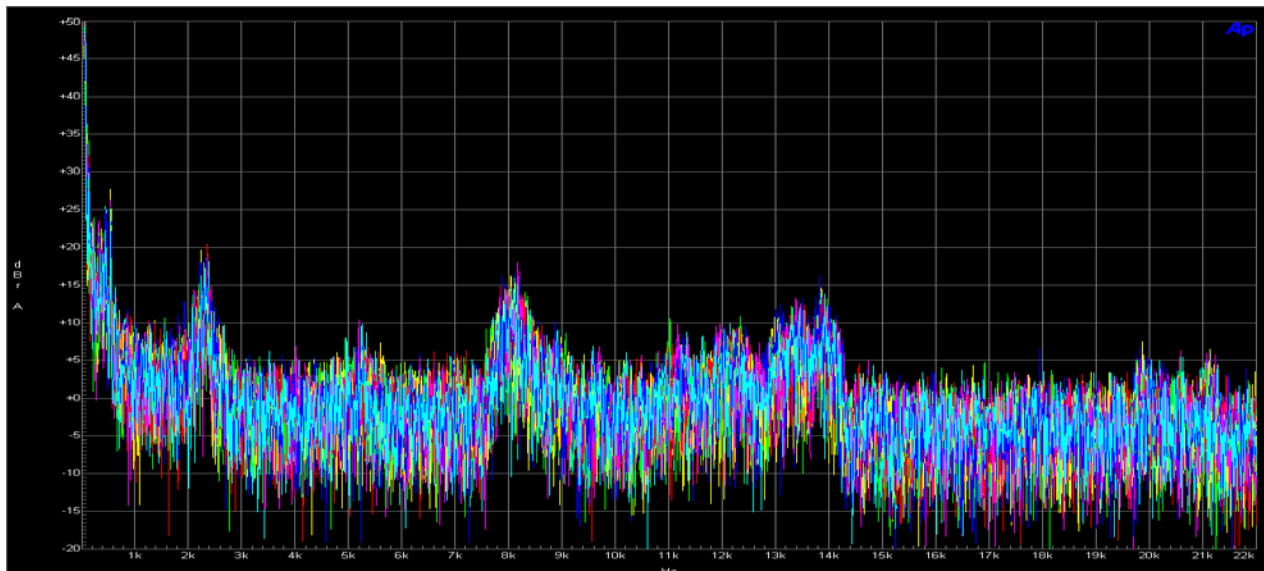


Figure 45 – Audible Noise Spectrum: No-load, V_{IN} Swept from 85 VAC to 264 VAC.

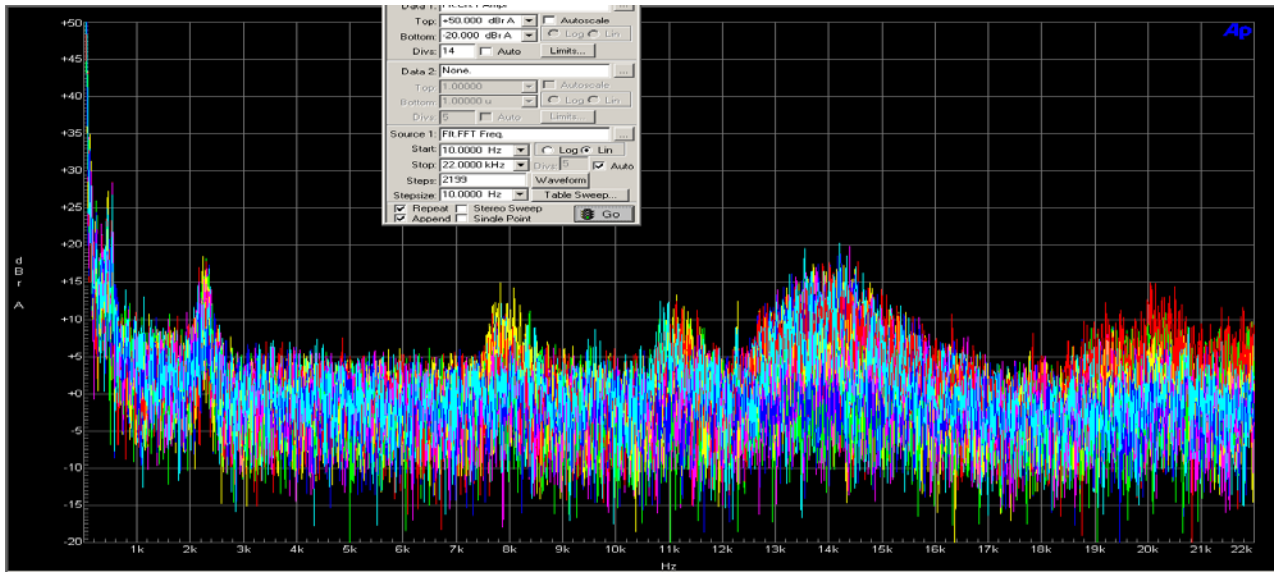


Figure 46 – Audible Noise Spectrum: 85 VAC, I_{OUT} Swept from 0 A to 2.0 A.

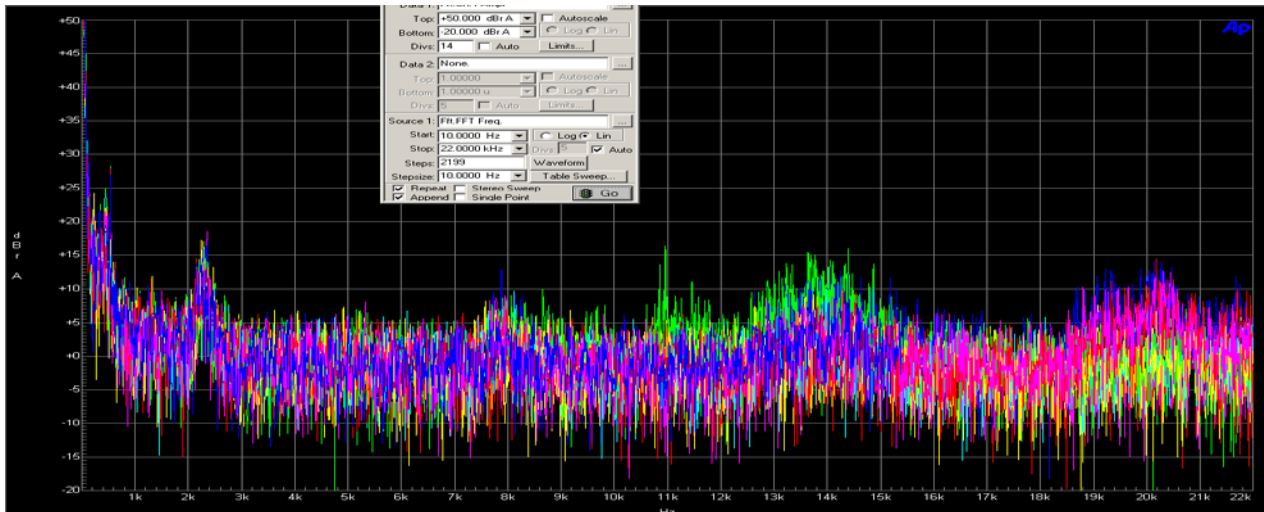


Figure 47 – Audible Noise Spectrum: 110 VAC, I_{OUT} Swept from 0 A to 2.0 A.

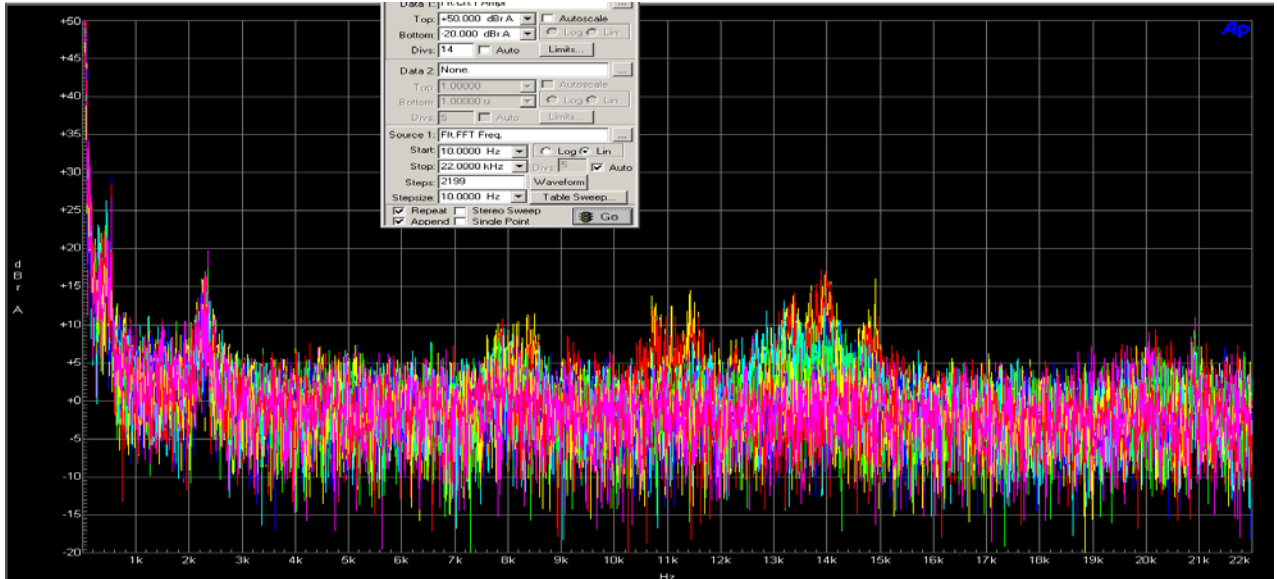


Figure 48 – Audible Noise Spectrum: 220 VAC, I_{OUT} Swept from 0 A to 2.0A.



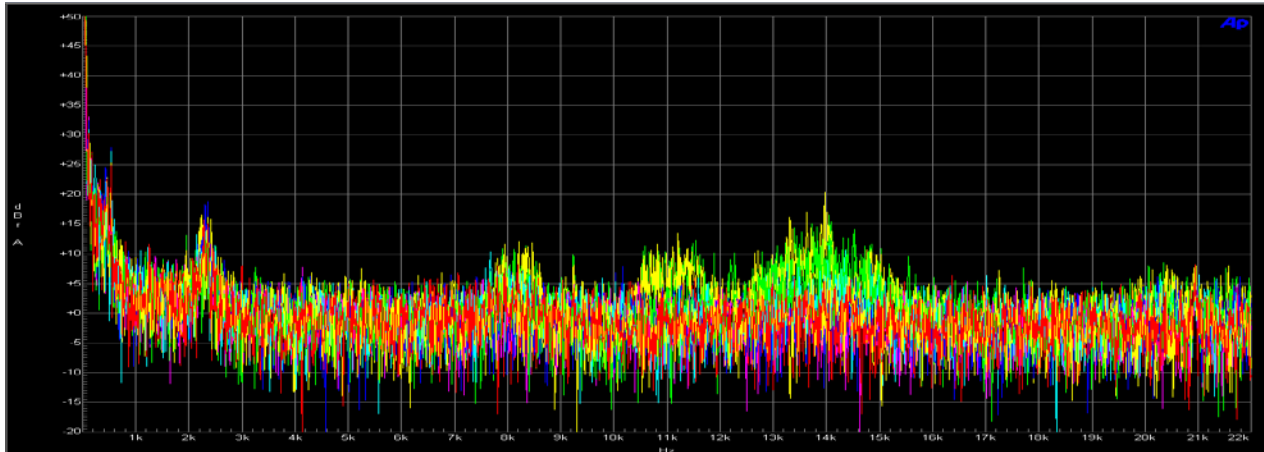


Figure 49 – Audible Noise Spectrum: 265 VAC, I_{OUT} Swept from 0 A to 2.0 A.

15 Lighting Surge & ESD Test

15.1 *Differential Mode Test*

Passed ± 1 kV, 500 A surge test

15.2 *Common Mode Test*

Passed ± 6 KV, 500 A ring wave test.

Need to install plastic barrier for > 5 kV ring wave common mode surge test.

15.3 *ESD Test*

Passed ± 16.5 kV air, 8 kV contact.

Need to install plastic barrier to pass ESD test.

16 Revision History

| Date | Author | Revision | Description & Changes | Reviewed |
|-----------|--------|----------|--|-------------|
| 11-Nov-14 | DK | 1.0 | Initial Release | Mktg & Apps |
| 20-Apr-15 | KM | 1.1 | Updated Transformer Resonant Frequency Spec, CV/CC Graph and Output Ripple Table | |
| | | | | |



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