Title	***Reference Design report for a 30 W Supply For Wall Outlet Using InnoSwitch3™-CP INN3268C-H202***
Specification	180 VAC – 265 VAC Input; 5.1 V, 6 A / 9.2 V, 3.3 A / 15.3 V, 2 A Output
Application	AC Outlet with USB Ports
Author	Applications Engineering Department
Document Number	RDR-659
Date	July 16, 2020
Revision	1.2

Summary and Features

- 30W compact power supply for high power USB type A/C port charging.
- >89% average efficiency at nominal AC input
- <30 mW no-load input power
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing
- Synchronous rectification for higher efficiency
- Accurate thermal protection with hysteretic shutdown
- Input voltage monitor with accurate brown-in/brown-out and overvoltage protection
- Meets IEC 2.0 kV common mode surge, 1.0 kV differential surge and EN55022 conducted EMI

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes an output power supply intended for a USB wall outlet charger. The 30 W output (selectable 5.1 V / 6 A or 9.2 V / 3.3 A or 15.3 V / 2 A) rail is designed for a high power USB charging with Type-A or Type-C ports. The output utilizes INN3268C from the InnoSwitch3-CP family of ICs. This design shows high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-CP controller providing exceptional performance.

DER-659 is a high-line input flyback converter design. The key design goals were high power density, high efficiency, low no load consumption, and best in class thermal performance. This is intended for wall outlet USB chargers.

This document contains the power supply specification, schematic diagram, bill of materials, printed circuit layout, and performance data.

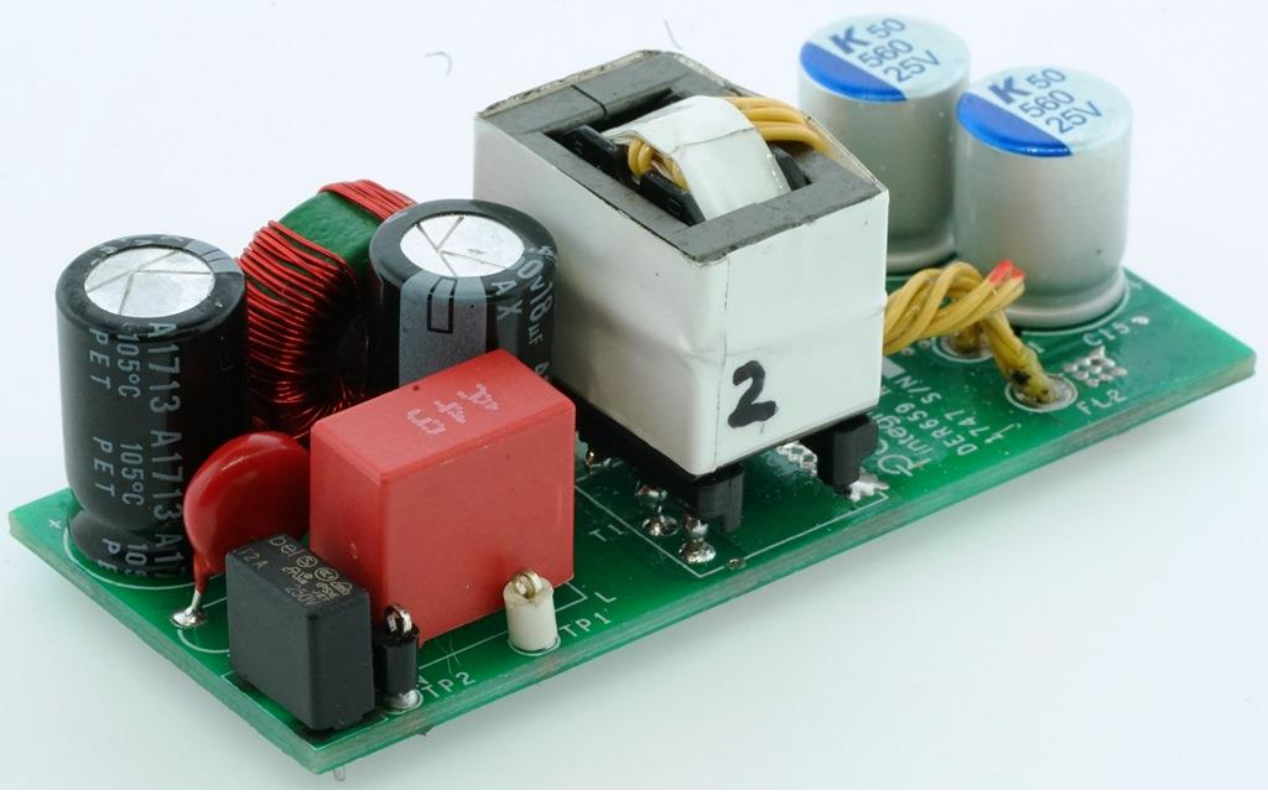

Figure 1 – Populated Circuit Board.

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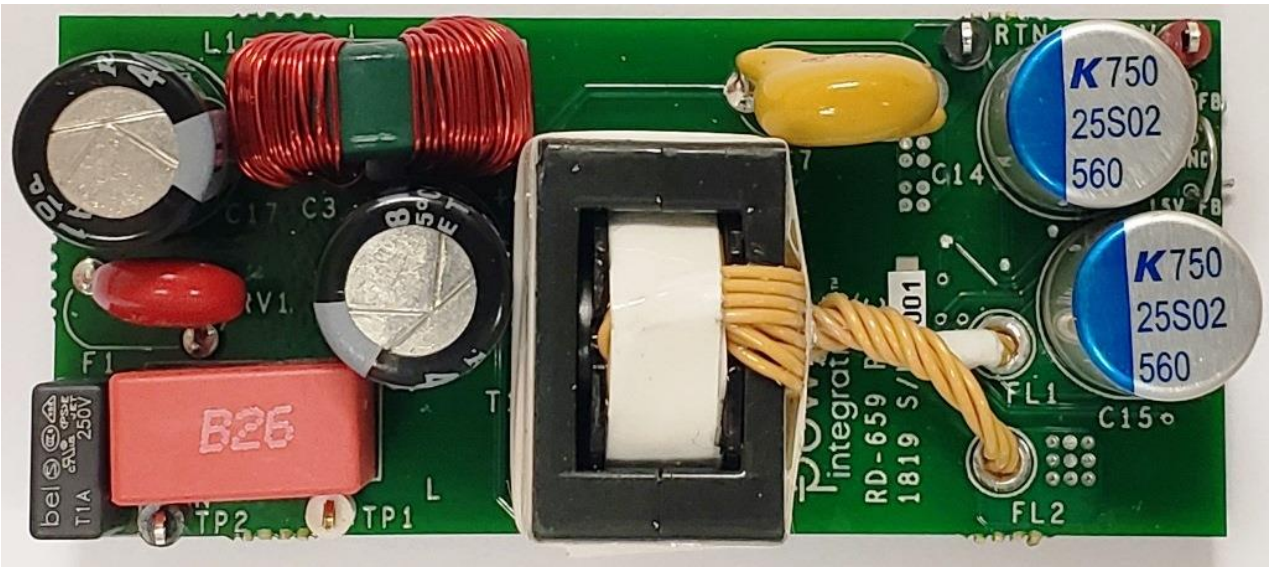

Figure 2 – Populated Circuit Board, Top View.

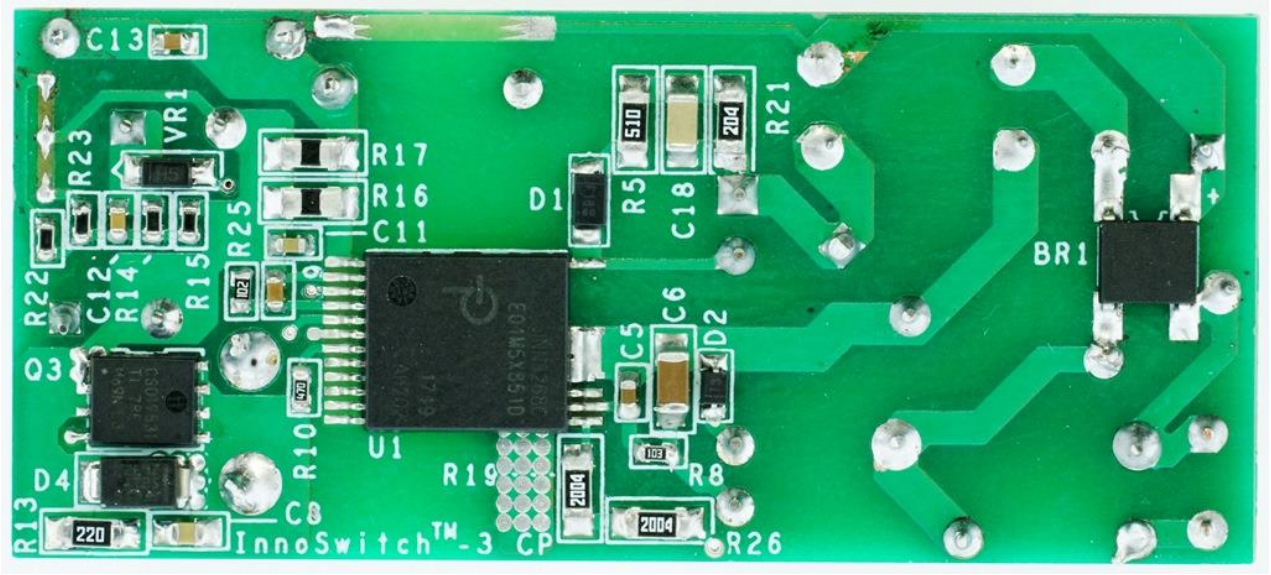

Figure 3 – Populated Circuit Board, Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	180	230	265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	60	63	Hz	
No-load Input Power (230 VAC)				30	mW	Measured at 230 VAC.
5 V Output						
Output Voltage	V_{OUT1}		5.1		V	±3%
Output Ripple Voltage	$V_{RIPPLE1}$			150	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT1}	6		6.3	A	20 MHz Bandwidth.
9 V Output						
Output Voltage	V_{OUT1}		9.2		V	±5%
Output Ripple Voltage	$V_{RIPPLE1}$			150	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT1}			3.3	A	20 MHz Bandwidth.
15 V Output						
Output Voltage	V_{OUT1}		15.3		V	±5%
Output Ripple Voltage	$V_{RIPPLE1}$			150	mV	At End of Cable. Cable Needs a Resistance of 100 mΩ.
Output Current	I_{OUT1}			2	A	20 MHz Bandwidth.
Continuous Output Power	P_{OUT}			30	W	
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC60950 / UL1950 Class II				
Ambient Temperature	T_{AMB}	0		50	ºC	Free Convection, Sea Level.

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3 Schematic

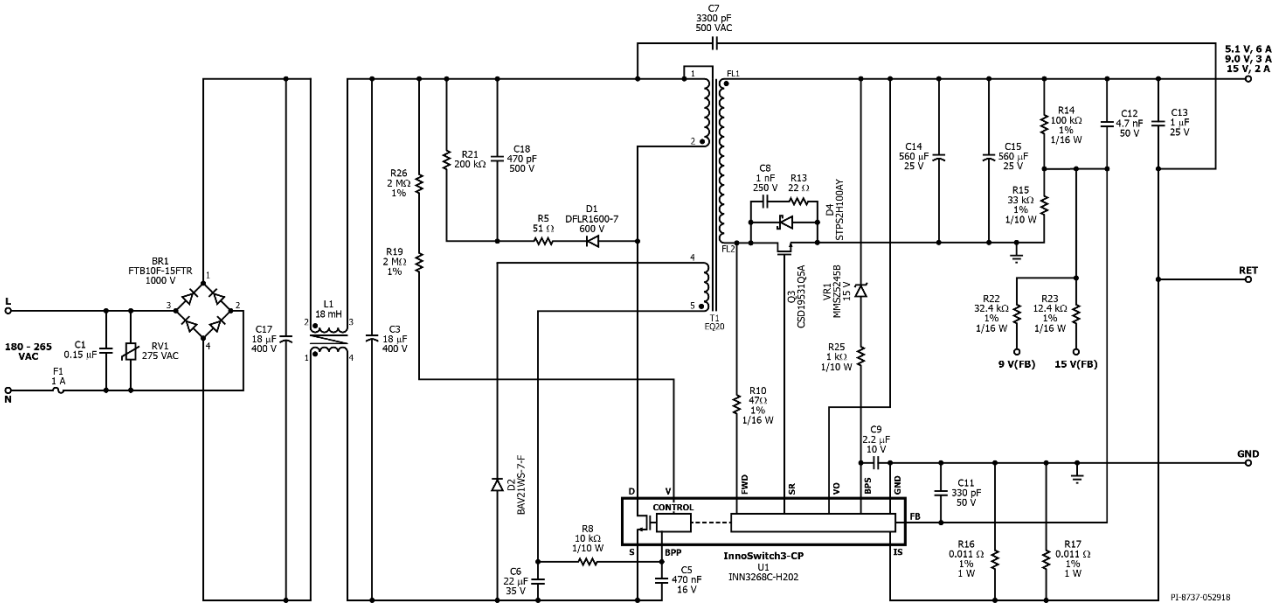

Figure 4 – Schematic.

4 Circuit Description

The InnoSwitch3-CP IC combines primary, secondary and feedback circuits in a single surface mounted off-line flyback switcher IC. The IC incorporates the primary MOSFET, the primary-side controller, the secondary-side controller for synchronous rectification and the Fluxlink™ technology that eliminates the need for an optocoupler needed on a secondary sensed feedback system.

4.1 *Input Circuit Description*

Fuse F1 isolates the circuit and provides protection from component failure, and the capacitor C1 provides attenuation for EMI. Common mode inductor L1 and capacitors C3 and C17 form a π-filter that provides filtering for both common mode and differential mode noise. Bridge rectifiers BR1 rectifies the AC line voltage and provides a full wave rectified DC across the input capacitors C3 and C17.

4.2 *Primary-Side Circuit*

One end of the transformer T1 primary is connected to the rectified DC bus; the other is connected to the drain terminal of the MOSFET inside the INN3268C (U1).

A low cost RCD clamp formed by diode D1, resistors R5 and R21, and capacitor C18 limits the peak Drain voltage of U1 at the instant turn-off of the MOSFET. The clamp helps dissipate the energy stored in the leakage reactance of transformer T1.

The IC is kick-started by an internal high-voltage current source that charges the BPP pin capacitor C5 when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer. The output of this is configured as a flyback winding which is rectified and filtered using diode D2 and capacitor C6. Resistor R8 limits the current being supplied to the BPP pin of the InnoSwitch3-CP (U1). An R-C network can be placed across D2 to offer damping of the high frequency ringing, which can reduce radiated EMI.

The primary-side controller has a current limit threshold ramp that is inversely proportional to time from the end of the last primary switching cycle. The nature of this characteristic introduces a primary current limit that reduces as the switching frequency reduces. It is similar to the state machine of ON/OFF control but the reduction is now linear in nature rather than the discrete jumps in current limit that the ON/OFF state machine introduces. This produces a primary MOSFET switching pulse train that looks similar to a traditional PWM waveform under steady state conditions with consistent time and peak current between cycles rather than the ON/OFF cycle skipping.

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information where the start of the next switching cycle is immediate when a feedback switching cycle request is received.

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Resistors R19 and R26 provide line voltage sensing and supply a current to the V pin of U1, which is proportional to the DC voltage across capacitor C3. At approximately 55 V DC, the current through these resistors exceed the line undervoltage threshold, which results in enabling of U1. At approximately 460 V DC, the current through this resistor exceeds the line overvoltage threshold, which results in disabling of U1.

4.3 *Secondary-Side Circuit*

The secondary-side of the INN3268C IC provides output voltage, output current sensing and drive a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by MOSFET Q3 and filtered by capacitors C14 and C15. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via RC snubber, R13 and C8.

The gate of Q3 is turned on by the secondary-side controller inside IC U1, based on the winding voltage sensed via resistor R10 and fed into the FWD pin of the IC.

In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary-side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below ground. Secondary-side control of the primary-side MOSFET ensures that it is never on at the same time with the synchronous rectification MOSFET on time. The MOSFET drive signal is the output on the SR pin.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device then fed into VO pin and charges the decoupling capacitor C9 via an internal regulator.

During CC operation, when the output voltage falls, the device will power itself from the secondary winding directly. During the on-time of the primary-side power MOSFET, the forward voltage that appears across the secondary winding is used to charge the decoupling capacitor C9 via resistor R10 and an internal regulator. This allows output current regulation to be maintained down to ~3.0 V. Below this level the unit enters auto-restart until the output load is reduced.

Output current is sensed by monitoring the voltage drop across resistors R16 and R17 between the IS and GND pins with a threshold of approximately 30 mV to reduce losses. Once the internal current sense threshold is exceeded the device adjusts the number of switch pulses to maintain a fixed output current. If no fixed current requirement, the IS and GND pins can be shorted.

Below the CC threshold, the device operates in constant voltage mode. Output voltage is regulated so as to achieve an internal reference voltage of 1.265 V on the FB pin. Capacitor C12 form a phase-lead network that ensures stable operation and minimizes

output voltage overshoot and undershoot during transient load conditions. Capacitor C11 provides noise filtering of the signal at the FB pin.

Resistors R14 and R15 form the feedback divider network to sense the output voltage. To change the output to 9 V, resistor R22 is added in parallel to the bottom resistor R15. And to change the output to 15 V, resistor R23 is added in parallel to the bottom resistor R15.To vary the output voltage using a USB PD interface, the ports must be connected to the terminals 9V_FB and GND to make it a 9V output and to the terminals 15V_FB and GND to make it a 15 V output.

VR1 protects the power supply from output overvoltage. If the output voltage exceeds VR1 + BPS voltage, current will flow through the BPS pin that will result to auto-restart. A 15 V Zener regulator was used to not exceed the voltage rating of the output capacitors.

In order to improve conversion efficiency and reduce switching losses, InnoSwitch3-CP introduces a secondary-based QR functionality. The secondary controller has a means to allow switching when the voltage across the primary switch is near its minimum voltage when the converter operates in critical (CRM) or discontinuous conduction mode (DCM). Rather than detecting the magnetizing ring valley on the primary-side, the peak voltage of the FW pin voltage as it rises above the output voltage level is used to gate secondary request to initiate the switch "on" cycle in the primary controller.

4.4 *Design Key Points*

The design targets greater than 89% average efficiency for the 3 outputs. Efficiency was optimized with transformer design, chosen active devices and bias voltages. For the transformer design, it is best to keep the reflected voltage (VOR) low to decrease the RMS current on the secondary side. Lower VOR also means lower drain to source voltage on the primary side MOSFET that can reduce switching loss. In this design, the VOR was set to 50 V for the 5 V output. This will ensure the 5 V, 9 V and 15 V output operations in discontinuous mode (DCM) with valley switching.

Aside from the VOR consideration it is also important to lower the leakage inductance of the transformer. The energy being stored in the leakage inductance which is dissipated on the clamping circuit contributes to lower efficiency. Reducing the leakage is an utmost important in this design, to significantly increase the efficiency. A sandwich winding was used to lower the leakage inductance to a value less than 5 μH (< 2% of magnetizing inductance). Detailed transformer construction is described on section 7 of this report.

For higher efficiency, it is also necessary to choose the active devices that offer lower conduction losses. For the InnoSwitch3-CP family, INN3268C offers the lowest $R_{DS(On)}$. For the secondary rectifier (SR), a MOSFET was chosen instead of a Schottky diode. A MOSFET of 4.9 mΩ $R_{DS(ON)}$ was used in the design. An added Schottky diode in parallel with the SR MOSFET gives a slight improvement on the efficiency. This diode conducts

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instead of the MOSFET body diode during the start of secondary MOSFET ON and before the secondary current reaches zero or secondary MOSFET OFF. These delays on transition are needed to avoid cross-conduction with the primary MOSFET.

The sweet spot (efficiency and small form factor consideration) for switching frequency operation is at the range from 70 kHz to 80 kHz. An EQ20 transformer with AE of 60 mm^2 is enough without saturating the core. The design chooses the minimum number of secondary turns at 390 mT flux density.

Auxiliary bias voltage was chosen at range from 8 V to 10 V at no-load condition. This helps improves no load consumption as well as light load efficiency.

5 PCB Layout

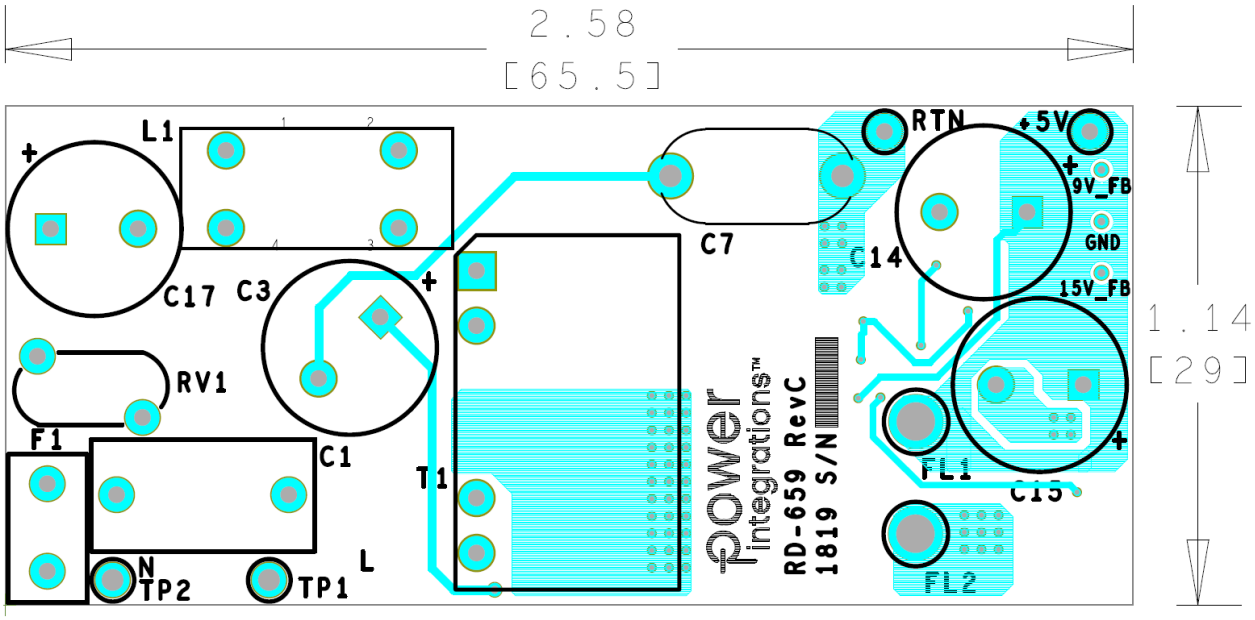

Figure 5 – Top Side.

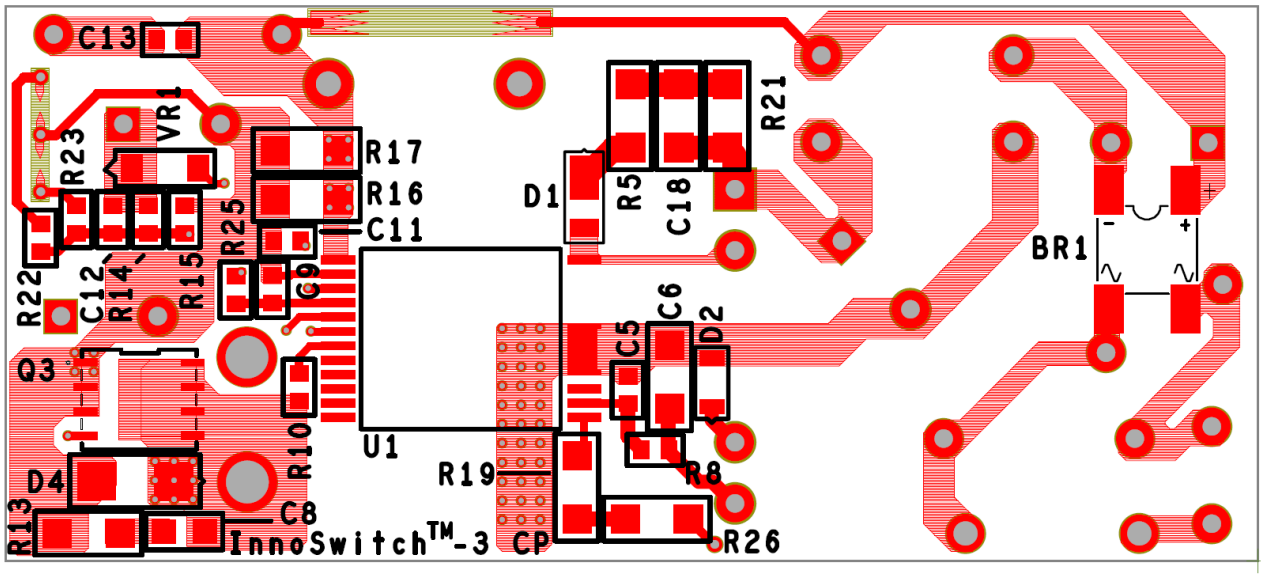

Figure 6 – Bottom Side.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	BRIDGE RECT, 1PH, 1 kV, 1.5 A, 4-SMD	FTB10F-15FTR	SMC
2	1	C1	150 nF, 275 VAC, Film, X2	890324023025CS	Wurth
3	1	C3	18 µF, 20%, 400 V, Electrolytic, Gen. Purpose, (10 x 16 mm), 2000 Hrs @ 105°C	400AX18MEFC10X16	Rubycon
4	1	C5	470 nF, 50 V, Ceramic, X7R, 0603	UMK107B7474KA-TR	Taiyo Yuden
5	1	C6	22 µF, 35 V, Ceramic, X5R, 1206	C3216X5R1V226M160AC	TDK
6	1	C7	CAP CER 3300 pF 500 VAC Y5V RADIAL	VY1332M43Y5VQ63V0	Vishay
7	1	C8	1 nF, 250 V, Ceramic, X7R, 0805	GRM21AR72E102KW01D	Murata
8	1	C9	2.2 µF, 10 V, Ceramic, X7R, 0603	GRM188R71A225KE15D	Murata
9	1	C11	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
10	1	C12	4.7 nF 50 V, Ceramic, X7R, 0603	GRM188R71H472KA01D	Murata
11	1	C13	1 µf 25 V, Ceramic, X7R, 0603	CGA3E1X7R1E105K080AE	TDK
12	1	C14	560 µF, 25 V,±20%, Al Organic Polymer, Gen. Purpose, Can, 15 mΩ, 2000 Hrs @ 105°C	A750MS567M1EAAE015	KEMET
13	1	C15	560 µF, 25 V,±20%, Al Organic Polymer, Gen. Purpose, Can, 15 mΩ, 2000 Hrs @ 105°C	A750MS567M1EAAE015	KEMET
14	1	C17	18 µF, 20%, 400 V, Electrolytic, Gen. Purpose, (10 x 16 mm), 2000 Hrs @ 105°C	400AX18MEFC10X16	Rubycon
15	1	C18	470 pF, ±10%, 500 V, X7R, Ceramic Capacitor, -55°C ~ 125°C, SMT, MLCC 1206 (3216 Metric) 0.126" L x 0.063" W (3.20 mm x 1.60 mm)	CC1206KKX7RBBB471	Yageo
16	1	D1	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
17	1	D2	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
18	1	D4	100 V, 2 A, Schottky, SMA	STPS2H100AY	ST Micro
19	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
20	1	L1	Toroidal Common Mode Choke,18 mH, ±25%, Core Effective Inductance = 5500 nH//N2, leakage inductance = 80 µH ±10%, custom, DER-659, wound on 32-00286-00 core (14.90 mm O.D. 6.5 mm Th 7.0 mm ID) with #28AWG Heavy Nyleze Magnet Wire and 66-00042-00 fish paper	32-00370-00 TSD-4501	Power Integrations Premier Magnetics
21	1	Q3	MOSFET, N-ch, Enhancement mode, 100 V, 110 A, 5.3 mΩ Pwr MOSFET, 150C Tmax, 8-VSON (5x6)	CSD19531Q5A	Texas Instruments
22	1	R5	RES, 51 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ510V	Panasonic
23	1	R8	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
24	1	R10	RES, 47.0 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF47R0V	Panasonic
25	1	R13	RES, 22 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ220V	Panasonic
26	1	R14	RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
27	1	R15	RES, SMD, 33 kΩ, 1%, 1/10 W, ±100ppm/°C, 0603	RC0603FR-0733KL	Yageo
28	1	R16	0.011 Ω, ±1%, ±75ppm/°C, 1 W, 1206 (3216 Metric), Automotive AEC-Q200, Current Sense,-55°C ~ 155°C	ERJ-8CWFR011V	Panasonic
29	1	R17	0.011 Ω, ±1%, ±75ppm/°C, 1 W, 1206 (3216 Metric), Automotive AEC-Q200, Current Sense,-55°C ~ 155°C	ERJ-8CWFR011V	Panasonic
30	1	R19	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
31	1	R21	RES, 200 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ204V	Panasonic
32	1	R22	RES, 32.4 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3242V	Panasonic
33	1	R23	RES, 12.4 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1242V	Panasonic
34	1	R25	RES, 1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
35	1	R26	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
36	1	RV1	275 VAC, 23 J, 7 mm, RADIAL	V275LA4P	Littlefuse
37	1	T1	Bobbin, EQ20, 10 pins, 5pri, 5sec Transformer	P-2042 POL-INN042	Pinshine Premier Magnetics
38	1	U1	InnoSwitch3-CP Integrated Circuit, InSOP24D	INN3268C-H202	Power Integrations
39	1	VR1	15 V, 5%, 500 mW, SOD-123	MMSZ5245B-E3-08	Vishay

Mechanical Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	TP2	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
2	1	TP1	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
3	1	RTN	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
4	1	5V	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone

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7 Transformer (T1) Specification

7.1 *Electrical Diagram*

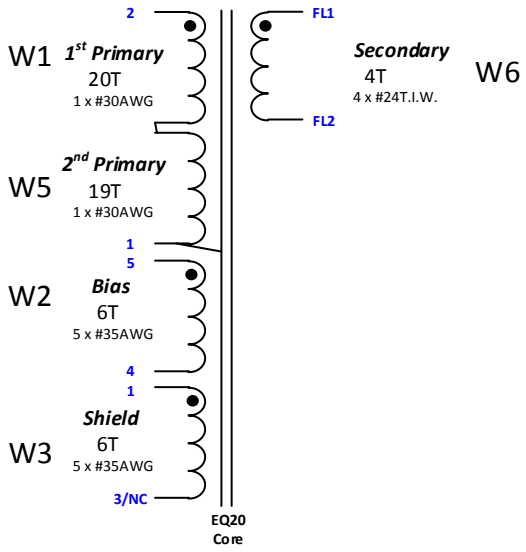

Figure 7 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Electrical Strength	1 second, 60 Hz, from pins 1, 2, 4 and 5 to FL1, FL2.	3000 VAC
Primary Inductance	Pins 1-2, all other open, measured at 100 kHz, 0.4 V_{RMS}.	460 µH ±5%
Primary Leakage	Pins 1-2, with FL1-FL2 shorted, measured at 100 kHz, 0.4 V_{RMS}.	7 µH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: EQ20.
[2]	Bobbin: EQ20, Horizontal, 10 pins.
[3]	Magnet Wire: #30AWG Double Coated, Solderable.
[4]	Magnet Wire: #35AWG Double Coated, Solderable.
[5]	Magnet Wire: #24AWG Triple Insulated Wire.
[6]	Tape: 3M 1298 Polyester Film, 1 mil thick, 6 mm Wide.
[7]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

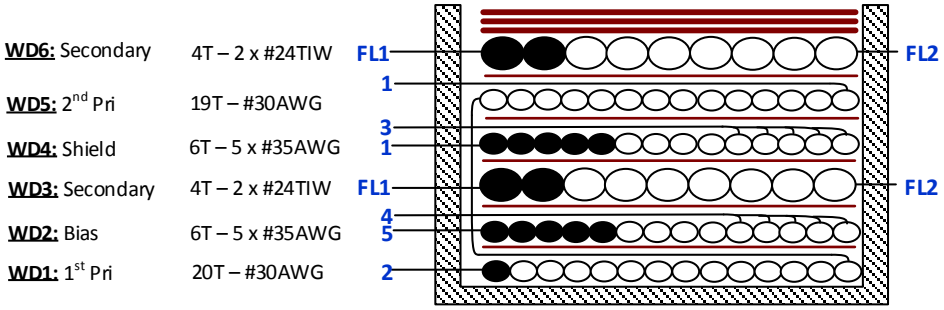

Figure 8 – Transformer Build Diagram.

7.5 *Transformer Construction*

Winding Preparation	Place the bobbin Item [2] on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
WD1 1st Primary	Start at pin 2, wind 20 turns of wire Item [3] in 1 layer. At the last turn, bring wire back to the left side floating.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD2 Bias	Start at pin 5, wind 6 (5-filars) turns of wire Item [4] in 1 layer. At the last turn, bring 5-filars wire back to the left finish at pin 4.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD3 1st Secondary	Start at FL1 from the left side of the bobbin, wind 4 bifilar turns of wire Item [5] in 1 layer. At the last turn, finish winding at FL2.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD4 Shield	Start at pin 1, wind 6 (5-filars) turns of wire Item [4] in 1 layer. At the last turn, bring 5-filars wire back to the left finish at pin 3.
WD5 2nd Primary	Continue primary winding of 19 turns from left to right. At the last turn finish at pin 1.
Insulation	Place 1 layer of tape Item [6] for insulation.
WD5 2nd Secondary	Start at FL1 from the left side of the bobbin, wind 4 bifilar turns of wire Item [5] in 1 layer. At the last turn, finish winding at FL2.
Insulation	Place 3 layers of tape Item [6] for insulation and secure the windings.
Core Shield	Gap core halves to get 490 μH inductance. Secure core and wind bifilar tin wire around the core. Terminate the wire at pin 1.
Finish Assembly	Cover core with 2 layers of tape. Cut pin 3. Varnish Item [7].

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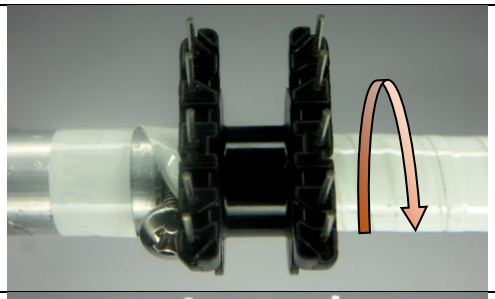
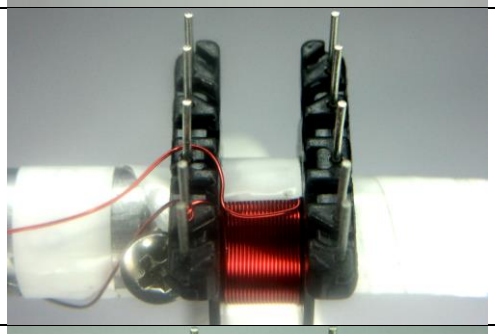
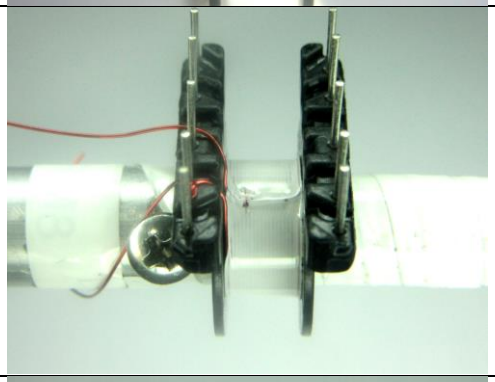
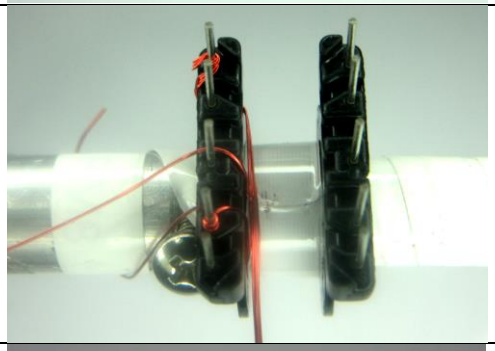
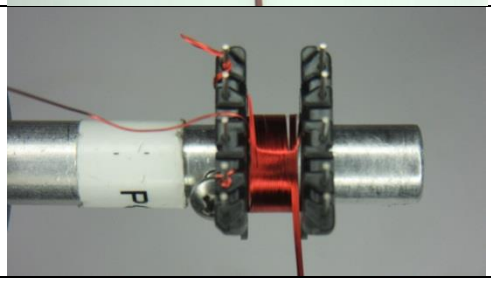
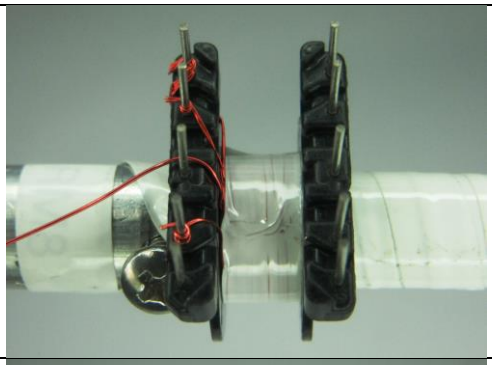
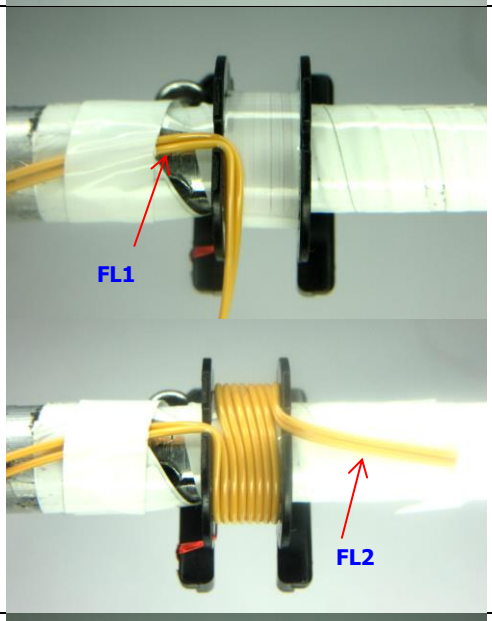
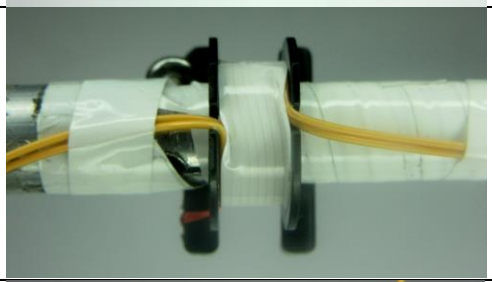
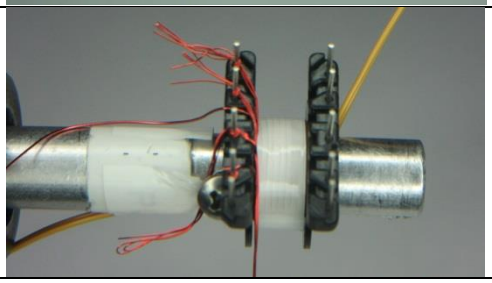
7.6 *Winding Illustrations*

Winding Preparation		Place the bobbin Item [2] on the mandrel with the pin side is on the left side Winding direction is clockwise direction.
WD1 **1st Primary**		Start at pin 2, wind 20 turns of wire Item [3] in 1 layer. At the last turn, bring wire back to the left side floating.
Insulation		Place 1 layer of tape Item [6] for insulation.
WD2 **Bias**		Start at pin 5, wind 6 (5-filars) turns of wire Item [4] in 1 layer. At the last turn, bring 5-filar wire back to the left and finish at pin 4.
		

Insulation		Place 1 layer of tape Item [6] for insulation.
WD3 Secondary		Start at FL1 from the left side of the bobbin, wind 4 bifilar turns of wire Item [5] in 1 layer. At the last turn, finish winding at FL2.
Insulation		Place 1 layer of tape Item [6] for insulation.
WD4 Shield		Start at pin 1, wind 6 (5-filars) turns of wire Item [4] in 1 layer. At the last turn, bring 5-filars wire back to the left finish at pin 3.

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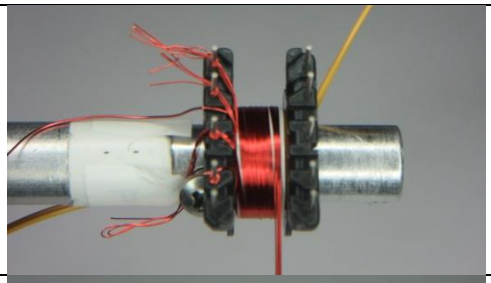
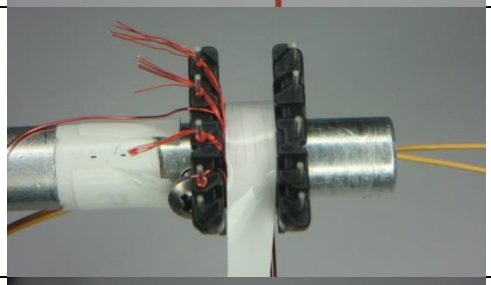
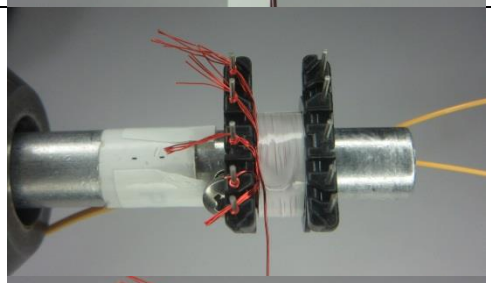
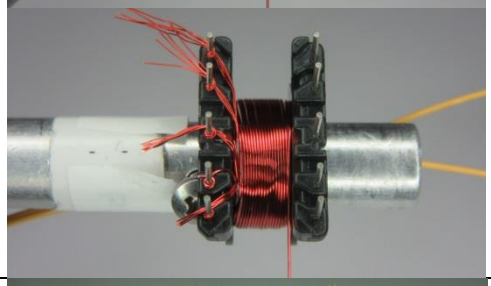
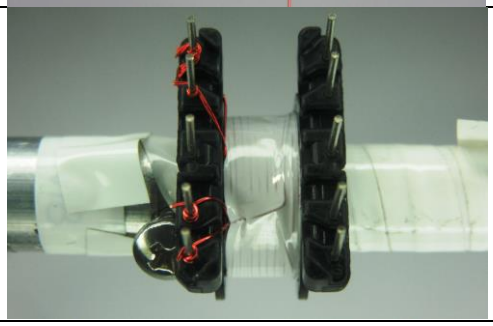
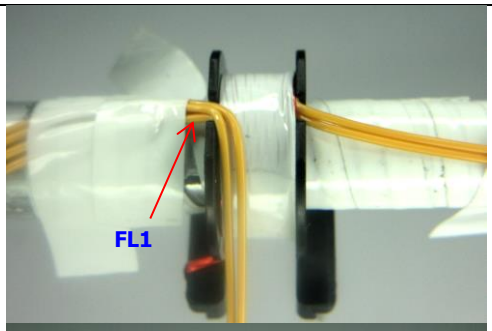
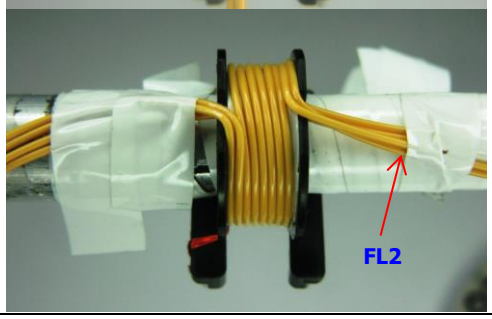
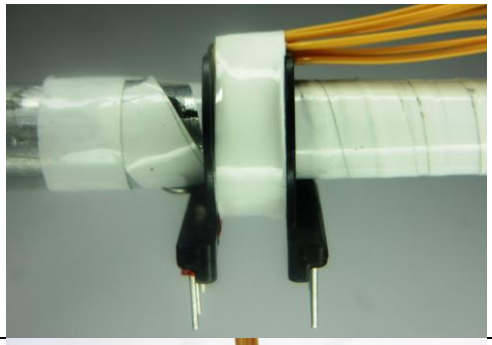
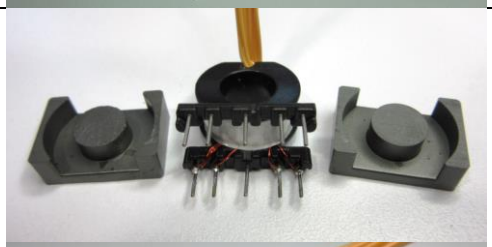
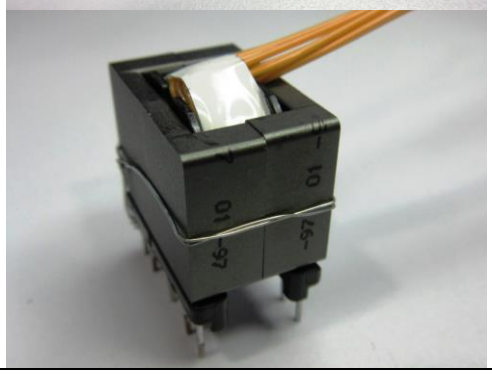
		
Insulation		Place 1 layer of tape Item [6] for insulation.
WD5 **2nd Primary**	 	Continue primary winding of 19 turns from left to right. At the last turn finish at pin 1.
Insulation		Place 1 layer of tape Item [6] for insulation.

WD6 Secondary	 	Start at FL1 from the left side of the bobbin, wind 4 bifilar turns of wire Item [5] in 1 layer. At the last turn, finish winding at FL2.
Insulation		Place 3 layers of tape Item [6] for insulation and bring FL1 to right side then secure the windings.
Core Shield	 	Gap core halves to get 460 µH inductance. Secure core and wind bifilar tin wire around the core. Terminate the wire at pin 1.

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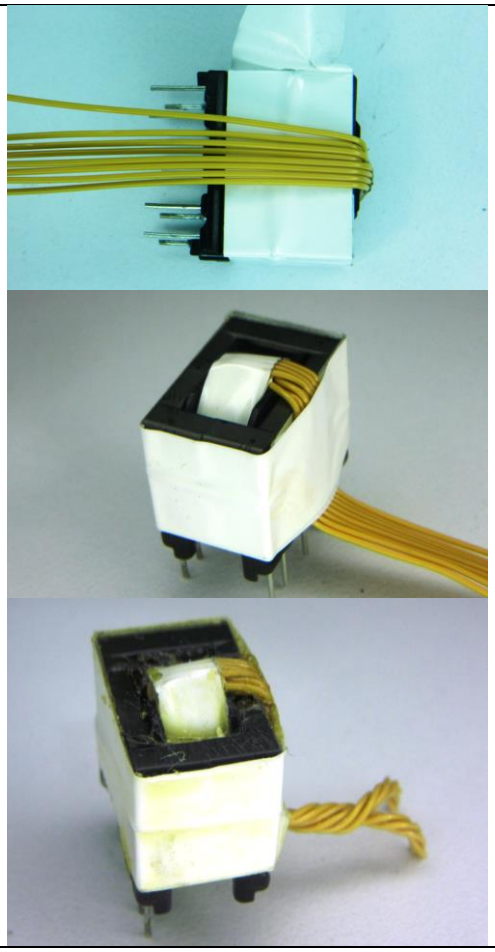
Finish Assembly		Cover core with 2 layers of tape. Cut pin 3. Varnish Item [7].

8 Common Mode Choke (L1) Specification

8.1 *Electrical Diagram*

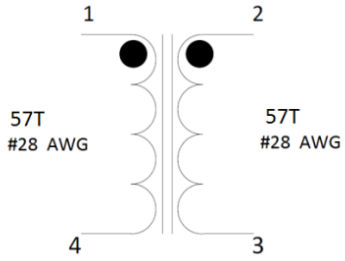


Figure 9 – Inductor Electrical Diagram.

8.2 *Electrical Specifications*

Inductance	Pins 1-4 and pins 2-3 measured at 100 kHz, 0.4 RMS.	~18 mH ±25%
Core Effective Inductance		5500 nH/N^2
Primary Leakage Inductance	Pins 1-4, with 2-3 shorted.	~80 μH

8.3 *Material List*

Item	Description
[1]	Toroid: FERRITE INDUCTOR TOROID T14 x 8 x 5.5, PI P/N: 32-00286-00.
	Divider - Fish Paper, Insulating Cotton Rag, 0.010” thick, PI #: 66-00042-00.
[2]	Magnet Wire: #28 AWG Heavy Nyleze.

8.4 *Winding Instructions*

- Place Fish paper item [2] onto toroid item [1] to divide 2 equal sections
- Use 4 ft of wire item [3], start as pin 1 wind 57 turns and end at pin 4
- Do the same for another section of toroid, start at pin 2 then end at pin 3 symmetrically with last winding

8.5 *Illustrations*

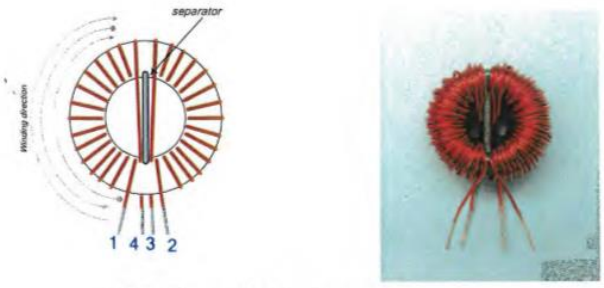


Figure 10 – Side View.

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9 Transformer Design Spreadsheet

ACDC_InnoSwitch3-CP_Flyback_092217; Rev.1.0; Copyright Power Integrations 2017	INPUT	OUTPUT	UNITS	InnoSwitch3-CP Flyback Design Spreadsheet
APPLICATION VARIABLES				
VAC_MIN	180	180	V	Minimum AC line voltage
VAC_MAX	265	265	V	Maximum AC input voltage
VAC_RANGE		HIGH LINE		AC line voltage range
FLINE		60	Hz	AC line voltage frequency
CAP_INPUT	36	36	uF	Input capacitance
SETPOINT 1				
VOUT1	15.00	15.00	V	Output voltage 1, should be the highest output voltage required
IOUT1	2.00	2.00	A	Output current 1
POUT1		30.00	W	Output power 1
EFFICIENCY1	0.90	0.90		Converter efficiency for output 1
Z_FACTOR1	0.50	0.50		Z-factor for output 1
SETPOINT 2				
VOUT2	9.00	9.00	V	Output voltage 2
IOUT2	3.30	3.30	A	Output current 2
POUT2		29.70	W	Output power 2
EFFICIENCY2	0.90	0.90		Converter efficiency for output 2
Z_FACTOR2	0.50	0.50		Z-factor for output 2
SETPOINT 3				
VOUT3	5.00	5.00	V	Output voltage 3
IOUT3	6.00	6.00	A	Output current 3
POUT3		30.00	W	Output power 3
EFFICIENCY3	0.90	0.90		Converter efficiency for output 3
Z_FACTOR3	0.50	0.50		Z-factor for output 3
PERCENT_CDC	0%	0%		Percentage (of output voltage) cable drop compensation desired at full load
CDC_SCALING_SETPOINT	3	3		Select the setpoint number for the voltage used for cable drop compensation (typically the 5V output)
PRIMARY CONTROLLER SELECTION				
ENCLOSURE	ADAPTER	ADAPTER		Power supply enclosure
ILIMIT_MODE	STANDARD	STANDARD		Device current limit mode
VDRAIN_BREAKDOWN	650	650	V	Device breakdown voltage
DEVICE_GENERIC	INN32X8	INN32X8		Device selection
DEVICE_CODE		INN3268C		Device code
PDEVICE_MAX		55	W	Device maximum power capability
RDSON_25DEG		0.99	Ω	Primary MOSFET on-time resistance at 25°C
RDSON_100DEG		1.54	Ω	Primary MOSFET on-time resistance at 100°C
ILIMIT_MIN		1.534	A	Primary MOSFET minimum current limit
ILIMIT_TYP		1.650	A	Primary MOSFET typical current limit
ILIMIT_MAX		1.766	A	Primary MOSFET maximum current limit
VDRAIN_ON_MOSFET		0.21	V	Primary MOSFET on-time voltage drop
VDRAIN_OFF_MOSFET		588.31	V	The peak drain voltage on the MOSFET is higher than 90% of the device BVDSS: Decrease the device VOR
WORST CASE ELECTRICAL PARAMETERS				
FSWITCHING_MAX	68000	68000	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
VOR	145.0	145.0	V	Voltage reflected to the primary winding (corresponding to setpoint 1) when the primary MOSFET turns off
VMIN		228.44	V	Valley of the minimum input AC voltage
KP		0.916		Measure of continuous/discontinuous mode of operation
MODE_OPERATION		CCM		Mode of operation
DUTYCYCLE		0.192		Primary MOSFET duty cycle

TIME_ON		3.39	us	Primary MOSFET on-time
TIME_OFF		11.97	us	Primary MOSFET off-time
LPRIMARY_MIN		435.9	uH	Minimum primary magnetizing inductance
LPRIMARY_TYP		458.9	uH	Typical primary magnetizing inductance
LPRIMARY_TOL		5.0		Primary magnetizing inductance tolerance
LPRIMARY_MAX		481.8	uH	Maximum primary magnetizing inductance
PRIMARY CURRENT				
IAVG_PRIMARY		0.139	A	Primary MOSFET average current
IPEAK_PRIMARY		1.627	A	Primary MOSFET peak current
IPEDESTAL_PRIMARY		0.122	A	Primary MOSFET current pedestal
IRIPPLE_PRIMARY		1.627	A	Primary MOSFET ripple current
IRMS_PRIMARY		0.388	A	Primary MOSFET RMS current
SECONDARY CURRENT				
IPEAK_SECONDARY		15.868	A	Secondary MOSFET peak current
IPEDESTAL_SECONDARY		1.190	A	Secondary MOSFET pedestal current
IRMS_SECONDARY		8.167	A	Secondary MOSFET RMS current
IRIPPLE_CAP_OUT		5.540	A	Output capacitor ripple current
TRANSFORMER CONSTRUCTION PARAMETERS				
CORE SELECTION				
CORE	Custom	Custom		#N/A
CORE NAME	EQ20	EQ20		Core code
AE	59.8	59.8	mm^2	Core cross sectional area
LE	25.1	25.1	mm	Core magnetic path length
AL	3150	3150	nH	Ungapped core effective inductance per turns squared
VE	1500	1500	mm^3	Core volume
BOBBIN NAME	EQ20	EQ20		Bobbin name
AW		#N/A	mm^2	Enter the window area for the custom bobbin
BW	6.0	6.0	mm	Bobbin width
MARGIN		0.0	mm	Bobbin safety margin
PRIMARY WINDING				
NPRIMARY		39		Primary winding number of turns
BPEAK		3734	Gauss	Peak flux density
BMAX		3315	Gauss	Maximum flux density
BAC		1658	Gauss	AC flux density
ALG		302	nH	Typical gapped core effective inductance per turns squared
LG		0.225	mm	Core gap length
LAYERS_PRIMARY	2	2		Primary winding number of layers
AWG_PRIMARY		30		Primary wire gauge
OD_PRIMARY_INSULATED		0.303	mm	Pimary wire insulated outer diameter
OD_PRIMARY_BARE		0.255	mm	Primary wire bare outer diameter
CMA_PRIMARY		259.0	Cmils/A	Primary winding wire CMA
SECONDARY WINDING				
NSECONDARY	4	4		Secondary winding number of turns
AWG_SECONDARY		17		Secondary wire gauge
OD_SECONDARY_INSULATED		1.454	mm	Secondary wire insulated outer diameter
OD_SECONDARY_BARE		1.150		Secondary wire bare outer diameter
CMA_SECONDARY		250.8	Cmils/A	Secondary winding wire CMA
BIAS WINDING				
NBIAS		6		Bias winding number of turns
PRIMARY COMPONENTS SELECTION				
LINE UNDERVOLTAGE				
BROWN-IN REQURED		144.00	V	Required line brown-in threshold
RLS		7.14	MΩ	Connect two 3.57 MOhm resistors to the V-pin for the required UV/OV threshold
BROWN-IN ACTUAL		142.73	V	Actual brown-in threshold using standard resistors
BROWN-OUT ACTUAL		129.05	V	Actual brown-out threshold using standard resistors
LINE OVERVOLTAGE				
OVERVOLTAGE_LINE		596.21	V	The device voltage stress will be higher than 90% of the breakdown voltage when overvoltage is

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				trigerred
BIAS WINDING				
VBIAS	6.00	6.00	V	The rectified bias voltage maybe too low to supply the BP pin: Increase the rectified bias voltage to a value higher than 9V
VF_BIAS		0.70	V	Bias winding diode forward drop
VREVERSE_BIASDIODE		63.43	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
CBIAS		22	uF	Bias winding rectification capacitor
CBPP		0.47	uF	BPP pin capacitor
SECONDARY COMPONENTS SELECTION				
RECTIFIER				
VDRAIN_OFF_SRFET		53.29	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
SRFET	CSD19531Q5A	CSD19531Q5A		Secondary rectifier (Logic MOSFET)
VBREAKDOWN_SRFET		100	V	Secondary rectifier breakdown voltage
RDSON_SRFET		8.0	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
FEEDBACK COMPONENTS				
RFB_UPPER		100.00	kΩ	Upper feedback resistor (connected to the output terminal)
RFB_LOWER		34.00	kΩ	Lower feedback resistor required to obtain the output for cable drop compensation
CFB_LOWER		330	pF	Lower feedback resistor decoupling capacitor
VARIABLE OUTPUTS ANALYSIS				
TOLERANCE CORNER				
CORNER_VAC		180	V	Input AC RMS voltage corner to be evaluated
CORNER_ILIMIT	TYP	1.650	A	Current limit corner to be evaluated
CORNER_LPRIMARY	TYP	458.9	uH	Primary inductance corner to be evaluated
SETPOINT SELECTION				
SETPOINT	1	1		Select the setpoint which needs to be evaluated
FSWITCHING		58354.4	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
VOR		145.0	V	Voltage reflected to the primary winding when the primary MOSFET turns off
VMIN		228.44	V	Valley of the minimum input AC voltage
KP		2.886		Measure of continuous/discontinuous mode of operation
MODE_OPERATION		DCM		Mode of operation
DUTYCYCLE		0.180		Primary MOSFET duty cycle
TIME_ON		3.09	us	Primary controller's maximum on-time
TIME_OFF		14.04	us	Primary controller's minimum off-time
PRIMARY CURRENT				
IAVG_PRIMARY		0.139	A	Primary MOSFET average current
IPEAK_PRIMARY		1.538	A	Primary MOSFET peak current
IPEDESTAL_PRIMARY		0.000	A	Primary MOSFET current pedestal
IRIPPLE_PRIMARY		1.538	A	Primary MOSFET ripple current
IRMS_PRIMARY		0.377	A	Primary MOSFET RMS current
SECONDARY CURRENT				
IPEAK_SECONDARY		14.994	A	Secondary MOSFET peak current
IPEDESTAL_SECONDARY		0.000	A	Secondary MOSFET pedestal current
IRMS_SECONDARY		4.614	A	Secondary MOSFET RMS current
IRIPPLE_CAP_OUT		4.158	A	Output capacitor ripple current
MAGNETIC FLUX DENSITY				
BPEAK		3323	Gauss	Peak flux density
BMAX		3026	Gauss	Maximum flux density
BAC		1513	Gauss	AC flux density (0.5 x Peak to Peak)

Note:

1) The measured rectified bias voltage is close to 9 V due to the peak charging of the bias capacitor.
2) Actual RFB_LOWER is 33 kΩ, trimmed for the required Vout level.

10 Performance Data

10.1 *Efficiency*

Note: Output voltage measured at PCB end.

10.1.1 Efficiency vs. Line

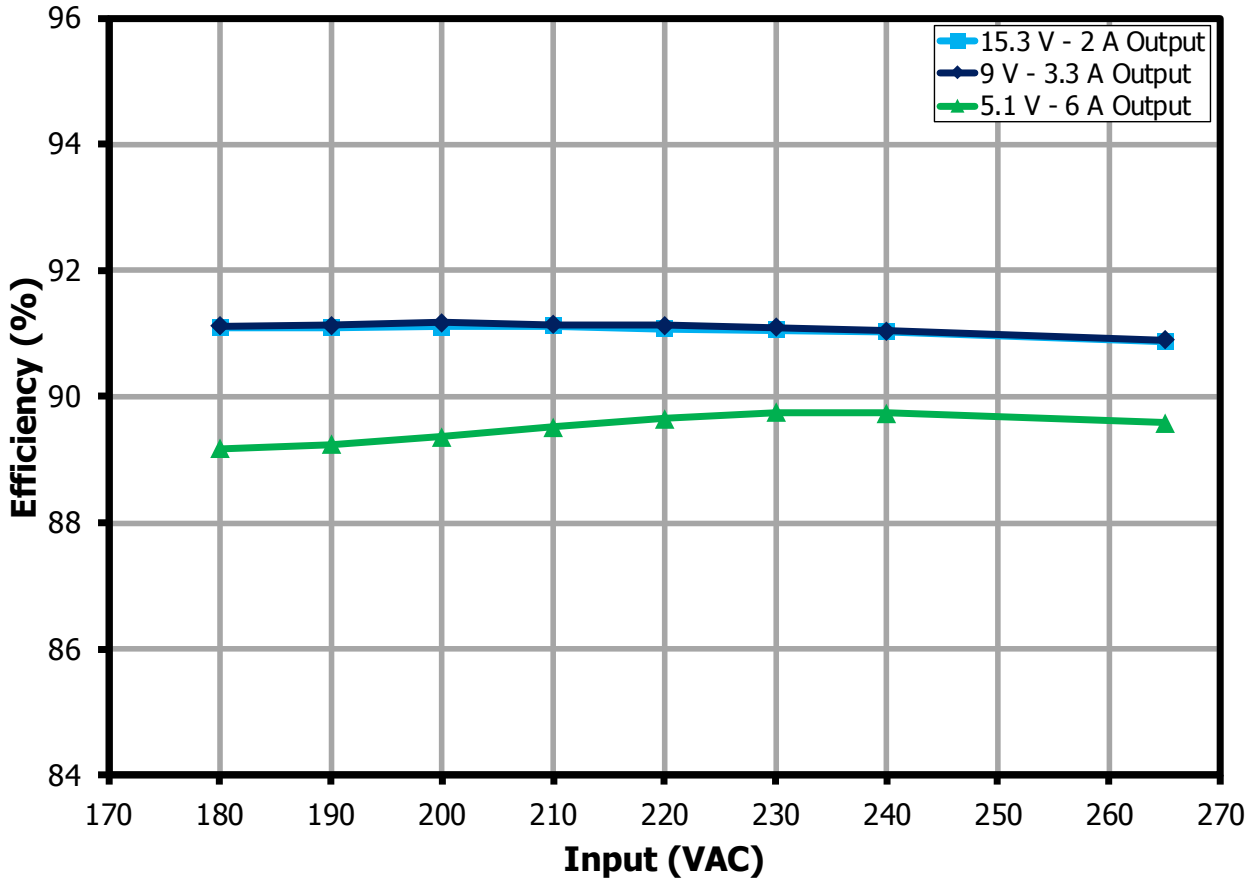

Figure 11 – Efficiency vs. Input Line Voltage.

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10.1.2 Efficiency vs. Load

Note: Output voltage measured at PCB end.

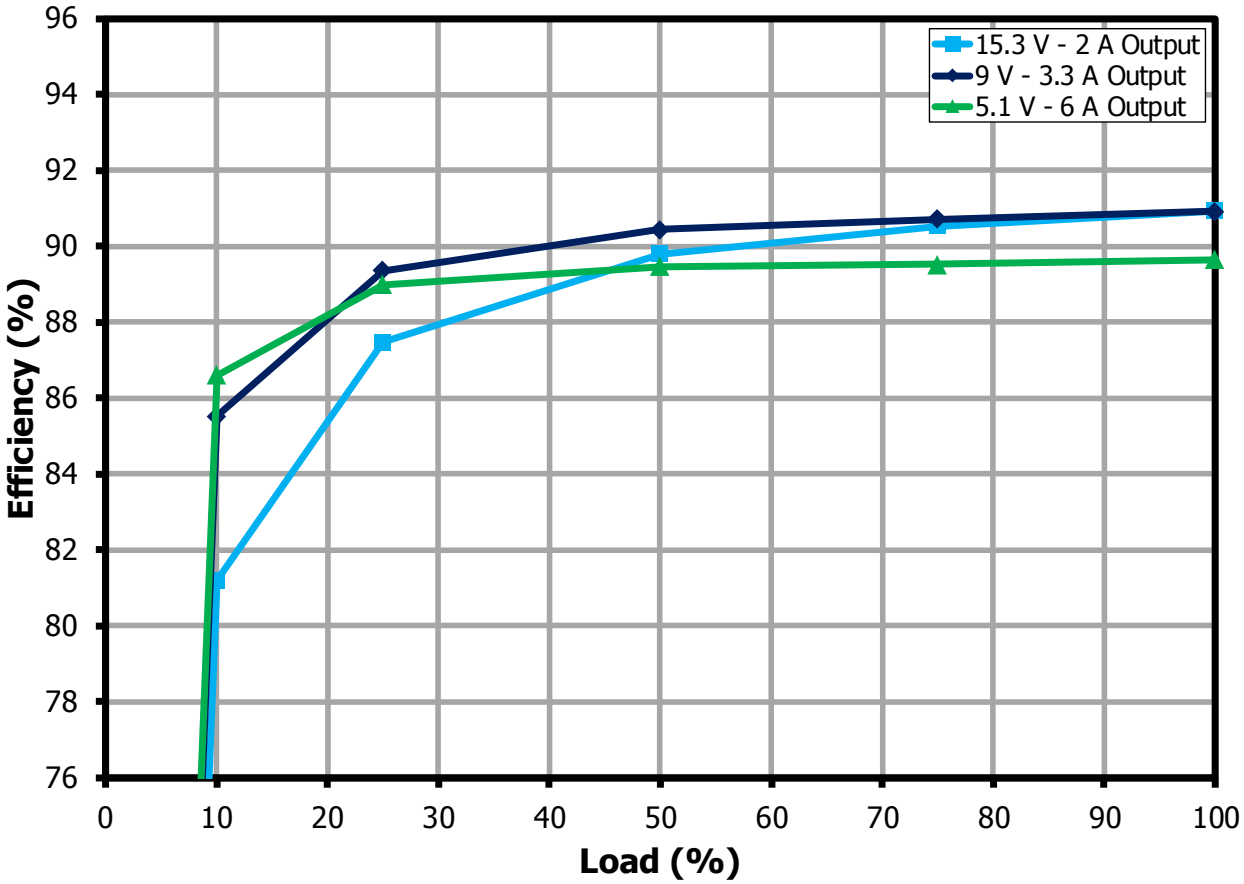

Figure 12 – Efficiency vs. Percent Load (230 VAC).

10.1.3 No-Load Input Power

Note: 5 V output at no-load.

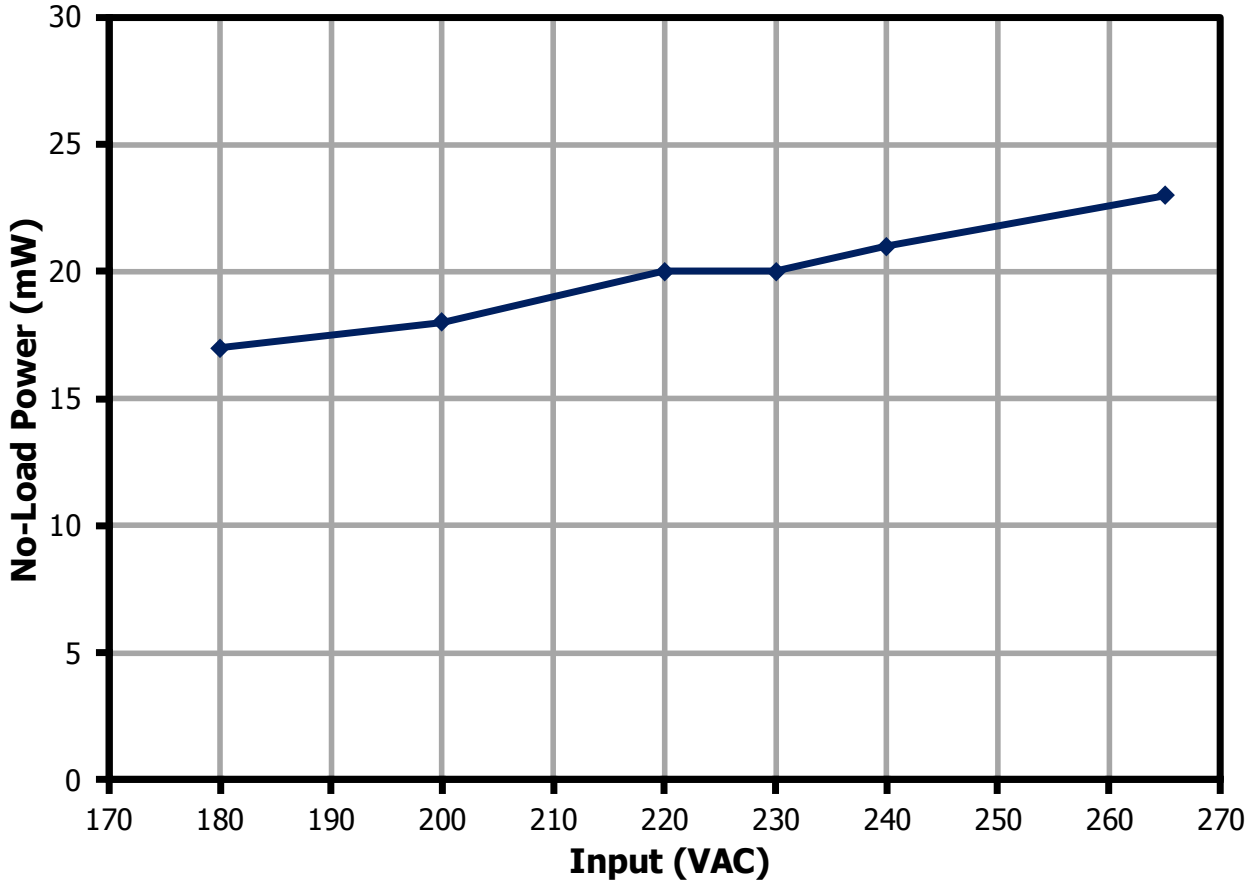

Figure 13 – No-Load Power vs. Input Line Voltage.

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10.2 *Line and Load Regulation*

10.2.1 5.1 V Line Regulation at 6 A Load

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

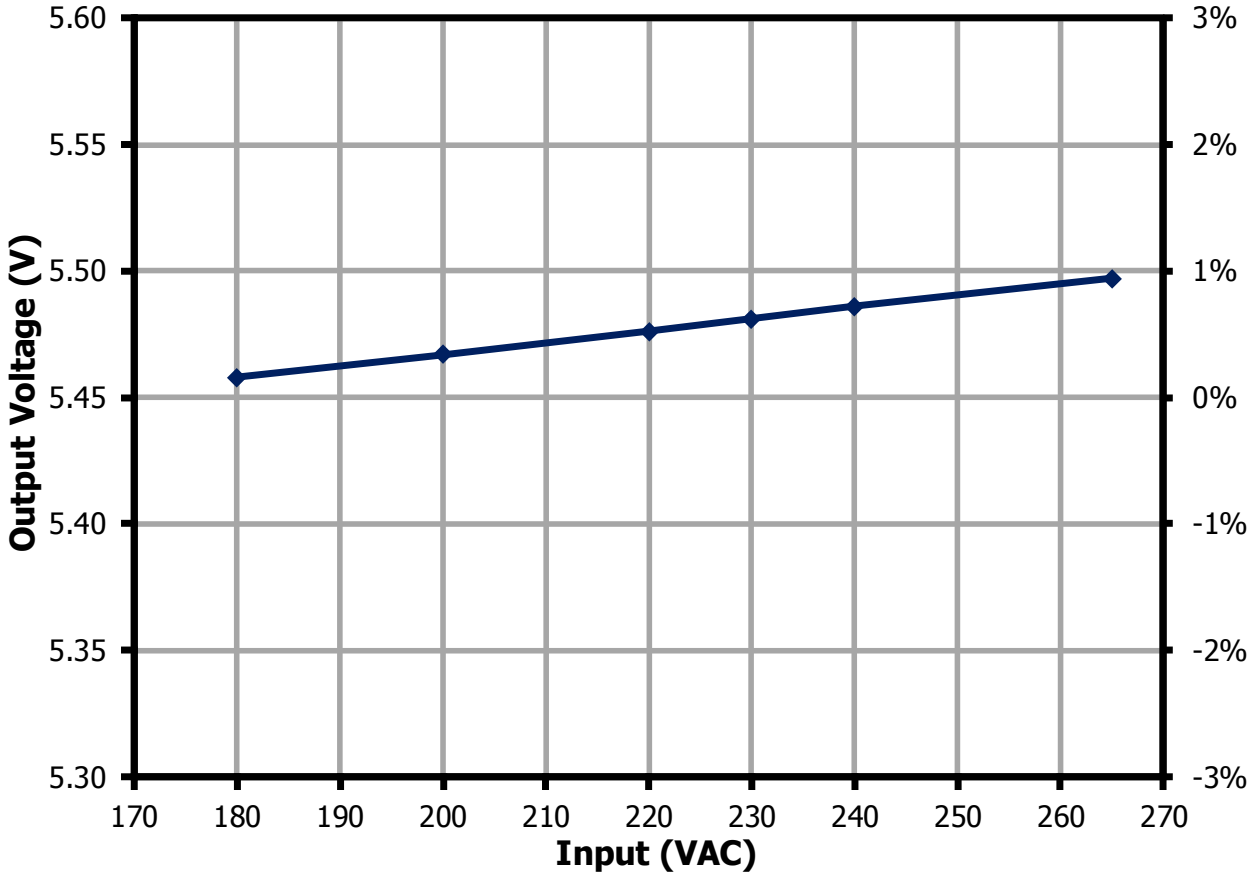

Figure 14 – 5.1 V Output Regulation vs. Input Line Voltage.

10.2.2 9.2 V Line Regulation at 3.3 A Load

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

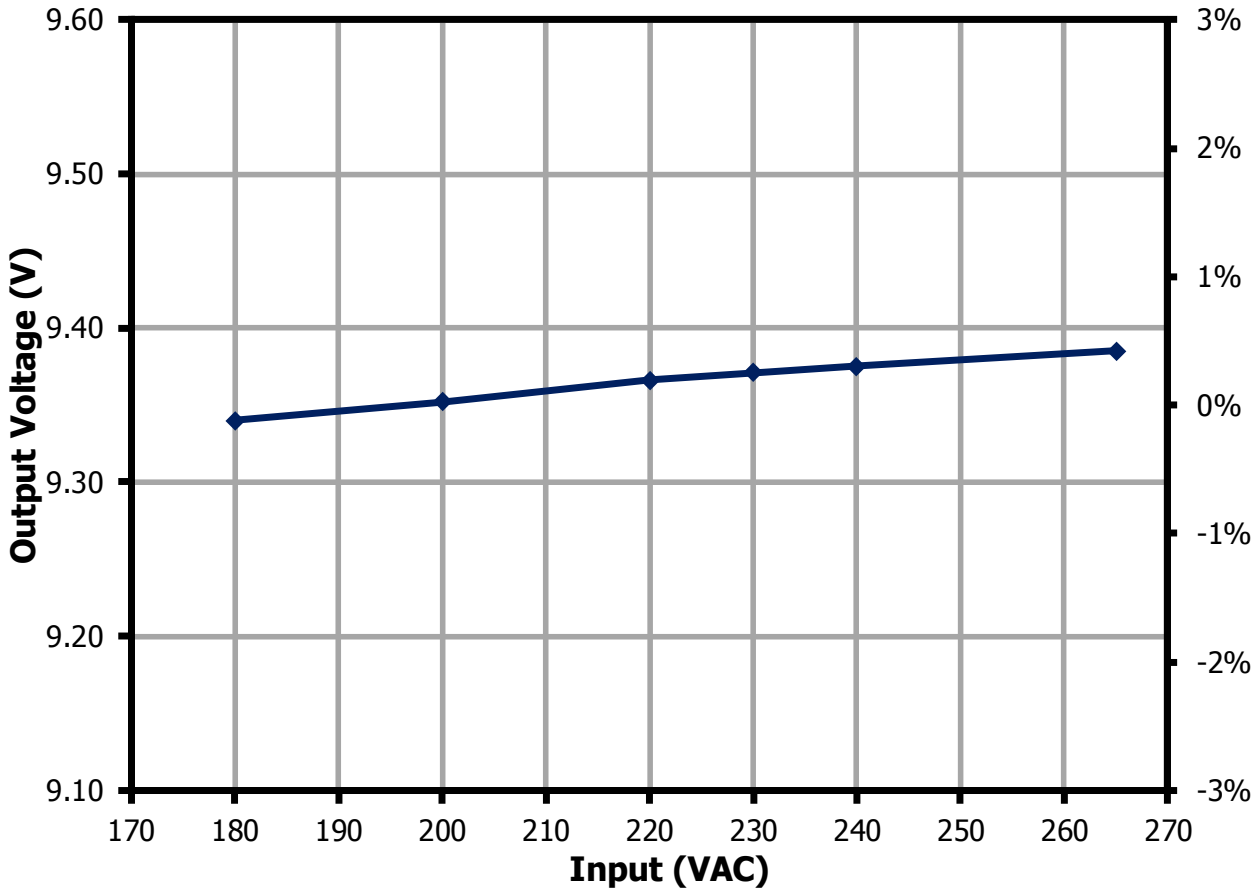

Figure 15 – 9.2 V Output Regulation vs. Input Line Voltage.

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10.2.3 15.3 V Line Regulation at 2 A Load

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

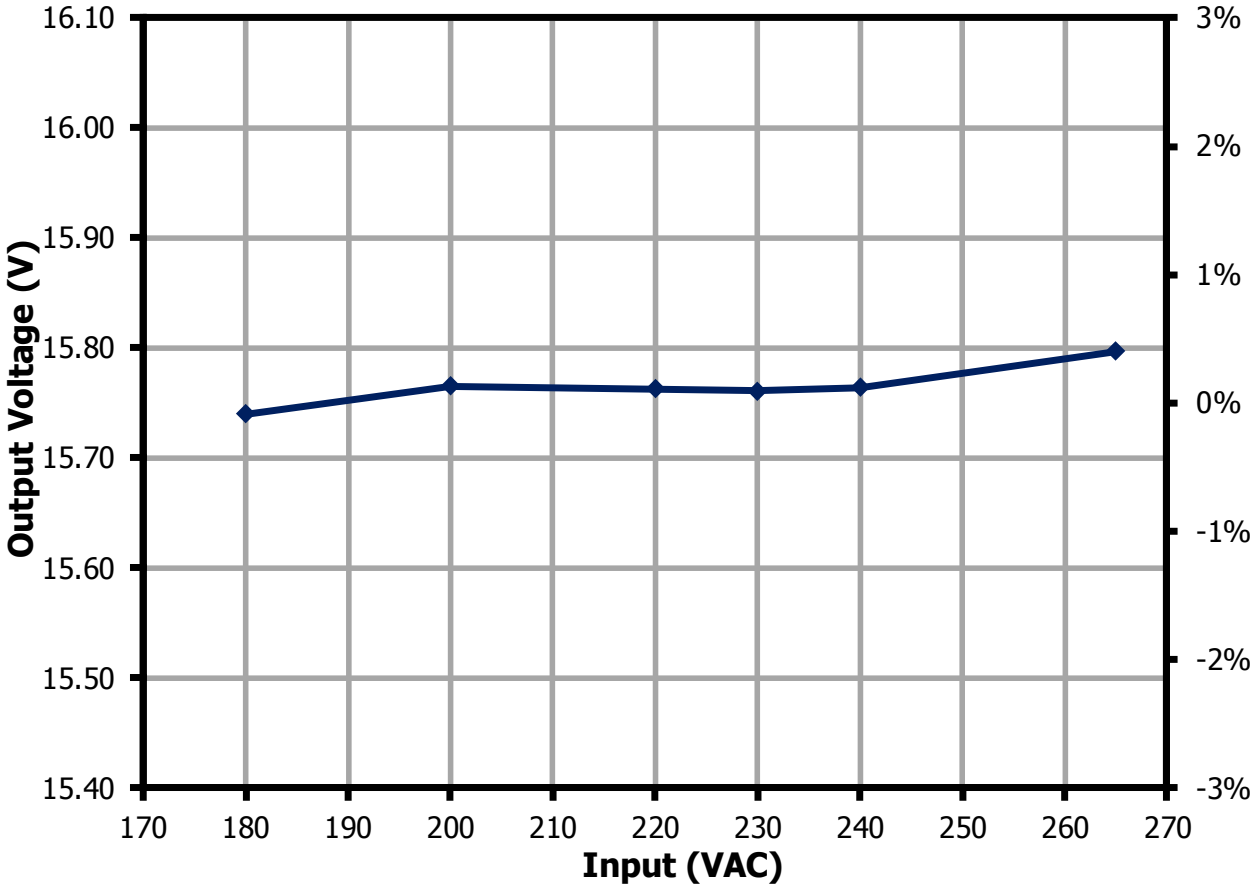

Figure 16 – 15.3 V Output Regulation vs. Input Line Voltage.

10.2.4 5.1 V Load Regulation

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

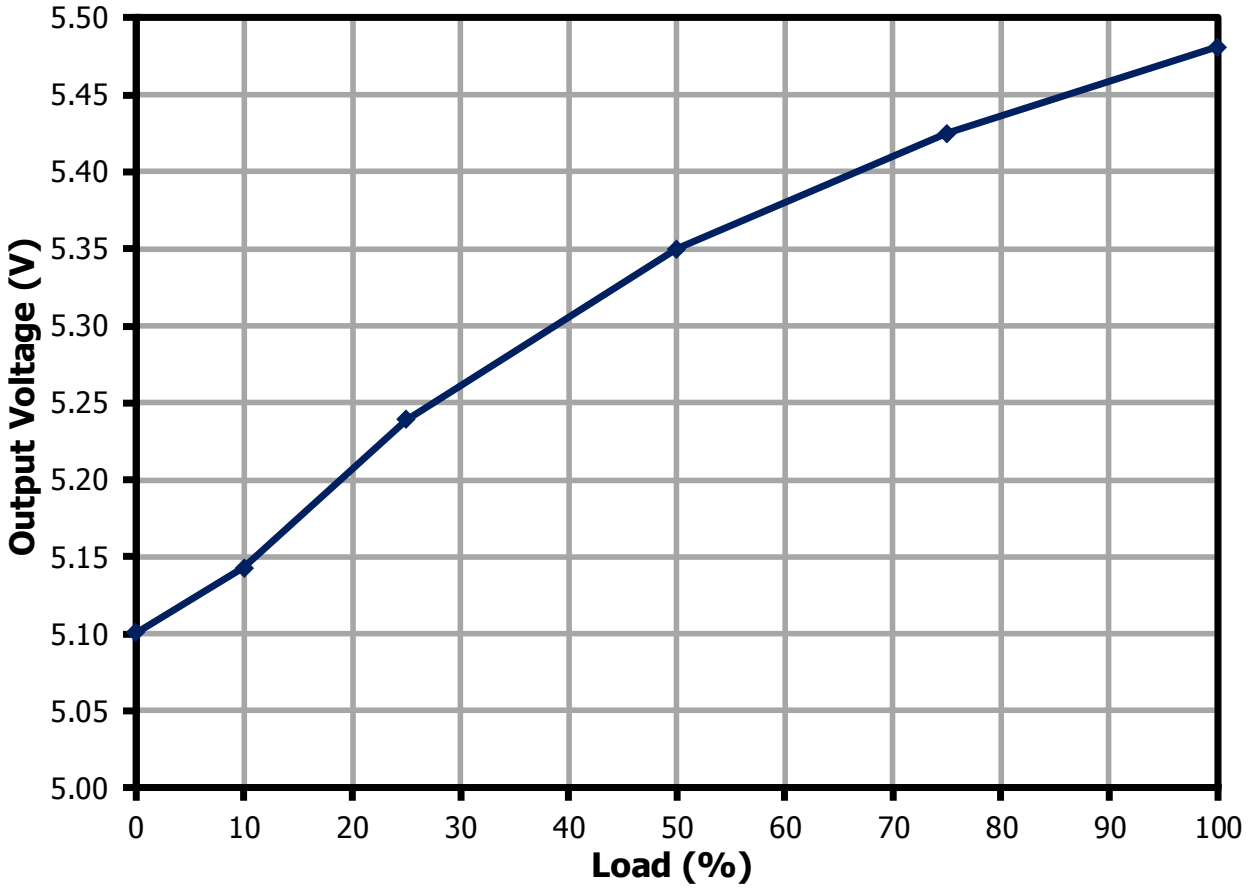

Figure 17 – 5.1 V Output Regulation vs. Percent Load.

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10.2.5 9.2 V Load Regulation

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

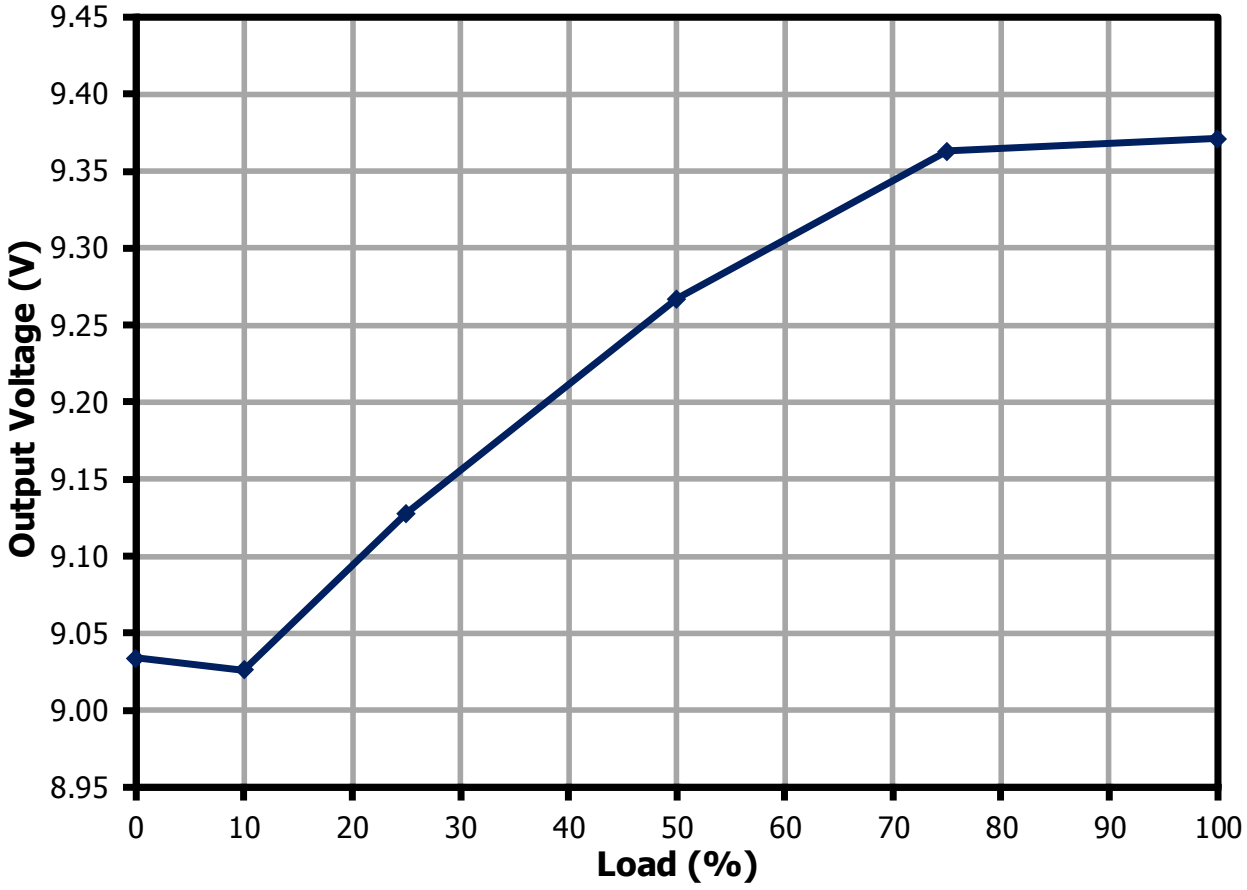

Figure 18 – 9.2 V Output Regulation vs. Percent Load.

10.2.6 15.3 V Load Regulation

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

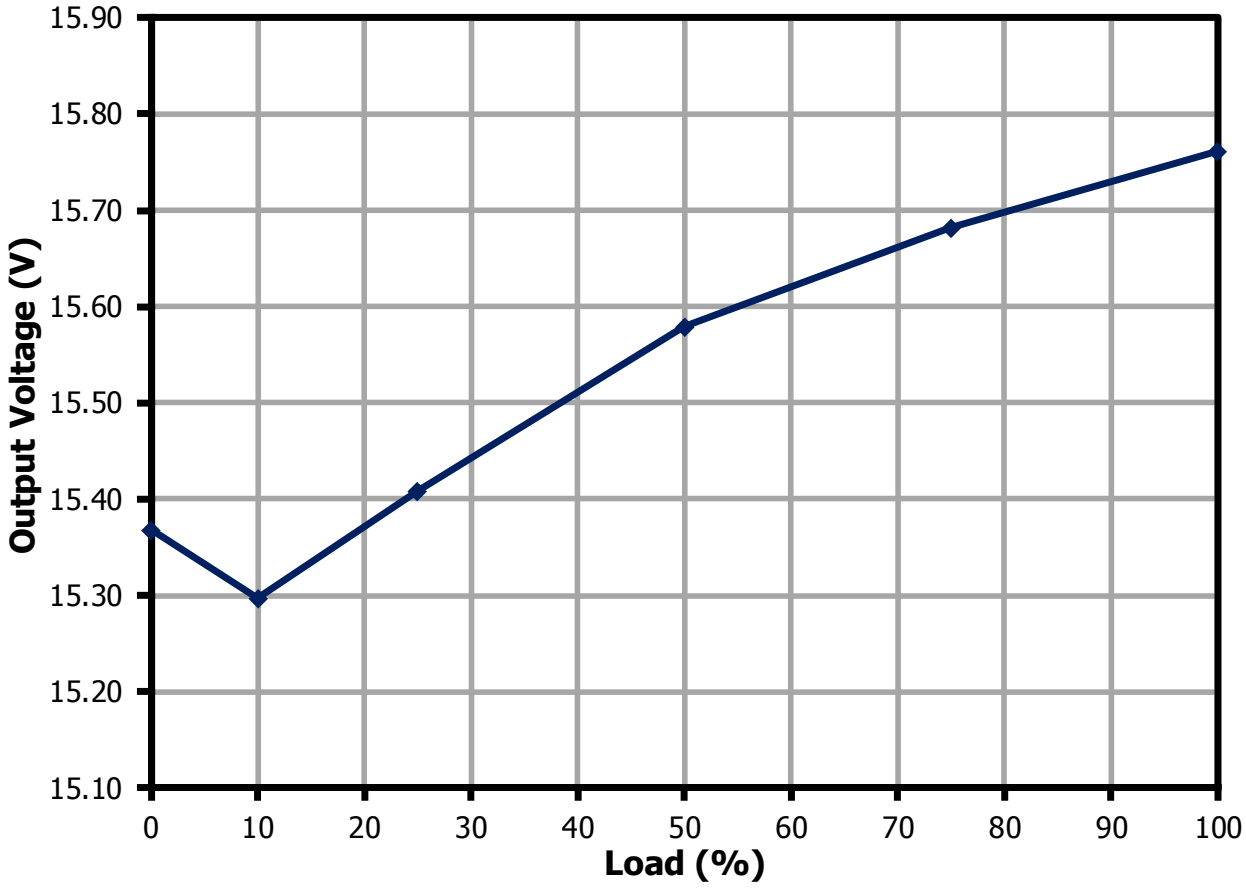

Figure 19 – 15.3 V Output Regulation vs. Percent Load.

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10.2.7 CV/CC vs. Line (5.1 V / 6 A)

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

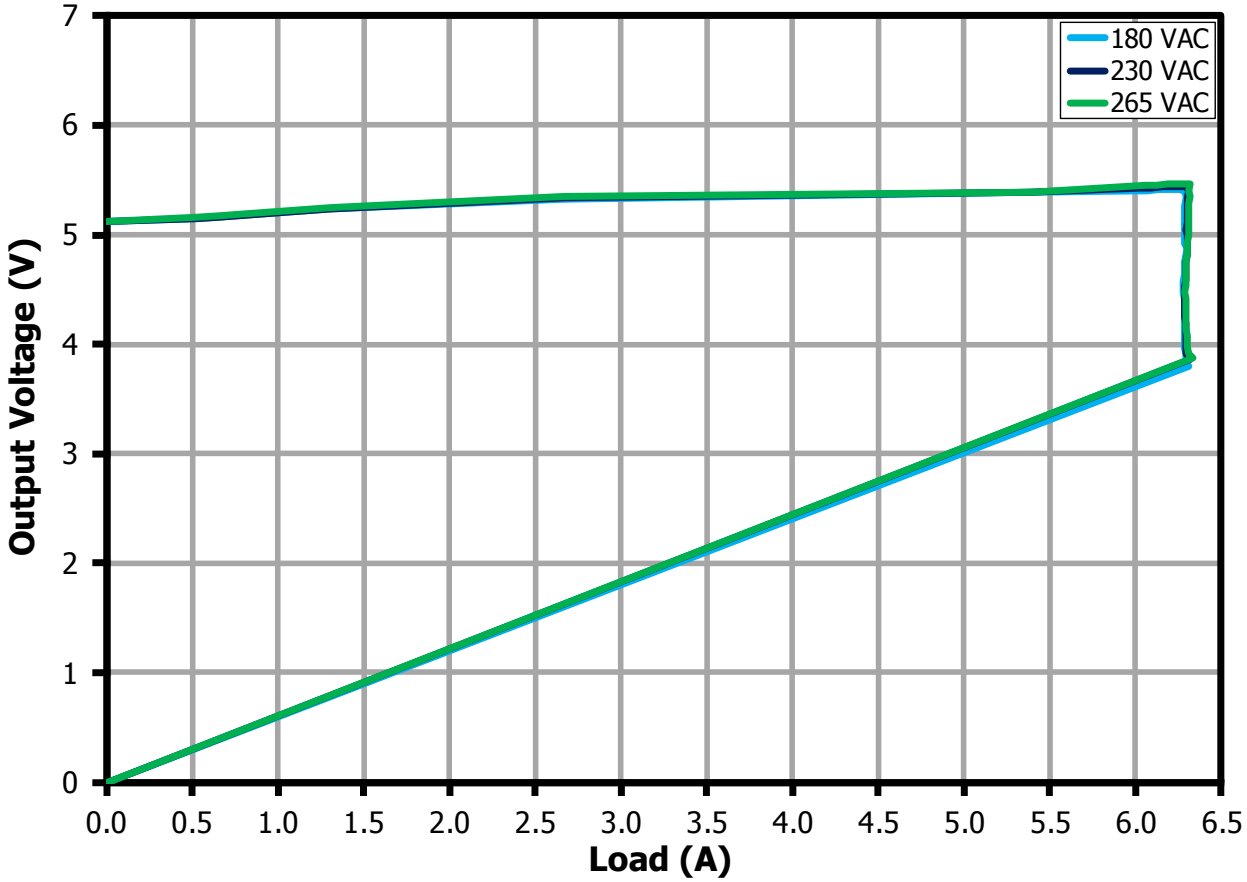

Figure 20 – CV/CC for 5.1 V Output at Different Input Line.

10.2.8 CV/CC vs. Line (9.2 V / 3.3 A)

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

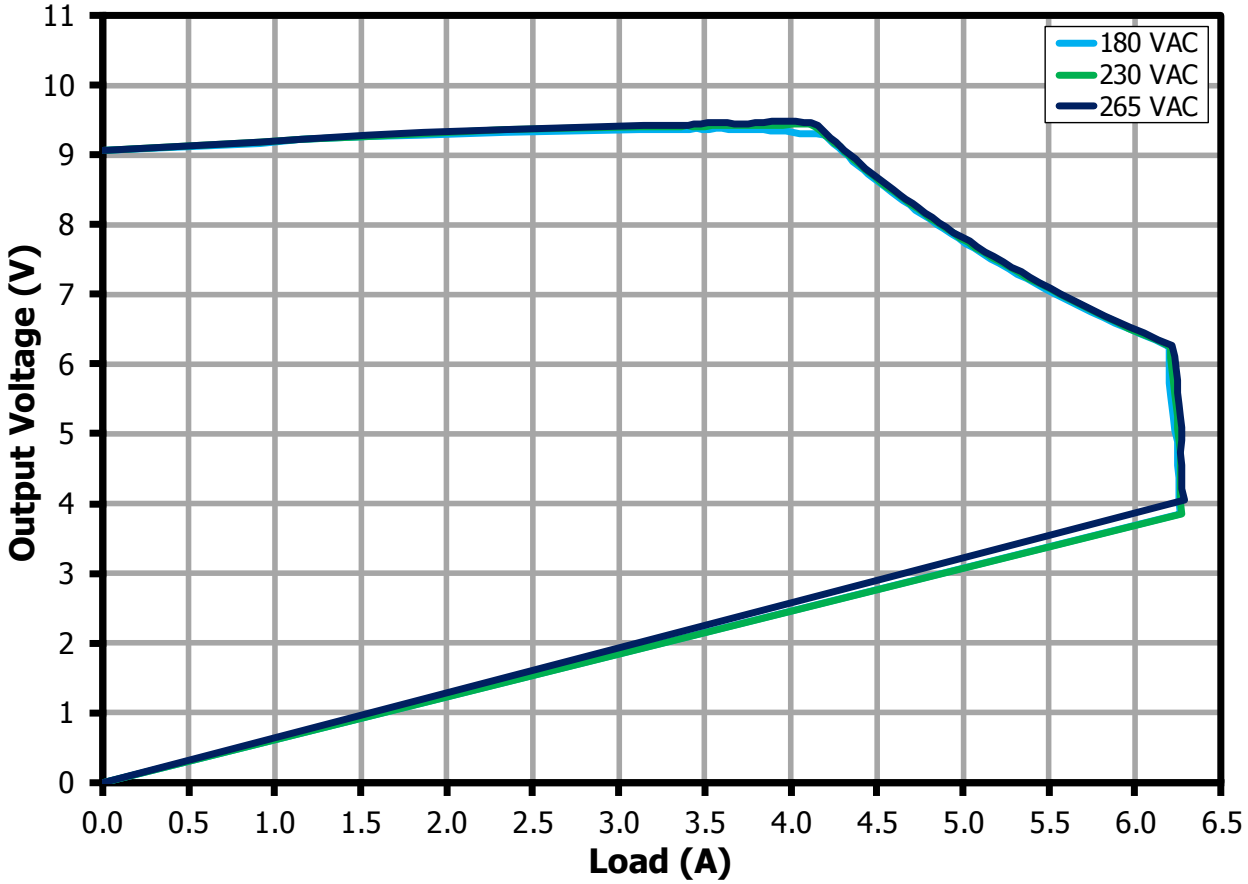

Figure 21 – CV/CC for 9.2 V Output at Different Input Line.

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10.2.9 CV/CC vs. Line (15.3 V / 2 A)

Note: Output voltage measured at PCB end. This considers the 300 mV cable drop compensation.

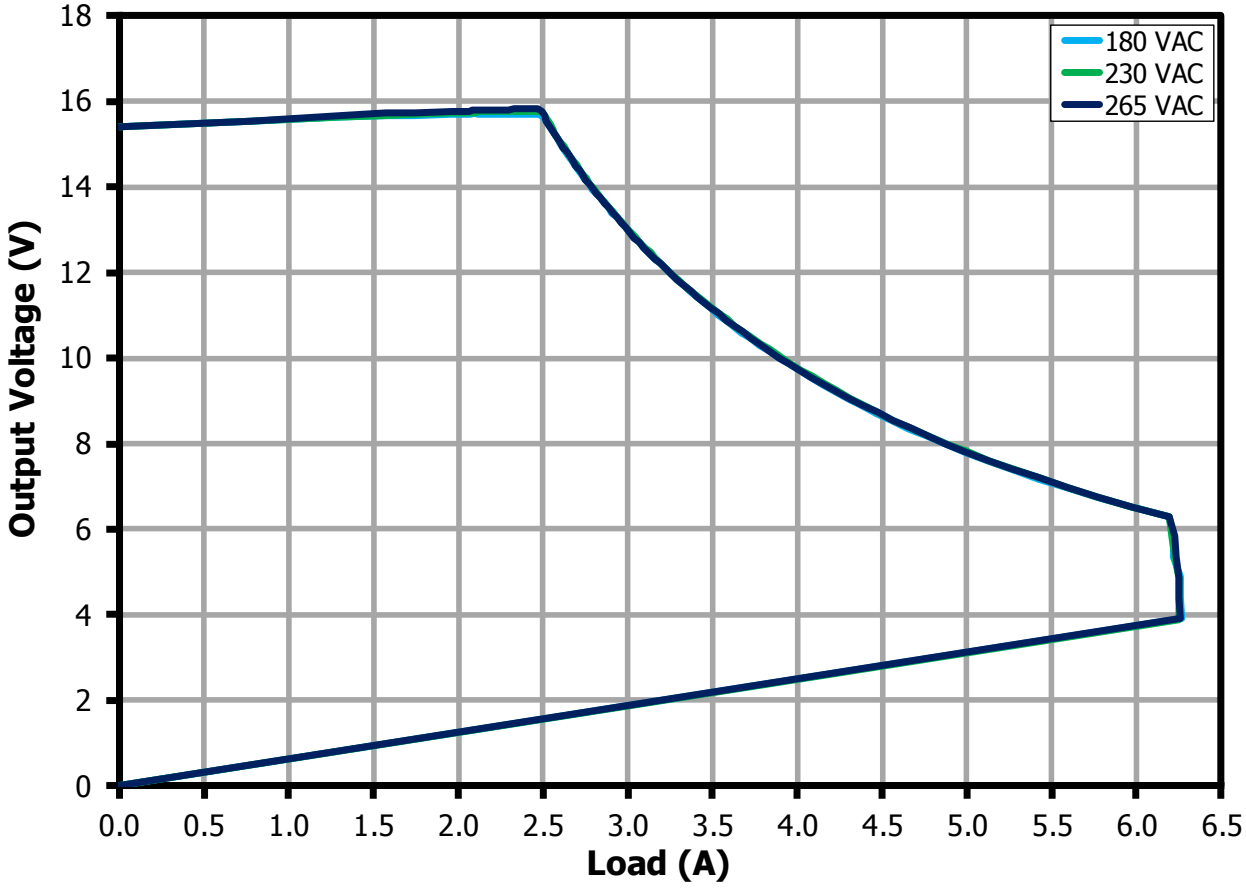

Figure 22 – CV/CC for 15 V Output at Different Input Line.

11 Test Data

11.1 *Test Data Efficiency vs. Line, 5.1 V / 6 A (PCB End)*

Input		Input Measurement			5.1 V / 6 A			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	
180	50	179.90	0.40	36.71	5.46	6.00	32.74	89.18
190	50	189.94	0.39	36.72	5.46	6.00	32.77	89.25
200	50	199.88	0.38	36.69	5.46	6.00	32.79	89.37
210	50	209.92	0.37	36.64	5.47	6.00	32.80	89.51
220	50	219.93	0.36	36.61	5.47	6.00	32.82	89.66
230	50	229.96	0.35	36.61	5.48	6.00	32.86	89.75
240	50	239.90	0.34	36.65	5.48	6.00	32.89	89.74
265	50	264.94	0.32	36.74	5.49	6.00	32.91	89.59

11.2 *Test Data Efficiency vs. Line, 9.2 V / 3.3 A (PCB End)*

Input		Input Measurement			9.2 V / 3.3 A			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	
180	50	179.91	0.38	34.06	9.40	3.30	31.03	91.12
190	50	189.95	0.37	34.11	9.42	3.30	31.09	91.13
200	50	199.89	0.36	34.13	9.43	3.30	31.12	91.17
210	50	209.93	0.35	34.14	9.43	3.30	31.11	91.14
220	50	219.94	0.34	34.14	9.43	3.30	31.11	91.13
230	50	229.97	0.33	34.15	9.43	3.30	31.11	91.09
240	50	239.91	0.32	34.18	9.43	3.30	31.12	91.04
265	50	264.95	0.31	34.32	9.45	3.30	31.20	90.90

11.3 *Test Data Efficiency vs. Line, 15.3 V / 2 A (PCB End)*

Input		Input Measurement			15.3 V / 2 A			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	
180	50	179.91	0.38	34.56	15.74	2.00	31.48	91.09
190	50	189.95	0.37	34.59	15.76	2.00	31.51	91.10
200	50	199.89	0.36	34.59	15.76	2.00	31.52	91.11
210	50	209.93	0.35	34.58	15.76	2.00	31.51	91.12
220	50	219.94	0.34	34.59	15.75	2.00	31.50	91.08
230	50	229.97	0.33	34.61	15.76	2.00	31.51	91.05
240	50	239.91	0.33	34.66	15.78	2.00	31.55	91.03
265	50	264.95	0.31	34.74	15.79	2.00	31.57	90.87

Note: Outputs measurement at PCB end.

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11.4 *Test Data Efficiency vs. Percent Load, 5.1 V / 6 A @ 230 VAC (PCB End)*

Load Settings	Input Measurement			5.1 V / 6 A Measurement Variable			
% Load	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)
100	229.95	0.35	36.64	5.47	6.00	32.84	89.64
75	229.97	0.28	27.27	5.43	4.50	24.41	89.53
50	229.98	0.20	17.94	5.35	3.00	16.05	89.45
25	229.99	0.12	8.82	5.23	1.50	7.85	88.98
10	229.99	0.06	3.56	5.14	0.60	3.08	86.60

11.5 *Test Data Efficiency vs. Percent Load, 9.2 V / 3.3 A @ 230 VAC (PCB End)*

Load Settings	Input Measurement			5.1 V / 6 A Measurement Variable			
% Load	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)
100	229.97	0.33	34.22	9.43	3.30	31.11	90.91
75	229.98	0.26	25.55	9.36	2.48	23.18	90.72
50	229.99	0.19	16.92	9.27	1.65	15.30	90.44
25	230.00	0.11	8.42	9.12	0.82	7.52	89.35
10	230.00	0.06	3.48	9.03	0.33	2.98	85.52

11.6 *Test Data Efficiency vs. Percent Load, 15.3 V / 2 A @ 230 VAC (PCB End)*

Load Settings	Input Measurement			5.1 V / 6 A Measurement Variable			
% Load	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)
100	229.97	0.33	34.68	15.77	2.00	31.54	90.93
75	229.98	0.27	26.00	15.69	1.50	23.54	90.52
50	229.99	0.19	17.35	15.58	1.00	15.58	89.80
25	230.00	0.12	8.80	15.41	0.50	7.70	87.47
10	230.00	0.06	3.76	15.31	0.20	3.05	81.18

Note: Outputs measurement at PCB end.

11.7 *Test Data Line Regulation, 5.1 V / 6 A*

Input		5.1 V / 6 A		
VAC (V_{RMS})	Freq (Hz)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)
180	50	5.46	5991.70	32.68
200	50	5.47	5991.60	32.74
220	50	5.48	5991.70	32.79
230	50	5.48	5991.90	32.82
240	50	5.49	5992.10	32.85
265	50	5.49	5992.60	32.92

11.8 *Test Data Line Regulation, 9.2 V / 3.3 A*

Input		9.2 V / 3.3 A		
VAC (V_{RMS})	Freq (Hz)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)
180	50	9.34	3583.50	33.43
200	50	9.35	3591.30	33.55
220	50	9.37	3597.50	33.66
230	50	9.37	3594.60	33.65
240	50	9.38	3596.90	33.68
265	50	9.39	3599.90	33.75

11.9 *Test Data Line Regulation, 15.3 V / 2 A*

Input		15.3 V / 2 A		
VAC (V_{RMS})	Freq (Hz)	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)
180	50	15.74	1999.60	31.47
200	50	15.76	1999.50	31.52
220	50	15.76	1999.50	31.52
230	50	15.76	1999.60	31.52
240	50	15.76	1999.60	31.52
265	50	15.80	1999.60	31.59

Note: Output voltage measurement at PCB end.

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11.10 *Test Data Load Regulation, 5.1 V @ 230 VAC*

Load Settings	5.1 V / 6 A Measurement Variable		
% Load	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)
100	5.48	5991.90	32.82
75	5.43	4595.30	24.91
50	5.35	3008.60	16.08
25	5.24	1498.80	7.85
10	5.14	599.40	3.08
0	5.10	0.005	0.00

11.11 *Test Data Load Regulation, 9.2 V / 3.3 A @ 230 VAC*

Load Settings	5.1 V / 6 A Measurement Variable		
% Load	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)
100	9.37	3594.60	33.65
75	9.36	2470.20	23.12
50	9.27	1647.80	15.26
25	9.13	824.40	7.53
10	9.03	329.60	2.98
0	9.03	0.01	0.00

11.12 *Test Data Load Regulation, 15.3 V / 2 A @ 230 VAC*

Load Settings	5.1 V / 6 A Measurement Variable		
% Load	V_{OUT} (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)
100	15.76	1999.60	31.52
75	15.68	1499.40	23.51
50	15.58	999.20	15.57
25	15.41	499.40	7.69
10	15.30	199.04	3.05
0	15.37	0.01	0.00

Note: Output voltage measurement at PCB end.

11.13 *Test Data No-Load Consumption, 5.1 V / 0 A*

Input		Input Measurement		
VAC (V_{RMS})	Freq (Hz)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (mW)
180	50	179.91	81.90	17.00
200	50	199.94	79.77	18.00
220	50	219.88	77.21	20.00
230	50	229.90	75.83	20.00
240	50	239.92	74.51	21.00
265	50	264.93	71.40	23.00

12 Thermal Performance

12.1 *Open Case at 5.1 V / 6 A (25 ºC)*

12.1.1 180 VAC @ 25 ºC Ambient

Ambient	INN3268C (U1)	SR FET (Q3)	Transformer (T1)
25	83.8	99.6	84.1

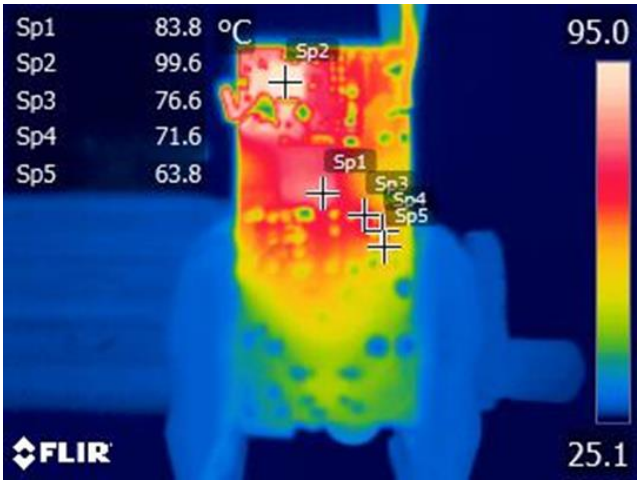

Figure 23 – Ambient = 25 ºC.
Solder Side.

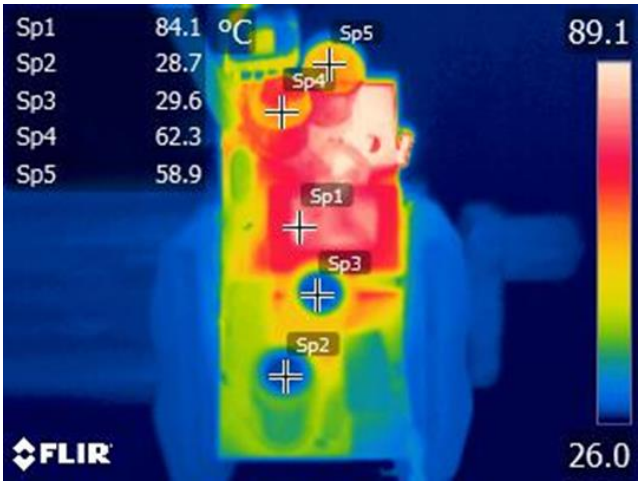

Figure 24 – Ambient = 25 ºC.
Component Side.

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12.1.2 265 VAC @ 25 ºC Ambient

Ambient	INN3268C (U1)	SR FET (Q3)	Transformer (T1)
25	88.2	102.6	87.0

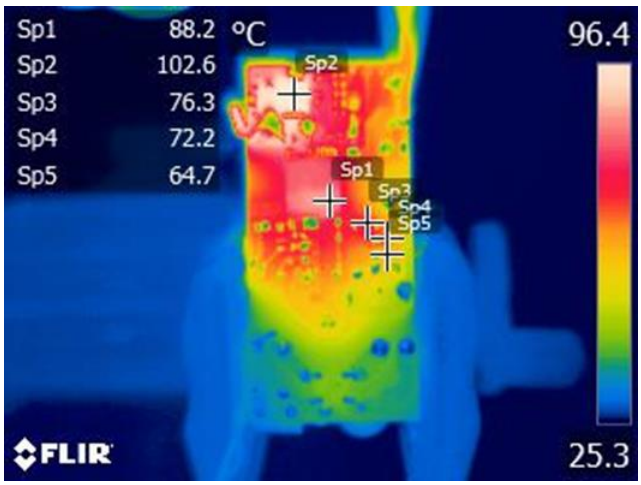

Figure 25 – Ambient = 25 ºC.
Solder Side.

Figure 26 – Ambient = 25 ºC.
Component Side.

12.2 *Open Case at 9.2 V / 3.3 A (25 ºC)*

12.2.1 180 VAC @ 25 ºC Ambient

Ambient	INN3268C (U1)	SR FET (Q3)	Transformer (T1)
25	70.9	75.7	74.2

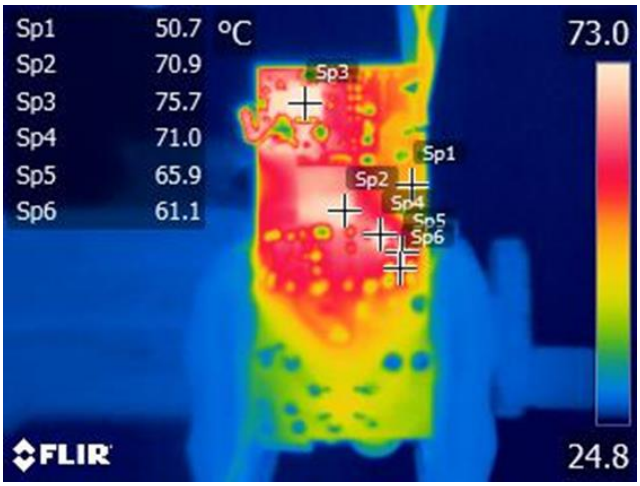

Figure 27 – Ambient = 25 ºC.
Solder Side.

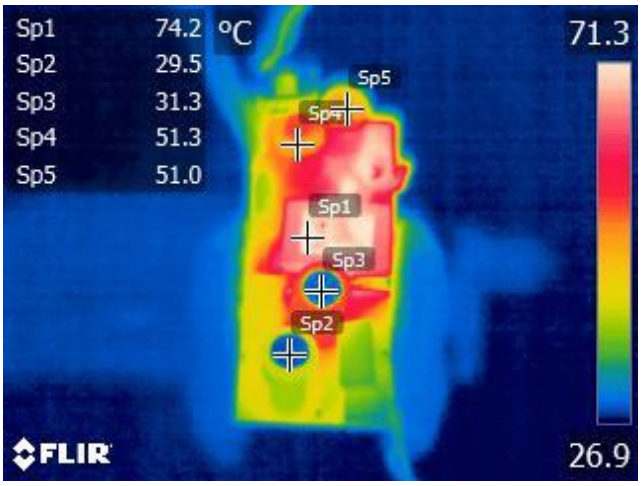

Figure 28 – Ambient = 25 ºC.
Component Side.

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12.2.2 265 VAC @ 25 ºC Ambient

Ambient	INN3268C (U1)	SR FET (Q3)	Transformer (T1)
25	73.4	76.3	75.5

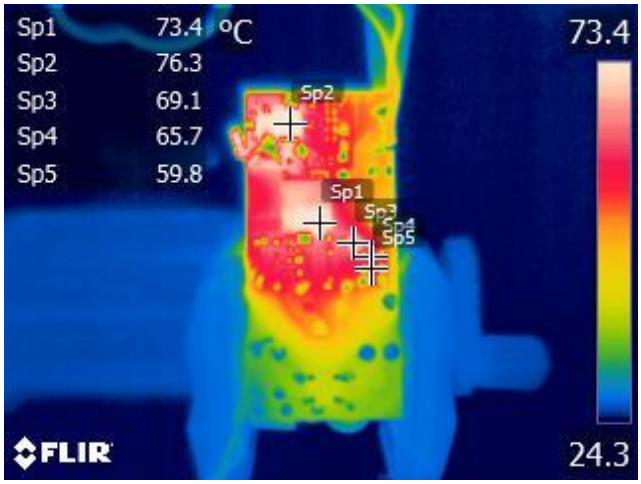

Figure 29 – Ambient = 25 ºC.
Solder Side.

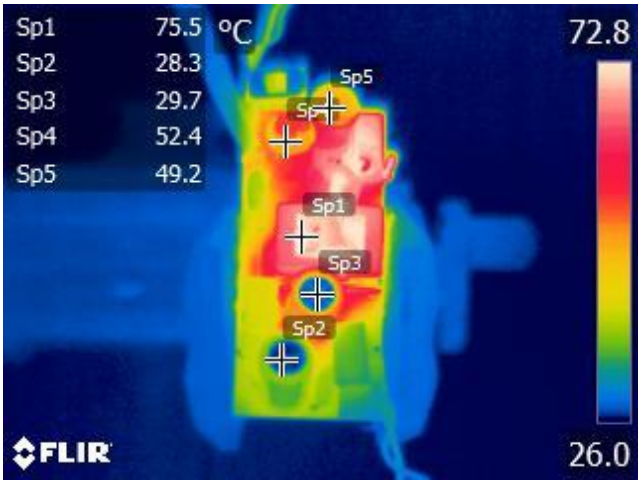

Figure 30 – Ambient = 25 ºC.
Component Side.

12.3 *Open Case at 15.3 V / 2 A (25 ºC)*

12.3.1 180 VAC @ 25 ºC Ambient

Ambient	INN3268C (U1)	SR FET (Q3)	Transformer (T1)
25	73.2	68.7	72.4

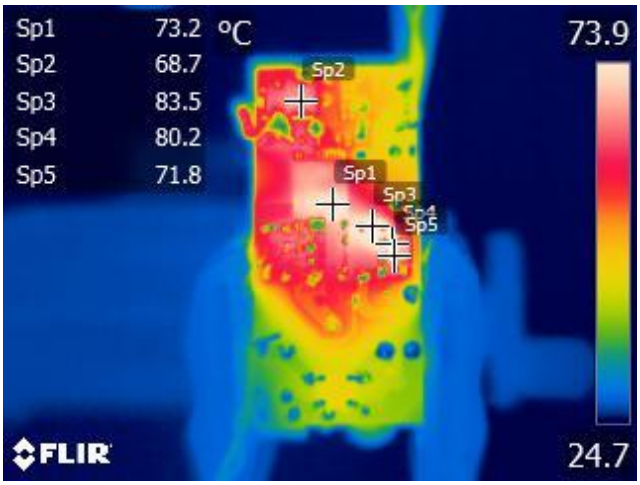

Figure 31 – Ambient = 25 ºC.
Solder Side.

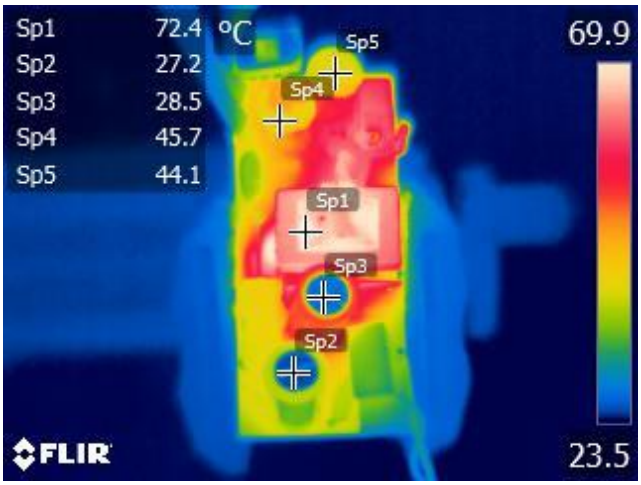

Figure 32 – Ambient = 25 ºC.
Component Side.

12.3.2 265 VAC @ 25 ºC Ambient

Ambient	INN3268C (U1)	SR FET (Q3)	Transformer (T1)
25	77.7	71.2	72.6

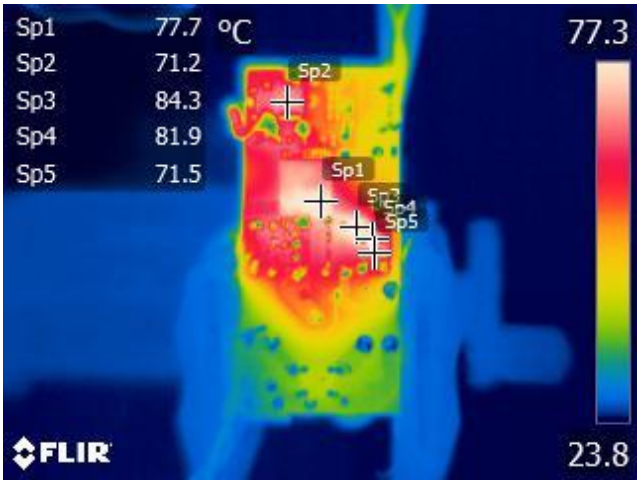

Figure 33 – Ambient = 25 ºC.
Solder Side.

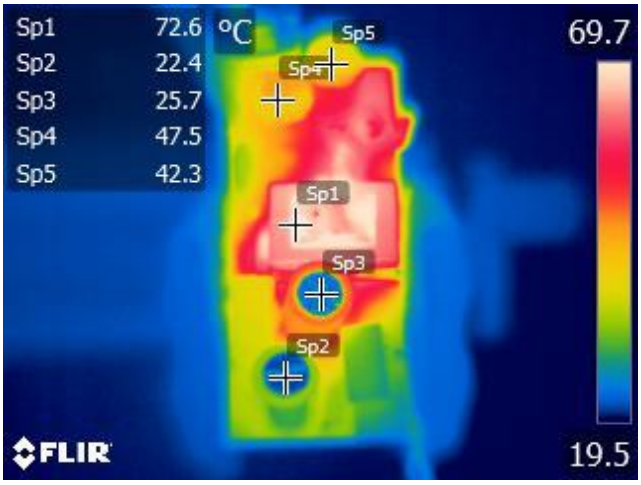

Figure 34 – Ambient = 25 ºC.
Component Side

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12.4 *Open Case at 5.1 V / 6 A (50 ºC)*

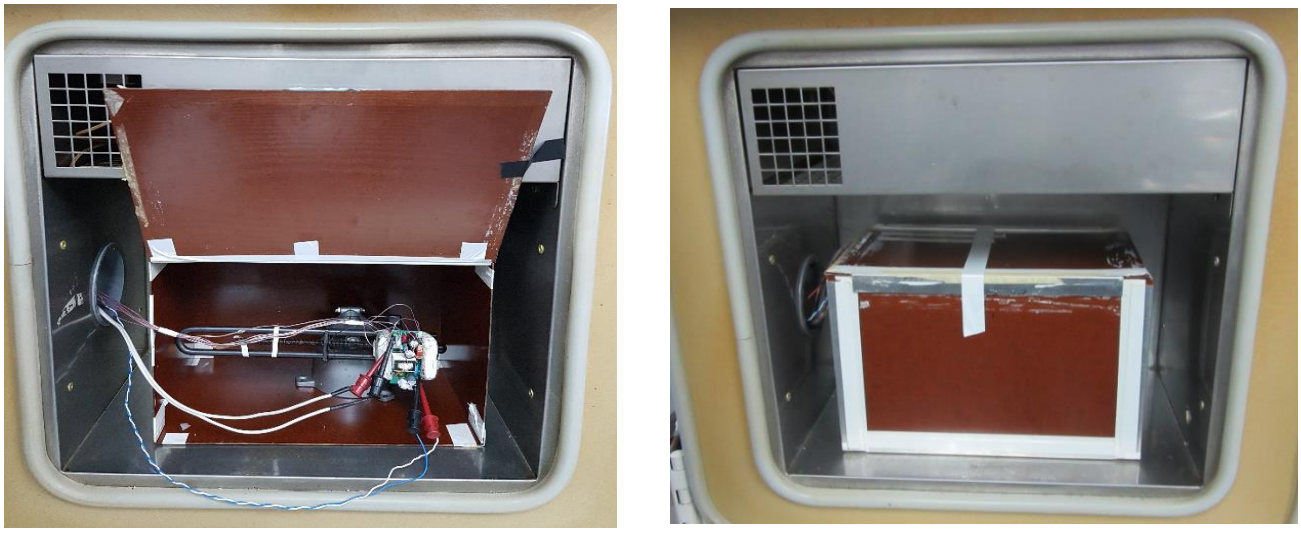
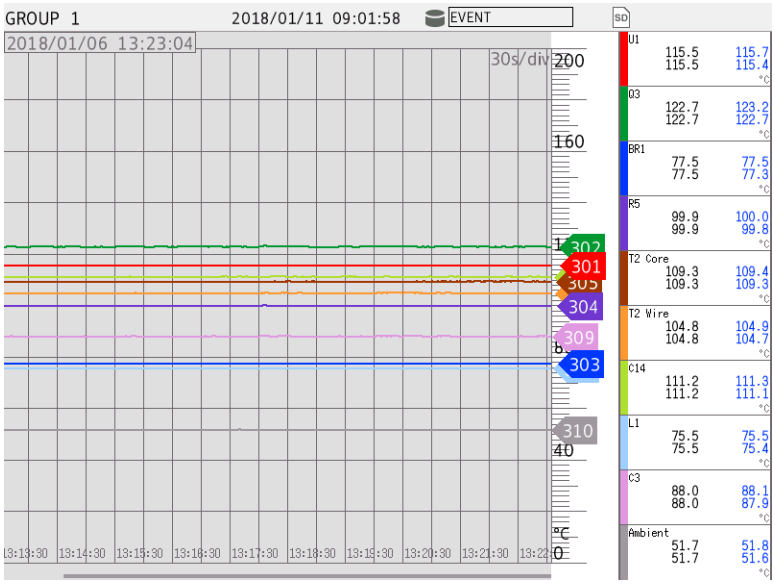


Figure 35 – Test Set-up Picture.

Unit was placed inside a box enclosure to prevent airflow that might affect the thermal measurements. Ambient temperature was set to 50 ºC. Temperature was measured using type T thermocouple.

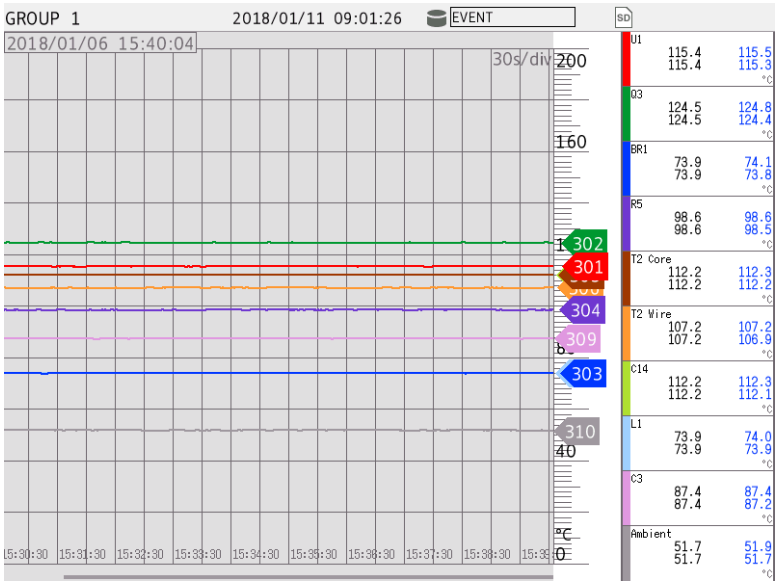
12.4.1 180 VAC @ 50 ºC Ambient

Ambient	INN3268C (U1)	SR FET (Q3)	Transformer (T1)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C14)
51.8	115.7	123.2	109.4	77.5	75.5	88.1	111.3



12.4.2 265 VAC @ 50 ºC Ambient

Ambient	INN3268C (U1)	SR FET (Q3)	Transformer (T1)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C14)
51.9	115.5	124.8	112.3	74.1	74	87.4	112.3



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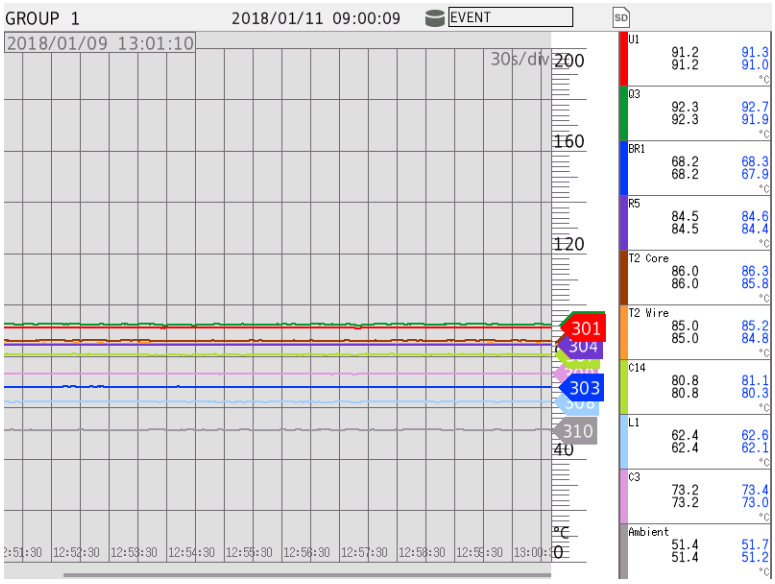
12.5 *Open Case at 9.2 V / 3.3 A (50 ºC)*

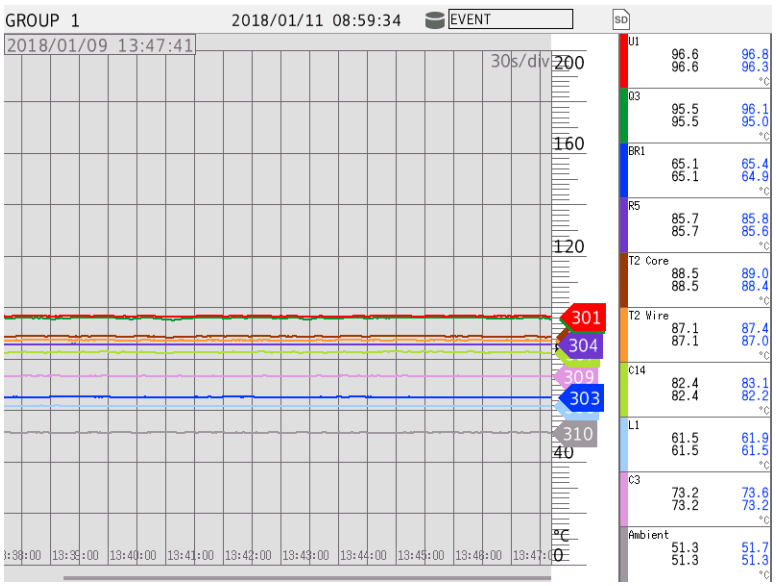
12.5.1 180 VAC @ 50 ºC Ambient

Ambient	INN3268C (U1)	SR FET (Q3)	Transformer (T1)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C14)
51.7	91.3	92.7	86.3	68.3	62.6	73.4	81.1



12.5.2 265 VAC @ 50 ºC Ambient

Ambient	INN3268C (U1)	SR FET (Q3)	Transformer (T1)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C14)
51.7	96.8	96.1	89	65.4	61.9	73.6	83.1



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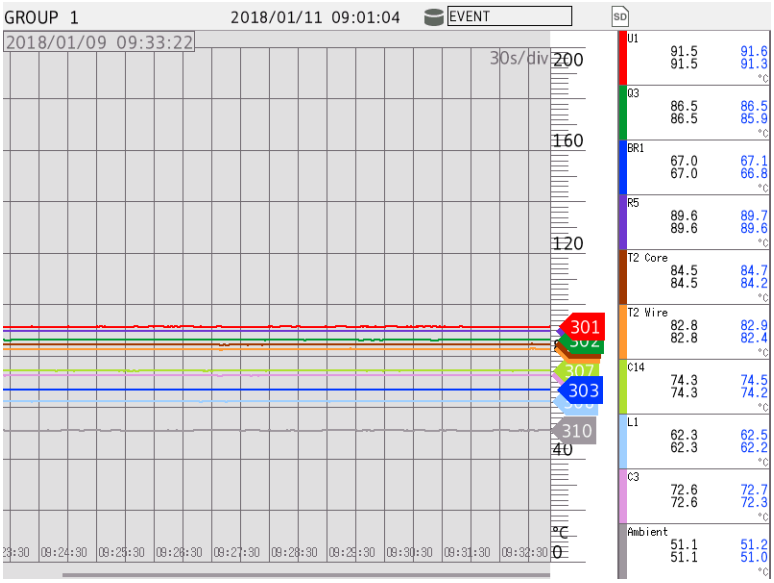
12.6 *Open Case at 15.3 V / 2 A (50°C)*

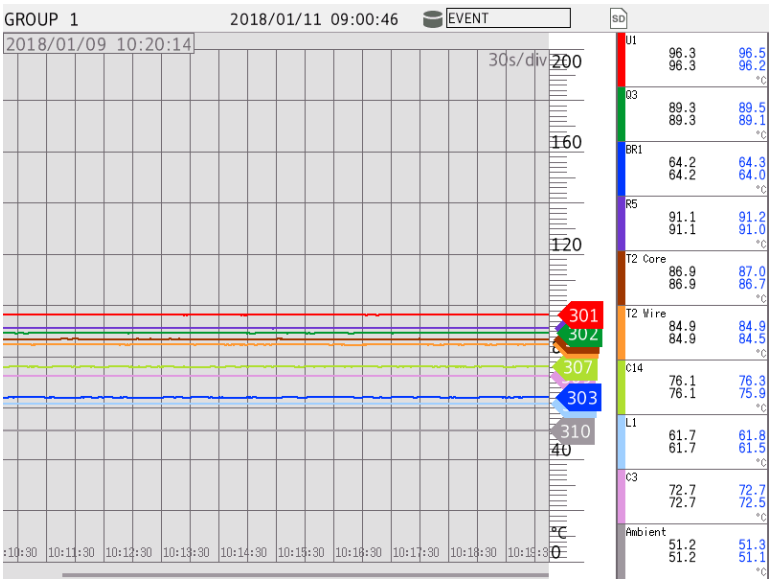
12.6.1 180 VAC @ 50 ºC Ambient

Ambient	INN3268C (U1)	SR FET (Q3)	Transformer (T1)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C14)
51.2	91.6	86.5	84.7	67.1	62.5	72.7	74.5



12.6.2 265 VAC @ 50 ºC Ambient

Ambient	INN3268C (U1)	SR FET (Q3)	Transformer (T1)	Bridge (BR1)	CMC (L1)	Input Capacitor (C3)	Output Capacitor (C14)
51.3	96.5	89.5	87	64.3	61.8	72.7	76.3



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13 Waveforms

13.1 *Load Transient Response (PCB End)*

13.1.1 5.1 V Output

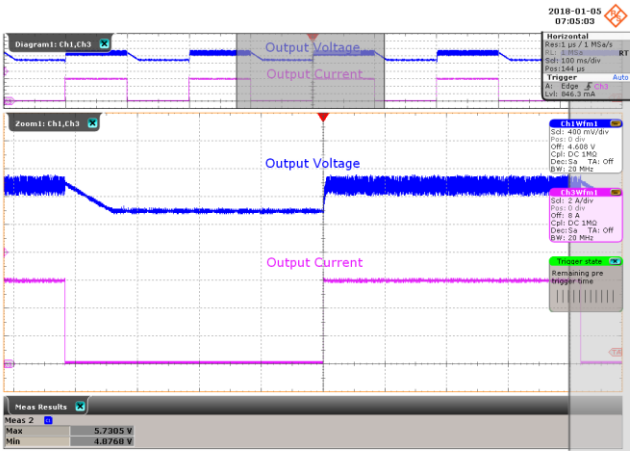

Figure 36 – Transient Response.
180 VAC, 5.1 V, 0 – 6 A Load Step.
V_{MIN}: 4.88 V, V_{MAX}: 5.73 V.
Upper: V_{OUT}, 0.4 V / div., 100 ms / div.
Lower: I_{LOAD}, 2 A / div.

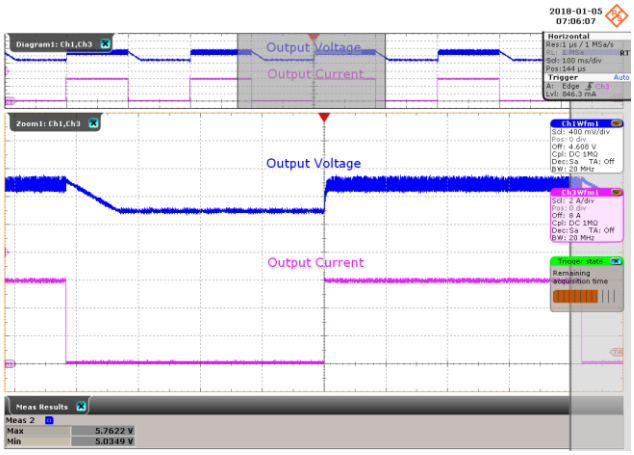

Figure 37 – Transient Response.
265 VAC, 5.1 V, 0 – 6 A Load Step.
V_{MIN}: 5.03 V, V_{MAX}: 5.76 V.
Upper: V_{OUT}, 0.4 V / div., 100 ms / div.
Lower: I_{LOAD}, 2 A / div.

13.1.2 9.2 V Output

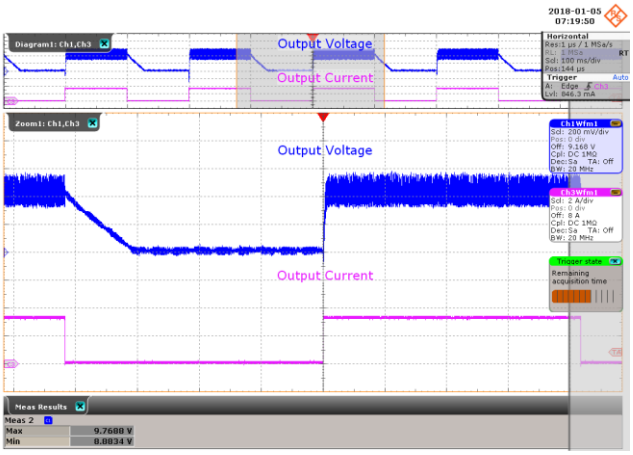

Figure 38 – Transient Response.
180 VAC, 9.2 V, 0 – 3.3 A Load Step.
V_{MIN}: 8.88 V, V_{MAX}: 9.76 V.
Upper: V_{OUT}, .2 V / div., 100 ms / div.
Lower: I_{LOAD}, 2 A / div.

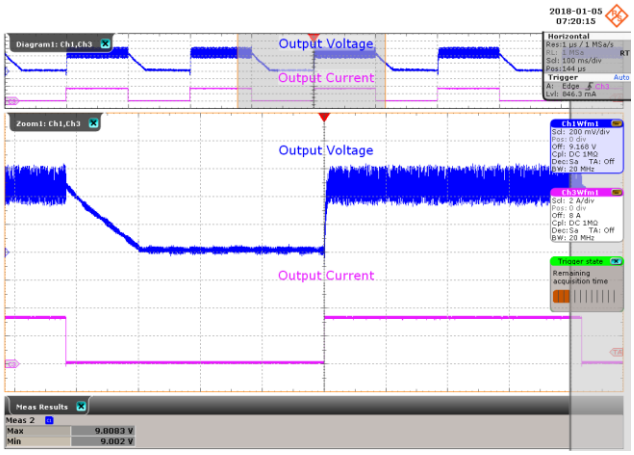

Figure 39 – Transient Response.
265 VAC, 9.2 V, 0 – 3.3 A Load Step.
V_{MIN}: 9.00 V, V_{MAX}: 9.81 V.
Upper: V_{OUT}, .2 V / div., 100 ms / div.
Lower: I_{LOAD}, 2 A / div.

13.1.3 15.3 V Output

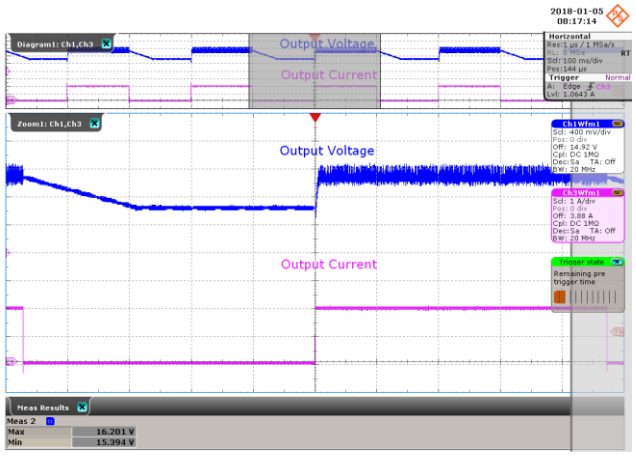

Figure 40 – Transient Response.
180 VAC, 15.3 V, 0 – 2 A Load Step.
V_{MIN}: 15.39 V, V_{MAX}: 16.20 V.
Upper: V_{OUT}, 0.4 V / div., 100 ms / div.
Lower: I_{LOAD}, 1 A / div.

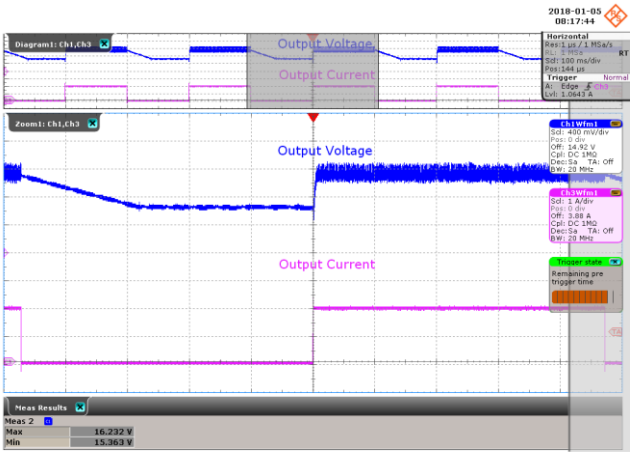

Figure 41 – Transient Response.
265 VAC, 15.3 V, 0 – 2 A Load Step.
V_{MIN}: 15.36 V, V_{MAX}: 16.23 V.
Upper: V_{OUT}, 0.4V / div., 100 ms / div.
Lower: I_{LOAD}, 1 A / div.

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13.2 ***Switching Waveforms***

13.2.1 Drain Voltage and Current (Normal Operation)

13.2.1.1 5 V Output

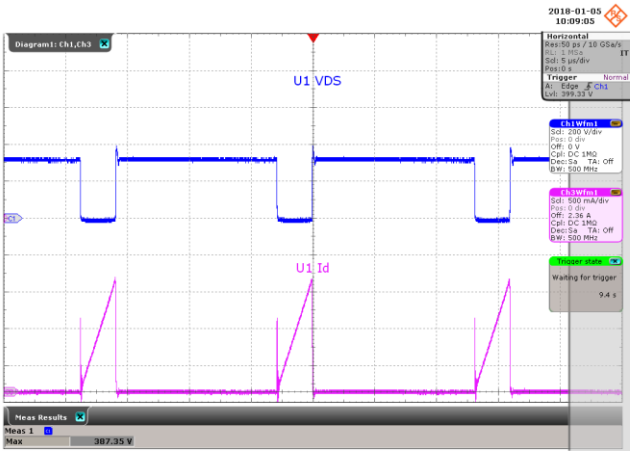

Figure 42 – Drain Voltage and Current Waveforms.
180 VAC, 5.1 V, 6.0 A Load, (387 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 5 µs / div.
Lower: I_{DRAIN}, 0.5 A / div.

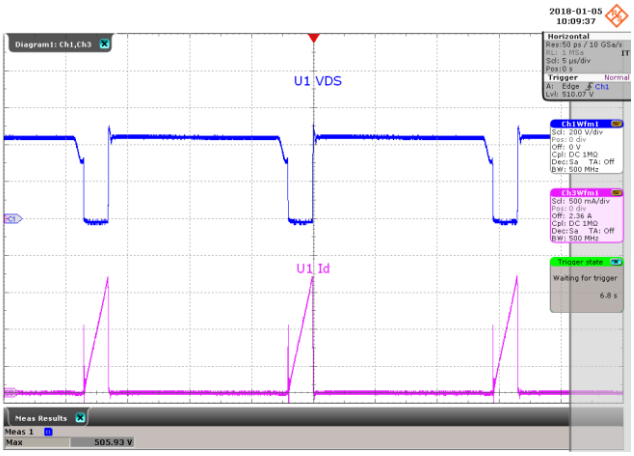

Figure 43 – Drain Voltage and Current Waveforms.
265 VAC, 5.1 V, 6.0 A Load, (506 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 5 µs / div.
Lower: I_{DRAIN}, 0.5 A / div.

13.2.1.2 9 V Output

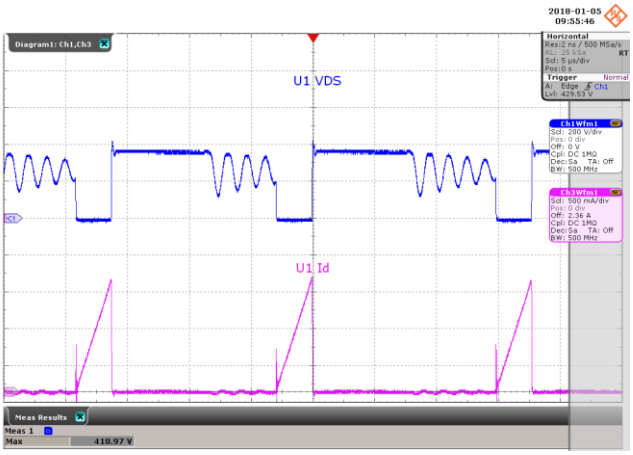

Figure 44 – Drain Voltage and Current Waveforms.
180 VAC, 9.0 V, 3.3 A Load, (419 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 5 µs / div.
Lower: I_{DRAIN}, 0.5 A / div.

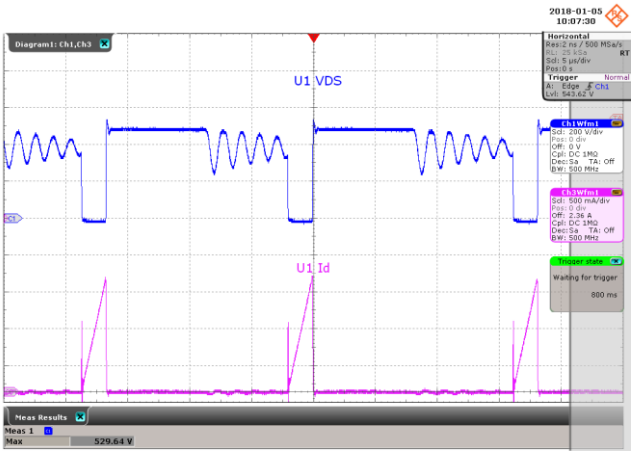

Figure 45 – Drain Voltage and Current Waveforms.
265 VAC, 9.0 V, 3.3 A Load, (530 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 5 µs / div.
Lower: I_{DRAIN}, 0.5 A / div.

13.2.1.3 15 V Output

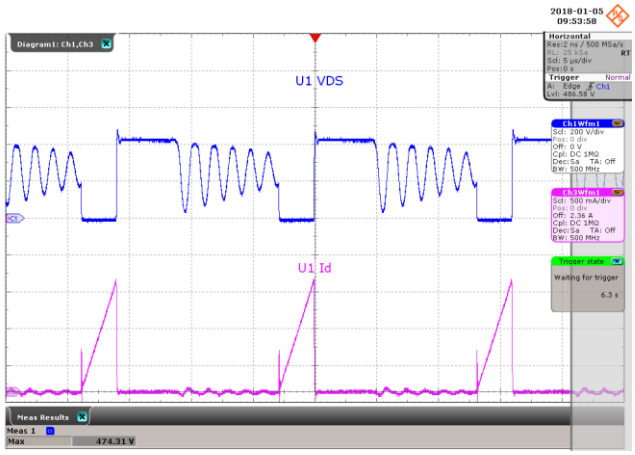

Figure 46 – Drain Voltage and Current Waveforms.
180 VAC, 15.0 V, 2.0 A Load, (474 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 5 μs / div.
Lower: I_{DRAIN}, 0.5 A / div.

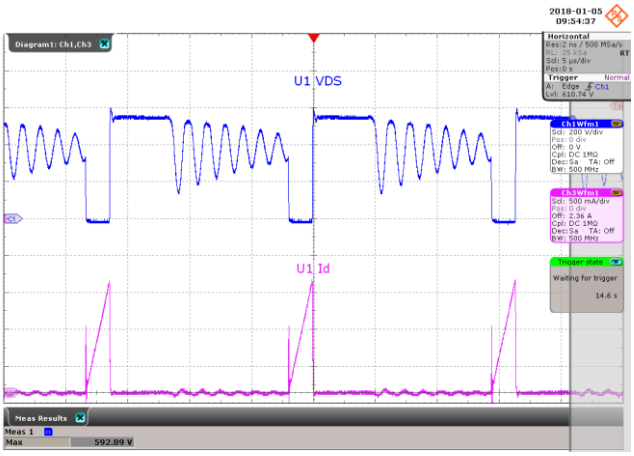

Figure 47 – Drain Voltage and Current Waveforms.
265 VAC, 15.0 V, 2.0 A Load, (593 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 5 μs / div.
Lower: I_{DRAIN}, 0.5 A / div.

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13.2.2 Drain Voltage and Current (Start-up)

13.2.2.1 5 V Output

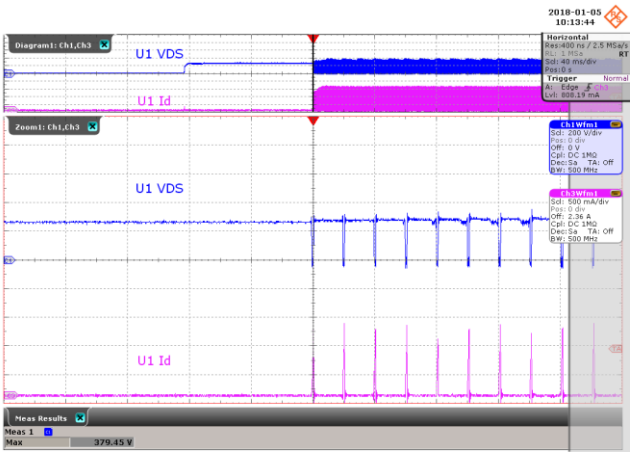

Figure 48 – Drain Voltage and Current Waveforms.
180 VAC, 5.1 V, 6.0 A Load, (379 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 40 ms / div.
Lower: I_{DRAIN}, 0.5 A / div.

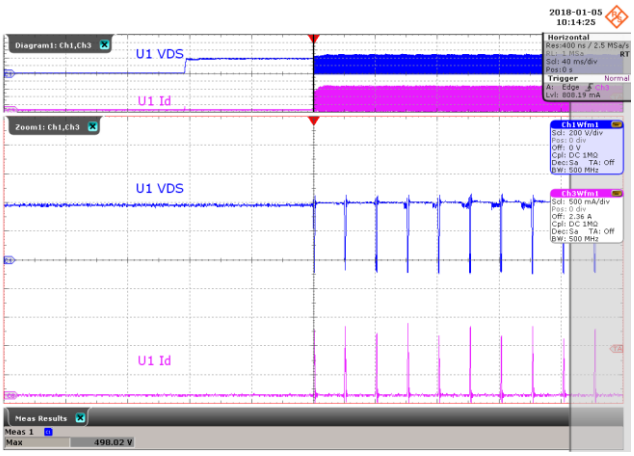

Figure 49 – Drain Voltage and Current Waveforms.
265 VAC, 5.1 V, 6.0 A Load, (498 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 40 ms / div.
Lower: I_{DRAIN}, 0.5 A / div.

13.2.2.2 9 V Output

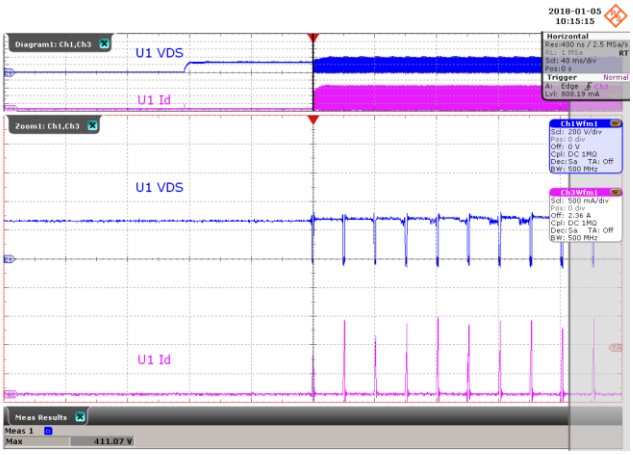

Figure 50 – Drain Voltage and Current Waveforms.
180 VAC, 9.0 V, 3.3 A Load, (411 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 40 ms / div.
Lower: I_{DRAIN}, 0.5 A / div.

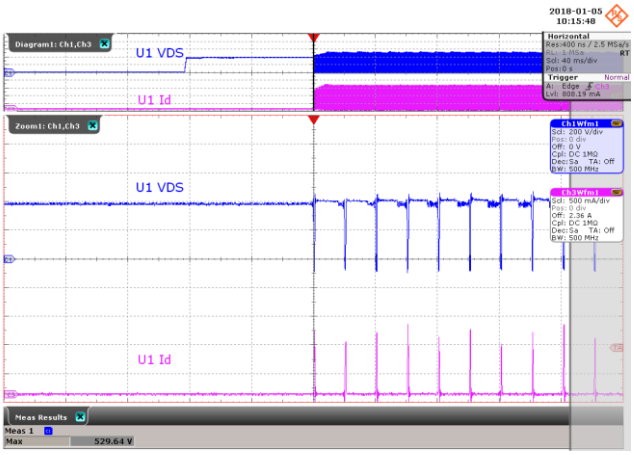

Figure 51 – Drain Voltage and Current Waveforms.
265 VAC, 9.0 V, 3.3 A Load, (530 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 40 ms / div.
Lower: I_{DRAIN}, 0.5 A / div.

13.2.2.3 15 V Output

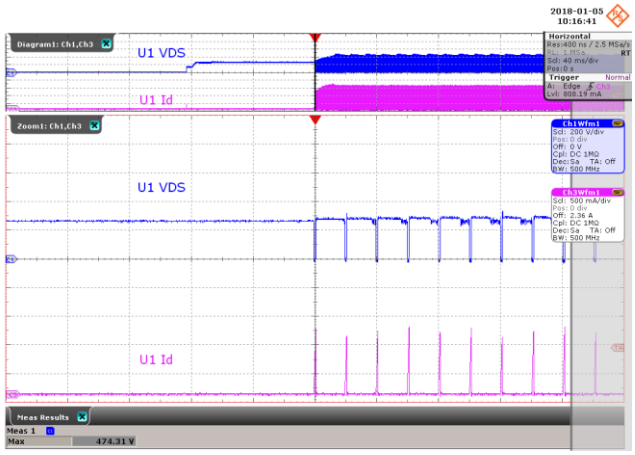

Figure 52 – Drain Voltage and Current Waveforms.
180 VAC, 15.0 V, 2.0 A Load, (474 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 40 ms / div.
Lower: I_{DRAIN}, 0.5 A / div.

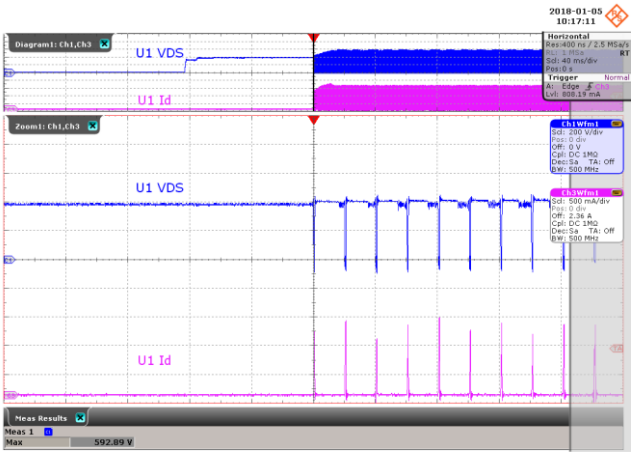

Figure 53 – Drain Voltage and Current Waveforms.
265 VAC, 15.0 V, 2.0 A Load, (593 V_{MAX}).
Upper: V_{DRAIN}, 200 V, 40 ms / div.
Lower: I_{DRAIN}, 0.5 A / div.

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13.2.3 SR MOSFET Voltage

13.2.3.1 5 V Output

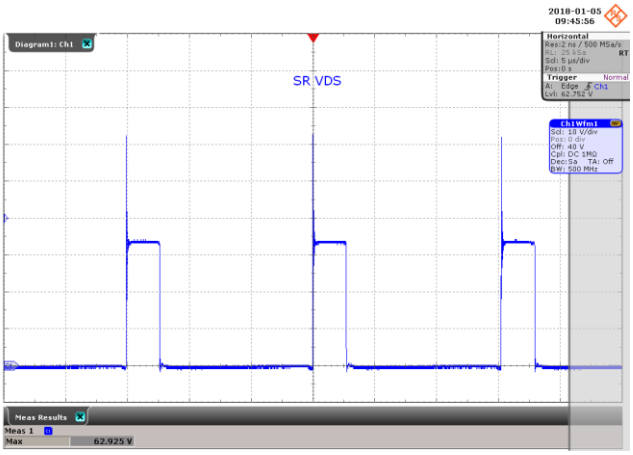

Figure 54 – SR FET Voltage Waveform.
180 VAC, 5.1 V, 6.0 A Load, (62.93 V_{MAX}).
V_{DRAIN}, 10 V, 5 µs / div.

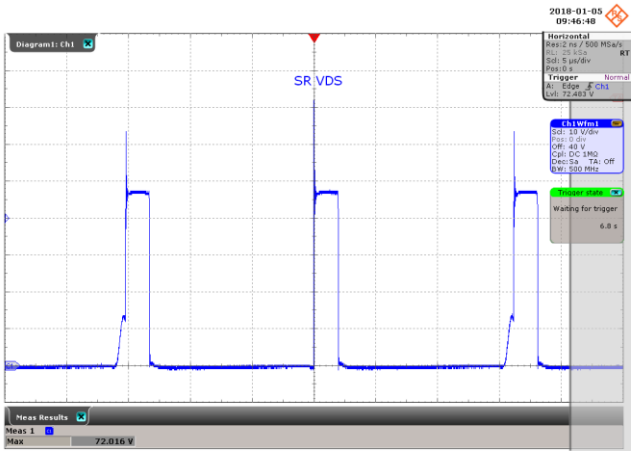

Figure 55 – SR FET Voltage Waveform.
265 VAC, 5.1 V, 6.0 A Load, (72.01 V_{MAX}).
V_{DRAIN}, 10 V, 5 µs / div.

13.2.3.2 9 V Output

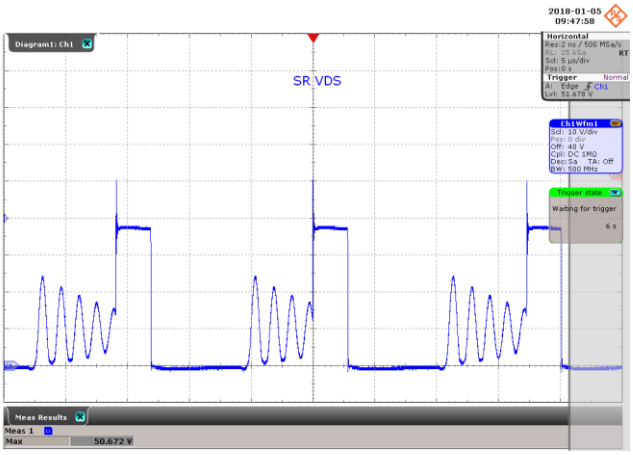

Figure 56 – SR FET Voltage Waveform.
180 VAC, 9.0 V, 3.3 A Load, (50.67 V_{MAX}).
V_{DRAIN}, 10 V, 5 µs / div.

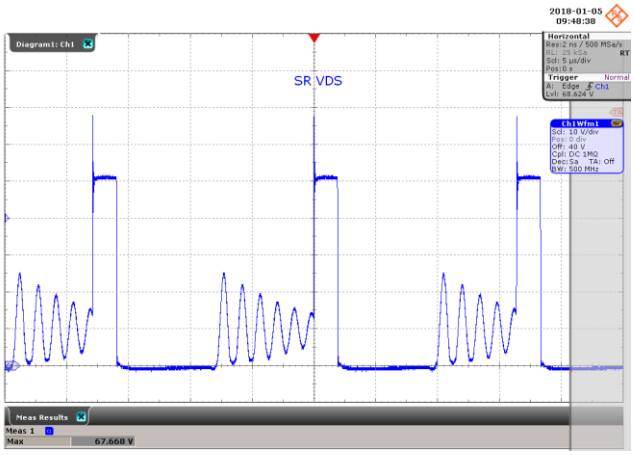

Figure 57 – SR FET Voltage Waveform.
265 VAC, 9.0 V, 3.3 A Load, (67.67 V_{MAX}).
V_{DRAIN}, 10 V, 5 µs / div.

13.2.3.3 15 V Output

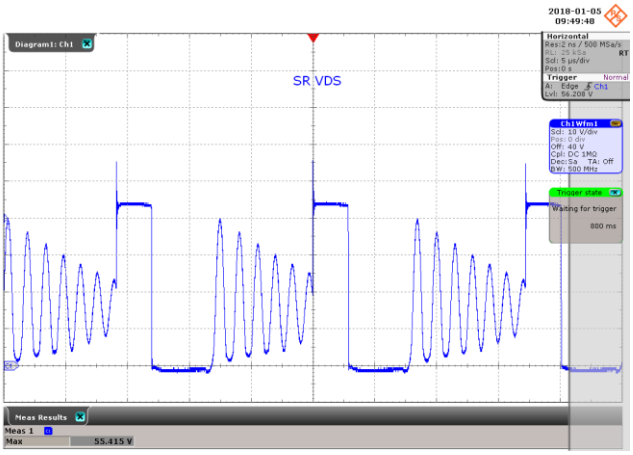

Figure 58 – SR FET Voltage Waveform.
180 VAC, 15.0 V, 2.0 A Load, (55.4 V_{MAX}).
V_{DRAIN}, 10 V, 5 µs / div.

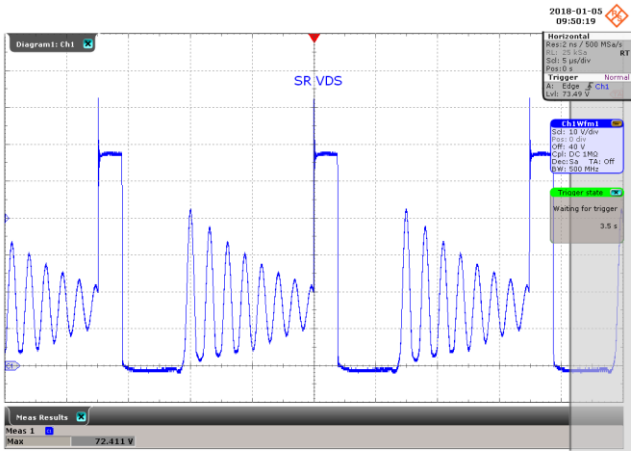

Figure 59 – SR FET Voltage Waveform.
265 VAC, 15.0 V, 2.0 A Load, (72.4 V_{MAX}).
V_{DRAIN}, 10 V, 5 µs / div.

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13.2.4 Output Voltage and Current Start-up (End of 100 mΩ Cable)

13.2.4.1 5 V Output

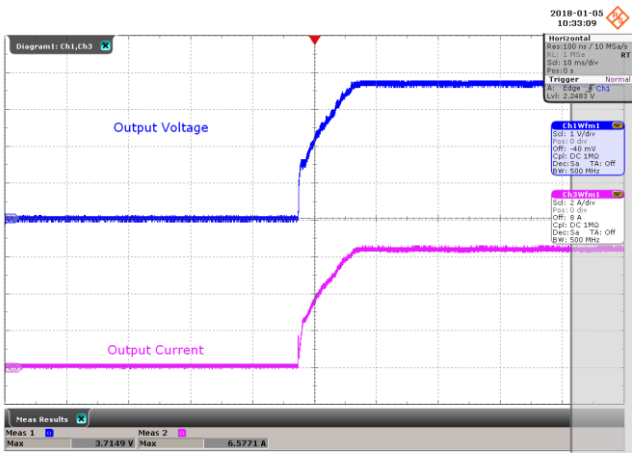

Figure 60 – Output Voltage and Current Waveforms.
180 VAC Input, 5.1 V, 0.85 Ω Load .
Upper: I_{OUT}, 2 A, 10 ms / div.
Lower: V_{OUT}, 1 V / div.

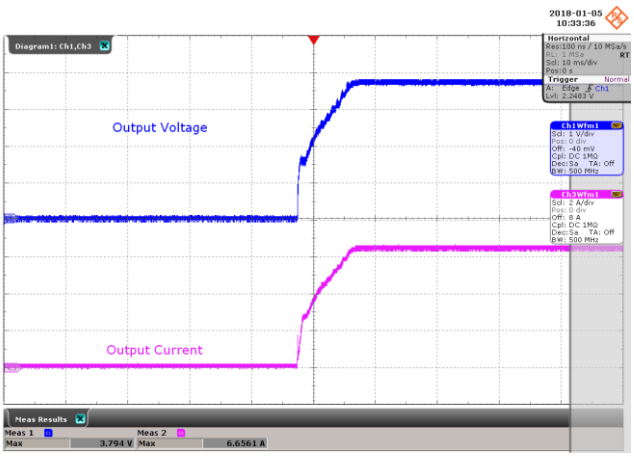

Figure 61 – Output Voltage and Current Waveforms.
265 VAC Input, 5.1 V, 0.85 Ω Load.
Upper: I_{OUT}, 2 A, 10 ms / div.
Lower: V_{OUT}, 1 V / div.

13.2.4.2 9 V Output

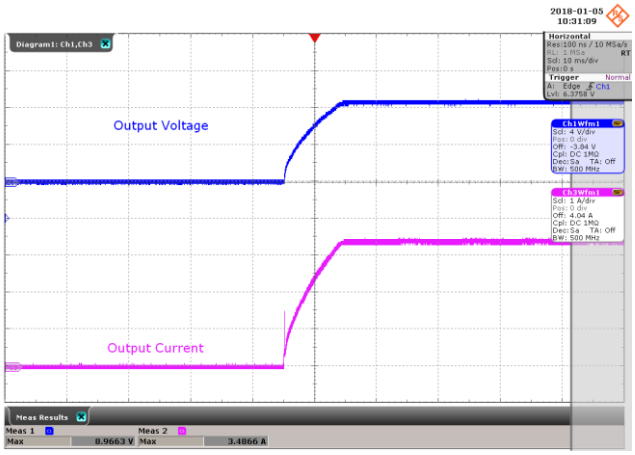

Figure 62 – Output Voltage and Current Waveforms.
180 VAC Input, 9 V, 2.75 Ω Load .
Upper: I_{OUT}, 1 A, 10 ms / div.
Lower: V_{OUT}, 4 V / div.

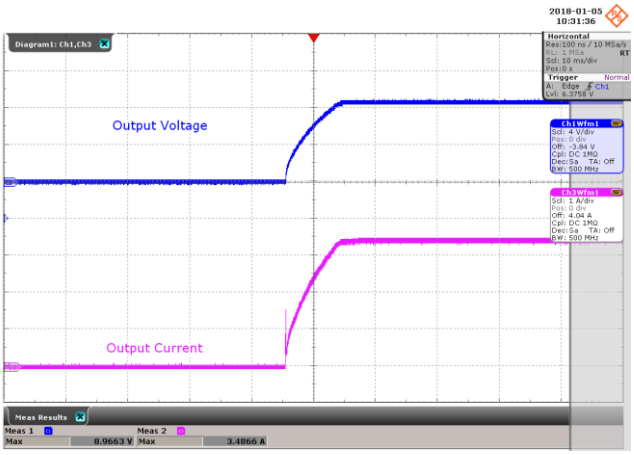

Figure 63 – Output Voltage and Current Waveforms.
265 VAC Input, 9 V, 2.75 Ω Load.
Upper: I_{OUT}, 1 A, 10 ms / div.
Lower: V_{OUT}, 4 V / div.

13.2.4.3 15 V Output

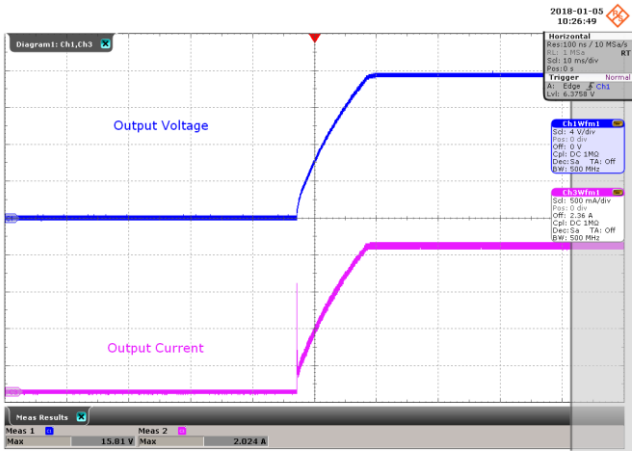

Figure 64 – Output Voltage and Current Waveforms.
180 VAC Input, 15 V, 7.5 Ω Load.
Upper: I_{OUT}, 0.5 A, 10 ms / div.
Lower: V_{OUT}, 4 V / div.

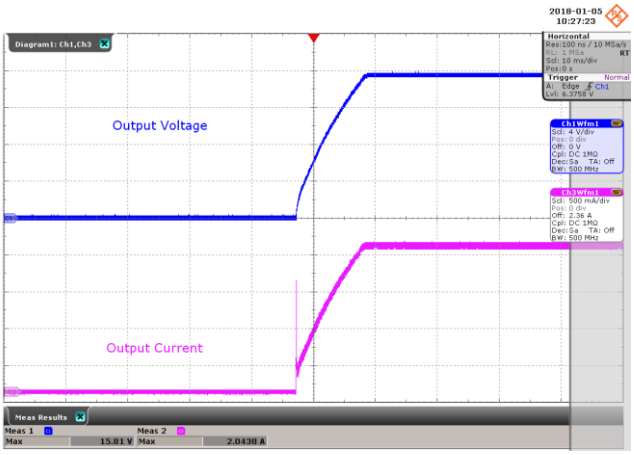

Figure 65 – Output Voltage and Current Waveforms.
265 VAC Input, 15 V, 7.5 Ω Load.
Upper: I_{OUT}, 0.5 A, 10 ms / div.
Lower: V_{OUT}, 4 V / div.

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13.3 ***Output Ripple Measurements***

13.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below). Ripple measurement done at the end of a 100mΩ cable.

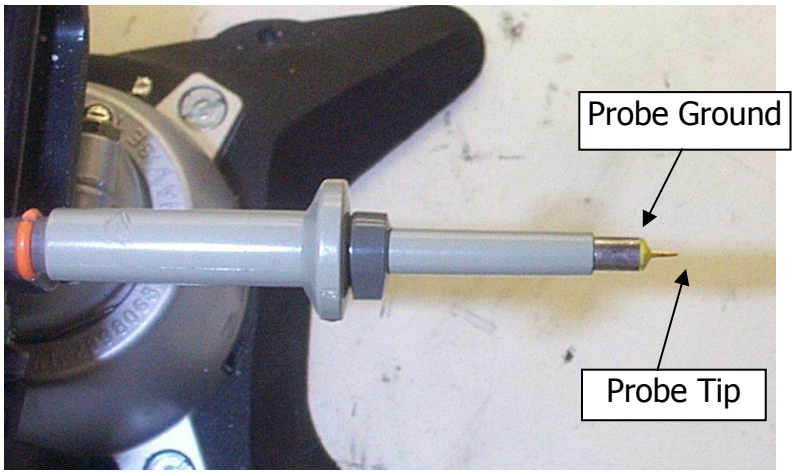

Figure 66 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

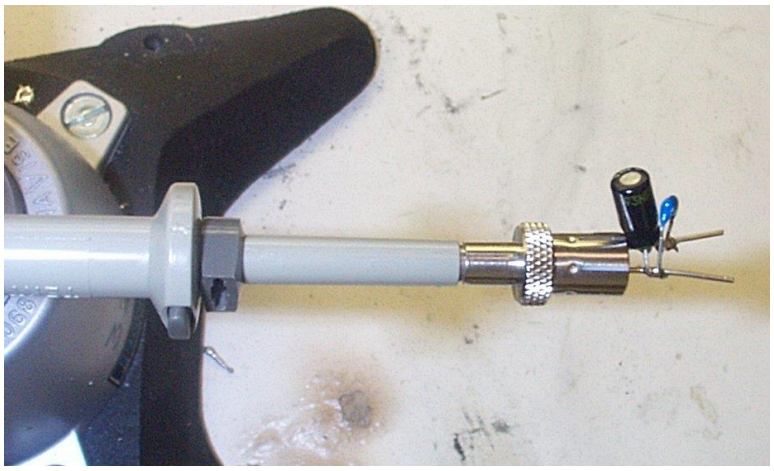

Figure 67 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

13.3.1.1 5 V Output

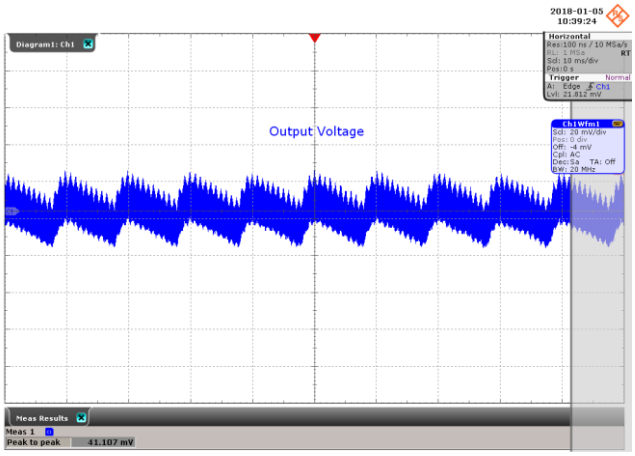

Figure 68 – Output Ripple.
180 VAC Input 5.1 V, 6.0 A Load.
V_{OUT}, 20 mV / div., 10 ms / div.

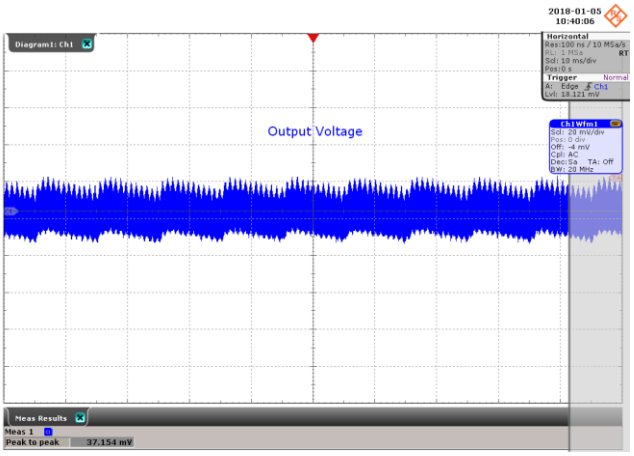

Figure 69 – Output Ripple.
265 VAC Input 5.1 V, 6.0 A Load.
V_{OUT}, 20 mV / div., 10 ms / div.

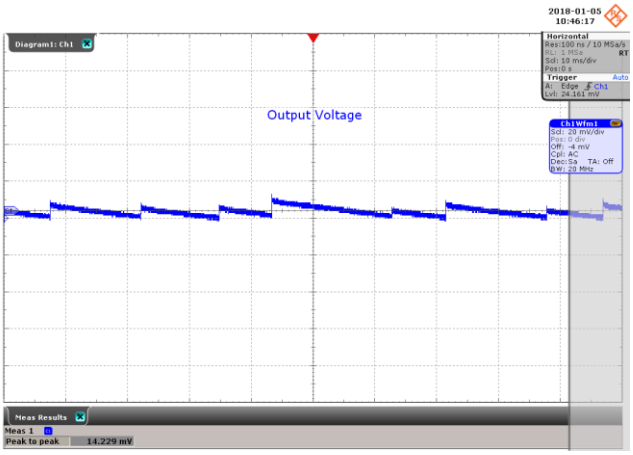

Figure 70 – Output Ripple.
180 VAC Input 5.1 V, 0 A Load.
V_{OUT}, 20 mV / div., 10 ms / div.

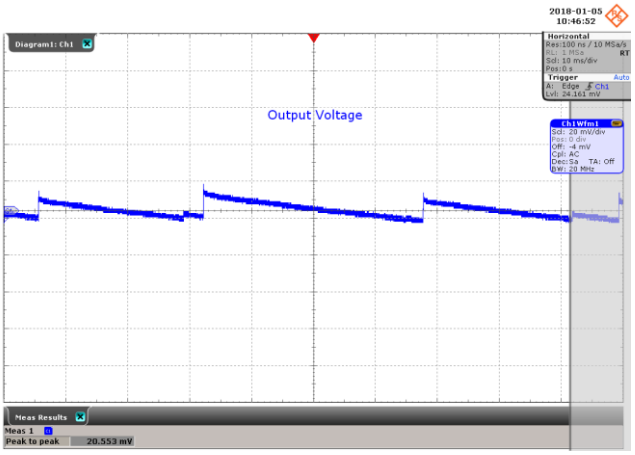

Figure 71 – Output Ripple.
265 VAC Input 5.1 V, 0 A Load.
V_{OUT}, 20 mV / div., 10 ms / div.

Input (VAC)	Full Load (mV)	No-Load (mV)
180	41.1	14.2
265	37.1	20.5

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13.3.1.2 9 V Output

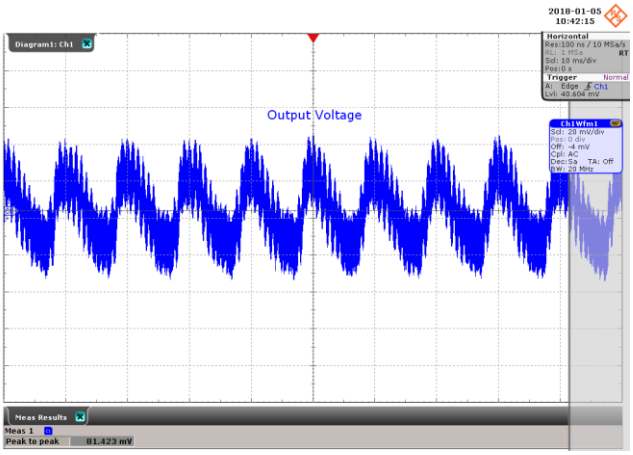

Figure 72 – Output Ripple.
180 VAC Input, 9.0 V, 3.3 A Load.
V_{OUT}, 20 mV / div., 10 ms / div.

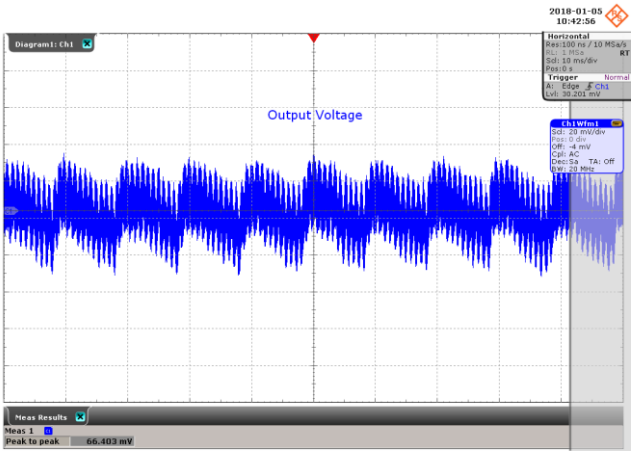

Figure 73 – Output Ripple.
265 VAC Input 9.0 V, 3.3 A Load.
V_{OUT}, 20 mV / div., 10 ms / div.

13.3.1.3 15 V Output

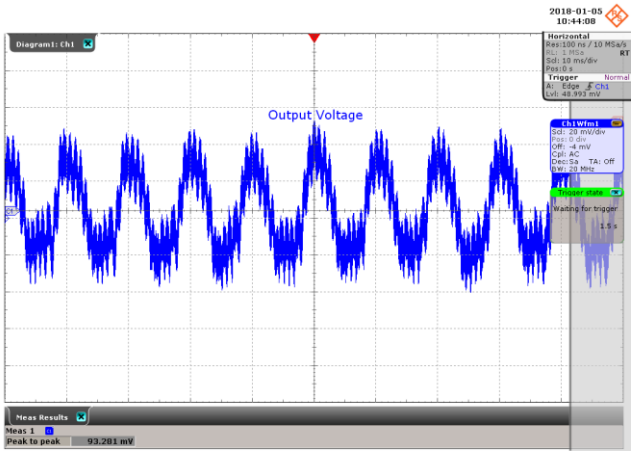

Figure 74 – Output Ripple.
180 VAC Input, 15.0 V, 2.0 A Load.
V_{OUT}, 20 mV / div., 10 ms / div.

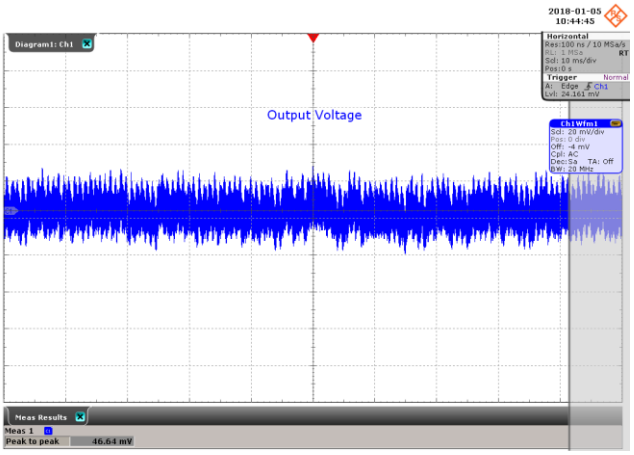

Figure 75 – Output Ripple.
265 VAC Input 15.0 V, 2.0 A Load.
V_{OUT}, 20 mV / div., 10 ms / div.

Input (VAC)	9V (mV)	15V (mV)
180	81.4	93.2
265	66.4	46.6

14 Conducted EMI

14.1 *Test Set-up*

14.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power hitester.
4. Chroma measurement test fixture, model A662003.
5. Resistor load with input voltage set at 230 VAC.

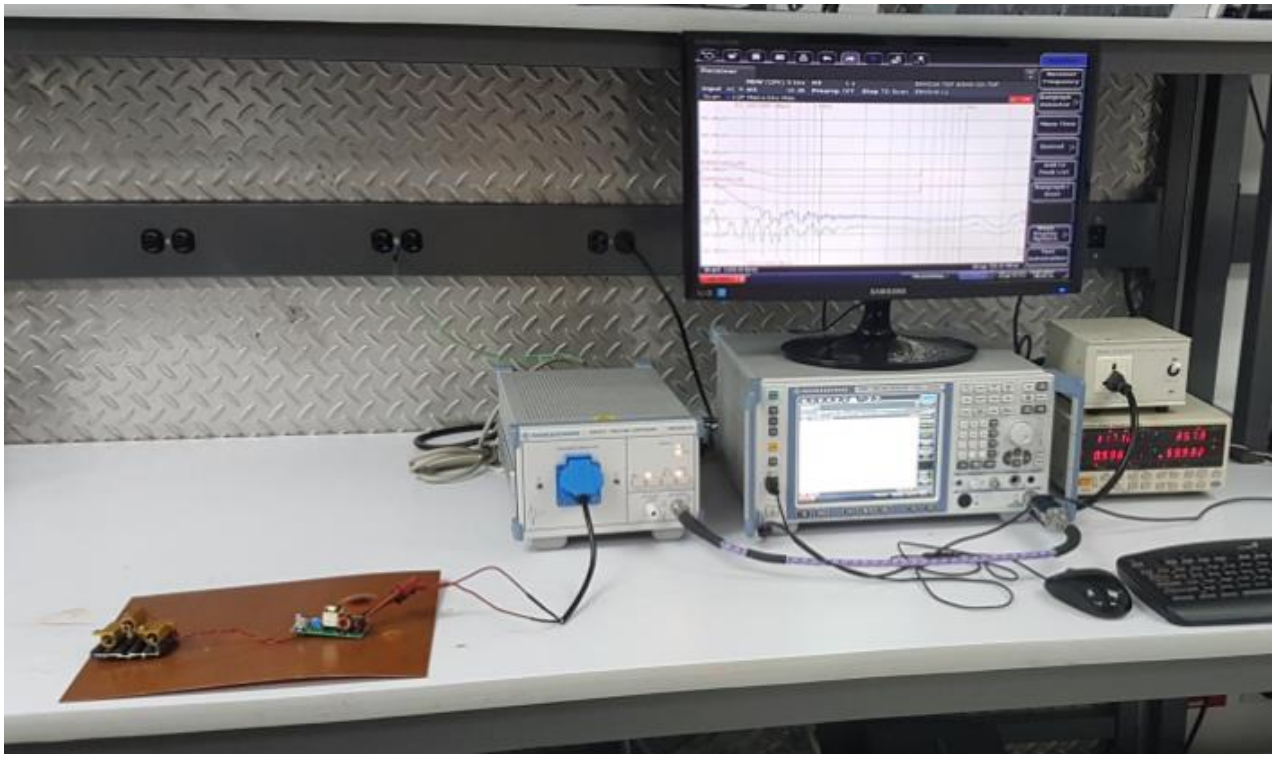

Figure 76 – Conducted EMI Test Set-up.

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14.2 *EMI Test Result*

14.2.1 Floating Output

14.2.1.1 Output 5.1 V / 6 A

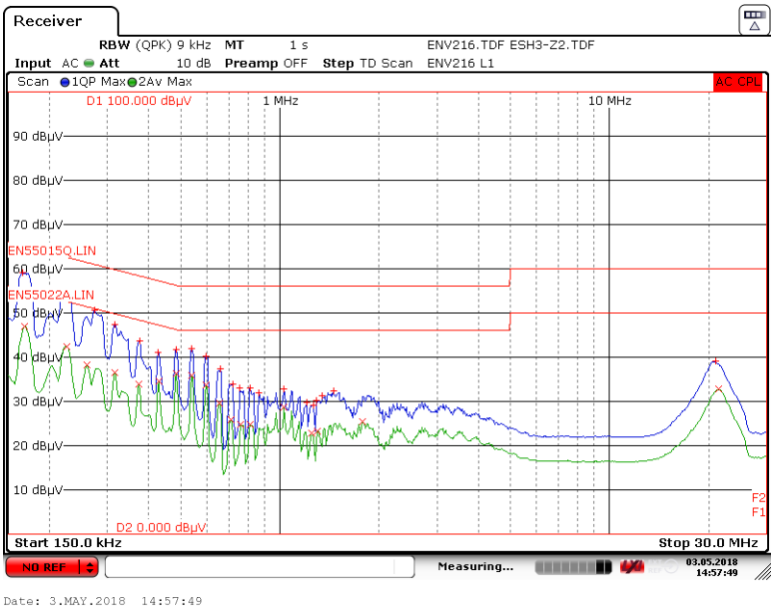

Figure 77 – Conducted EMI, 5.1 V / 6 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

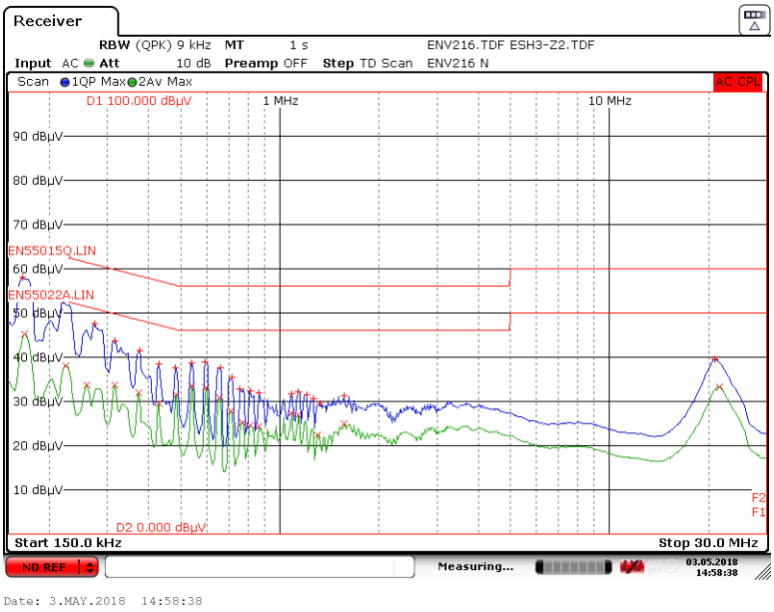

Figure 78 – Conducted EMI, 5.1 V / 6 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

14.2.1.2 Output 9 V / 3.3 A

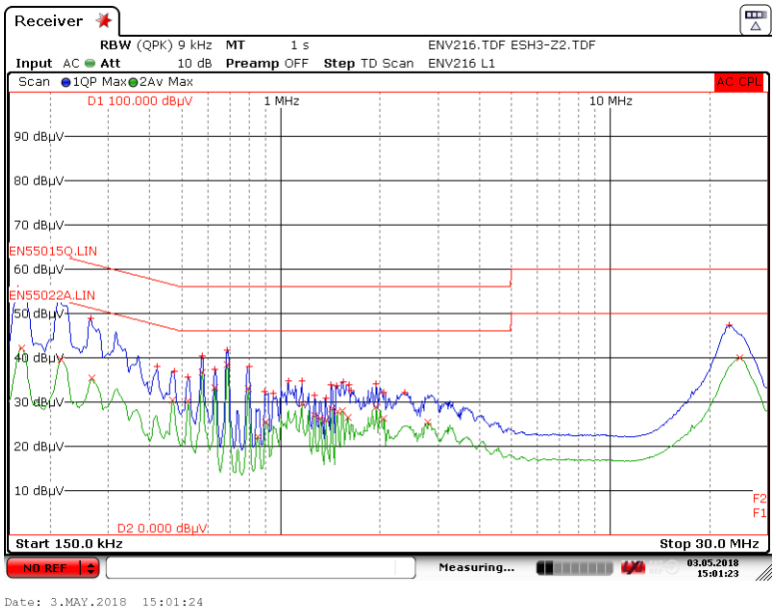

Figure 79 – Conducted EMI, 9 V / 3.3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

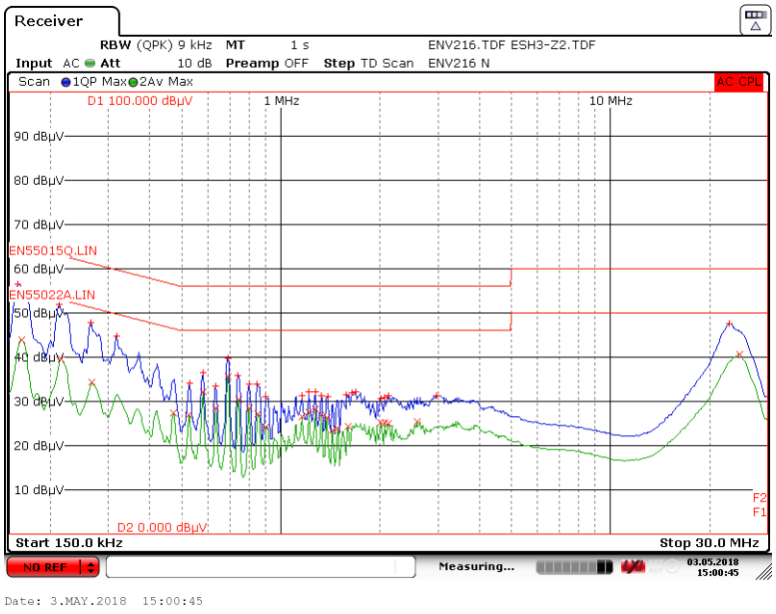

Figure 80 – Conducted EMI, 9 V / 3.3 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

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14.2.1.3 Output 15 V / 2 A

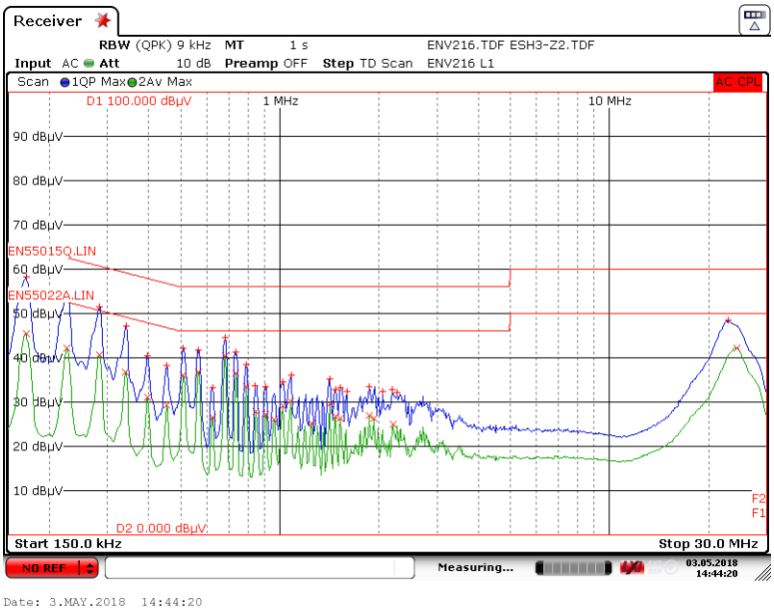

Figure 81 – Conducted EMI, 15 V / 2 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line).

Trace1: EN55015Q.LIN Trace2: EN55022A.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	681.0000 kHz	40.45 L1	-5.55 dB
1 Quasi Peak	170.2500 kHz	58.33 L1	-6.62 dB
2 Average	24.2948 MHz	42.22 L1	-7.78 dB
1 Quasi Peak	226.5000 kHz	54.57 L1	-8.01 dB
2 Average	566.2500 kHz	36.79 L1	-9.21 dB
1 Quasi Peak	282.7500 kHz	51.46 L1	-9.27 dB
2 Average	735.0000 kHz	36.47 L1	-9.53 dB
2 Average	170.2500 kHz	45.38 L1	-9.57 dB
2 Average	510.0000 kHz	36.14 L1	-9.86 dB
2 Average	282.7500 kHz	40.75 L1	-9.98 dB
2 Average	226.5000 kHz	42.08 L1	-10.50 dB
1 Quasi Peak	681.0000 kHz	44.53 L1	-11.47 dB
1 Quasi Peak	22.9133 MHz	48.42 L1	-11.58 dB
1 Quasi Peak	341.2500 kHz	47.13 L1	-12.04 dB

Figure 82 – Conducted EMI, 15 V / 2 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Line, Delta Limit).

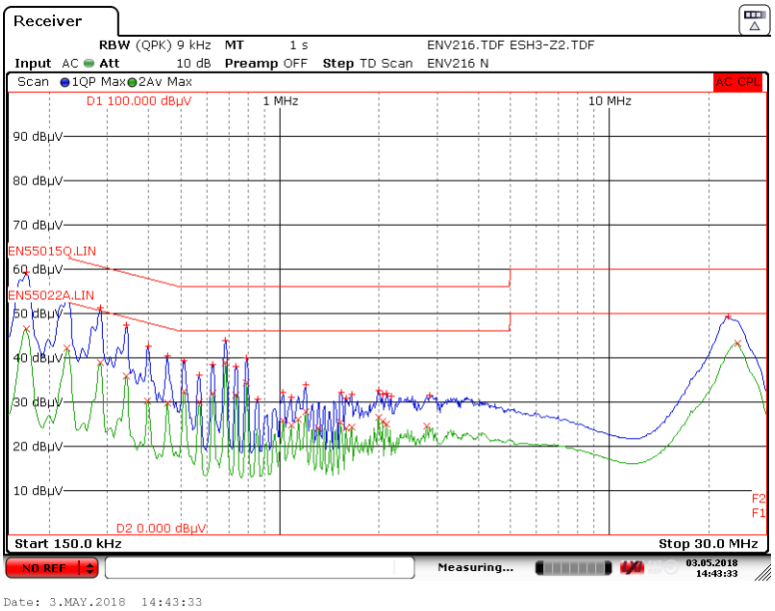

Figure 83 – Conducted EMI, 15 V / 2 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral).

Trace1: EN55015Q.LIN Trace2: EN55022A.LIN

Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	170.2500 kHz	59.33 N	-5.62 dB
2 Average	24.5153 MHz	43.24 N	-6.76 dB
2 Average	683.2500 kHz	38.97 N	-7.03 dB
1 Quasi Peak	226.5000 kHz	54.49 N	-8.09 dB
2 Average	170.2500 kHz	46.57 N	-8.38 dB
1 Quasi Peak	285.0000 kHz	51.30 N	-9.37 dB
2 Average	226.5000 kHz	42.13 N	-10.45 dB
1 Quasi Peak	22.9493 MHz	49.31 N	-10.69 dB
2 Average	285.0000 kHz	38.94 N	-11.73 dB
2 Average	793.5000 kHz	34.24 N	-11.76 dB
1 Quasi Peak	341.2500 kHz	47.41 N	-11.76 dB
1 Quasi Peak	683.2500 kHz	43.82 N	-12.18 dB
2 Average	341.2500 kHz	35.88 N	-13.29 dB
2 Average	512.2500 kHz	32.32 N	-13.68 dB

Figure 84 – Conducted EMI, 15 V / 2 A Load 230 VAC, 60 Hz, and EN55022 B Limits (Neutral, Delta Limit).

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15 ESD Test

Passed ±8 kV contact test.

Contact Voltage (kV)	Applied to	Number of Strikes	Test Result
8	5V	10	PASS
-8	5V	10	PASS
8	9V	10	PASS
-8	9V	10	PASS
8	15V	10	PASS
-8	15V	10	PASS

Passed ±15 kV air test.

Differential Voltage (kV)	Applied to	Number of Strikes	Test Result
15	5V	10	PASS
-15	5V	10	PASS
15	9V	10	PASS
-15	9V	10	PASS
15	15V	10	PASS
-15	15V	10	PASS

16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
23-Jan-17	IB/AO	1.0	Initial Release.	Apps & Mktg
29-May-18	MAGM	1.1	Update in Transformer and Choke.	Apps & Mktg
16-Jul-20	JPB	1.2	Added Test Points to BOM. Added L1 and T1 Supplier. Converted to RDR.	Apps & Mktg

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