Title	***Reference Design Report for a 65 W Power Supply Using InnoSwitch™3-EP PowiGaN™ INN3679C-H606***
Specification	90 VAC – 265 VAC Input; 20 V / 3.25 A Output
Application	Adapter
Author	Applications Engineering Department
Document Number	RDR-747
Date	June 23, 2020
Revision	1.1

Summary and Features

- InnoSwitch3-EP is industry first AC/DC IC with isolated, safety rated integrated feedback
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Built-in synchronous rectification for high efficiency
- Meets DOE6 and CoC Tier 2 V5 2016
- <40 mW no-load input power
- Primary sensed overvoltage protection
- Very low component count: 43 components
- >6db margin on conducted EMI
- Very high average efficiency
  - 92.5% at 115 VAC and 230 VAC
- Very high full-load efficiency
  - 92.0% at 115 VAC and 93.5% at 230 VAC

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a 20 V / 3.25 A output charger using the InnoSwitch3-EP. This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-EP controller providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

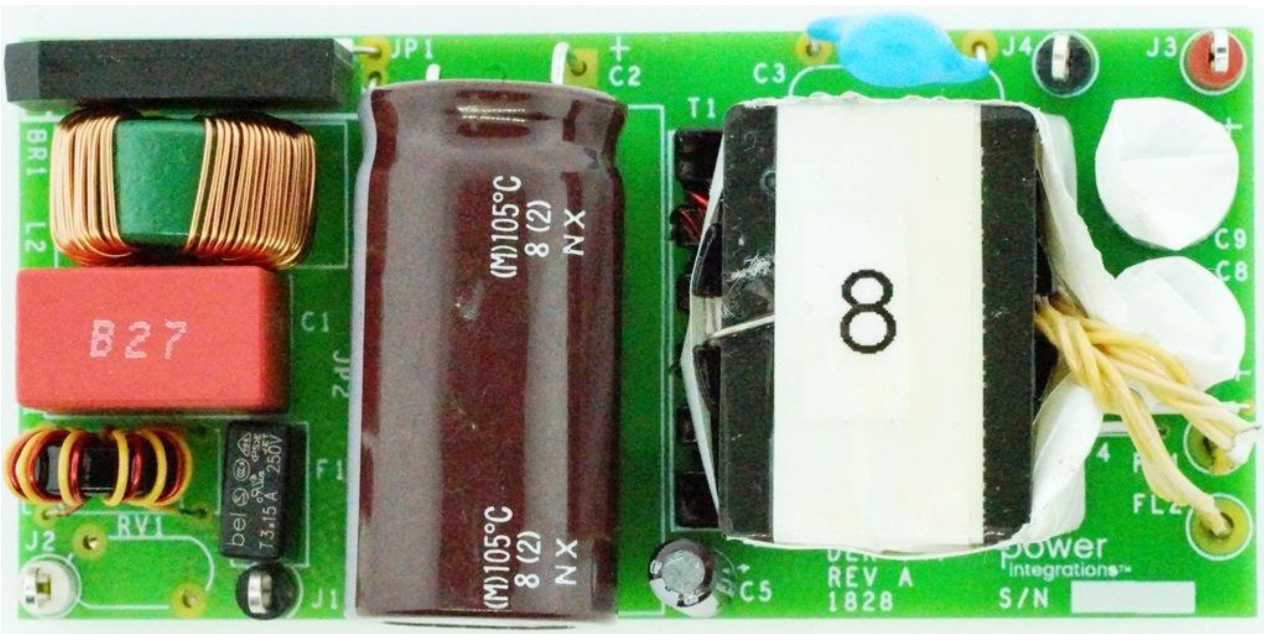

Figure 1 – Populated Circuit Board Photograph, Top.

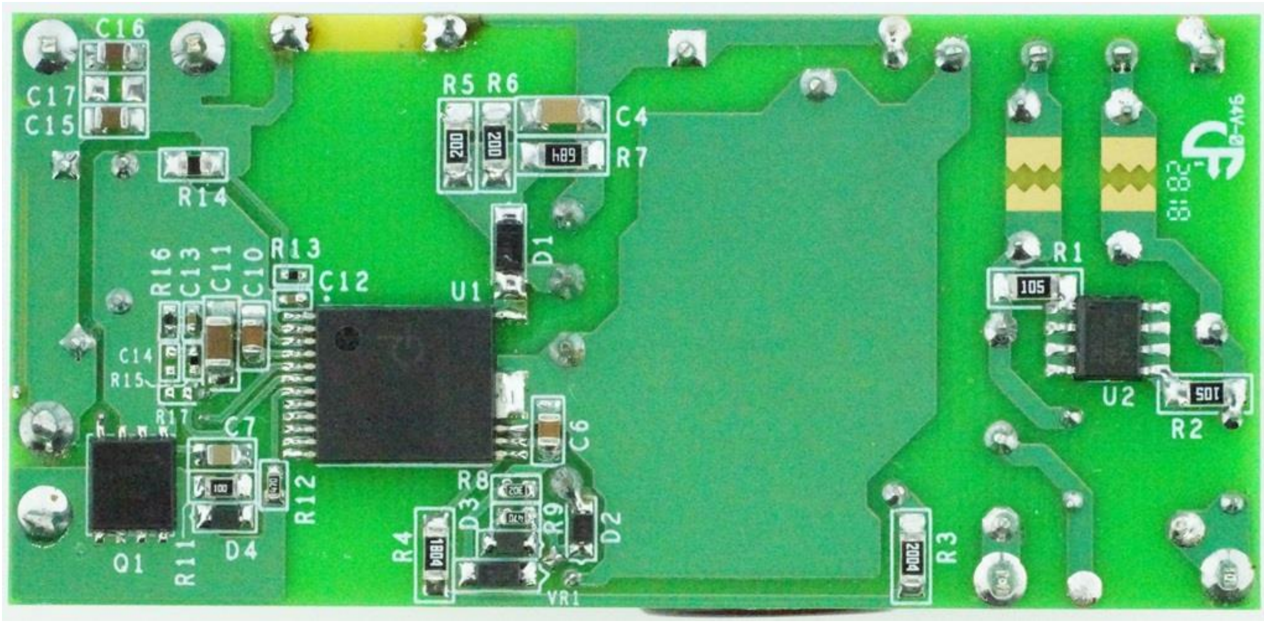

Figure 2 – Populated Circuit Board Photograph, Bottom.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the result section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				40	mW	Measured at 230 VAC.
20 V Output						
Output Voltage	V_{OUT1}		20		V	±5%
Output Ripple Voltage	$V_{RIPPLE1}$			450	mV	On Board.
Output Current	I_{OUT1}	3.25			A	On Board.
Continuous Output Power	P_{OUT}			65	W	
Conducted EMI						Meets CISPR22B / EN55022B
Safety						Designed to meet IEC60950 / UL1950 Class II
Ambient Temperature	T_{AMB}	0		40	°C	Enclosed in Adapter, Sea Level.

3 Schematic

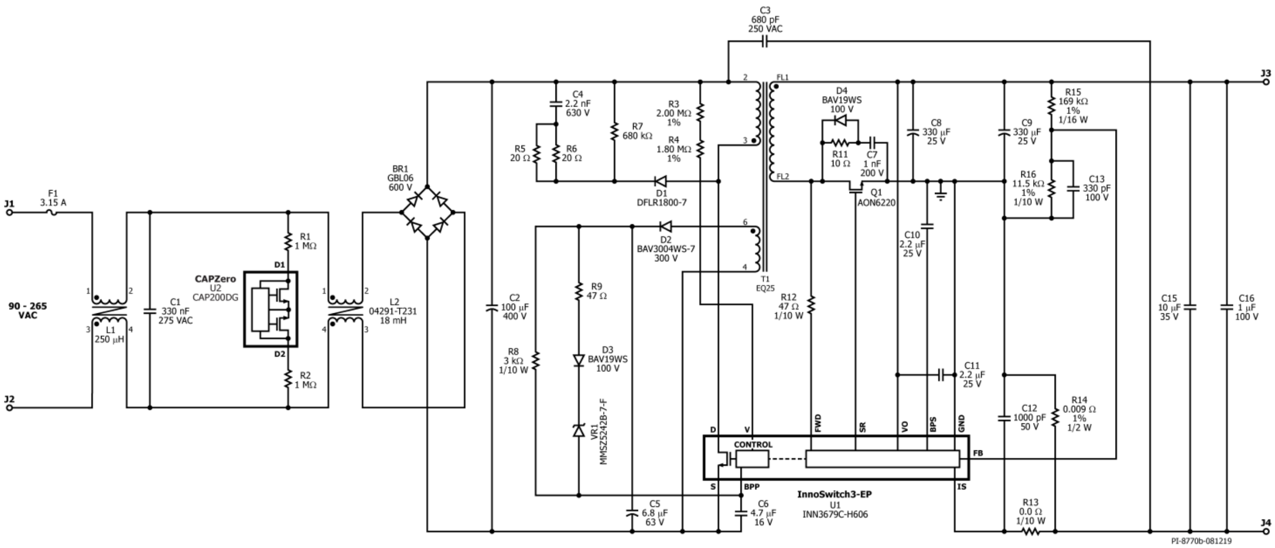

Figure 3 – Power Stage Schematic.

4 Circuit Description

4.1 *Input EMI Filtering*

Fuse F1 isolates the circuit and provides protection from component failure, and the common mode choke L1 and L2 with capacitor C1 attenuation for EMI. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter capacitor C2. Capacitor C3 is used to mitigate the common mode EMI.

Resistors R1 and R2 along with U2 discharges capacitor C1 when the power supply is disconnected from AC mains.

4.2 InnoSwitch3-EP IC Primary

One end of the transformer (T1) primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch3-EP IC (U1). Resistors R3 and R4 provide Input voltage sense protection for under voltage and over voltage conditions.

A low cost RCD clamp formed by diode D1, resistors R5, R6, and R7, and capacitor C4 limits the peak drain voltage of U1 at the instant of turn off of the switch inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C6) when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. Resistor R8 limits the current being supplied to the BPP pin of the InnoSwitch3-EP IC (U1).

Zener diode VR1 along with R9 and D3 offers primary sensed output over voltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of over voltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR1 which then causes a current to flow into the BPP pin of InnoSwitch3-EP IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch3-EP controller will latch off and prevent any further increase in output voltage.

4.3 InnoSwitch3-EP IC Secondary

The secondary side of the InnoSwitch3-EP IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by MOSFET Q1 and filtered by capacitors C8 and C9. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RCD snubber R11, C7 and D4. Diode D4 was used to minimize the dissipation in resistor R11.

The gate of Q1 is turned on by secondary side controller inside IC U1, based on the winding voltage sensed via resistor R12 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the MOSFET is turned off just prior to the secondary side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold of approximately 3 mV. Secondary side control of the primary side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectification.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C10 connected to the BPS pin of InnoSwitch3-EP IC U1 provides decoupling for the internal circuitry. Capacitor C11 provides decoupling for the VO pin.

Output current is sensed by monitoring the voltage drop across resistor R14 between the IS and GND pins with a threshold of approximately 35 mV to reduce losses. C12 provides filtering on the IS pin from external noise.

Below the CC threshold, the device operates in constant voltage mode. During constant voltage mode operation, output voltage regulation is achieved through sensing the output voltage via divider resistors R15 and R16. The voltage across R16 is fed into the FB pin with an internal reference voltage threshold of 1.265 V. Output voltage is regulated so as to achieve a voltage of 1.265 V on the FB pin. Capacitor C13 provides noise filtering of the signal at the FB pin.

The capacitors C15 and C17 are used to reduce the high frequency output voltage ripple.

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5 PCB Layout

PCB copper thickness is 2.0 oz.

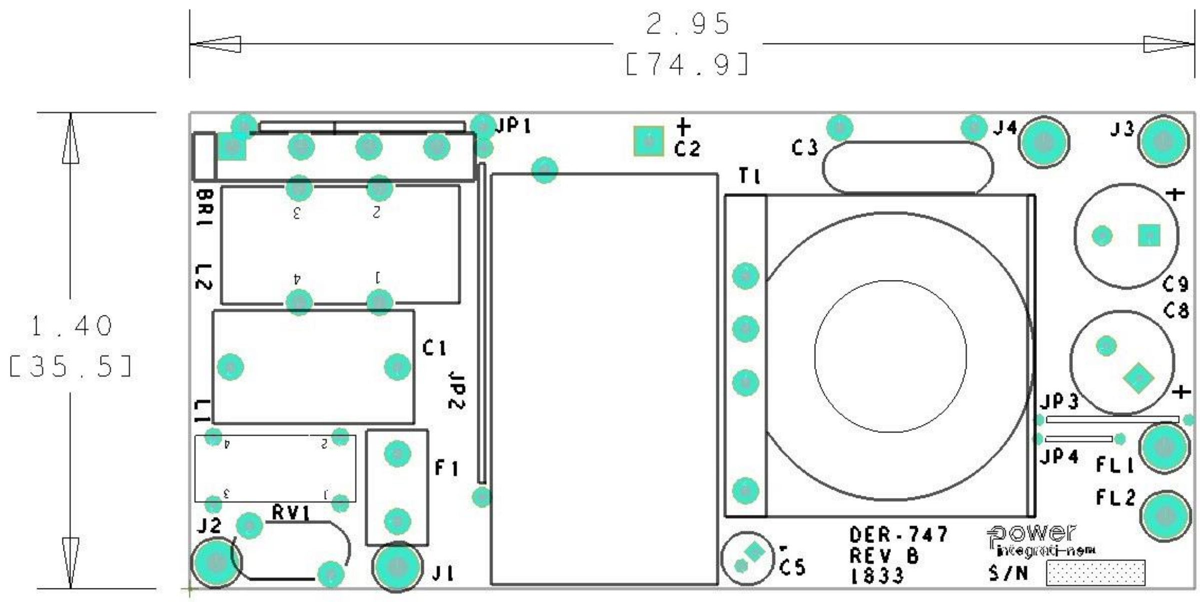

Figure 4 – Printed Circuit Layout, Top.

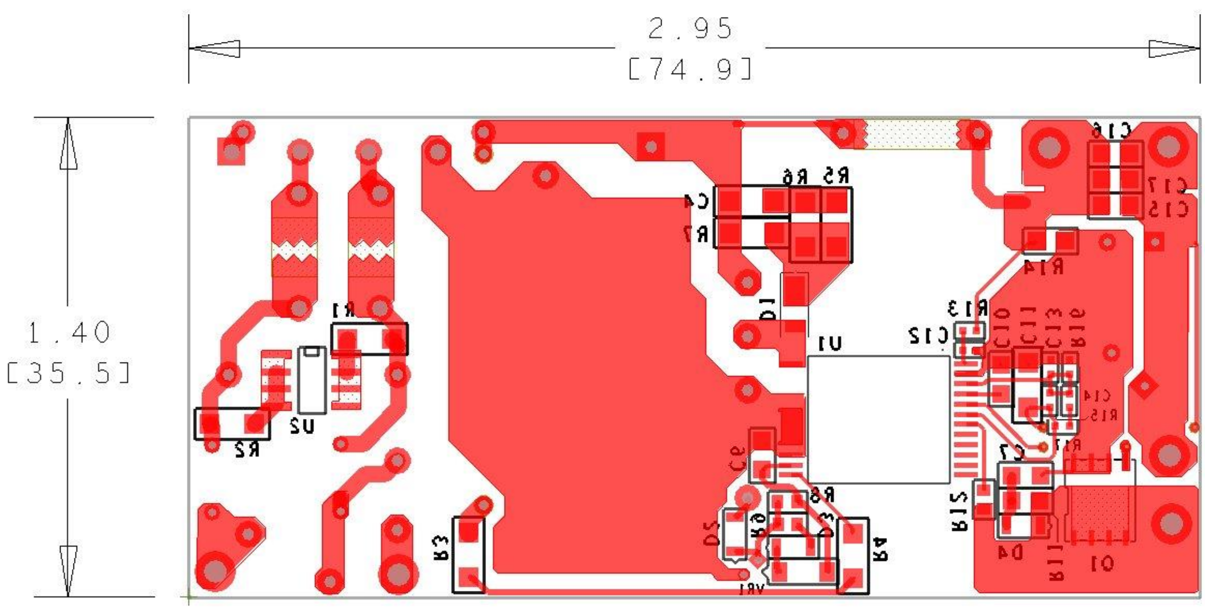

Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	DIODE BRIDGE 600 V 4A GB	GBL06	Genesic Semi
2	1	C1	330 nF, ±10%, 275 VAC, Film, X2, 15.00 mm x 8.50 mm	890324024003CS	Wurth
3	1	C2	100 μF, 400 V, Electrolytic, Low ESR, (16 x 30)	EPAG401ELL101ML30S	Nippon Chemi-Con
4	1	C3	470 pF, 250 VAC, Film, X1Y1	DE1B3KX471KN4AN01F	Murata
5	1	C4	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K	TDK
6	1	C5	6.8 μF, ±20%, 63 V, Electrolytic, (4 mm x 11 mm)	UPW1J6R8MDD6	Nichicon
7	1	C6	4.7 μF, 16 V, Ceramic, X7R, 0805	CL21B475KOFNNNE	Samsung
8	1	C7	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
9	2	C8 C9	330 μF,±20%, 25 V, Al Organic Polymer, Gen. Purpose, Can, 18 mΩ, 2000 Hrs @ 105°C, (8 mm x 13 mm)	A750KS337M1EAAE018	KEMET
10	1	C10	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
11	1	C11	2.2 μF, 25 V, Ceramic, X7R, 1206	TMK316B7225KL-T	Taiyo Yuden
12	1	C12	1000 pF, ±10%, 50V,X7R, -55°C ~ 125°C, Low ESL, 0402	C0402C102K5RACTU	Kemet
13	1	C13	330 pF, ±10%, 100 V, Ceramic, X7R, 0402	HMK105B7331KV-F	Taiyo Yuden
14	1	C15	10 μF, 35 V, Ceramic, X5R, 0805	C2012X5R1V106K085AC	TDK
15	1	C16	1 μF, 100 V, Ceramic, X7S, 0805	C2012X7S2A105K125AB	TDK
16	1	D1	800 V, 1 A, Rectifier, POWERDI123	DFLR1800-7	Diodes, Inc.
17	1	D2	DIODE, GEN PURP, FAST RECOVERY, 300 V, 225 mA, SOD323	BAV3004WS-7	Diodes, Inc.
18	2	D3 D4	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
19	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
20	J1	1	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
21	J2 J4	2	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
22	J3	1	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
23	JP1	1	Wire Jumper, Insulated, 24 AWG, 0.7 in	C2003A-12-02	Gen Cable
24	JP2	1	Wire Jumper, Insulated, 24 AWG, 1.0 in	C2003A-12-02	Gen Cable
25	JP3	1	Wire Jumper, Insulated, 28 AWG, 0.5 in	2842/1 WH005	Alpha Wire
26	JP4	1	Wire Jumper, Insulated, 28 AWG, 0.3 in	2842/1 WH005	Alpha Wire
27	1	L1	250 μH, Toroidal Common Mode Choke, custom, wound on 35T0375-10H core. Assembled CMC	32-00367-00 TSD-4500	Power Integrations Premier Magnetics
28	1	L2	CMC, 18 mH @ 10 kHz, Toroidal, 17.5 mm OD x 11.0 mm thick. 40 turns x 2, 0.40 mm wire 190 mΩ max	04291-T231	Sumida
29	1	Q1	MOSFET, N-CH, 100 V, 48 A (at VGS = 10 V), Trench Power AlphaSGT 100 V TM technology, DFN5X6	AON6220	Alpha & Omega Semi
30	2	R1 R2	RES, 1 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105V	Panasonic
31	1	R3	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
32	1	R4	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
33	2	R5 R6	RES, 20 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ200V	Panasonic
34	1	R7	RES, 680 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ684V	Panasonic
35	1	R8	RES, 3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ302V	Panasonic
36	2	R9 R12	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
37	1	R11	RES, 10 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
38	1	R13	RES, 0 Ω, 1/16 W, Thick Film, 0402	CRCW04020000Z0ED	Panasonic
39	1	R14	RES, 0.009 Ω, 0.5 W, 5%, 0805	ERJ-6LWJR009V	Panasonic
40	1	R15	RES, 169.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1693X	Panasonic
41	1	R16	RES, 11.5 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1152X	Panasonic
42	1	T1	Bobbin, EQ25, 6 pins, 6pri, 0sec	TBD_EQ-2506-6	
43	1	U1	InnoSwitch3-EP, InSOP24A	INN3679C-H606	Power Integrations
44	1	U2	CAPZero-2, SO-8C	CAP200DG	Power Integrations

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45	1	VR1	DIODE ZENER 12 V 500 mW SOD123	MMSZ5242B-7-F	Diodes, Inc.

7 Transformer Specification

7.1 Electrical Diagram

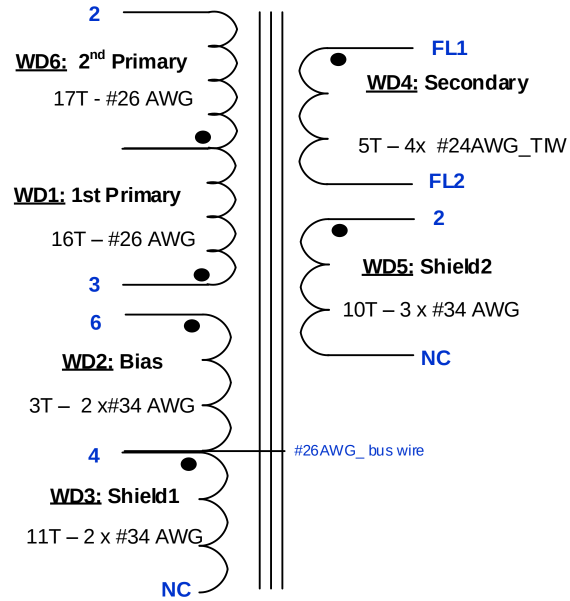

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Electrical Strength	60 second, 60 Hz, from Pins 1, 2, 3, 4 to FL1 - FL2.	3000 VAC
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 2 and 3, with all other windings open.	505 μH ± 5%
Resonant Frequency	Between pin 2 and 3, other windings open.	1,000 kHz (min.)
Primary Leakage Inductance	Between pin 2 and 3, with pins:FL1 - FL2 shorted.	4.5 μH (max.)

7.3 Material List

Item	Description
[1]	Core: EQ25, Ferroxcube: 3C95.
[2]	Bobbin: EQ25-Vert-6pins (6/0); PI#: 25-01136-00.
[3]	Magnet Wire: #26 AWG, Double Coated.
[4]	Magnet Wire: #34 AWG, Double Coated.
[5]	Magnet Wire: #24 AWG, Triple Insulated Wire.
[6]	Bus wire: #26AWG, Alpha Wire, Tinned Copper.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 7.5 mm Width.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 33 mm x 58 mm.
[9]	Varnish: Dolph BC-359.

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7.4 Transformer Build Diagram

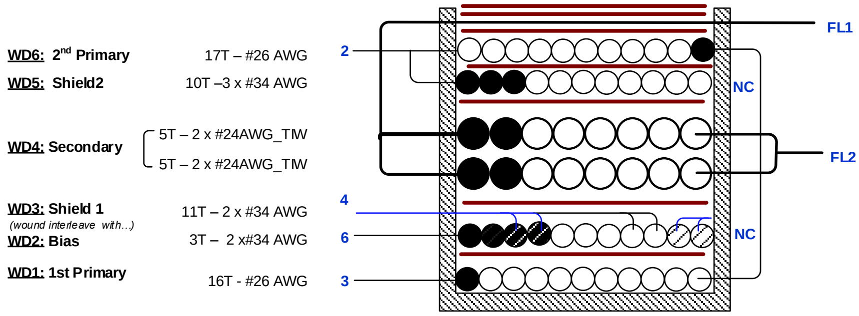
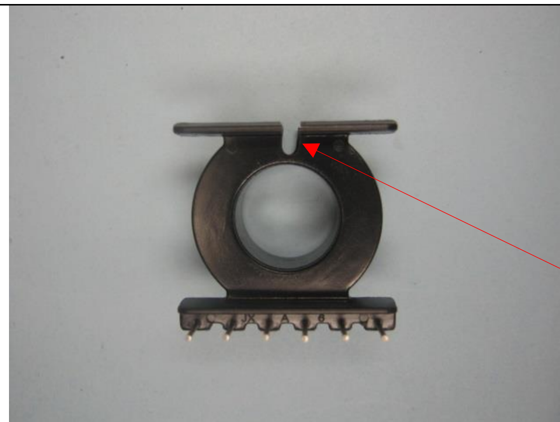
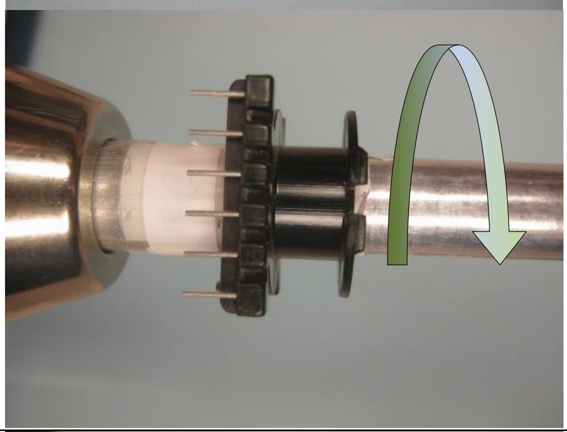
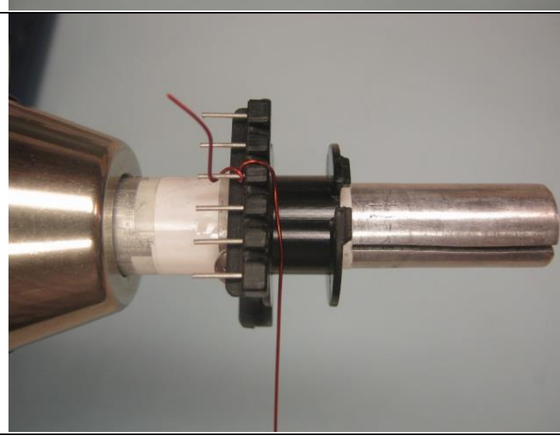


Figure 7 – Transformer Build Diagram.

7.5 Transformer Construction

Winding Preparation	Make slots with 2.0mm width on both flanges of secondary side of bobbin Item [2] (*see picture below*) Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 1st Primary	Start at pin 3, wind 16 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn, leave the wire floating and enough length for WD6-2nd Primary.
Insulation	1 layer of tape Item [7].
WD2: Bias & WD3: Shield1	Use 2 wires Item [4] start at pin 6 for bias winding, also use 2 wires same Item [4] start at pin 4 for Shield1 winding. Wind all 4 wires in parallel, at the 3rd turn, place 1 piece of tape to hold the wires, and bring first 2 wires for bias winding to the left to terminate at pin 4. Continue winding other 2 wires with 8 turns, at the last turn cut short to leave as No-Connect.
Insulation	1 layer of tape Item [7].
WD4 Secondary	Start at left slot of secondary side, use 2 wires Item [5], leaving ~ 40.0mm, and mark as FL1.Wind 5 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 30.0mm and mark FL2. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2.
Insulation	1 layer of tape Item [7].
WD5 Shield2	Start at pin 2, wind 10 tri-filar turns of wire Item [4], from left to right. At the last turn, cut short to leave as No-Connect.
Insulation	1 layer of tape Item [7].
WD6 2nd Primary	Use floating wire from WD1-1st Primary, wind 17 turns from right to left and finish at pin 2.
Insulation	1 layer of tape Item [7].
Finish	Bring 4 wires marked as FL1 to the right and secure with 2 layers of tape Item [7]. Gap core halves to get 505 uH. Solder pin 4 with bus-wire Item [6] then lean along core halves and secure with tape. Varnish with Item [9]. Place 2 layers of tape Item [8] at the bottom then wrap up to the body of transformer, and tape around 1layer of tape Item [7]. (*See pictures below*).

7.6 *Winding Illustrations*

Winding Preparation	 	<u>Make slots with 2.0mm width</u> on both flanges of secondary side of bobbin Item [2]. Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction. (*see picture beside*)
WD1 1st Primary		Start at pin 3, wind 16 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn, leave the wire floating and enough length for WD6-2nd Primary.

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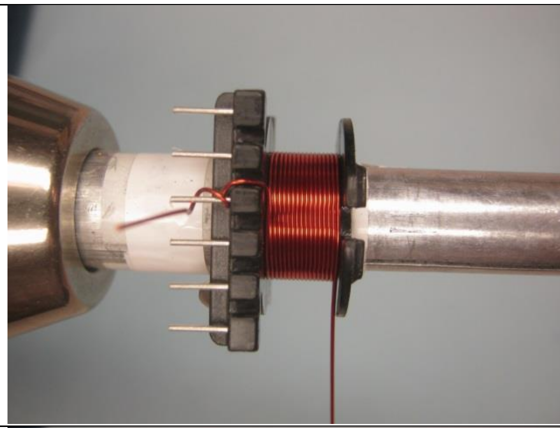
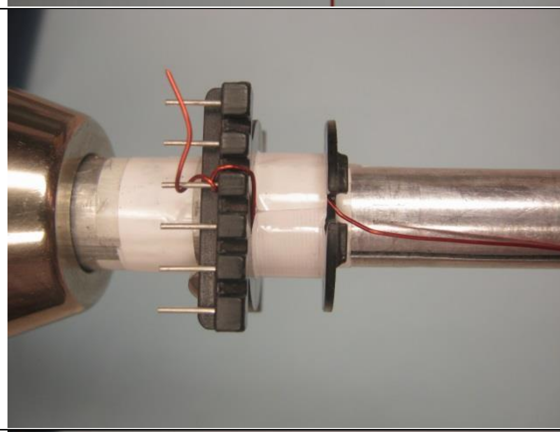
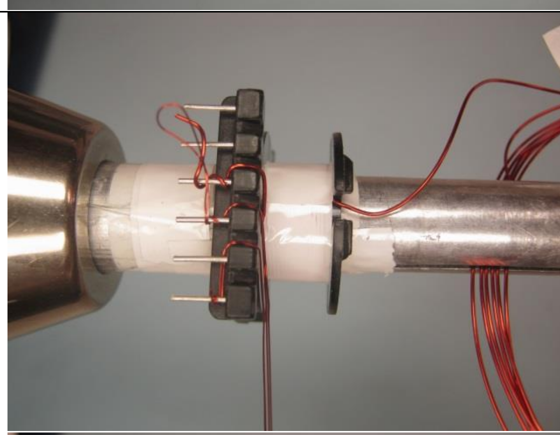
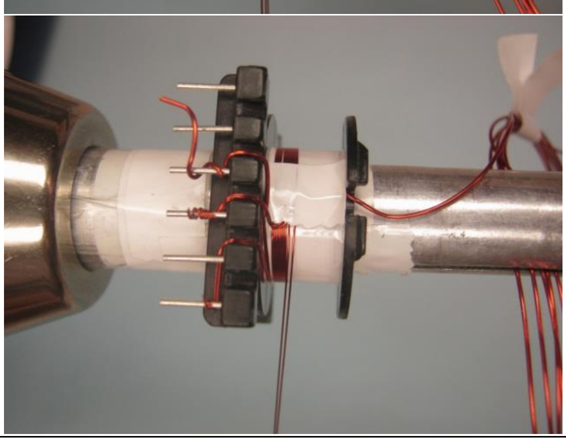
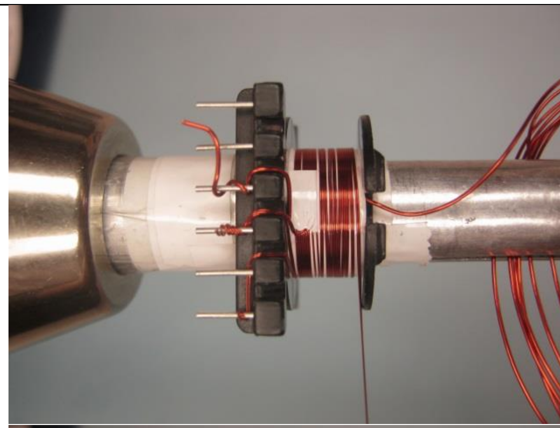
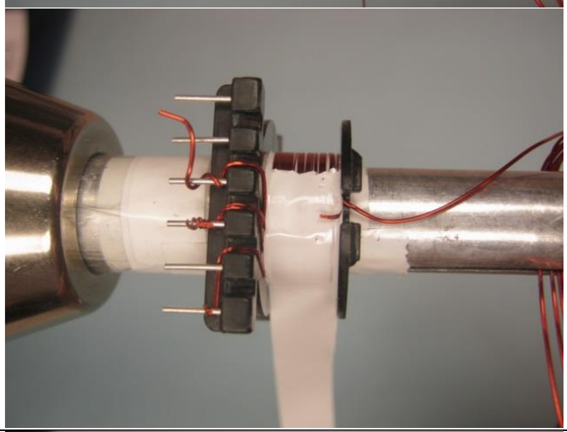
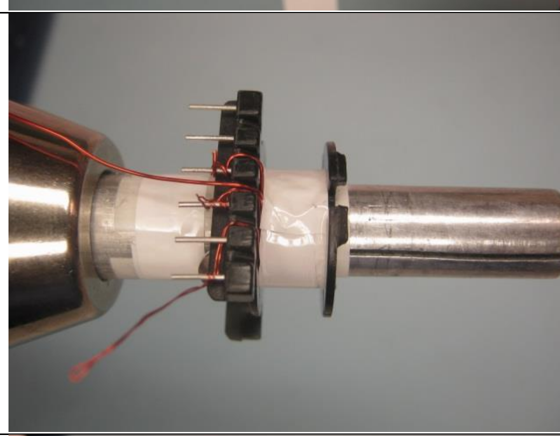
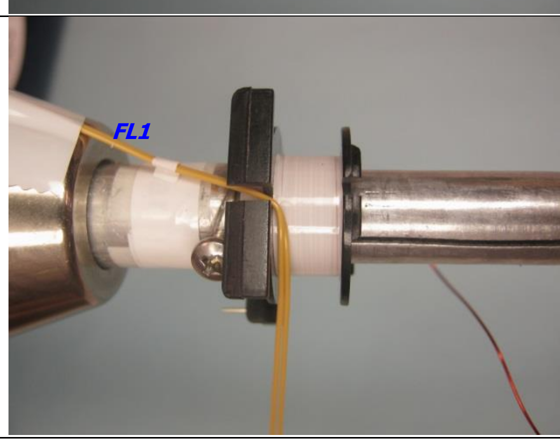
		
Insulation		1 layer of tape Item [7].
WD2: Bias & WD3: Shield1	 	Use 2 wires Item [4] start at pin 6 for bias winding, also use 2 wires same Item [4] start at pin 4 for Shield1 winding. Wind all 4 wires in parallel, at the 3rd turn, place 1 piece of tape to hold the wires, and bring first 2 wires for bias winding to the left to terminate at pin 4. Continue winding other 2 wires with 8 turns, at the last turn cut short to leave as No-Connect.

		
Insulation		1 layer of tape Item [7].
WD4 Secondary		Start at left slot of secondary side, use 2 wires Item [5], leaving ~ 40.0mm, and mark as FL1.Wind 5 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~ 30.0mm and mark FL2. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and

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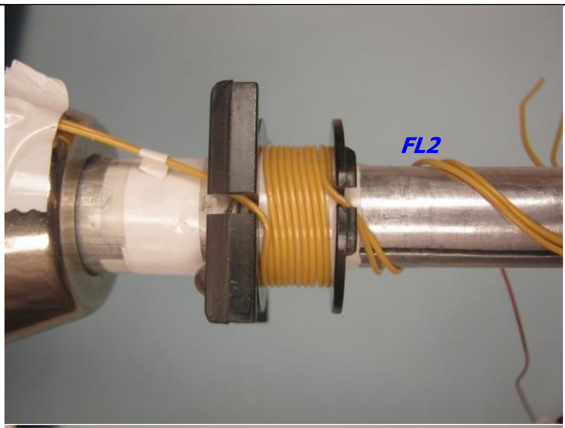
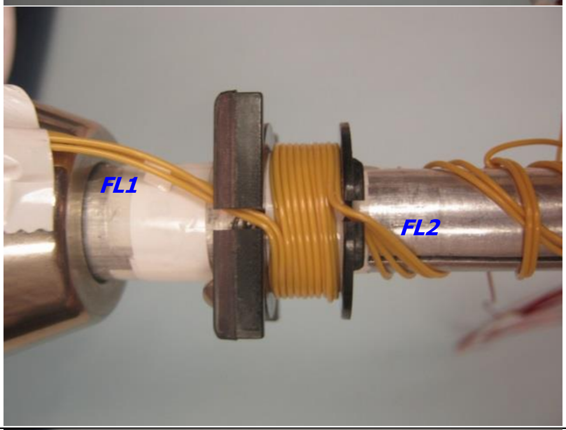
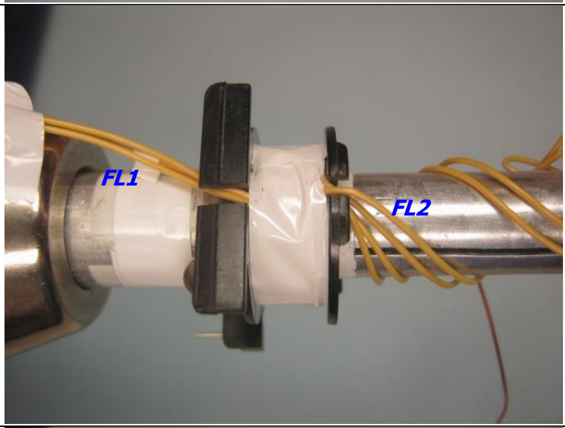
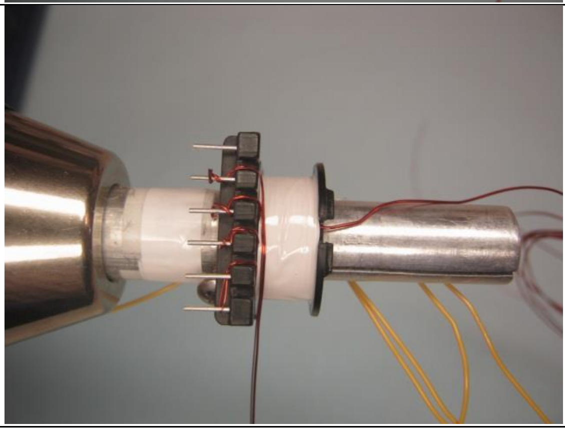
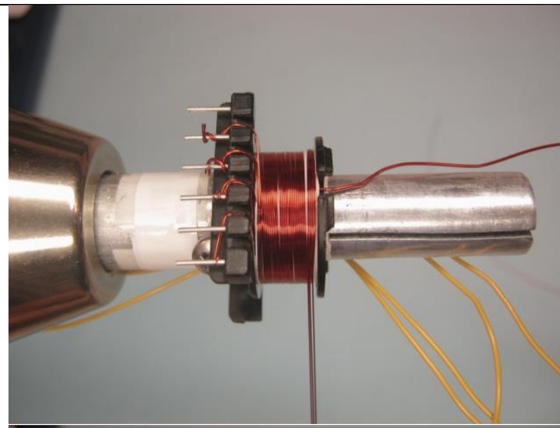
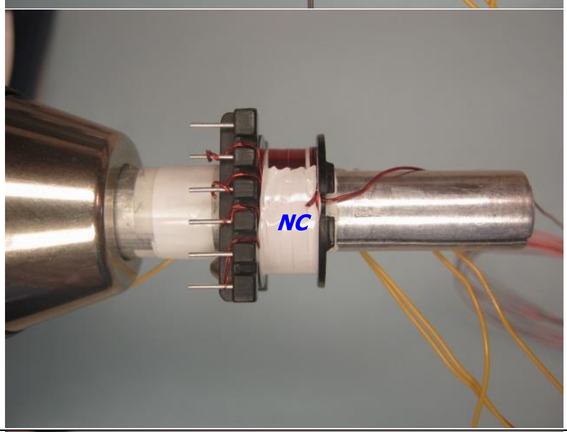
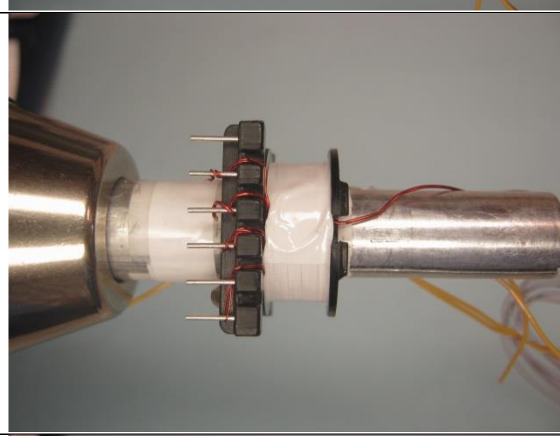
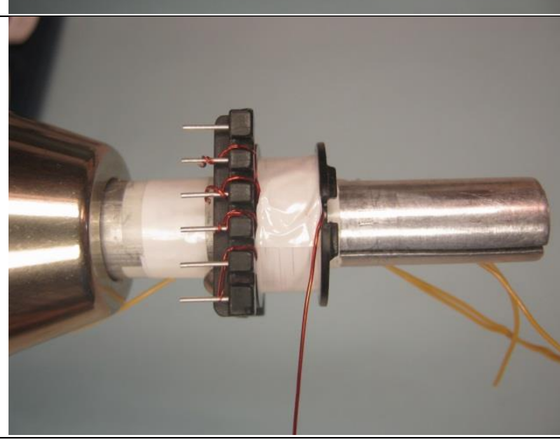
	 	FL2.
Insulation		1 layer of tape Item [7].
WD5 Shield2		St Start at pin 2, wind 10 tri-filar turns of wire Item [4], from left to right. At the last turn, cut short to leave as No-Connect.

	 	
Insulation		1 layer of tape Item [7].
WD6 **2nd Primary**		Use floating wire from WD1-1st Primary, wind 17 turns from right to left and finish at pin 2.

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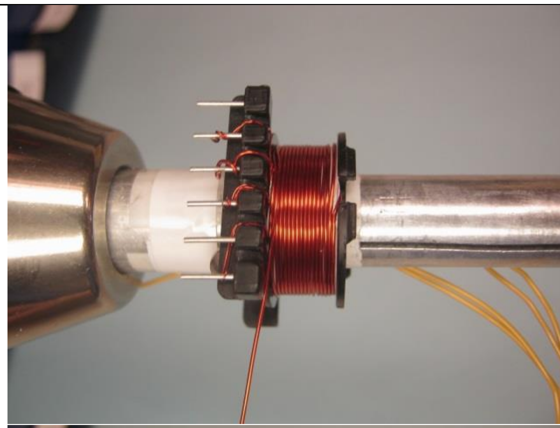
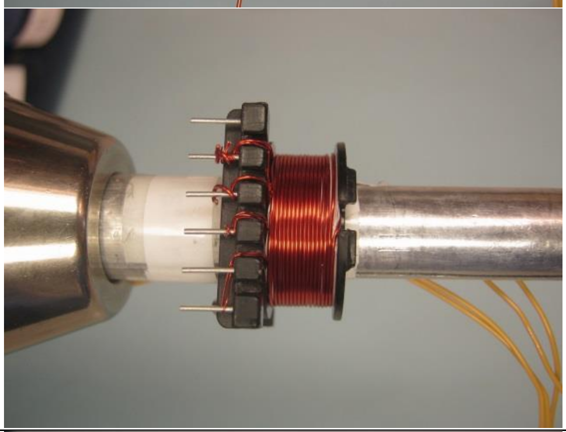
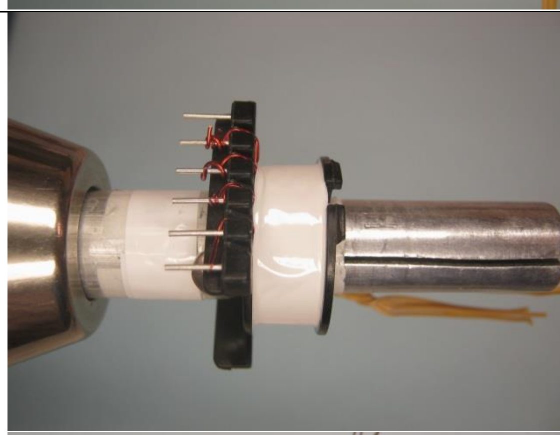
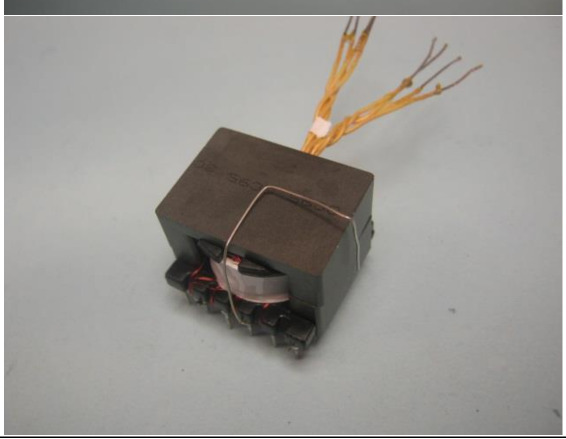
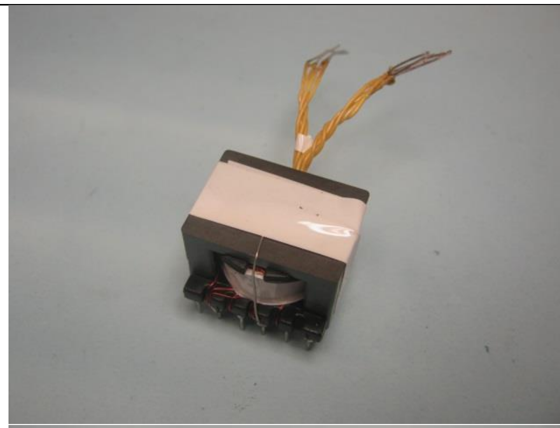
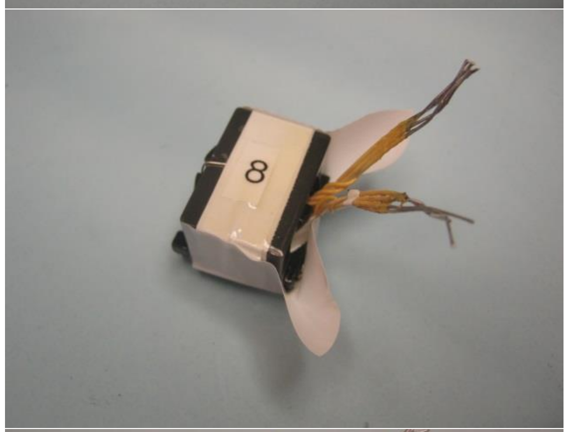
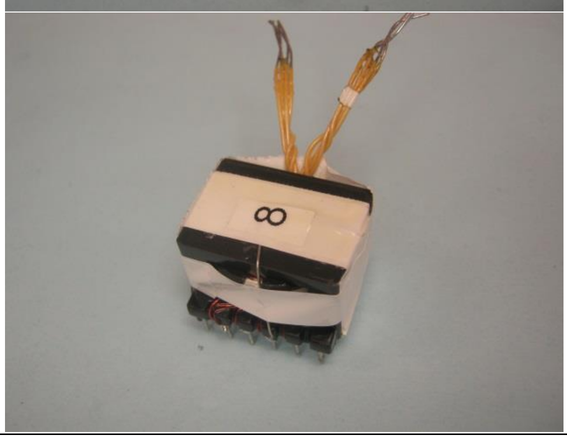
	 	
Finish	 	Bring 4 wires marked as FL1 to the right and secure with 2 layers of tape Item [7]. Gap core halves to get 505uH. Solder pin 4 with bus-wire Item [6] then lean along core halves and secure with tape. Varnish with Item [9]. Place 2 layers of tape Item [8] at the bottom then wrap up to the body of transformer, and tape around 1 layer of tape Item [7]. (*See pictures beside*).







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8 Common Mode Choke Specifications

8.1 *250 μH Common Mode Choke (L1)*

8.1.1 Electrical Diagram

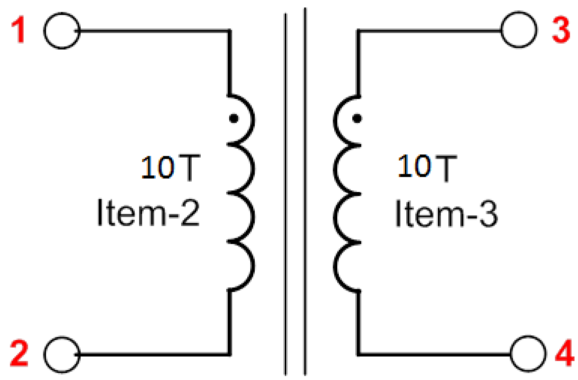


Figure 8 — Inductor Electrical Diagram.

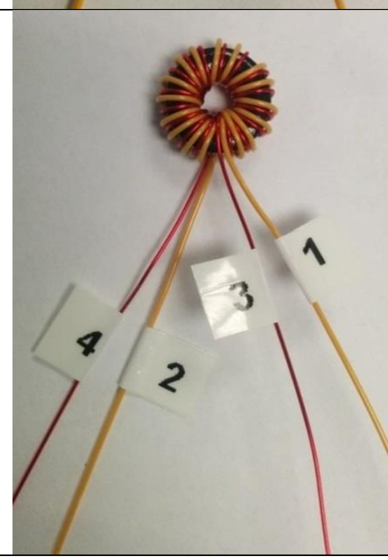
8.1.2 Electrical Specifications

Inductance	Pins 1 - 2 measured at 100 kHz, 0.4 RMS.	250 μH ±20%
Primary Leakage Inductance	Pins 1 - 2, with 3 - 4 shorted.	1 μH

8.1.3 Material List

Item	Description
[1]	Toroid: FERRITE INDUCTR TOROID .415" O.D.;Mfg Part number: 35T0375-10H. Dim: 9.53 mm O.D. x 4.75 mm I.D. x 3.18 mm L.
[2]	Magnet Wire: #27 AWG.
[3]	Triple Insulated Wire #27 AWG.

8.1.4 Common Mode Choke Construction

Mark the start end of the winding as 1 and wind 10 turns of Item [2] on Item [1]. Mark the end of this winding as 2	
Repeat the same procedure as above for the other winding using Item [3], making sure that the start/end and the direction of winding is the same as the first winding. Varnish using Item [4]. Mark the start of this winding as 3 and the end as 4.	

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9 Transformer Design Spreadsheet

1	ACDC_Flyback_081518; Rev.0.1; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNITS	Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VAC_MIN	90		90	V	Minimum AC line voltage
4	VAC_MAX			265	V	Maximum AC input voltage
5	VAC_RANGE			UNIVERSAL		AC line voltage range
6	FLINE			60	Hz	AC line voltage frequency
7	CAP_INPUT	100.0		100.0	uF	Input capacitance
9	**SETPOINT 1**					
10	VOUT1	20.00		20.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	3.250		3.250	A	Output current 1
12	POUT1			65.00	W	Output power 1
13	EFFICIENCY1	0.92		0.92		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
16	**SETPOINT 2**					
17	VOUT2			0.00	V	Output voltage 2
18	IOUT2			0.000	A	Output current 2
19	POUT2			0.00	W	Output power 2
20	EFFICIENCY2			0.00		Converter efficiency for output 2
21	Z_FACTOR2			0.00		Z-factor for output 2
23	**SETPOINT 3**					
24	VOUT3			0.00	V	Output voltage 3
25	IOUT3			0.000	A	Output current 3
26	POUT3			0.00	W	Output power 3
27	EFFICIENCY3			0.00		Converter efficiency for output 3
28	Z_FACTOR3			0.00		Z-factor for output 3
30	**SETPOINT 4**					
31	VOUT4			0.00	V	Output voltage 4
32	IOUT4			0.000	A	Output current 4
33	POUT4			0.00	W	Output power 4
34	EFFICIENCY4			0.00		Converter efficiency for output 4
35	Z_FACTOR4			0.00		Z-factor for output 4
37	**SETPOINT 5**					
38	VOUT5			0.00	V	Output voltage 5
39	IOUT5			0.000	A	Output current 5
40	POUT5			0.00	W	Output power 5
41	EFFICIENCY5			0.00		Converter efficiency for output 5
42	Z_FACTOR5			0.00		Z-factor for output 5
44	**SETPOINT 6**					
45	VOUT6			0.00	V	Output voltage 6
46	IOUT6			0.000	A	Output current 6
47	POUT6			0.00	W	Output power 6
48	EFFICIENCY6			0.00		Converter efficiency for output 6
49	Z_FACTOR6			0.00		Z-factor for output 6
51	**SETPOINT 7**					
52	VOUT7			0.00	V	Output voltage 7
53	IOUT7			0.000	A	Output current 7
54	POUT7			0.00	W	Output power 7
55	EFFICIENCY7			0.00		Converter efficiency for output 7
56	Z_FACTOR7			0.00		Z-factor for output 7
58	**SETPOINT 8**					

59	VOUT8			0.00	V	Output voltage 8
60	IOUT8			0.000	A	Output current 8
61	POUT8			0.00	W	Output power 8
62	EFFICIENCY8			0.00		Converter efficiency for output 8
63	Z_FACTOR8			0.00		Z-factor for output 8
65	**SETPOINT 9**					
66	VOUT9			0.00	V	Output voltage 9
67	IOUT9			0.000	A	Output current 9
68	POUT9			0.00	W	Output power 9
69	EFFICIENCY9			0.00		Converter efficiency for output 9
70	Z_FACTOR9			0.00		Z-factor for output 9
71						
72	PERCENT_CDC			0%		Percentage (of output voltage) cable drop compensation desired at full load
73	CDC_SCALING_SETPOINT	1		1		Select the setpoint number for the voltage used for cable drop compensation (typically the 5V output)
77	**PRIMARY CONTROLLER SELECTION**					
78	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
79	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
80	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
81	DEVICE_GENERIC	AUTO		INN3679C		Device selection
82	DEVICE_CODE			INN3679C		Device code
83	PDEVICE_MAX			65	W	Device maximum power capability
84	RDSON_25DEG			0.34	Ω	Primary MOSFET on-time resistance at 25°C
85	RDSON_100DEG			0.53	Ω	Primary MOSFET on-time resistance at 100°C
86	ILIMIT_MIN			1.981	A	Primary MOSFET minimum current limit
87	ILIMIT_TYP			2.130	A	Primary MOSFET typical current limit
88	ILIMIT_MAX			2.279	A	Primary MOSFET maximum current limit
89	VDRAIN_ON_MOSFET			0.42	V	Primary MOSFET on-time voltage drop
90	VDRAIN_OFF_MOSFET			573.31	V	Peak drain voltage on the primary MOSFET during turn-off
94	**WORST CASE ELECTRICAL PARAMETERS**					
95	FSWITCHING_MAX	84500		84500	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
96	VOR	130.0		130.0	V	Voltage reflected to the primary winding (corresponding to setpoint 1) when the primary MOSFET turns off
97	VMIN			86.84	V	Valley of the rectified minimum input AC voltage at full load
98	KP			0.646		Measure of continuous/discontinuous mode of operation
99	MODE_OPERATION			CCM		Mode of operation
100	DUTYCYCLE			0.601		Primary MOSFET duty cycle
101	TIME_ON			11.66	us	Primary MOSFET on-time
102	TIME_OFF			4.73	us	Primary MOSFET off-time
103	LPRIMARY_MIN			479.7	uH	Minimum primary magnetizing inductance
104	LPRIMARY_TYP			504.9	uH	Typical primary magnetizing inductance
105	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
106	LPRIMARY_MAX			530.2	uH	Maximum primary magnetizing inductance
108	**PRIMARY CURRENT**					

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109	IAVG_PRIMARY			0.785	A	Primary MOSFET average current
110	IPEAK_PRIMARY			2.156	A	Primary MOSFET peak current
111	IPEDESTAL_PRIMARY			0.683	A	Primary MOSFET current pedestal
112	IRIPPLE_PRIMARY			1.698	A	Primary MOSFET ripple current
113	IRMS_PRIMARY			1.082	A	Primary MOSFET RMS current
115	**SECONDARY CURRENT**					
116	IPEAK_SECONDARY			14.227	A	Secondary MOSFET peak current
117	IPEDESTAL_SECONDARY			4.509	A	Secondary MOSFET pedestal current
118	IRMS_SECONDARY			5.820	A	Secondary MOSFET RMS current
119	IRIPPLE_CAP_OUT			4.828	A	Output capacitor ripple current
123	**TRANSFORMER CONSTRUCTION PARAMETERS**					
124	**CORE SELECTION**					
125	CORE	CUSTOM		CUSTOM		Core selection
126	CORE NAME	EQ25		EQ25		Core code
127	AE	100.0		100.0	mm^2	Core cross sectional area
128	LE	41.4		41.4	mm	Core magnetic path length
129	AL	5700		5700	nH	Ungapped core effective inductance per turns squared
130	VE	4145		4145	mm^3	Core volume
131	BOBBIN NAME	EQ25		EQ25		Bobbin name
132	AW	52.0		52.0	mm^2	Bobbin window area
133	BW	7.60		7.60	mm	Bobbin width
134	MARGIN			0.0	mm	Bobbin safety margin
136	**PRIMARY WINDING**					
137	NPRIMARY			33		Primary winding number of turns
138	BPEAK			3748	Gauss	Peak flux density
139	BMAX			3423	Gauss	Maximum flux density
140	BAC			1324	Gauss	AC flux density (0.5 x Peak to Peak)
141	ALG			464	nH	Typical gapped core effective inductance per turns squared
142	LG			0.249	mm	Core gap length
143	LAYERS_PRIMARY			2		Primary winding number of layers
144	AWG_PRIMARY	26		26		Primary wire gauge
145	OD_PRIMARY_INSULATED			0.465	mm	Primary wire insulated outer diameter
146	OD_PRIMARY_BARE			0.405	mm	Primary wire bare outer diameter
147	CMA_PRIMARY			234.9	Cmils/A	Primary winding wire CMA
149	**SECONDARY WINDING**					
150	NSECONDARY	5		5		Secondary winding number of turns
151	AWG_SECONDARY			19		Secondary wire gauge
152	OD_SECONDARY_INSULATED			1.217	mm	Secondary wire insulated outer diameter
153	OD_SECONDARY_BARE			0.912	mm	Secondary wire bare outer diameter
154	CMA_SECONDARY			221.3	Cmils/A	Secondary winding wire CMA
156	**BIAS WINDING**					
157	NBIAS			3		Bias winding number of turns
161	**PRIMARY COMPONENTS SELECTION**					
162	**LINE UNDERVOLTAGE**					
163	BROWN-IN REQURED			72.00	V	Required line brown-in threshold
164	RLS			3.56	MΩ	Connect two 1.78 MOhm resistors to the V-pin for the required UV/OV threshold
165	BROWN-IN ACTUAL			71.40	V	Actual brown-in threshold using standard resistors
166	BROWN-OUT ACTUAL			64.58	V	Actual brown-out threshold using standard resistors
168	**LINE OVERVOLTAGE**					
169	OVERVOLTAGE_LINE			297.50	V	Actual AC RMS line over-voltage threshold

170						
171	BIAS WINDING					
172	VBIAS			9.00	V	Rectified bias voltage at the lowest output setpoint
173	VF_BIAS			0.70	V	Bias winding diode forward drop
174	VREVERSE_BIASDIODE			42.94	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
175	CBIAS			22	uF	Bias winding rectification capacitor
176	CBPP			4.70	uF	BPP pin capacitor
180	**SECONDARY COMPONENTS SELECTION**					
181	**RECTIFIER**					
182	VDRAIN_OFF_SRFET			76.56	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
183	SRFET	AUTO		AO4294		Secondary rectifier (Logic MOSFET)
184	VBREAKDOWN_SRFET			100	V	Secondary rectifier breakdown voltage
185	RDSON_SRFET			15.5	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
187	**FEEDBACK COMPONENTS**					
188	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the output terminal)
189	RFB_LOWER			6.81	kΩ	Lower feedback resistor required to obtain the output for cable drop compensation
190	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
194	**SETPOINTS ANALYSIS**					
195	**TOLERANCE CORNER**					
196	USER_VAC	115		115	V	Input AC RMS voltage corner to be evaluated
197	USER_ILIMIT	TYP		2.130	A	Current limit corner to be evaluated
198	USER_LPRIMARY	TYP		504.9	uH	Primary inductance corner to be evaluated
200	**SETPOINT SELECTION**					
201	SETPOINT	1		1		Select the setpoint which needs to be evaluated
202	FSWITCHING			65628.5	Hz	Maximum switching frequency at full load and the valley of the minimum input AC voltage
203	VOR			130.0	V	Voltage reflected to the primary winding when the primary MOSFET turns off
204	VMIN			131.28	V	Valley of the minimum input AC voltage
205	KP			0.973		Measure of continuous/discontinuous mode of operation
206	MODE_OPERATION			CCM		Mode of operation
207	DUTYCYCLE			0.498		Primary MOSFET duty cycle
208	TIME_ON			7.71	us	Primary MOSFET on-time
209	TIME_OFF			7.65	us	Primary MOSFET off-time
211	**PRIMARY CURRENT**					
212	IAVG_PRIMARY			0.518	A	Primary MOSFET average current
213	IPEAK_PRIMARY			2.024	A	Primary MOSFET peak current
214	IPEDESTAL_PRIMARY			0.055	A	Primary MOSFET current pedestal
215	IRIPPLE_PRIMARY			1.969	A	Primary MOSFET ripple current
216	IRMS_PRIMARY			0.836	A	Primary MOSFET RMS current
218	**SECONDARY CURRENT**					
219	IPEAK_SECONDARY			13.358	A	Secondary MOSFET peak current
220	IPEDESTAL_SECONDARY			0.363	A	Secondary MOSFET pedestal current
221	IRMS_SECONDARY			5.540	A	Secondary MOSFET RMS current
222	IRIPPLE_CAP_OUT			4.486	A	Output capacitor ripple current

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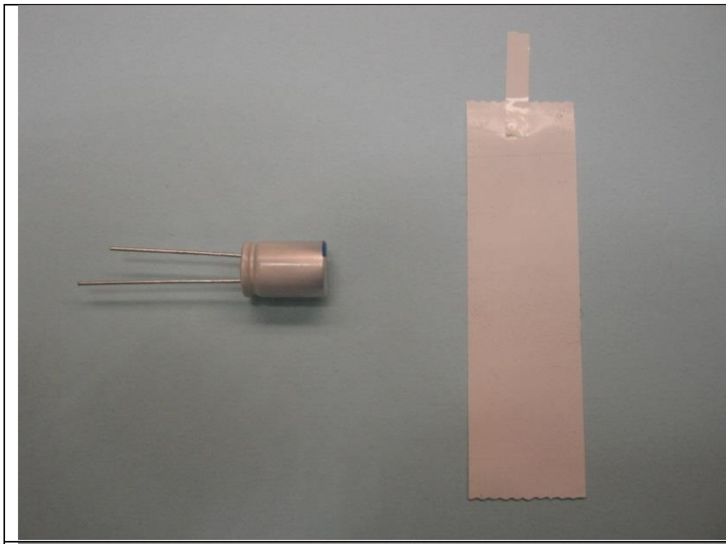
224	**MAGNETIC FLUX DENSITY**					
225	BPEAK			3336	Gauss	Peak flux density
226	BMAX			3097	Gauss	Maximum flux density
227	BAC			1506	Gauss	AC flux density (0.5 x Peak to Peak)

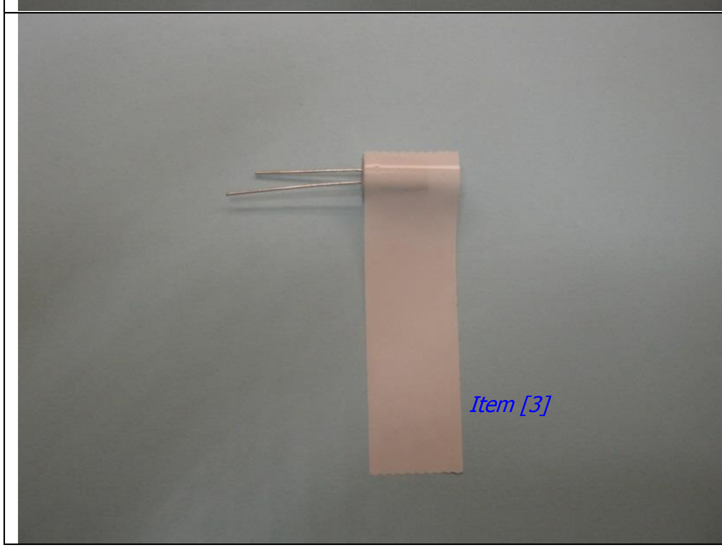
10 PCB Assembly Instructions

10.1 *Materials*

Item	Description
[1]	Capacitor C8 on RDR-747 Schematic.
[2]	Capacitor C9 on RDR-747 Schematic.
[3]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 16.4 mm Wide, 25 mm Long.
[4]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 5.0 mm Wide, 15 mm Long.
[5]	Tape: 3M 4026W Double Coated Urethane Foam Tape 1.6 mm Thick, 12.7 mm Wide, 22 mm Long.

10.2 *Output Capacitor Assembly Instructions*





Wrap C8 and C9 with tape Item [3] to insulate the capacitor form transformer core.

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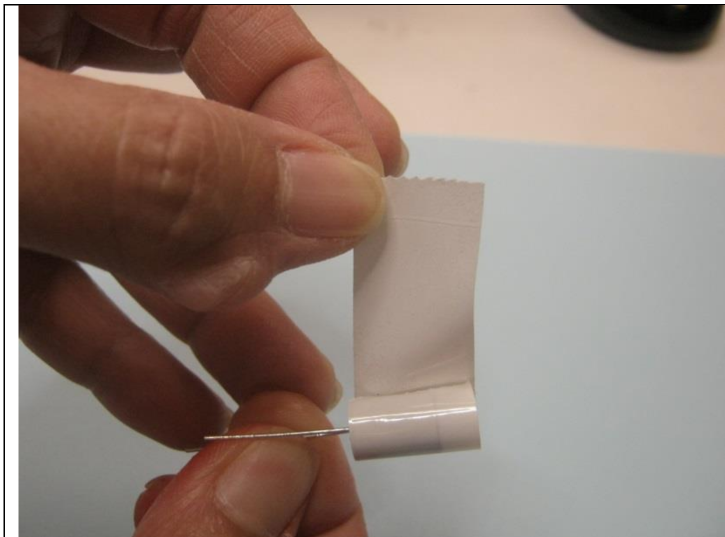
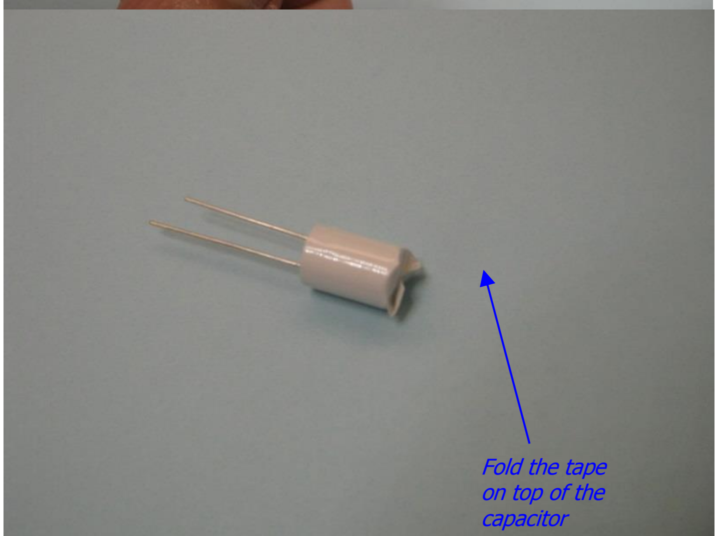
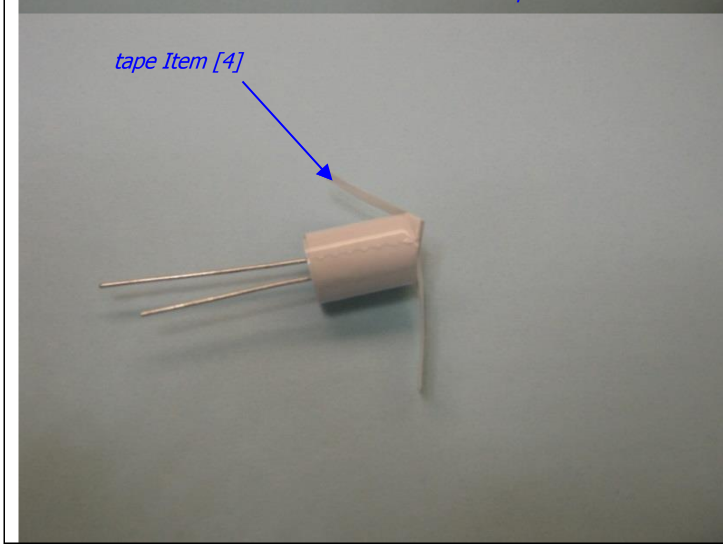



Fold the tape
on top of the
capacitor


tape Item [4]

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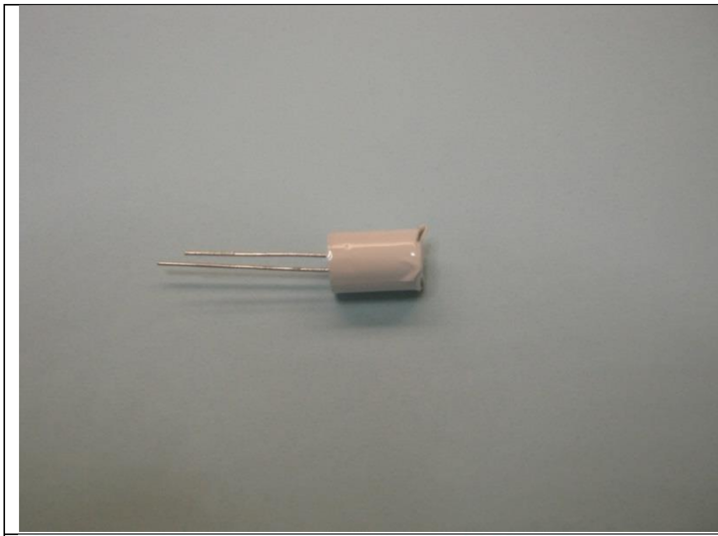
<tr><td></td><td></td></tr>
<tr><td>
</td><td>Finish assembly.</td></tr>
</table>

Note: Cut all the TH (PTH and NPTH) pins to <0.5 mm on the bottom side of the board after completing the assembly.

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11 Performance Data

All the performance data have been taken on the board unless otherwise specifically mentioned.

11.1 Full-load Efficiency vs. Line

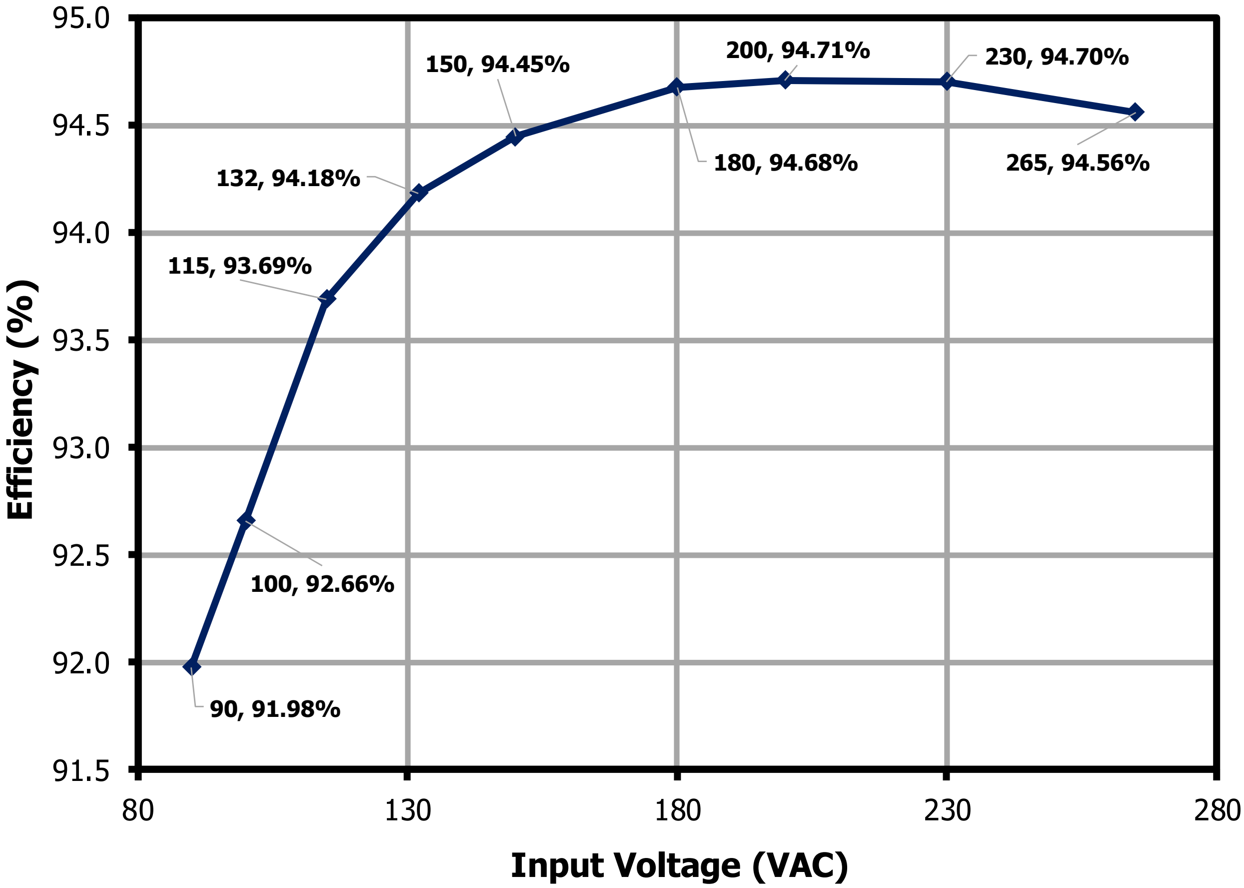

Figure 9 – Full-load Efficiency vs. Line, Room Ambient.

11.2 No-Load Input Power

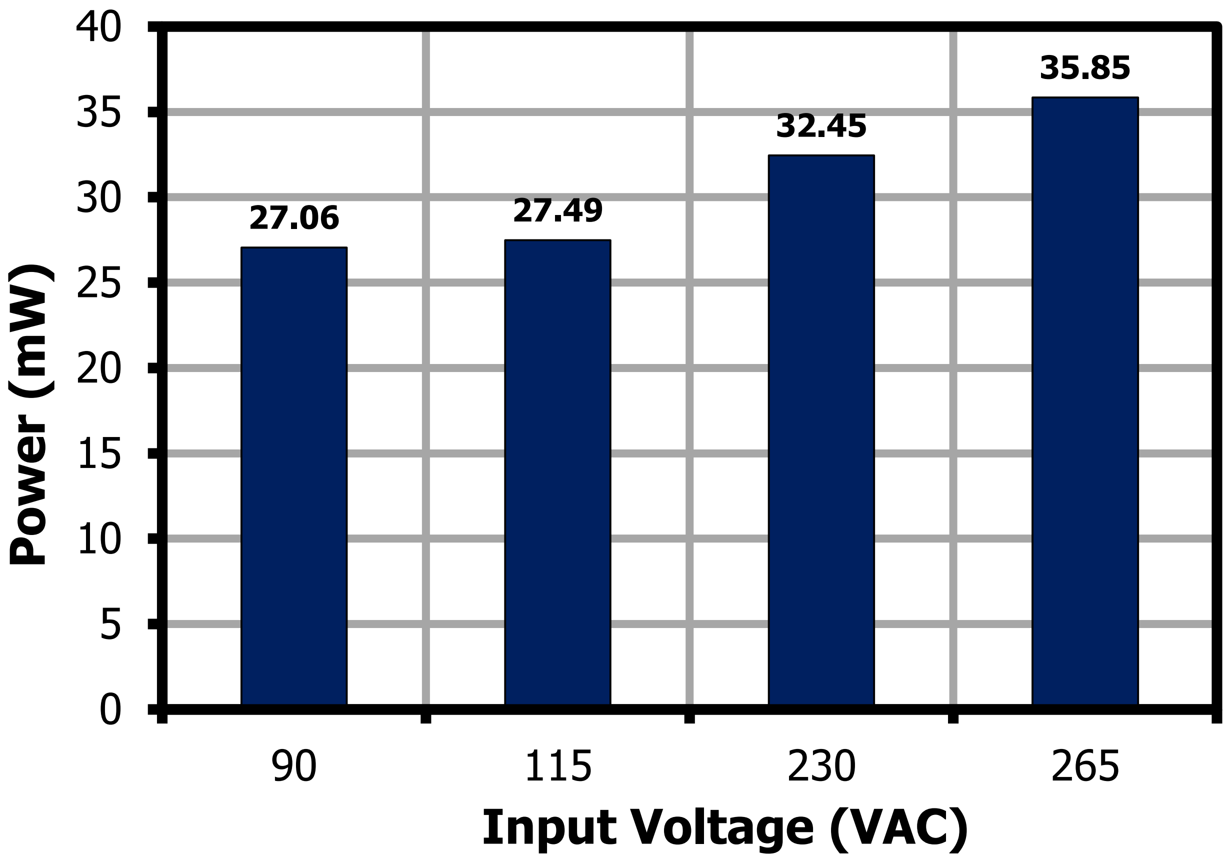

Figure 10 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

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11.3 *Average Efficiency*

		Test	Average	Average	10% Load
Output Voltage	**Model**	**Power [W]**	**DOE6 Limit**	**CoC v5 Tier 2**	**CoC v5 Tier 2**
20	>6 V	65	88.00%	89.00%	79.00%

11.4 Average and 10% Efficiency at 90 VAC Input

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	63.36	91.98	93.09
75	47.68	93.18	
50	31.96	93.52	
25	16.02	93.69	
10	6.25	92.47	

11.5 Average and 10% Efficiency at 115 VAC Input

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	63.50	93.69	94.01
75	47.83	94.04	
50	32.01	94.17	
25	16.06	94.13	
10	6.25	92.57	

11.6 Average and 10% Efficiency at 230 VAC Input

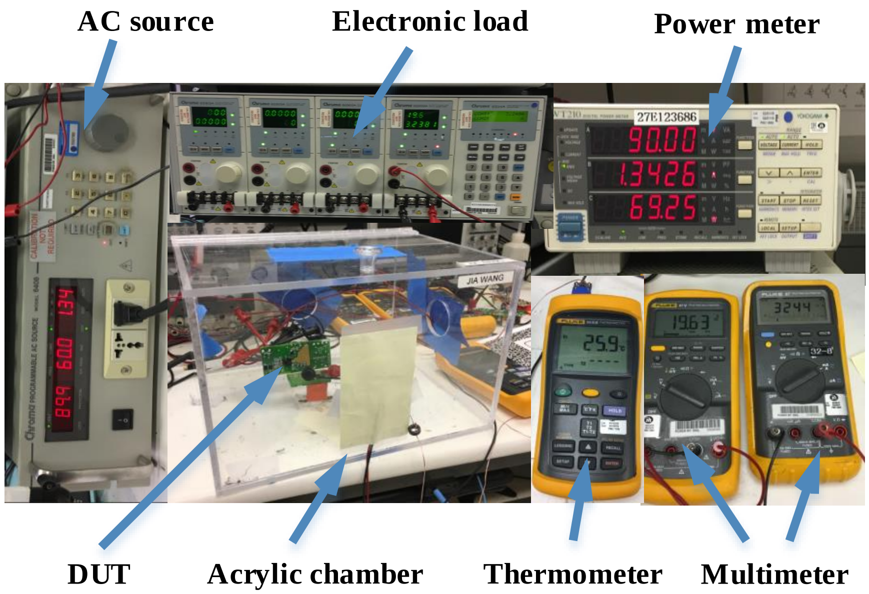
% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	63.76	94.70	94.32
75	47.93	94.64	
50	32.04	94.43	
25	16.06	93.52	
10	6.25	90.94	

11.7 Average and 10% Efficiency at 265 VAC Input

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	63.74	94.56	94.04
75	47.97	94.51	
50	32.02	94.18	
25	16.03	92.92	
10	6.25	90.09	

12 Thermal Performance

Thermal performance is measured in thermal chamber, as shown below.



Test setup

12.1 90 VAC, 65 W at 25.9 ºC Ambient

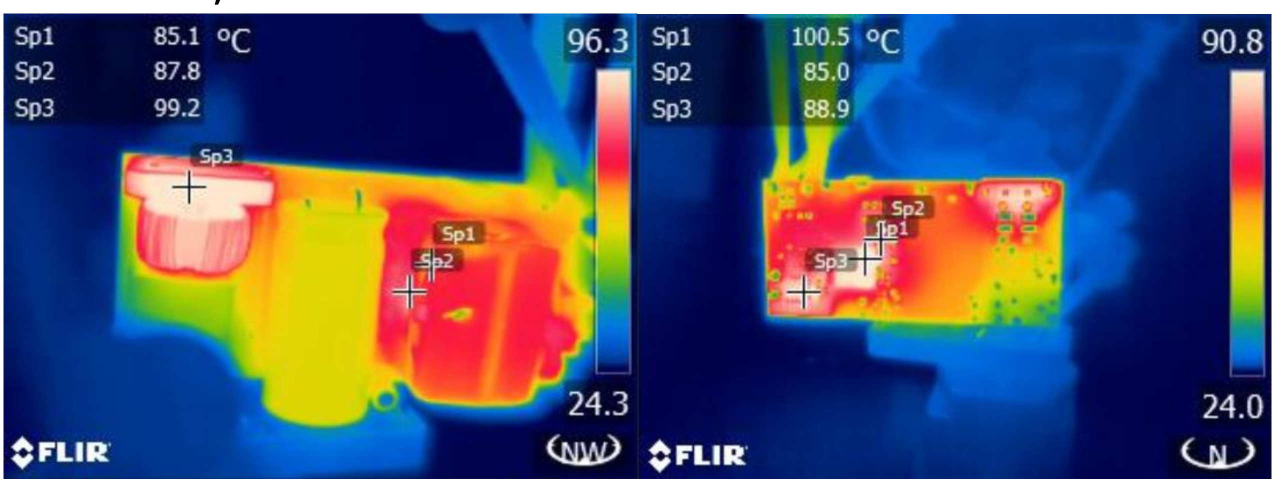


Figure 11 – Thermal Performance.

Test condition setting: full load soaking up for 120 mins

Component	Transformer Core (EQ25)	Transformer Winding (T1)	Bridge Rectifier (BR1)	InnoSwitch 3-EP (U1)	Primary-side RCD Snubber	SR FET (Q1)
Max Temperature (ºC)	85.1	87.8	99.2	100.5	85.0	88.9

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12.2 **265 VAC Input, 65 W at 25.2 ºC Ambient**

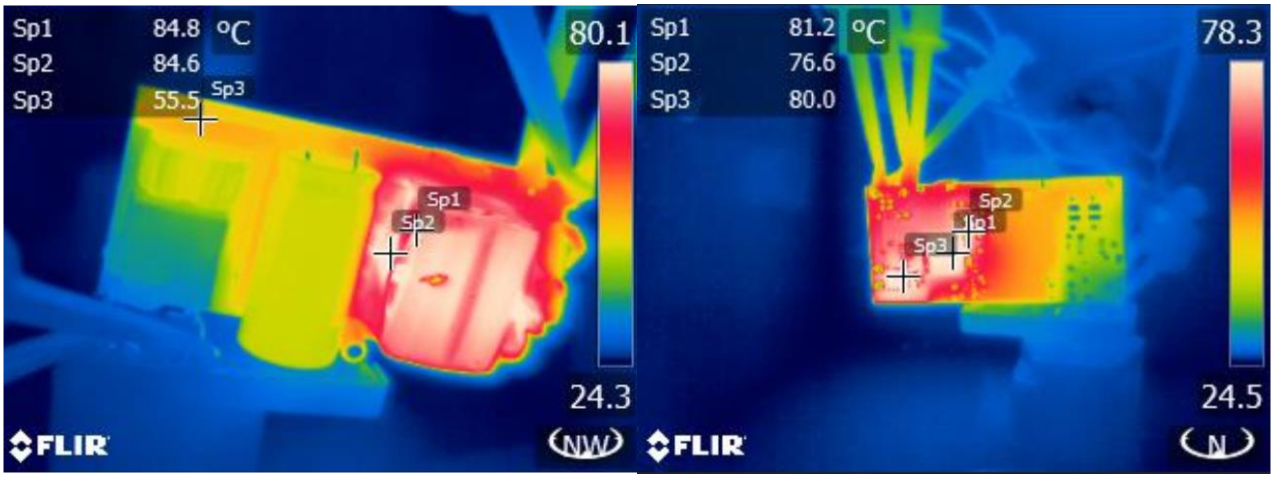

Figure 12 – Thermal Performance Over Time.

Test condition setting: full load soaking up for 120mins

Component	Transformer Core (EQ25)	Transformer Winding (T1)	Bridge Rectifier (BR1)	InnoSwitch3-EP (U1)	Primary-side RCD Snubber	SR FET (Q1)
Max Temperature (ºC)	84.8	84.6	55.5	81.2	76.6	80.0

13 Waveforms

13.1 *Load Transient Response (On Board)*

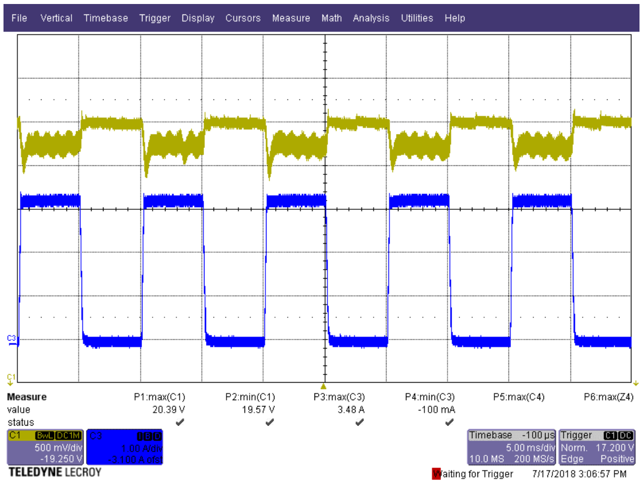

Figure 13 – Transient Response.
90 VAC, 0% – 100% Load Step.
V_{MIN}: 19.57 V, V_{MAX}: 20.39 V.
Upper: V_{OUT}, 0.5 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.

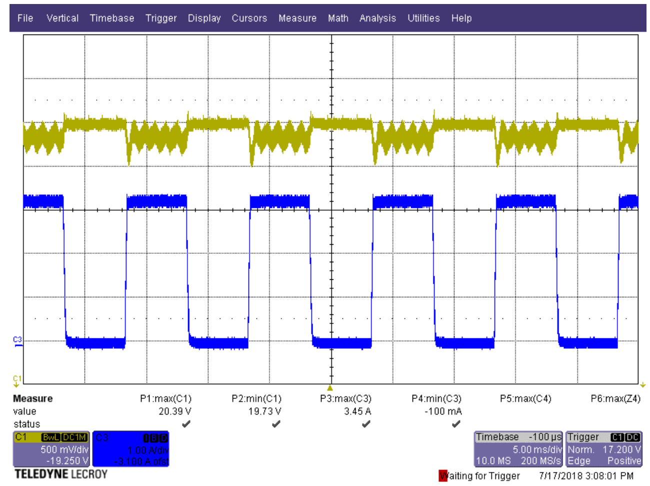

Figure 14 – Transient Response.
265 VAC, 0% – 100% Load Step.
V_{MIN}: 19.73 V, V_{MAX}: 20.39 V.
Upper: V_{OUT}, 0.5 V / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.

13.2 **Switching Waveforms**

13.2.1 Drain Voltage and Current

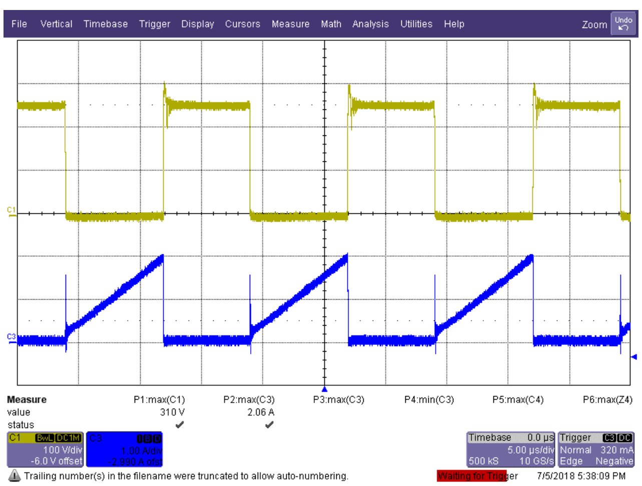

Figure 15 – Drain Voltage and Current Waveforms.
90 VAC, 100% Load, (310 V_{MAX}).
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 1 A / div., 5 µs / div.

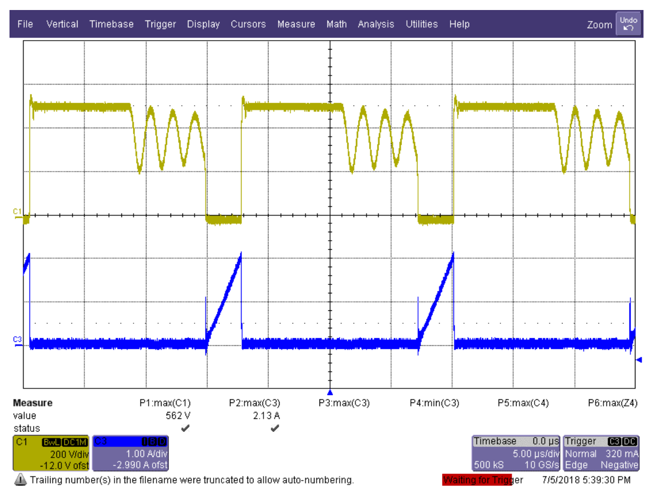

Figure 16 – Drain Voltage and Current Waveforms.
265 VAC, 100% Load, (562 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 1 A / div., 5 µs / div.

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13.2.2 SR FET Voltage

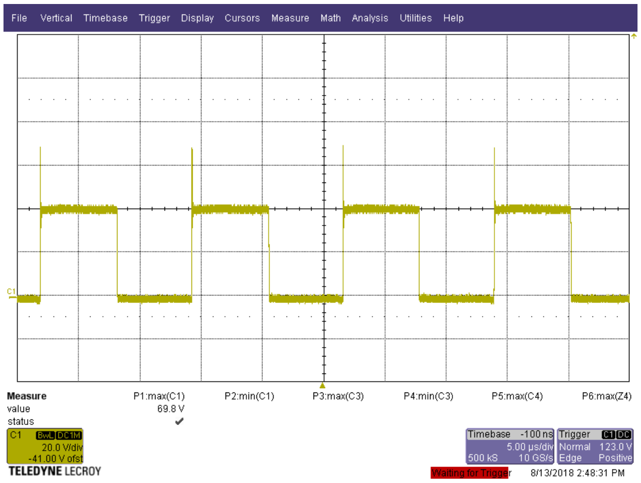

Figure 17 – SR FET Voltage Waveforms.
90 VAC, 100% Load, (69.8 V_{MAX}).
C1: SR_V_{DRAIN}, 20 V / div., 5 µs / div.

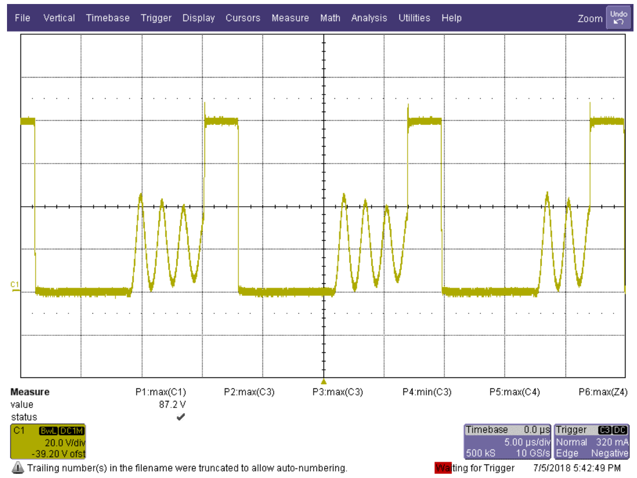

Figure 18 – SR FET Voltage Waveforms.
265 VAC, 100% Load, (87.2 V_{MAX}).
C1: SR_V_{DRAIN}, 20 V / div., 5 µs / div.

13.3 ***Output Ripple Measurements***

13.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

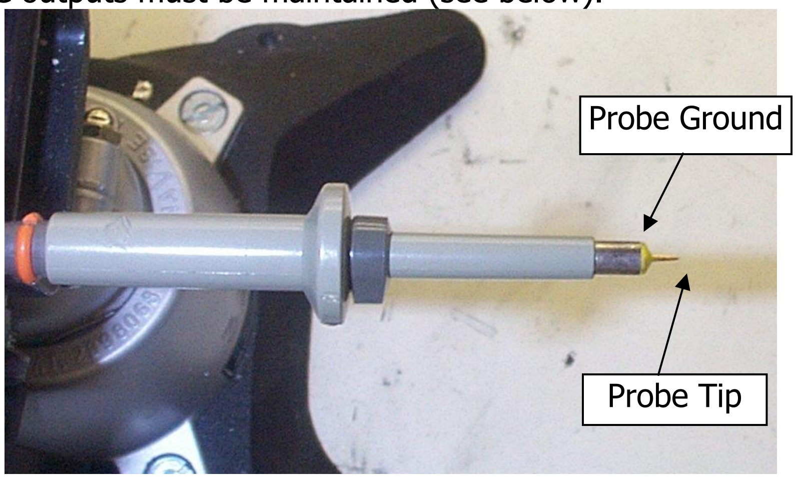

Figure 19 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

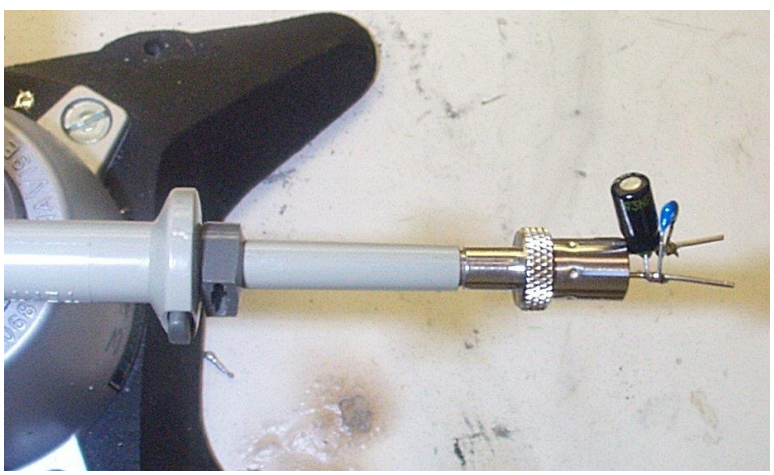

Figure 20 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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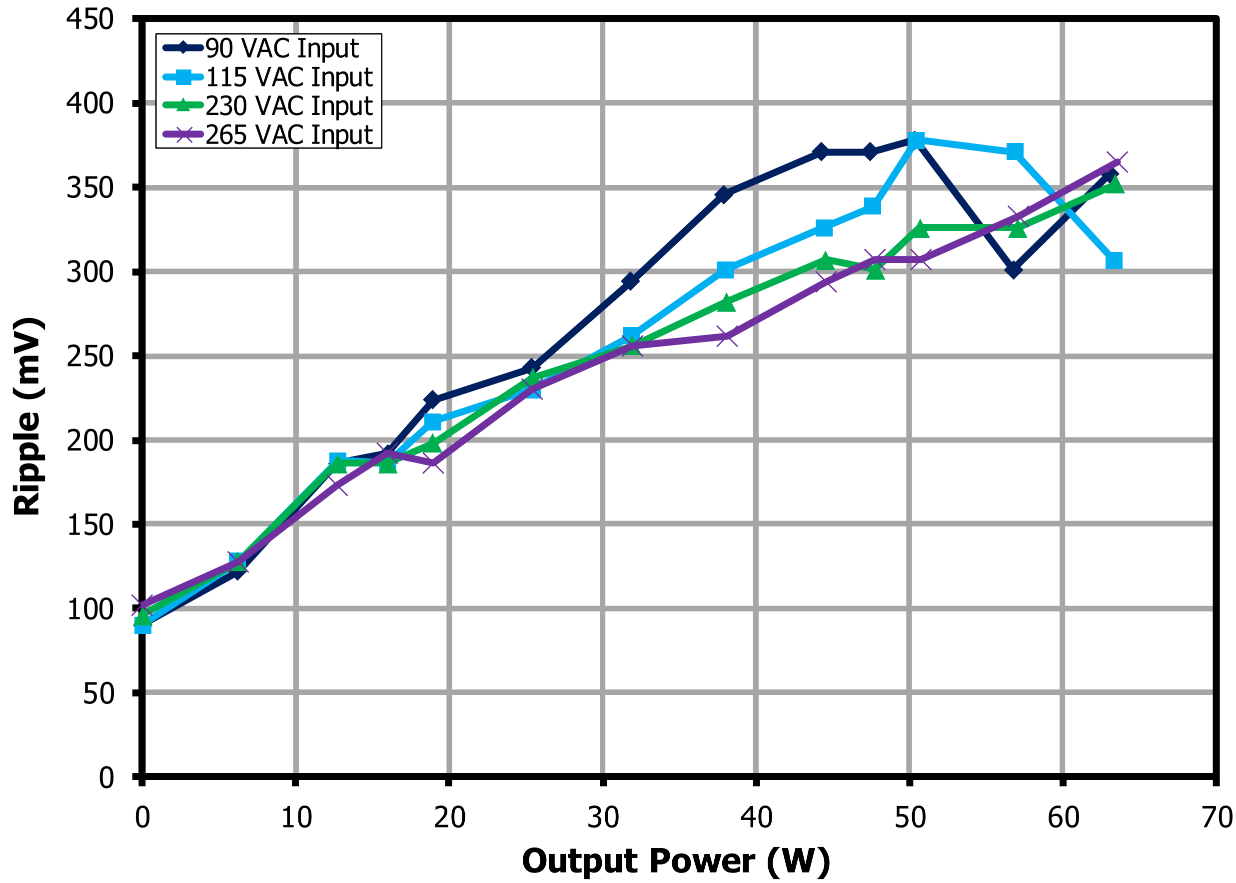
13.3.2 Ripple Amplitude vs. Line

13.3.2.1 Ripple Plot



Input	**90 VAC**	**115 VAC**	**230 VAC**	**265 VAC**
Max Ripple (mV)	378	378	352	365

Figure 21 – Ripple Amplitude vs. Output Power 20 V.

13.3.2.2 Ripple waveforms

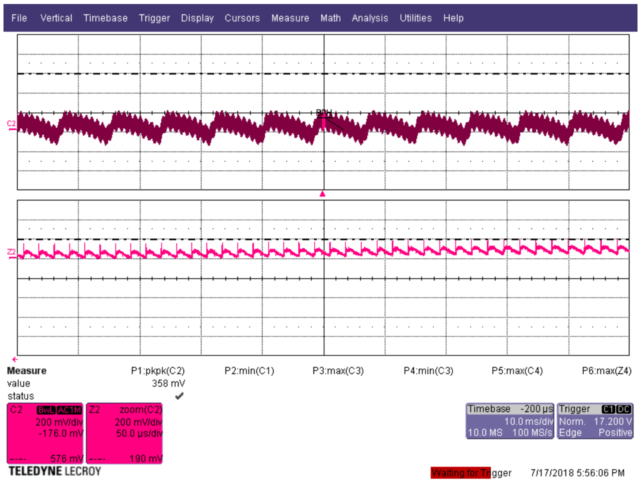


Figure 22 – Output Ripple.(PK-PK – 358 mV)
90 VAC Input, 100% Load.
V_{OUT}, 200 mV / div., 10 ms / div.

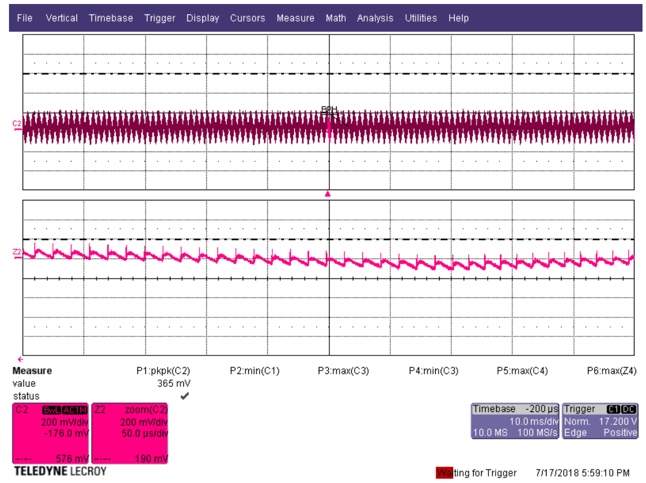


Figure 23 – Output Ripple.(PK-PK – 365 mV)
265 VAC Input, 100% Load.
V_{OUT}, 200 mV / div., 10 ms / div.

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14 **Conducted EMI**

14.1 **Floating Output (QP / AV)**

14.1.1 20 V, 100% Load

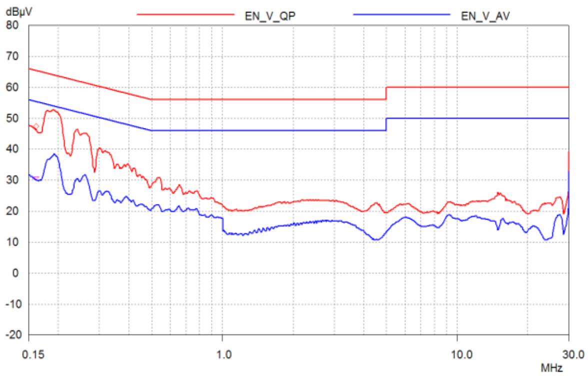

Figure 24 – Floating Ground EMI (Neutral), 20 V / 100% Load for 115 VAC.

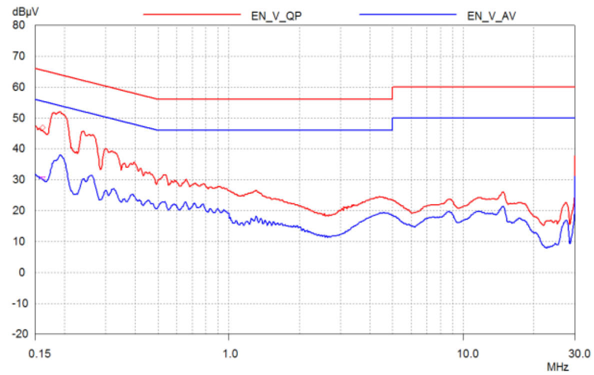

Figure 25 – Floating Ground EMI (Line), 20 V / 100% Load for 115 VAC.

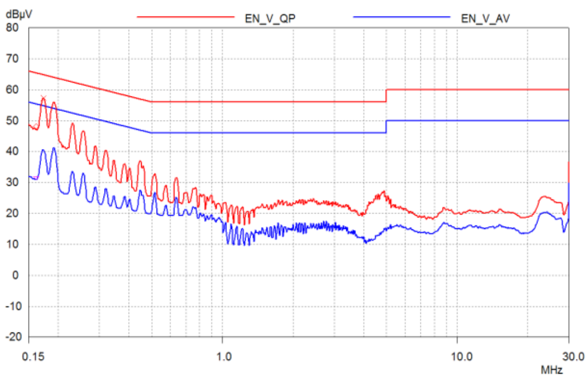

Figure 26 – Floating Ground EMI (Neutral), 20 V / 100% Load for 230 VAC.

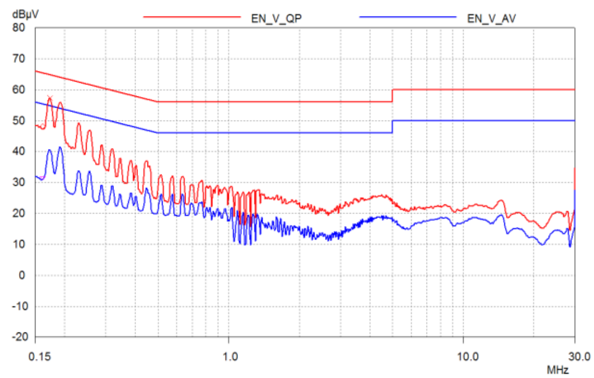

Figure 27 – Floating Ground EMI (Line), 20 V / 100% Load for 230 VAC.

14.2 **Earth Ground (QP / AV)**

14.2.1 20 V, 100% Load

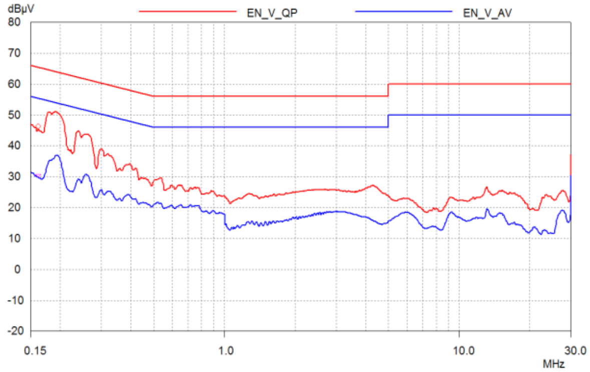

Figure 28 – Earth Ground EMI (Neutral), 20 V / 100% Load for 115 V AC.

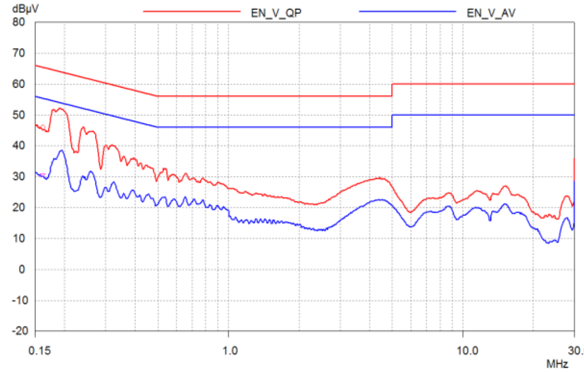

Figure 29 – Earth Ground EMI (Line), 20 V / 100% Load for 115 V AC.

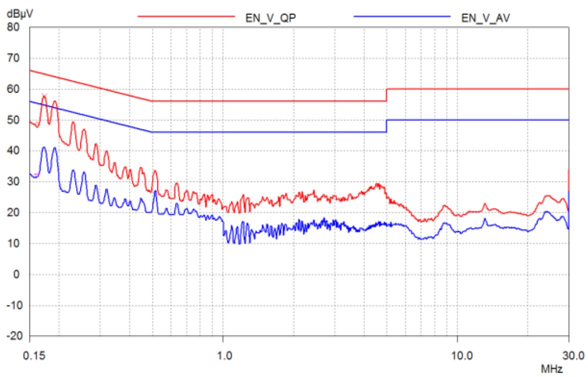

Figure 30 – Earth Ground EMI (Neutral), 20 V / 100% Load for 230 V AC.

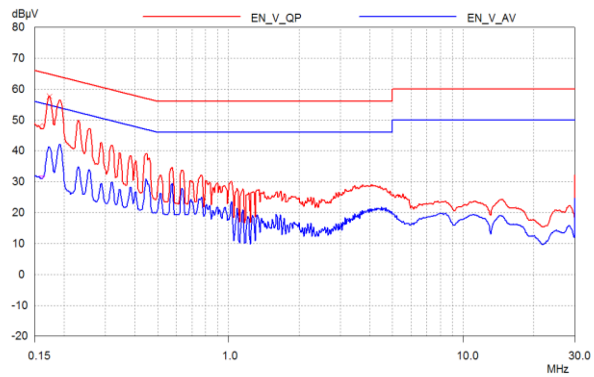

Figure 31 – Earth Ground EMI (Line), 20 V / 100% Load for 230 V AC.

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15 Line Surge

15.1 *Combination Wave Differential Mode Test*

Passed ±1 kV.

Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (W)	Number of Strikes	Test Result
±1	0	2	10	PASS
±1	90	2	10	PASS
±1	180	2	10	PASS
±1	270	2	10	PASS

Note: Input line OVP gets triggered when the test is done at no-load.

16 ESD

Passed ±16.5 kV air discharge and ±8.8 kV contact discharge at both output positive and negative terminals, under both full-load and no-load conditions.

Air Discharge (kV)	Number of Strikes	Test Result
+16.5	10	PASS
-16.5	10	PASS

Contact Discharge (kV)	Number of Strikes	Test Result
+8.8	10	PASS
-8.8	10	PASS

17 Revision History

Date	Author	Revision	Description & Changes	Reviewed
24-Jul-19	Haibo Li	1.0	Initial Release.	Apps & Mktg
23-Jun-20	KM	1.1	Converted to RDR.	Apps & Mktg

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