Design Example Report

Title	***100 W USB PD 3.0 Power Supply With 3.3 V – 21V PPS Output Using InnoSwitch™ 3-Pro GaN-based INN3370C-H302 and VIA Labs VP302***
Specification	90 VAC – 265 VAC Input; 3.3 V / 5 A, 5 V / 5 A, 9 V / 5 A, 15 V / 5 A, 20 V / 5 A or 3.3 V ~ 21 V / 5 A PPS Outputs
Application	Mobile Phone/Tablet/Laptop Adapter
Author	Applications Engineering Department
Document Number	RDR-805
Date	September 23, 2020
Revision	1.5

Summary and Features

- InnoSwitch3-Pro is industry first AC/DC IC with isolated, safety rated integrated feedback controller
- All the benefits of secondary-side control with the simplicity of primary-side regulation
    - Insensitive to transformer variation
    - Built in synchronous rectification for high efficiency
- Meets DOE6 and CoC Tier 2 V5 2016
- <50 mW no-load input power at 230 VAC
- Primary sensed overvoltage protection
- Very high power density using GaN switch
    - 14.5 W / inch^3 without enclosure
- Very low component count
    - EMI filter and PFC stage – 44 components
    - Flyback stage - 52 components
    - USB PD controller stage - 14 components

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- Very high average efficiency
  - 3.3 V Output – 89.33% at 115 VAC and 87.14% at 230 VAC
  - 5 V Output – 91.53% at 115 VAC and 91.49% at 230 VAC
  - 9 V Output – 91.96% at 115 VAC and 92.59% at 230 VAC
  - 15 V Output – 90.80% at 115 VAC and 90.48% at 230 VAC
  - 20 V Output – 91.09% at 115 VAC and 91.17% at 230 VAC

Table of Contents

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 3.3 V – 21 V / 5 A PPS output USB Type-C and USB PD charger using the HiperPFS-4 PFS7628C PFC controller, InnoSwitch3-Pro flyback controller and VIA Labs VP302 USB Type-C USB PD controller. This design shows the high power density and efficiency that is possible due to the high level of integration of the HiperPFS-4 and InnoSwitch3-Pro controllers.

The report contains the power supply specification, schematic diagram, printed circuit board layout, bill of materials, magnetics, adapter case, and heat spreader specifications, and performance data.

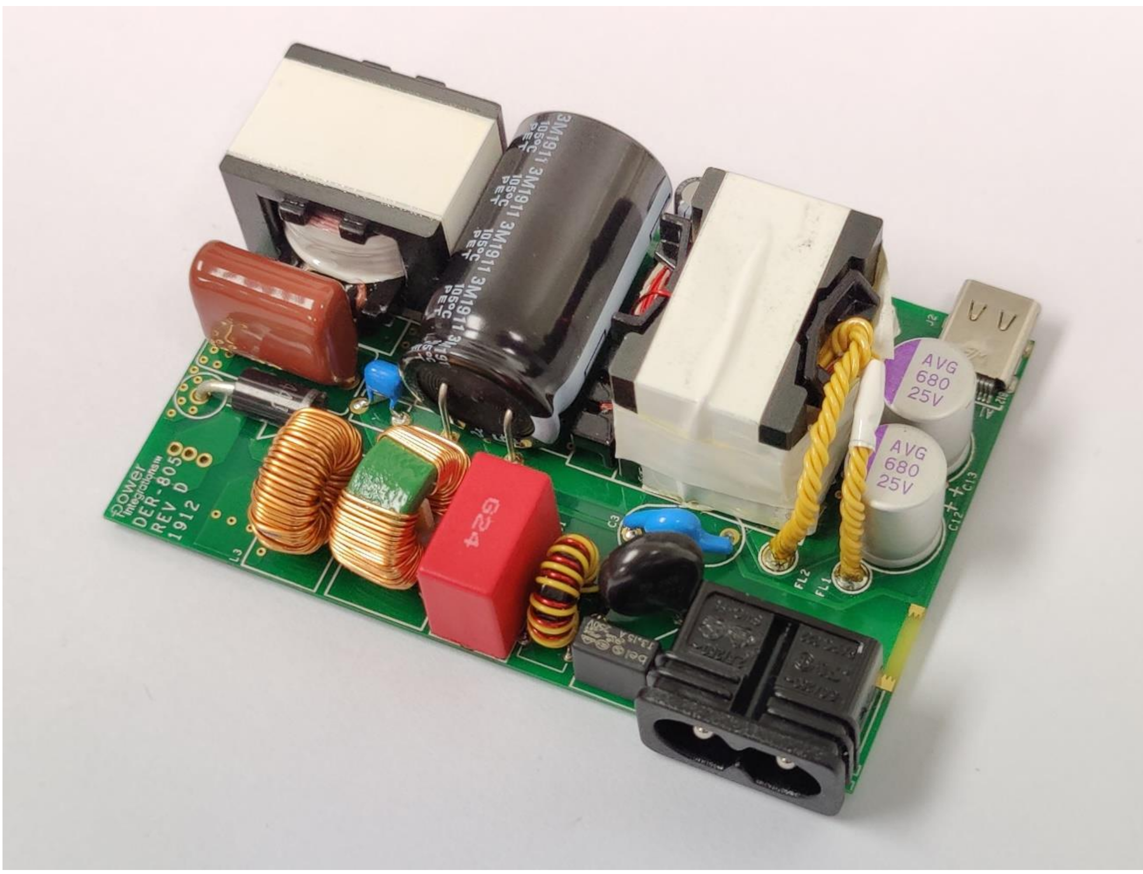

Figure 1 – Populated Circuit Board Photograph.

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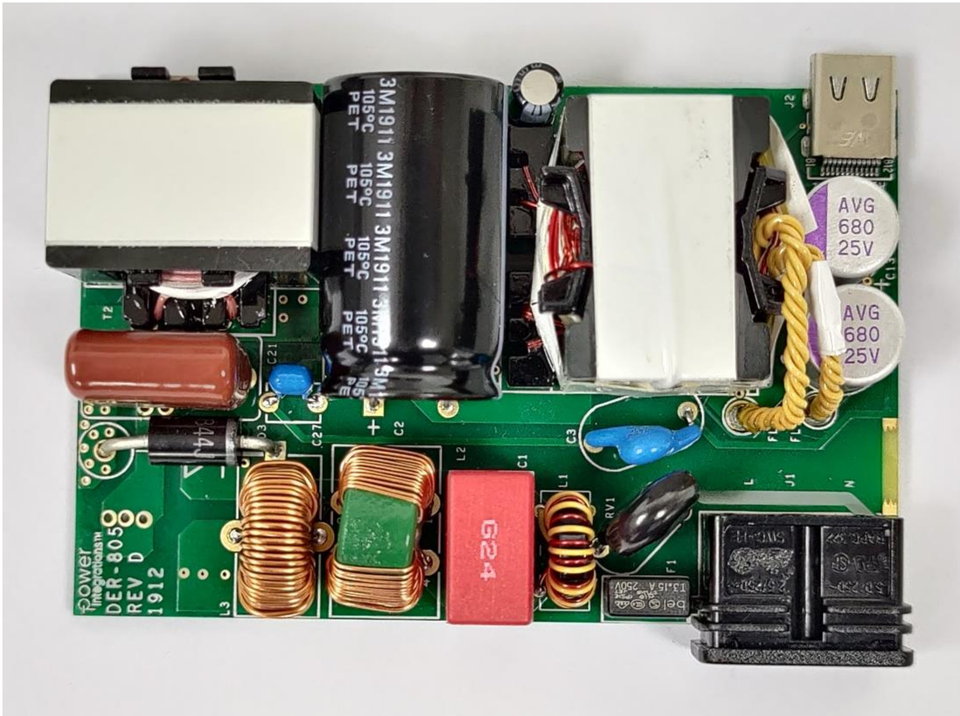

Figure 2 – Populated Circuit Board Photograph, Top.

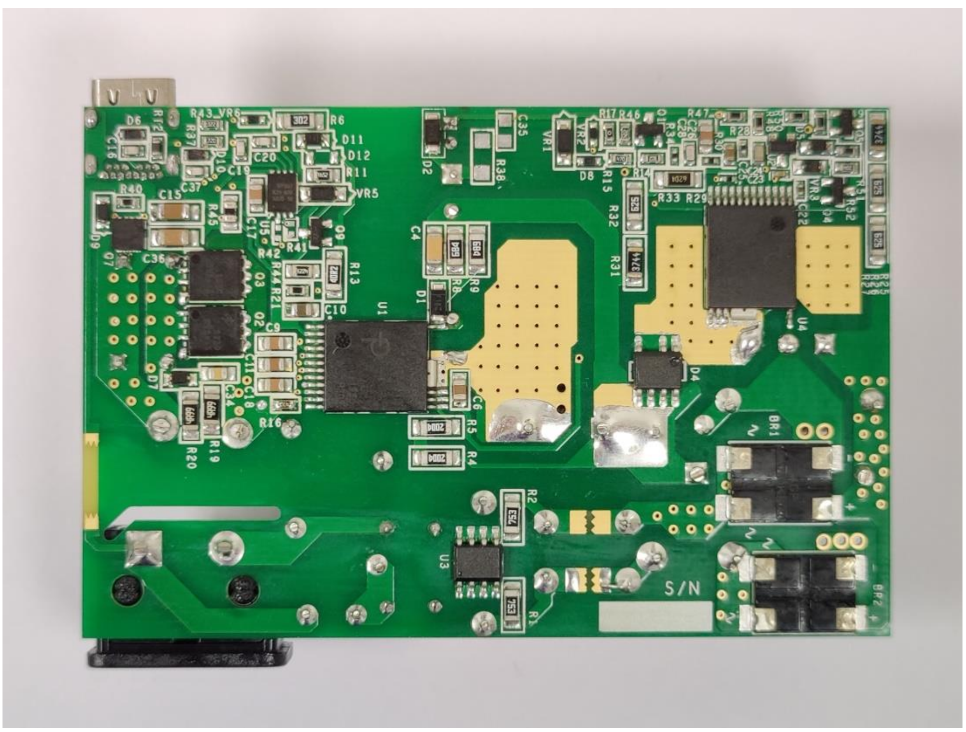

Figure 3 – Populated Circuit Board Photograph, Bottom.

Figure 4 – Enclosed Power Supply Unit Photograph.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				45	mW	Measured at 230 VAC.
3.3 V Output						
Output Voltage	V_{OUT1}		3.3		V	±3%
Output Ripple Voltage	$V_{RIPPLE1}$			300	mV	On board
Output Current	I_{OUT1}	5			A	On board
5 V Output						
Output Voltage	V_{OUT1}		5		V	±3%
Output Ripple Voltage	$V_{RIPPLE1}$			300	mV	On board
Output Current	I_{OUT1}	5			A	On board
9 V Output						
Output Voltage	V_{OUT1}		9		V	±3%
Output Ripple Voltage	$V_{RIPPLE1}$			300	mV	On board
Output Current	I_{OUT1}	5			A	On board
15 V Output						
Output Voltage	V_{OUT1}		15		V	±3%
Output Ripple Voltage	$V_{RIPPLE1}$			300	mV	On board
Output Current	I_{OUT1}	5			A	On board
20 V Output						
Output Voltage	V_{OUT1}		20		V	±3%
Output Ripple Voltage	$V_{RIPPLE1}$			300	mV	On board
Output Current	I_{OUT1}	5			A	On board
Continuous Output Power	P_{OUT}	100			W	
Maximum Programmable Output Voltage	V_{OUT}	21			V	APDO Maximum Voltage .
Minimum Programmable Output Voltage	V_{OUT}	3.3			V	APDO Minimum Voltage.
PPS Voltage Step	V_{OUT}		20		mV	PPS Voltage Step (USB PD 3.0).
PPS Current Step	I_{OUT}		50		mA	PPS current Step (USB PD 3.0).
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC60950 / UL1950 Class II				
Ambient Temperature	T_{AMB}	0		40	^{o}C	Enclosed in adapter, sea level.

3 Schematic

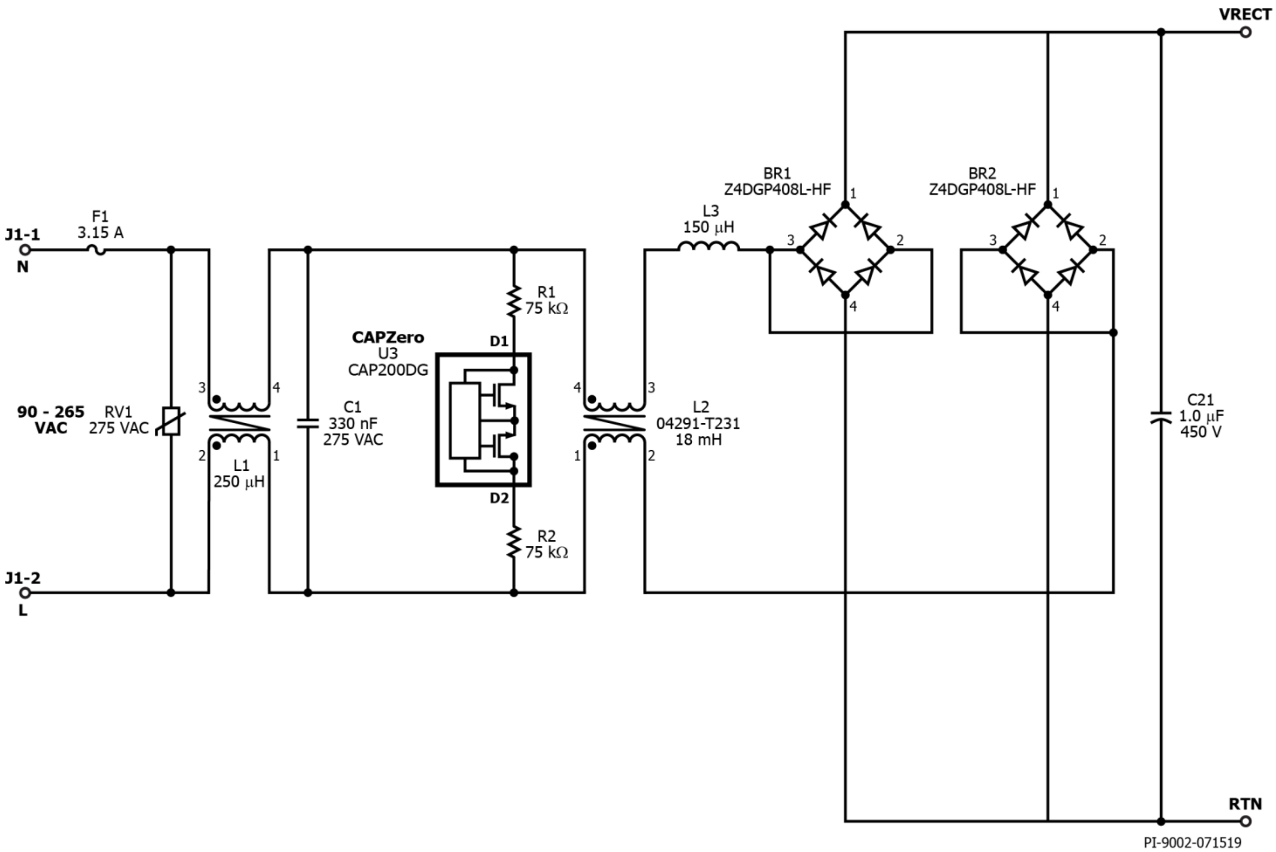

Figure 5 – Input protection and EMI Filter stage schematic

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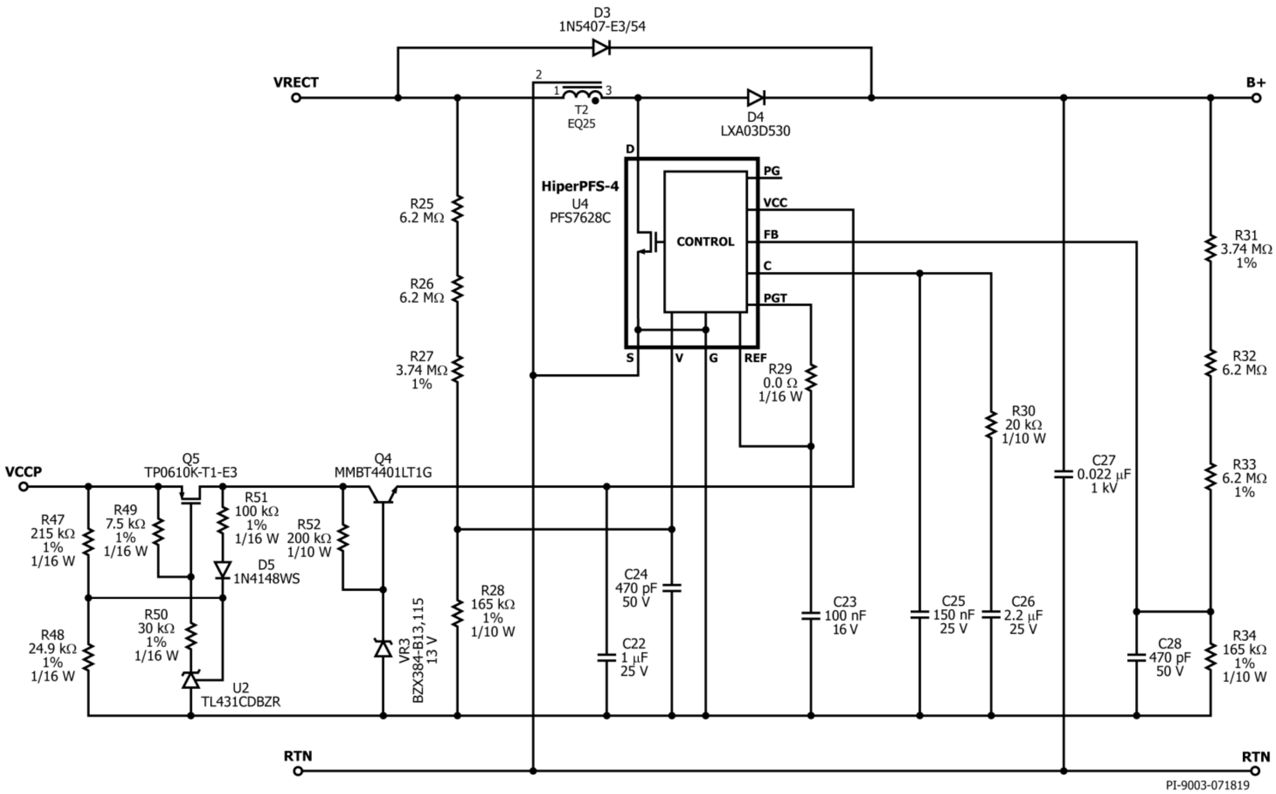

Figure 6 – PFC Stage Schematic.

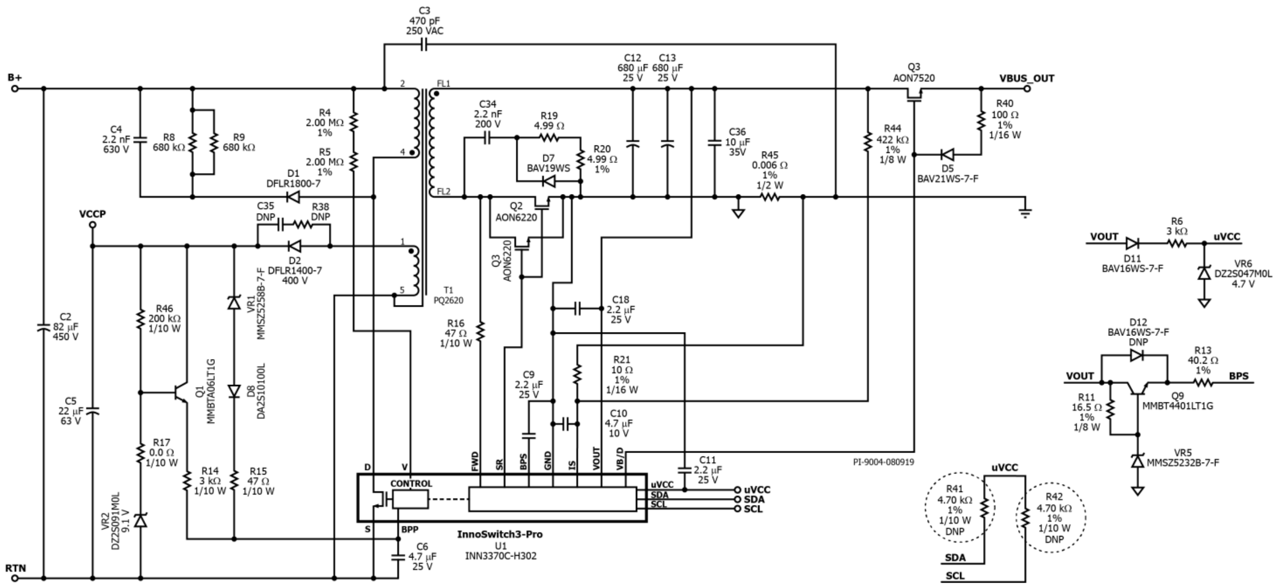

Figure 7 – Flyback Stage Schematic.

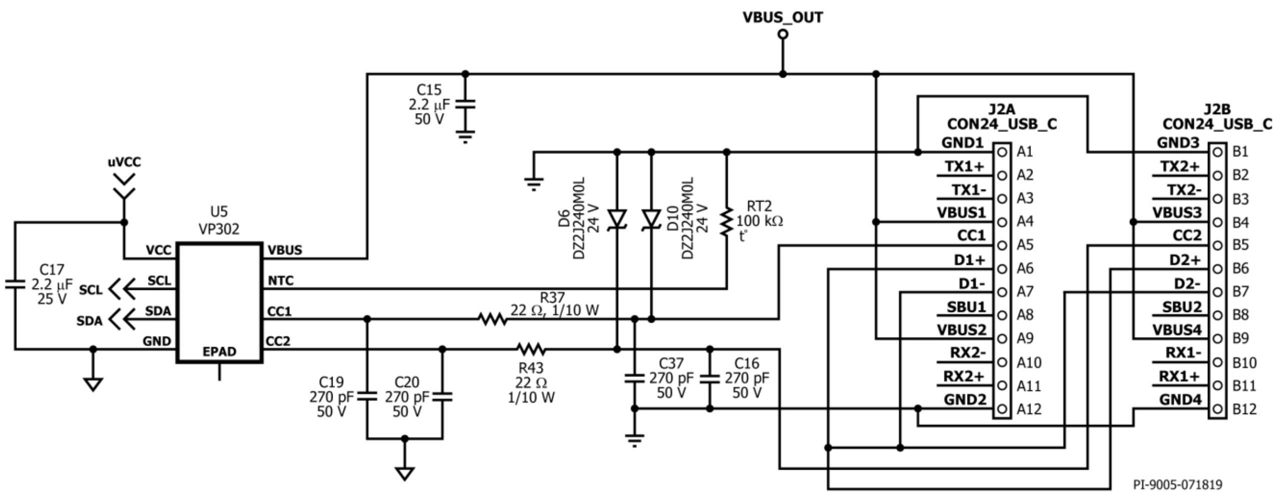

Figure 8 – USBD PD Controller Stage Schematic.

Note: Do not populate R38, R41, R42, C35 and D12.

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4 Circuit Description

4.1 *Input EMI Filtering*

Fuse F1 isolates the circuit and provides protection from component failure and the common mode chokes L1, L2 and differential mode choke L3 along with capacitors C1 and C21 attenuation for EMI. Capacitor C3 is used to reduce common mode noise on the power supply. Bridge rectifiers BR1 and BR2 rectifies the AC line voltage and provides a full wave rectified DC. Film capacitor C21 provides input decoupling charge storage to reduce input ripple current at the switching frequencies and harmonics.

Resistors R1 and R2 along with U3 discharges capacitor C1 when the power supply is disconnected from AC mains.

Metal oxide varistor (MOV) RV1 protects the circuit during line surge events by effectively clamping the input voltage seen by the power supply.

4.2 *PFS7628C Boost Converter*

The boost converter stage consists of the boost inductor T2 and the PFS7628C IC U4. This converter stage operates as a PFC boost converter, thereby maintaining a sinusoidal input current to the power supply while regulating the output DC voltage.

Boost diode D4 is a Qspeed X-Series LXA03D530 for cost effective solution with balanced EMI and switching speed performance.

During start-up, diode D3 provides an inrush current path to the output capacitor C2, bypassing the switching inductor T2 and switch U4 in order to prevent a resonant interaction between the switching inductor and output capacitor.

Capacitor C27 provide a short, high-frequency return path to RTN for improved EMI results and to reduce U4 MOSFET Drain voltage overshoot during turn-off. Capacitor C22 decouples and bypasses the U4 VCC pin.

Resistor R29 programs the output voltage level [via the POWER GOOD THRESHOLD (PGT) pin] below which the POWER GOOD pin will go into a high-impedance state.

Capacitor C23 on the REF pin of U4 is a noise decoupler for the internal reference and also programs the output power for either full mode, 100% of rated power [C23 = 1 μF] or efficiency mode, 80% [C23 = 0.1 μF] of rated power.

4.3 *PFC Input Feed Forward Sense Circuit*

The input voltage of the power supply is sensed by the IC U4 using resistors R25, R26, R27 and R28. The capacitor C24 bypasses the V pin on IC U4.

4.4 *PFC Output Feedback*

An output voltage resistive divider network consisting of resistors R31, R32, R33, and R34 provide a scaled voltage proportional to the output voltage as feedback to the controller IC U4 setting the PFC output at 380V. Capacitor C28 decouples the U4 FB pin.

Resistor R30 and capacitor C26 provide the control loop dominant pole. C25 attenuates high-frequency noise.

4.5 *Bias Supply with Hysteresis Control to PFC IC*

The PFS7628C IC requires a regulated V_{CC} supply of 12 V nominal for operation, with an absolute maximum voltage rating of 15 V. V_{CC} levels in excess of this maximum could result in failure of the IC. Resistor R47-R52, Zener diode VR3, regulator U2 and transistor Q4, Q5 form a hysteresis controlled regulator that regulates the supply voltage to IC U4 to 12.4 V nominal. Capacitor C22 decouples the input auxiliary supply voltage to ensure reliable operation of IC U4.

PFC bias supply is derived from flyback stage auxiliary output. The hysteresis circuit control Q5 to disable the PFC stage at 5 V and 9 V output to improve efficiency performance. PFC stage will start switching as output voltage exceeds 15 V operation.

4.6 *InnoSwitch3-Pro IC Primary*

One end of the transformer (T1) primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch3-Pro IC (U1). Resistors R4 and R5 provide input voltage sense protection for under voltage and over voltage conditions.

A low cost RCD clamp formed by diode D1, resistors R8 and R9, and capacitor C4 limits the peak drain voltage of U1 at the instant of turn off of the switch inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C6) when AC is first applied. During normal operation, the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. Resistor R14 limits the current being supplied to the BPP pin of the InnoSwitch3-Pro IC (U1). A linear regulator comprising of resistor R46, R17, BJT Q1 and Zener diode VR2 prevent any change in current through R14.

Output regulation is achieved using ramp time modulation control, the frequency and the current limit (I_{LIM}) of switching cycles are adjusted based on the output load. At high load, most switching cycles are enabled have high value for I_{LIM} in the selected I_{LIM} range, and at light load or no-load most cycles are disabled and the ones enabled have low value of I_{LIM} in the selected I_{LIM} range. Once a cycle is enabled, the switch will

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remain on until the primary current ramps to the device current limit for the specific operating state.

Zener diode VR1 along with D8 and R15 offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of over voltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR1 which then causes a current to flow into the BPP pin of InnoSwitch3-Pro IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch3-Pro controller will latch off and prevent any further increase in output voltage.

4.7 **InnoSwitch3-Pro IC Secondary**

The secondary-side of the InnoSwitch3-Pro IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification. The secondary of the transformer is rectified by MOSFETS Q2, Q3 and filtered by capacitors C12 and C13. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a RCD snubber R19, C34 and D7. Diode D7 was used to minimize the dissipation in resistor R19.

The gate of Q2 and Q3 is turned on by secondary-side controller inside IC U1, based on the winding voltage sensed via resistor R16 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the MOSFET is turned off just prior to the secondary-side commanding a new switching cycle to the primary. In discontinuous mode of operation, the power MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold of approximately 3 mV. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectification.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage through resistor R16 or the output voltage. Capacitor C9 connected to the BPS pin of InnoSwitch3-Pro IC U1 provides decoupling for the internal circuitry.

Output current is sensed by monitoring the voltage drop across resistor R45 between the IS and GND pins with a threshold of approximately 32 mV to reduce losses. Resistor R21 and capacitor C10 provides filtering on the IS pin from external noise.

Output voltage is regulated to achieve a voltage of 1.265 V on the internal FB pin. No feedback resistor divider network was used since VP302 was used to regulate the output voltage incompliance USB PD standard. Capacitor C18 is used to decouple the VOUT pin InnoSwitch3-Pro IC (U1).

The VP302 power is supplied from both sources, InnoSwitch3-Pro IC (U1) internal regulator uVcc and external D11, R6, VR6 circuit. As the output voltage increases, the external can provide a current to supply VP302 and prevent overheating the internal regulator.

4.8 USB Type-C and PD Interface

In this design, VIA Labs VP302 (U5) is the USB Type-C and PD controller. VP302 monitors PD command and sends an I^2C command to Innoswitch3-Pro IC (U1), which regulates the output voltage at required level. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation in which Type-C plug is connected.

Thermistor RT2 is used to sense USB Type-C connector temperature.

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5 PCB Layout

PCB copper thickness is 2.0 oz.

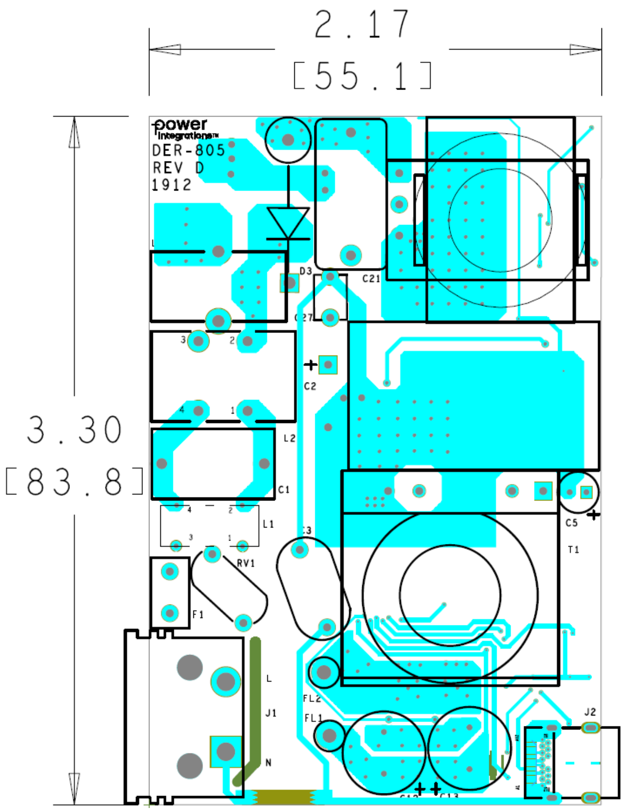

Figure 9 – Printed Circuit Layout, Top.

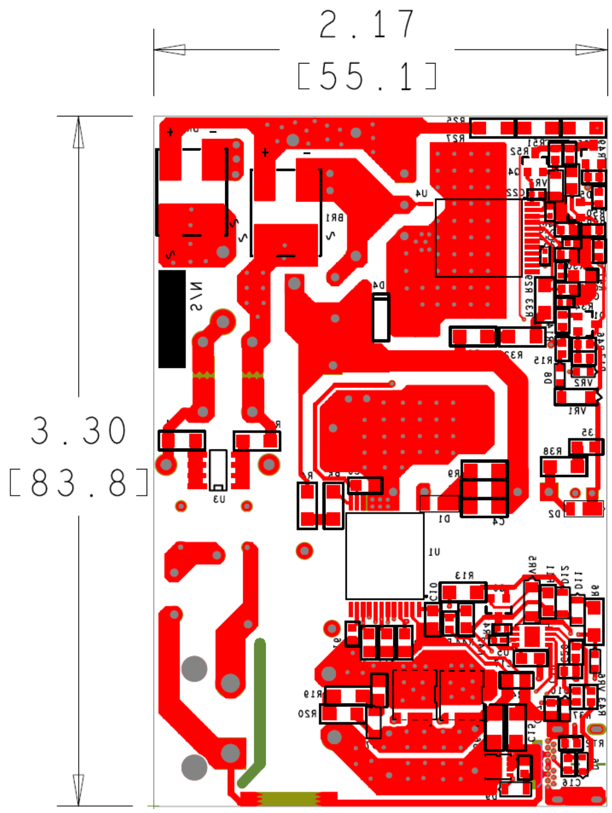

Figure 10 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	BR1 BR2	RECT BRIDGE, GP, 800 V, 4 A, Z4-D	Z4DGP408L-HF	Comchip
2	1	C1	330 nF, ±10%, 275 VAC, Polypropylene Film, X2, 15.00 mm x 8.50 mm	890324024003CS	Wurth
3	1	C2	82 μF, 450 V, Electrolytic, Low ESR, (18 x 30)	EPAG451ELL820MM30S 450BXW82MEFR18X30	Nippon Chemi-Con Rubycon
4	1	C3	470 pF, 250 VAC, Film, X1Y1	DE1B3KX471KN4AN01F	Murata
5	1	C4	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K115AA	TDK
6	1	C5	22 μF, ±20%, 63 V, Electrolytic, (5 x 12.5), LS 2 mm	63YXJ22M5X11 EWH1JM220D11OT	Rubycon Aishi
7	1	C6	4.7 μF ±10%, 25V, X7R, 0805,-55°C ~ 125°C	TMK212AB7475KG-T	Taiyo Yuden
8	5	C9 C11 C17 C18 C26	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M085AB	TDK
9	1	C10	4.7 μF, 10 V, Ceramic, X5R, 0805	C0805C475K8PACTU	Kemet
10	2	C12 C13	680 μF, ±20%, 25 V, Aluminum Polymer Capacitor Radial, Can, 292.56 mΩ, 1500 Hrs @ 125°C, (10 x 13.5)	687AVG025MGBJ	Illinois Capacitor
11	1	C15	2.2 μF, 50 V, Ceramic, Y5V, 1206	UMK316F225ZG-T UMK316B7225MD-T	Taiyo Yuden
12	4	C16 C19 C20 C37	CAP, CER, 270 pF,±5%, 50 V, Low ESL, C0G/NP0, 0603	C0603C271J5GACTU	Kemet
13	1	C21	1.0 μF, 450 V, Polyester Film	ECQ-E2W105KH	Panasonic
14	1	C22	1 μF 25 V, Ceramic, X5R, 0402	TMK105BJ105MV-F	Taiyo Yuden
15	1	C23	100 nF 16 V, Ceramic, X7R, 0402	L05B104KO5NNNC	Samsung
16	1	C24	470 pF 50 V, Ceramic, C0G/NP0, 0603	VJ0603A471JXAAC	Vishay
17	1	C25	150 nF, 25 V, Ceramic, X7R, 0603	C1608X7R1E154K080AA GCM188R71E154KA37D	TDK Murata
18	1	C27	0.022 μF, ±10%, 1KV, X7R, Radial, -55°C ~ 125°C, 0.217" L x 0.157" W (5.50 mm x 4.00 mm)	RDER73A223K3M1H03A	Murata
19	1	C28	470 pF 50 V, Ceramic, NP0, 0603	GRM1885C1H471JA01D C0603C471J5GACTU	Murata Kemet
20	1	C34	2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX
21	1	C35	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
22	1	C36	10 μF, 10%, 35 V, Ceramic, X7R, -55°C ~ 125°C, 1206	CL31B106KLHNNNE	Samsung
23	1	D1	800 V, 1 A, Rectifier, POWERDI123	DFLR1800-7	Diodes, Inc.
24	1	D2	400 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1400-7	Diodes, Inc.
25	1	D3	800 V, 3 A, Recitifier, DO-201AD	1N5407-E3/54	Vishay
26	1	D4	530 V, 3 A, D PACKAGE (SO-8C)	LXA03D530	Power Integrations
27	1	D5	DIODE, GEN PURP, 75 V 150 mA, SOD323	1N4148WS-7-F	Diodes, Inc.
28	2	D6 D10	DIODE, ZENER, 24 V, 200 mW, SC-90, SOD-323F, SMini2-F5-B	DZ2J240M0L MM3Z24VC	Panasonic On-Semi
29	1	D7	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
30	1	D8	DIODE SML SIG 80 V 100MA SSMINI2	DA2S10100L	Panasonic
31	1	D9	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
32	2	D11	75 V, 0.15 A, Switching,SOD-323	BAV16WS-7-F	Diodes, Inc.
33	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
34	2	FL1 FL2	Flying Lead , Hole size 70 mils	N/A	N/A
35	1	J1	Power Entry Connector Receptacle, Male Pins, IEC 320-C8, Non-Polarized, Panel Mount, Snap-In; TH, Right Angle	RAPC322X	Switchcraft
36	1	J2	Connector, "Certified",USB - C, USB 3.1, For 0.062" PCB Material!,Superspeed+, Receptacle	632723300011	Wurth

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			Connector, 24 Position, SMT, Right Angle, TH		
37	1	L1	250 µH, Toroidal Common Mode Choke, custom, DER-536, wound on 32-00275-00 core.	32-00367-00	Power Integrations
38	1	L2	Custom, CMC, 18mH @ 10KHz, Toroidal, 17.5 mm OD x 11.0 mm thick. 40 turns x 2, 0.40 mm wire 190 mΩ max	04291-T231	Sumida
39	1	L3	150 µH, 20%, 2.5 A , Rdc=0.01, INDUCTOR, TOROID, HI AMP, VERT, 16.5 mm Diam, 8.5 mm Thick, 8.5 mm LS	7447018	Wurth
40	1	Q1	NPN, Small Signal BJT, 80 V, 0.5 A, SOT-23	MMBTA06LT1G	On Semi
41	2	Q2 Q3	MOSFET, N-CH, 100V, 48A (Tc), 113.5W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
42	2	Q4 Q9	NPN, Small Signal BJT, GP, 40V, 600 mA, 250 MHz, 300 mW , SOT-23, SOT-23-3 (TO-236)	MMBT4401LT3G	On Semi
43	1	Q5	60 V, 0.185 A, , P-Channel, SOT 23-3	TP0610K-T1-E3	Siliconix
44	1	Q7	MOSFET, N-CH, 30 V, 21 A, 8-DFN-EP (3.3x3.3), 8-PowerWDFN	AON7520	Alpha & Omega Semi
45	2	R1 R2	RES, 75 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ753V	Panasonic
46	2	R4 R5	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
47	1	R6	RES, 3 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ302V	Panasonic
48	2	R8 R9	RES, 680 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ684V	Panasonic
49	1	R11	RES, 16.5 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1652V	Panasonic
50	1	R13	RES, 40.2 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF40R2V	Panasonic
51	1	R14	RES, 3 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ302V	Panasonic
52	2	R15 R16	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
53	1	R17	RES, 0 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic
54	2	R19 R20	RES, 4.99 Ω, 1%, 1/4 W, Thick Film, 1206	RC1206FR-074R99L	Yageo
55	1	R21	RES, 10 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF10R0V	Panasonic
56	3	R25 R26 R32	RES, 6.2 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ625V	Panasonic
57	2	R27 R31	RES, 3.74 MΩ, 1%, 1/4 W, Thick Film, 1206	CRCW12063M74FKEA	Vishay Dale
58	2	R28 R34	RES, 165.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1653X	Panasonic
59	1	R29	RES, 0 Ω, 1/16 W, Thick Film, 0402	CRCW04020000Z0ED	Panasonic
60	1	R30	RES, 20 kΩ, 5%, 1/10 W, Thick Film, 0402	ERJ-2GEJ203X	Panasonic
61	1	R33	RES, 6.2 M, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF6204	Rohm Semi
62	2	R37 R43	RES, 22 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ220V	Panasonic
63	1	R38	RES, 10 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ100V	Panasonic
64	1	R40	RES, 100 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1000V	Panasonic
65	2	R41 R42	RES, 4.70 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF4701X	Panasonic
66	1	R44	RES, 422 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4223V	Panasonic
67	1	R45	RES, 0.006 Ω, ±1%, 0.5 W, ½ W, 0805, Current Sense, Thick Film,±300ppm/°C, -55°C ~ 155°C	ERJ-6LWFR006V	Panasonic
68	2	R46 R52	RES, 200 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ204V	Panasonic
69	1	R47	RES, 215 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2153V	Panasonic
70	1	R48	RES, 24.9 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2492V	Panasonic
71	1	R49	RES, 7.5 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF7501V	Panasonic
72	1	R50	RES, 30.1 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3012V	Panasonic
73	1	R51	RES, 100 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1003V	Panasonic
74	1	RT2	NTC Thermistor, 100 kΩ, 1%, 4250K, 0603 (1608 Metric)	NCU18WF104F60RB	Murata
75	1	RV1	275 VAC, 80J, 10 mm, RADIAL	ERZ-V10D431	Panasonic
76	1	T1	Custom, DER-805 Transformer, Lp = 548uH, PQ2620, PC95 core material, Bobbin PQ-2628 Golden Bamboo Electronics Zhuhai, 6 pins, 6pri, 0sec		Power Integrations
77	1	T2	Custom, DER-805 PFC Inductor, Lp = 650uH, EQ25, 3C95 core material, Bobbin TBI-235-		Power Integrations

			01091.1206, 4 pins, 4pri, 0sec		
78	1	U1	InnoSwitchPro, InSOP24D	INN3370C-H302	Power Integrations
79	1	U2	IC, Shunt Regulator Adj.,2.495V, 2.2%, 100mA, 0°C ~ 70°C (TA), SOT23-3, TO-236-3, SC-59, SOT-23-3	TL431CDBZR	Texas Instruments
80	1	U3	CAPZero-2, SO-8C	CAP200DG	Power Integrations
81	1	U4	HiperPFS-4, InSOP24B	PFS7628C	Power Integrations
82	1	U5	IC, USB PD Type-C Controller for SMPS, DFN-8	VP302	VIA Labs
83	1	VR1	DIODE ZENER 36 V 500 mW SOD123	MMSZ5258B-7-F	Diodes, Inc.
84	1	VR2	9.1 V, 5%, 150 mW, SSMINI-2	DZ2S091M0L EDZVT2R9.1B	Panasonic Rohm
85	1	VR3	13 V, 2%, 300 mW, SOD-323	BZX384-B13,115	NXP Semi
86	1	VR5	DIODE ZENER 5.6 V 500 mW SOD123	MMSZ5232B-7-F	Diodes, Inc.
87	1	VR6	4.7 V, 5%, 150 mW, SSMINI-2	DZ2S047M0L EDZVT2R4.7B	Panasonic Rohm

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7 PFC Inductor Design Spreadsheet(T2)

1	Hiper_PFS-4_Boost_051319; Rev.1.2; Copyright Power Integrations 2019	INPUT	INFO	OUTPUT	UNITS	Continuous Mode Boost Converter Design Spreadsheet
2	**Enter Application Variables**					
3	Input Voltage Range	Universal		Universal		Input voltage range
4	VACMIN	90		90	VAC	Minimum AC input voltage. Spreadsheet simulation is performed at this voltage. To examine operation at other votlages, enter here, but enter fixed value for LPFC_ACTUAL.
5	VACMAX			265	VAC	Maximum AC input voltage
6	VBROWNIN		Info	78	VAC	Brown-IN voltage has been modified since the V-pin ratio is no longer 100:1
7	VBROWNOUT		Info	68	VAC	Brown-OUT voltage has been modified since the V-pin ratio is no longer 100:1
8	VO	380	Info	380	VDC	Brown IN/OUT voltage has changed due to modifications in the V-pin ratio from 100:1. Recommend Vpin ratio= FB pin ratio for optimized operation. Check the PF, input current distortion, brown in/out and power delivery
9	PO	105		105	W	Nominal Output power
10	fL	60		60	Hz	Line frequency
11	TA Max			40	°C	Maximum ambient temperature
12	Efficiency Estimate	0.95		0.95		Enter the efficiency estimate for the boost converter at VACMIN. Should approximately match calculated efficiency in Loss Budget section
13	VO_MIN			361	VDC	Minimum Output voltage
14	VO_RIPPLE_MAX			20	VDC	Maximum Output voltage ripple
15	T_HOLDUP	20		20	ms	Holdup time
16	VHOLDUP_MIN	280		280	VDC	Minimum Voltage Output can drop to during holdup
17	I_INRUSH			40	A	Maximum allowable inrush current
18	Forced Air Cooling	No		No		Enter "Yes" for Forced air cooling. Otherwise enter "No". Forced air reduces acceptable choke current density and core autopick core size
20	**KP and INDUCTANCE**					
21	KP_TARGET			0.60		Target ripple to peak inductor current ratio at the peak of VACMIN. Affects inductance value
22	LPFC_TARGET (0 bias)			1223	uH	PFC inductance required to hit KP_TARGET at peak of VACMIN and full load
23	LPFC_DESIRED (0 bias)	650		650	uH	LPFC value used for calculations. Leave blank to use LPFC_TARGET. Enter value to hold constant (also enter core selection) while changing VACMIN to examine brownout operation. Calculated inductance with rounded (integral) turns for powder core.
24	KP_ACTUAL			0.896		Actual KP calculated from LPFC_DESIRED
25	LPFC_PEAK			650	uH	Inductance at VACMIN and maximum bias current. For Ferrite, same as LPFC_DESIRED (0 bias)
27	**Basic current parameters**					
28	IAC_RMS			1.23	A	AC input RMS current at VACMIN and Full Power load
29	IO_DC			0.28	A	Output average current/Average diode

						current
32	**PFS Parameters**					
33	PFS Package	C		C		HiperPFS package selection
34	PFS Part Number	PFS7628C		PFS7628C		If examining brownout operation, over-ride autopick with desired device size
35	Operating Mode	Efficiency	Warning	Efficiency		C Package Only Supports Full Power Mode
36	IOCP min			3.15	A	Minimum Current limit
37	IOCP typ			3.33	A	Typical current limit
38	IOCP max			3.47	A	Maximum current limit
39	IP			3.13	A	MOSFET peak current
40	IRMS			1.23	A	PFS MOSFET RMS current
41	RDSON			0.39	Ohms	Typical RDSon at 100 'C
42	FS_PK			46.4	kHz	Estimated frequency of operation at crest of input voltage (at VACMIN)
43	FS_AVG			39.4	kHz	Estimated average frequency of operation over line cycle (at VACMIN)
44	PCOND_LOSS_PFS			0.589	W	Estimated PFS conduction losses
45	PSW_LOSS_PFS			0.630	W	Estimated PFS switching losses
46	PFS_TOTAL			1.219	W	Total Estimated PFS losses
47	TJ Max			100	deg C	Maximum steady-state junction temperature
48	Rth-JS			2.80	°C/W	Maximum thermal resistance (Junction to heatsink)
49	HEATSINK Theta-CA			46.42	°C/W	Maximum thermal resistance of heatsink
52	**INDUCTOR DESIGN**					
53	**Basic Inductor Parameters**					
54	LPFC (0 Bias)			650	uH	Value of PFC inductor at zero current. This is the value measured with LCR meter. For powder, it will be different than LPFC.
55	LP_TOL	5.0		5.0	%	Tolerance of PFC Inductor Value (ferrite only)
56	IL_RMS			1.44	A	Inductor RMS current (calculated at VACMIN and Full Power Load)
57	**Material and Dimensions**					
58	Core Type	Ferrite		Ferrite		Enter "Sendust", "Iron Powder" or "Ferrite"
59	Core Material	Auto		PC44/PC95		Select from 60u, 75u, 90u or 125 u for Sendust cores. Fixed at PC44/PC95 for Ferrite cores. Fixed at -52 material for Pow Iron cores.
60	Core Geometry	EQ		EQ		Toroid only for Sendust and Powdered Iron; EE or PQ for Ferrite cores.
61	Core	EQ25/I		EQ25/I		Core part number
62	Ae	100.00		100.00	mm^2	Core cross sectional area
63	Le	41.40		41.40	mm	Core mean path length
64	AL	4400.00		4400.00	nH/t^2	Core AL value
65	Ve	4.15		4.15	cm^3	Core volume
66	HT (EE/PQ/EQ/RM/POT) / ID (toroid)	4.95		4.95	mm	Core height/Height of window; ID if toroid
67	MLT	57.0		57.0	mm	Mean length per turn
68	BW	8.10		8.10	mm	Bobbin width
69	LG			0.61	mm	Gap length (Ferrite cores only)
70	**Flux and MMF calculations**					
71	BP_TARGET (ferrite only)	4000	Info	4000	Gauss	Info: Peak flux density is too high. Check for Inductor saturation during line transient operation
72	B_OCP (or BP)			3947	Gauss	Target flux density at worst case: IOCP and maximum tolerance inductance (ferrite only) - drives turns and gap
73	B_MAX			3385	Gauss	Peak flux density at AC peak, VACMIN and

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						Full Power Load, nominal inductance,minimum IOCP
74	µ_TARGET (powder only)			N/A	%	target µ at peak current divided by µ at zero current, at VACMIN, full load (powder only) - drives auto core selection
75	µ_MAX (powder only)			N/A	%	actual µ at peak current divided by µ at zero current, at VACMIN, full load (powder only)
76	µ_OCP (powder only)			N/A	%	µ at IOCPtyp divided by µ at zero current
77	I_TEST			3.3	A	Current at which B_TEST and H_TEST are calculated, for checking flux at a current other than IOCP or IP; if blank IOCP_typ is used.
78	B_TEST			3788	Gauss	Flux density at I_TEST and maximum tolerance inductance
79	µ_TEST (powder only)			N/A	%	µ at IOCP divided by µ at zero current, at IOCPtyp
80	**Wire**					
81	TURNS			61		Inductor turns. To adjust turns, change BP_TARGET (ferrite) or µ_TARGET (powder)
82	ILRMS			1.44	A	Inductor RMS current
83	Wire type	Litz		Litz		Select between "Litz" or "Magnet" for double coated magnet wire
84	AWG	42		42	AWG	Inductor wire gauge
85	Filar	75		75		Inductor wire number of parallel strands. Leave blank to auto-calc for Litz
86	OD (per strand)			0.064	mm	Outer diameter of single strand of wire
87	OD bundle (Litz only)			0.77	mm	Will be different than OD if Litz
88	DCR			0.321	ohm	Choke DC Resistance
89	P AC Resistance Ratio			1.06		Ratio of total copper loss, including HF AC, to the DC component of the loss
90	J		Warning	6.08	A/mm^2	Current density is high, if copper loss is high use thicker wire, more strands, or larger core
91	FIT			84	%	Percentage fill of winding window for EE/PQ core. Full window approx. 90%
92	Layers			6.01		Estimated layers in winding
93	**Loss calculations**					
94	BAC-p-p			3035	Gauss	Core AC peak-peak flux excursion at VACMIN, peak of sine wave
95	LPFC_CORE_LOSS			0.126	W	Estimated Inductor core Loss
96	LPFC_COPPER_LOSS			0.708	W	Estimated Inductor copper losses
97	LPFC_TOTAL_LOSS			0.835	W	Total estimated Inductor Losses
100	**External PFC Diode**					
101	PFC Diode Part Number	LXA03D530		LXA03D530		PFC Diode Part Number
102	Type / Part Number			Qspeed		PFC Diode Type / Part Number
103	Manufacturer			PI		Diode Manufacturer
104	VRRM			530.0	V	Diode rated reverse voltage
105	IF			3.00	A	Diode rated forward current
106	Qrr			75.0	nC	Qrr at High Temperature
107	VF			1.33	V	Diode rated forward voltage drop
108	PCOND_DIODE			0.394	W	Estimated Diode conduction losses
109	PSW_DIODE			0.068	W	Estimated Diode switching losses
110	P_DIODE			0.462	W	Total estimated Diode losses
111	TJ Max			100.0	deg C	Maximum steady-state operating temperature
112	Rth-JS		Info	27.00	degC/W	Rth too high. Will result in high diode loss
113	HEATSINK Theta-CA			102.40	degC/W	Maximum thermal resistance of heatsink

114	IFSM			25.0	A	Non-repetitive peak surge current rating. Consider larger size diode if inrush or thermal limited.
117	**Output Capacitor**					
118	COUT	82		82	uF	Minimum value of Output capacitance
119	VO_RIPPLE_EXPECTED			9.4	V	Expected ripple voltage on Output with selected Output capacitor
120	T_HOLDUP_EXPECTED			25.8	ms	Expected holdup time with selected Output capacitor
121	ESR_LF			2.93	ohms	Low Frequency Capacitor ESR
122	ESR_HF		Warning	1.17	ohms	High frequency ESR must be between 0.01 and 1 ohms
123	IC_RMS_LF			0.20	A	Low Frequency Capacitor RMS current
124	IC_RMS_HF			0.66	A	High Frequency Capacitor RMS current
125	CO_LF_LOSS			0.114	W	Estimated Low Frequency ESR loss in Output capacitor
126	CO_HF_LOSS			0.507	W	Estimated High frequency ESR loss in Output capacitor
127	Total CO LOSS			0.621	W	Total estimated losses in Output Capacitor
130	**Input Bridge (BR1) and Fuse (F1)**					
131	I^2t Rating			5.76	A^2*s	Minimum I^2t rating for fuse
132	Fuse Current rating			1.98	A	Minimum Current rating of fuse
133	VF			0.90	V	Input bridge Diode forward Diode drop
134	IAVG			1.23	A	Input average current at VBROWNOUT.
135	PIV_INPUT BRIDGE			375	V	Peak inverse voltage of input bridge
136	PCOND_LOSS_BRIDGE			1.990	W	Estimated Bridge Diode conduction loss
137	CIN	1.00		1.00	uF	Input capacitor. Use metallized polypropylene or film foil type with high ripple current rating
138	CIN_DF			0.001		Input Capacitor Dissipation Factor (tan Delta)
139	CIN_PLOSS			0.008	W	Input Capacitor Loss
140	RT1			9.37	ohms	Input Thermistor value
141	D_Precharge			1N5407		Recommended precharge Diode
144	**PFS4 small signal components**					
145	C_REF			0.1	uF	REF pin capacitor value
146	RV1			4.0	MOhms	Line sense resistor 1
147	RV2			6.0	MOhms	Line sense resistor 2
148	RV3			6.0	MOhms	Typical value of the lower resistor connected to the V-PIN. Use 1% resistor only!
149	RV4			163.8	kOhms	Description pending, could be modified based on feedback chain R1-R4
150	C_V			0.489	nF	V pin decoupling capacitor (RV4 and C_V should have a time constant of 80us) Pick the closest available capacitance.
151	C_VCC			1.0	uF	Supply decoupling capacitor
152	C_C			100	nF	Feedback C pin decoupling capacitor
153	Power good Vo lower threshold VPG(L)			333	V	Vo lower threshold voltage at which power good signal will trigger
154	PGT set resistor			337.4	kohm	Power good threshold setting resistor
157	**Feedback Components**					
158	RFB_1			4.00	Mohms	Feedback network, first high voltage divider resistor
159	RFB_2			6.00	Mohms	Feedback network, second high voltage divider resistor
160	RFB_3			6.00	Mohms	Feedback network, third high voltage divider resistor

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161	RFB_4			163.8	kohms	Feedback network, lower divider resistor
162	CFB_1			0.489	nF	Feedback network, loop speedup capacitor. (R4 and C1 should have a time constant of 80us) Pick the closest available capacitance.
163	RFB_5			29.4	kohms	Feedback network: zero setting resistor
164	CFB_2			1000	nF	Feedback component- noise suppression capacitor
167	**Loss Budget (Estimated at VACMIN)**					
168	PFS Losses			1.219	W	Total estimated losses in PFS
169	Boost diode Losses			0.462	W	Total estimated losses in Output Diode
170	Input Bridge losses			1.990	W	Total estimated losses in input bridge module
171	Input Capacitor Losses			0.008	W	Total estimated losses in input capacitor
172	Inductor losses			0.835	W	Total estimated losses in PFC choke
173	Output Capacitor Loss			0.621	W	Total estimated losses in Output capacitor
174	EMI choke copper loss			0.151	W	Total estimated losses in EMI choke copper
175	Total losses			5.286	W	Overall loss estimate
176	Efficiency			0.95		Estimated efficiency at VACMIN, full load.
179	**CAPZero component selection recommendation**					
180	CAPZero Device			CAP200DG		(Optional) Recommended CAPZero device to discharge X-Capacitor with time constant of 1 second
181	Total Series Resistance (Rcapzero1+Rcapzero2)			2.100	MOhms	Maximum Total Series resistor value to discharge X-Capacitors
184	**EMI filter components recommendation**					
185	CX2	0		0	nF	X capacitor after differencial mode choke and before bridge, ratio with Po
186	LDM_calc			254	uH	Estimated minimum differential inductance to avoid <10kHz resonance in input current
187	CX1	330		330	nF	X capacitor before common mode choke, ratio with Po
188	LCM			10.0	mH	typical common mode choke value
189	LCM_leakage			30	uH	estimated leakage inductance of CM choke, typical from 30~60uH
190	CY1 (and CY2)			220	pF	typical Y capacitance for common mode noise suppression
191	LDM_Actual			224	uH	cal_LDM minus LCM_leakage, utilizing CM leakage inductance as DM choke.
192	DCR_LCM			0.070	Ohms	Total DCR of CM choke for estimating copper loss
193	DCR_LDM			0.030	Ohms	Total DCR of DM choke(or CM #2) for estimating copper loss
195	Note: CX2 can be placed between CM chock and DM choke depending on EMI design requirement.					

Notes:

1) Info/Warnings are verified to be within the safe operating conditions.

8 PFC Inductor Specification (T2)

8.1 *Electrical Diagram*

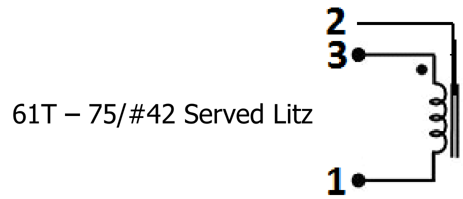

Figure 11 – Inductor Electrical Diagram.

8.2 *Electrical Specifications*

Inductance	Pins 3-1, measured at 100 kHz, 0.4 $V_{RMS.}$	650 µH ±5%

8.3 *Material List*

Item	Description
[1]	Core: Ferrox Cube Core, 3C95 ±25%.
[2]	Bobbin: EQ25, 4 pin (4/0); PI P/N: 25-01141-00
[3]	Wire: Served Litz 75/#42.
[4]	Tape, Polyester Web 3M, 8.1 mm Wide, 2 mil Thick.
[5]	Bus wire, #24 AWG (connect to pin 3).
[6]	Tape: 3M 1350F-1 Polyester Film, 12.5 mm wide.
[7]	Varnish: Dolph BC-359, or Equivalent.

8.4 *Inductor Build Diagram*

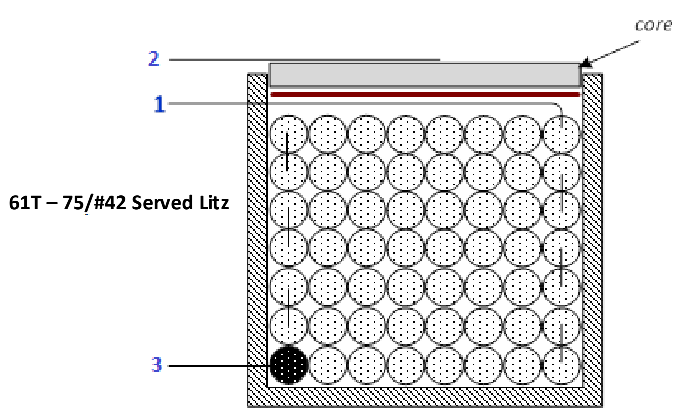

Figure 12 – Inductor Build Diagram.

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8.5 ***Bobbin Modification***

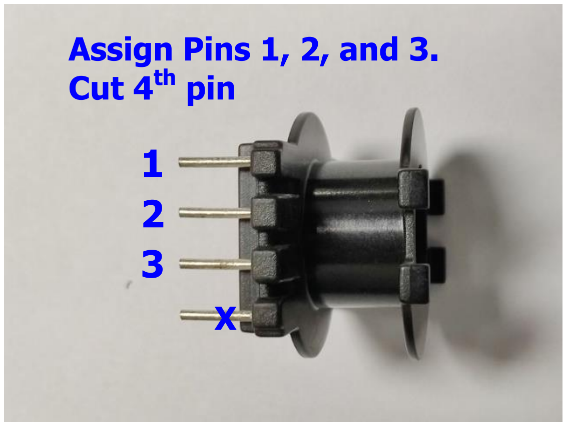

Figure 13 – Bobbin Modification.

8.6 ***Inductor Construction***

Winding Preparation	Place the bobbin on the mandrel with the pin side is on the left side. Winding direction is clockwise direction.
Winding #1	Starting at pin 3, wind 61 turns of served Litz wire Item [3], finish at pin 1.
Insulation	Apply 1 layer of tape Item [4]
Assembly	Grind both cores to specified inductance.
Final Assembly	Solder a wire of Item [5] at pin 2, and then attach the other end of the wire to the bottom side of the core. Secure the wire and the core halves with tape Item [6] and varnish the assembly with Item [7].

Note: The PFC inductor will have a thermal pad attached to the core bottom side before it is soldered into the board. See the section Adapter Case and Heat Spreader Assembly in this document for more details.

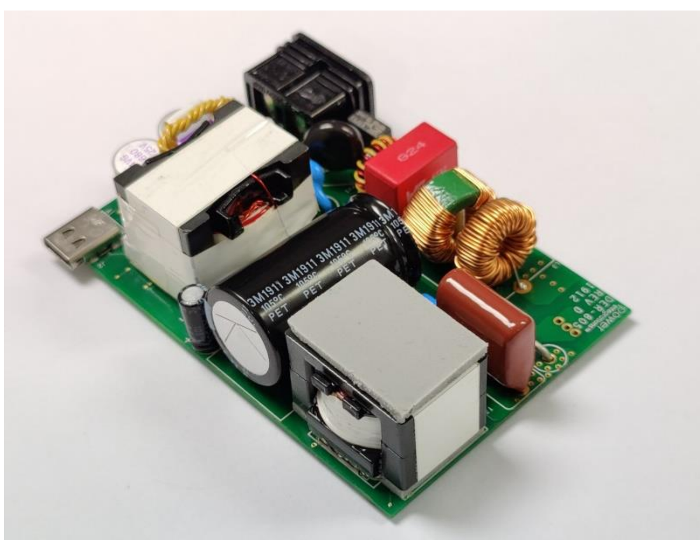

Figure 14 – PFC Inductor with Thermal Pad.

9 Transformer Design Spreadsheet (T1)

9.1 *Spreadsheet with PFC on for 20 V Output*

1	***ACDC_InnoSwitch3-Pro_Flyback_090320; Rev.1.4; Copyright Power Integrations 2020***	***INPUT***	***INFO***	***OUTPUT***	***UNITS***	***InnoSwitch3-Pro Flyback Design Spreadsheet***
2	APPLICATION VARIABLES					Design Title
3	VAC_MIN	270		270	V	Minimum AC line voltage
4	VAC_MAX	270		270	V	Maximum AC input voltage
5	VAC_RANGE			HIGH LINE		AC line voltage range
6	FLINE	60		60	Hz	AC line voltage frequency
7	CAP_INPUT	82.0		82.0	uF	Input capacitance
8						
9	SET-POINT 1					
10	VOUT1	20.00		20.00	V	Output voltage 1, should be the highest output voltage required
11	IOUT1	5.000		5.000	A	Output current 1
12	POUT1		Info	100.00	W	The output power required exceeds the device capability: Verify thermal performance if no other warnings
13	EFFICIENCY1	0.96		0.96		Converter efficiency for output 1
14	Z_FACTOR1	0.50		0.50		Z-factor for output 1
15						
16	SET-POINT 2					
17	VOUT2	15.00		15.00	V	Output voltage 2
18	IOUT2	5.000		5.000	A	Output current 2
19	POUT2			75.00	W	Output power 2
20	EFFICIENCY2	0.94		0.94		Converter efficiency for output 2
21	Z_FACTOR2	0.50		0.50		Z-factor for output 2
22						
23	SET-POINT 3					
24	VOUT3	9.00		9.00	V	Output voltage 3
25	IOUT3	5.000		5.000	A	Output current 3
26	POUT3			45.00	W	Output power 3
27	EFFICIENCY3	0.93		0.93		Converter efficiency for output 3
28	Z_FACTOR3	0.50		0.50		Z-factor for output 3
29						
30	SET-POINT 4					
31	VOUT4	5.00		5.00	V	Output voltage 4
32	IOUT4	5.000		5.000	A	Output current 4
33	POUT4			25.00	W	Output power 4
34	EFFICIENCY4	0.92		0.92		Converter efficiency for output 4

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35	Z_FACTOR4	0.50		0.50		Z-factor for output 4
36						
37	SET-POINT 5					
38	VOUT5	3.30		3.30	V	Output voltage 5
39	IOUT5	5.000		5.000	A	Output current 5
40	POUT5			16.50	W	Output power 5
41	EFFICIENCY5	0.90		0.90		Converter efficiency for output 5
42	Z_FACTOR5	0.50		0.50		Z-factor for output 5
43						
44	SET-POINT 6					
45	VOUT6			0.00	V	Output voltage 6
46	IOUT6			0.000	A	Output current 6
47	POUT6			0.00	W	Output power 6
48	EFFICIENCY6			0.00		Converter efficiency for output 6
49	Z_FACTOR6			0.00		Z-factor for output 6
50						
51	SET-POINT 7					
52	VOUT7			0.00	V	Output voltage 7
53	IOUT7			0.000	A	Output current 7
54	POUT7			0.00	W	Output power 7
55	EFFICIENCY7			0.00		Converter efficiency for output 7
56	Z_FACTOR7			0.00		Z-factor for output 7
57						
58	SET-POINT 8					
59	VOUT8			0.00	V	Output voltage 8
60	IOUT8			0.000	A	Output current 8
61	POUT8			0.00	W	Output power 8
62	EFFICIENCY8			0.00		Converter efficiency for output 8
63	Z_FACTOR8			0.00		Z-factor for output 8
64						
65	SET-POINT 9					
66	VOUT9			0.00	V	Output voltage 9
67	IOUT9			0.000	A	Output current 9
68	POUT9			0.00	W	Output power 9
69	EFFICIENCY9			0.00		Converter efficiency for output 9
70	Z_FACTOR9			0.00		Z-factor for output 9
71						
72	VOLTAGE_CDC	0.000		0.000	V	Cable drop compensation desired at maximum output current
73						
74						

75						
76	PRIMARY CONTROLLER SELECTION					
77	ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
78	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
79	VDRAIN_BREAKDOWN	750		750	V	Device breakdown voltage
80	DEVICE_GENERIC	INN33X0		INN33X0		Device selection
81	DEVICE_CODE			INN3370C		Device code
82	PDEVICE_MAX			90	W	Device maximum power capability
83	RDSON_25DEG			0.39	Ω	Primary switch on-time resistance at 25°C
84	RDSON_100DEG			0.54	Ω	Primary switch on-time resistance at 100°C
85	ILIMIT_MIN			2.395	A	Primary switch minimum current limit
86	ILIMIT_TYP			2.576	A	Primary switch typical current limit
87	ILIMIT_MAX			2.756	A	Primary switch maximum current limit
88	VDRAIN_ON_PRSW			0.15	V	Primary switch on-time voltage drop
89	VDRAIN_OFF_PRSW			590.38	V	Peak drain voltage on the primary switch during turn-off
90						
91						
92						
93	WORST CASE ELECTRICAL PARAMETERS					
94	FSWITCHING_MAX	73329	Info	73329	Hz	The worst case minimum operating frequency is less than 25kHz: may result in audible noise
95	VOR	140.0		140.0	V	Voltage reflected to the primary winding (corresponding to set-point 1) when the primary switch turns off
96	VMIN	380.00	Info	380.00	V	A manual overwrite of VMIN voids the value of input capacitor calculated by the tool or manually entered by the user and will be used for all calculations
97	KP			1.043		Measure of continuous/discontinuous mode of operation
98	MODE_OPERATION			DCM		Mode of operation
99	DUTYCYCLE			0.235		Primary switch duty cycle
100	TIME_ON			3.85	us	Primary switch on-time
101	TIME_OFF			10.47	us	Primary switch off-time
102	LPRIMARY_MIN			520.7	uH	Minimum primary magnetizing inductance
103	LPRIMARY_TYP			548.1	uH	Typical primary magnetizing inductance
104	LPRIMARY_TOL			5.0	%	Primary magnetizing inductance tolerance
105	LPRIMARY_MAX			575.5	uH	Maximum primary magnetizing inductance

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106						
107	PRIMARY CURRENT					
108	IAVG_PRIMARY			0.269	A	Primary switch average current
109	IPEAK_PRIMARY			2.575	A	Primary switch peak current
110	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
111	IRIPPLE_PRIMARY			2.575	A	Primary switch ripple current
112	IRMS_PRIMARY			0.679	A	Primary switch RMS current
113						
114	SECONDARY CURRENT					
115	IPEAK_SECONDARY			18.024	A	Secondary winding peak current
116	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
117	IRMS_SECONDARY			7.831	A	Secondary winding RMS current
118	IRIPPLE_CAP_OUT			6.027	A	Output capacitor ripple current
119						
120						
121						
122	TRANSFORMER CONSTRUCTION PARAMETERS					
123	CORE SELECTION					
124	CORE	PQ26/20	Info	PQ26/20		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
125	CORE NAME			B65877B0000R095		Core code
126	AE			122.3	mm^2	Core cross sectional area
127	LE			44.4	mm	Core magnetic path length
128	AL			6300	nH	Ungapped core effective inductance per turns squared
129	VE			5435	mm^3	Core volume
130	BOBBIN NAME			B65878E0012D001		Bobbin name
131	AW			33.0	mm^2	Bobbin window area
132	BW			9.00	mm	Bobbin width
133	MARGIN			0.0	mm	Bobbin safety margin
134						
135	PRIMARY WINDING					
136	NPRIMARY			35		Primary winding number of turns
137	BPEAK			3792	Gauss	Peak flux density
138	BMAX			3416	Gauss	Maximum flux density
139	BAC			1708	Gauss	AC flux density (0.5 x Peak to Peak)
140	ALG			447	nH	Typical gapped core effective inductance per turns squared
141	LG			0.319	mm	Core gap length
142	LAYERS_PRIMARY	2		2		Primary winding number of layers

143	AWG_PRIMARY	25		25		Primary wire gauge
144	OD_PRIMARY_INSULATED			0.518	mm	Primary wire insulated outer diameter
145	OD_PRIMARY_BARE			0.455	mm	Primary wire bare outer diameter
146	CMA_PRIMARY			471.8	Cmils/A	Primary winding wire CMA
147						
148	SECONDARY WINDING					
149	NSECONDARY	5		5		Secondary winding number of turns
150	AWG_SECONDARY			18		Secondary wire gauge
151	OD_SECONDARY_INSULATED			1.328	mm	Secondary wire insulated outer diameter
152	OD_SECONDARY_BARE			1.024	mm	Secondary wire bare outer diameter
153	CMA_SECONDARY			207.4	Cmils/A	Secondary winding wire CMA
154						
155	BIAS WINDING					
156	NBIAS			15		Bias winding number of turns
157						
158						
159						
160	PRIMARY COMPONENTS SELECTION					
161	LINE UNDERVOLTAGE					
162	BROWN-IN REQURED	80.00		80.00	V	Required line brown-in threshold
163	RLS			4.00	MΩ	Connect two 2 MOhm resistors to the V-pin for the required UV/OV threshold
164	BROWN-IN ACTUAL			80.16	V	Actual brown-in threshold using standard resistors
165	BROWN-OUT ACTUAL			72.50	V	Actual brown-out threshold using standard resistors
166						
167	LINE OVERVOLTAGE					
168	OVERVOLTAGE_LINE		Warning	334.21	V	The device voltage stress will be higher than 650V when overvoltage is trigerred
169						
170	BIAS WINDING					
171	VBIAS			9.00	V	Rectified bias voltage at the lowest output set-point
172	VF_BIAS			0.70	V	Bias winding diode forward drop
173	VREVERSE_BIASDIODE			172.02	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
174	CBIAS			22	uF	Bias winding rectification capacitor
175	CBPP			4.70	uF	BPP pin capacitor
176						
177						
178						
179	SECONDARY COMPONENTS					

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	SELECTION					
180	RECTIFIER					
181	VDRAIN_OFF_SRFET			74.34	V	Secondary rectifier reverse voltage (not accounting parasitic voltage ring)
182	SRFET	AUTO		SIR804DP		Secondary rectifier (Logic MOSFET)
183	VBREAKDOWN_SRFET			100	V	Secondary rectifier breakdown voltage
184	RDSON_SRFET			10.3	mΩ	SRFET on time drain resistance at 25degC for VGS=4.4V
185						
186						
187						
188	SET-POINTS ANALYSIS					
189	TOLERANCE CORNER					
190	USER_VAC		Info	270	V	The value of VMIN entered by the user will be used for calculations in this section
191	USER_ILIMIT	MIN		2.395	A	Current limit corner to be evaluated
192	USER_LPRIMARY	MIN		520.7	uH	Primary inductance corner to be evaluated
193						
194	SET-POINT SELECTION					
195	SET-POINT	1		1		Select the set-point which needs to be evaluated
196	FSWITCHING			73329.0	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
197	VOR			140.0	V	Voltage reflected to the primary winding when the primary switch turns off
198	VMIN			380.00	V	Valley of the minimum input AC voltage
199	KP			1.217		Measure of continuous/discontinuous mode of operation
200	MODE_OPERATION			DCM		Mode of operation
201	DUTYCYCLE			0.232		Primary switch duty cycle
202	TIME_ON			3.17	us	Primary switch on-time
203	TIME_OFF			10.47	us	Primary switch off-time
204						
205	PRIMARY CURRENT					
206	IAVG_PRIMARY			0.269	A	Primary switch average current
207	IPEAK_PRIMARY			2.312	A	Primary switch peak current
208	IPEDESTAL_PRIMARY			0.000	A	Primary switch current pedestal
209	IRIPPLE_PRIMARY			2.312	A	Primary switch ripple current
210	IRMS_PRIMARY			0.644	A	Primary switch RMS current
211						
212	SECONDARY CURRENT					
213	IPEAK_SECONDARY			16.187	A	Secondary winding peak current

214	IPEDESTAL_SECONDARY			0.000	A	Secondary winding pedestal current
215	IRMS_SECONDARY			7.422	A	Secondary winding RMS current
216	IRIPPLE_CAP_OUT			5.485	A	Output capacitor ripple current
217						
218	MAGNETIC FLUX DENSITY					
219	BPEAK			2982	Gauss	Peak flux density
220	BMAX			2813	Gauss	Maximum flux density
221	BAC			1406	Gauss	AC flux density (0.5 x Peak to Peak)
222						
223						

Note: Even though the spreadsheet shows that the output power required exceeds the device capability of INN3370C controller (lines 12 and 82), this power supply design has been verified to meet 100 W output operation for both (1) at open frame and (2) inside an adapter case together with a heat spreader assembly for thermal management.
For applications that require modification of form factor, PCB layout, or thermal cooling (heat spreader and thermal pads) of this design, both electrical and thermal performance must be carefully evaluated.

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10 Transformer Specification (T1)

10.1 Electrical Diagram

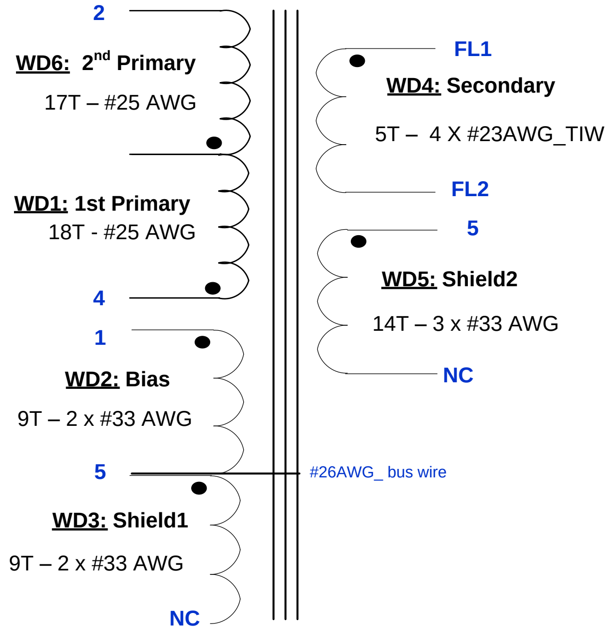

Figure 15 – Transformer Electrical Diagram.

10.2 *Electrical Specifications*

Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 2 and 4, with all other windings open.	548 µH± 5%
Resonant Frequency	Between pin 2 and 4, other windings open.	1,500 kHz (Min.)
Primary Leakage Inductance	Between pin 2 and 4, with pins:FL1-FL2 shorted.	4.5 µH (Max.)

10.3 Material List

Item	Description
[1]	Core: PQ2620, TDK-PC95.
[2]	Bobbin: PQ-2628; PI#: 25-01137-00.
[3]	Magnet Wire: #25 AWG, Double Coated.
[4]	Magnet Wire: #33 AWG, Double Coated.
[5]	Magnet Wire: #23 AWG, Triple Insulated Wire.
[6]	Bus wire: #26AWG, Alpha Wire, Tinned Copper.
[7]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 9.3 mm Width.
[8]	Tape: 3M 1350-F, Polyester Film, 1 mil Thickness, 33 mm x 63 mm.
[9]	Varnish: Dolph BC-359.

10.4 Transformer Build Diagram

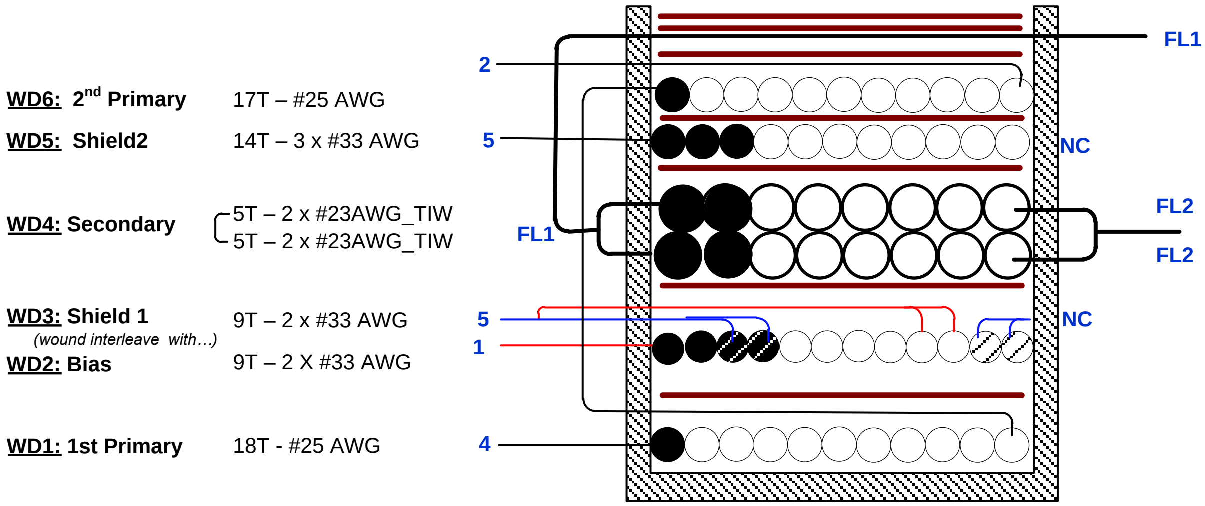

Figure 16 – Transformer Build Diagram.

10.5 Transformer Construction

Winding Preparation	Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 1st Primary	Start at pin 4, wind 18 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and leave enough length of wire-floating for WD6-2nd Primary.
Insulation	1 layer of tape Item [7].
WD2: Bias & WD3: Shield1	Use 2 wires Item [4] start at pin 1 for Bias winding, also use 2 wires same Item [4] start at pin 5 for Shield1 winding. Wind all 4 wires in parallel, at the 9th turn: - bring 2 wires for Bias winding to the left and terminate at pin 5, - cut short 2 wires for Shield1 Winding as No-Connect.
Insulation	1 layer of tape Item [7].
WD4 Secondary	Start at left slot of secondary side, use 2 wires Item [5], leaving ~40.0 mm floating, and mark as FL1.Wind 5 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~30.0 mm floating, and mark FL2. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2.
Insulation	3 layers of tape Item [7].
WD5 Shield2	Start at pin 5, wind 14 tri-filar turns of wire Item [4], from left to right. At the last turn, cut short to leave as No-Connect.
Insulation	1 layer of tape Item [7].
WD6 2nd Primary	Use floating wire from WD1-1st Primary, wind 17 turns from right to left and finish at pin 2.
Insulation	1 layer of tape Item [7].
Finish	Bring 4 wires marked as FL1 to the right and secure with 2 layers of tape Item [7]. Gap core halves to get 548 μH. Solder pin 5 with bus-wire Item [6] then lean along core halves and secure with tape. Varnish with Item [9]. Place 2 layers of tape Item [8] at the bottom then wrap up to the body of transformer, and tape around 1 layer of tape Item [8]. (*See pictures below*).

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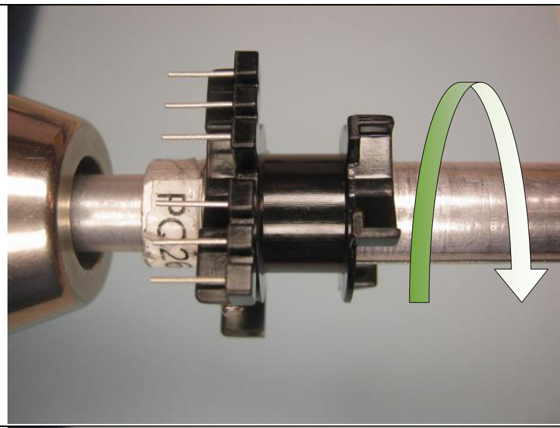
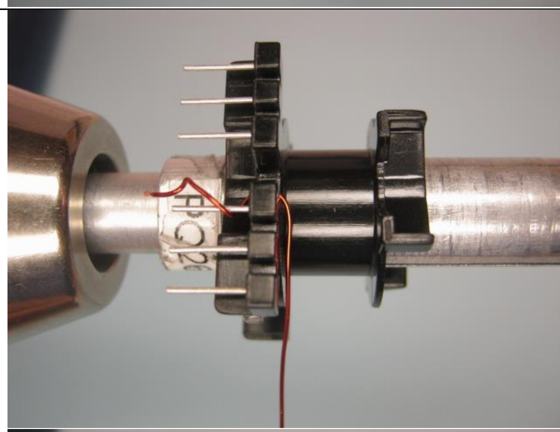
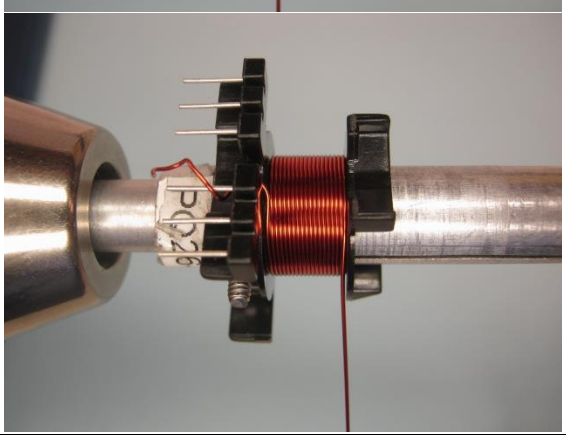
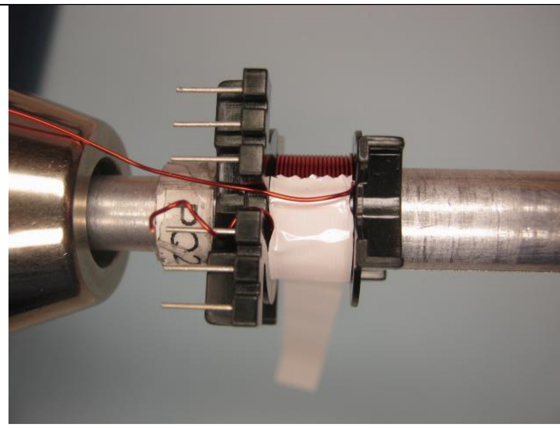
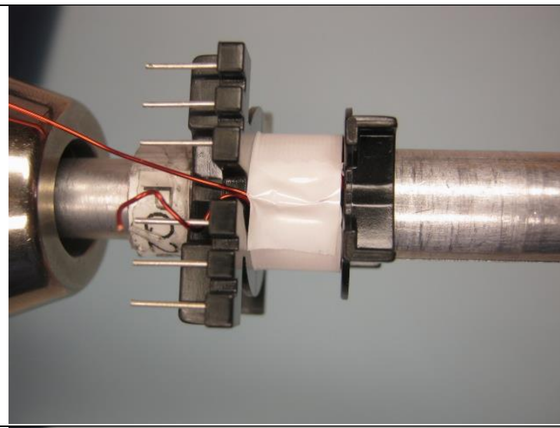
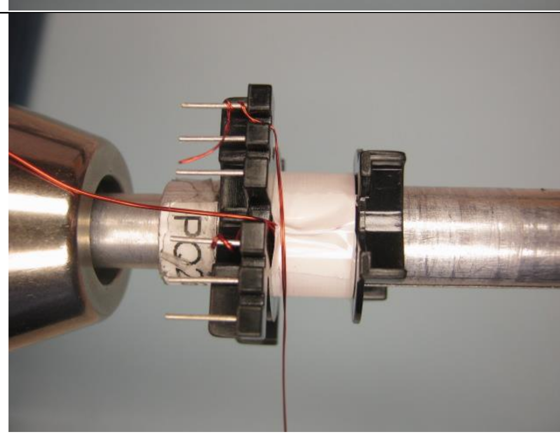
10.6 *Winding Illustrations*

Winding Preparation		Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 **1st Primary**	 	Start at pin 4, wind 18 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn, bring the wire back to left, and leave enough length of wire-floating for WD6-2nd Primary.

		
Insulation		1 layer of tape Item [7].
WD2: Bias **&** **WD3: Shield1**		Use 2 wires Item [4] start at pin 1 for Bias winding, also use 2 wires same Item [4] start at pin 5 for Shield1 winding. Wind all 4 wires in parallel, at the 9th turn: - bring 2 wires for Bias winding to the left and terminate at pin 5, - cut short 2 wires for Shield1 Winding as No-Connect.

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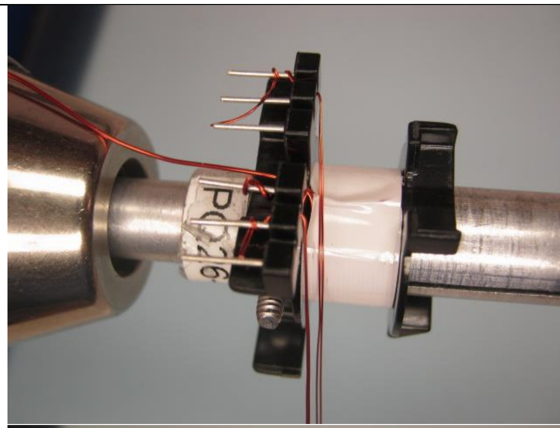
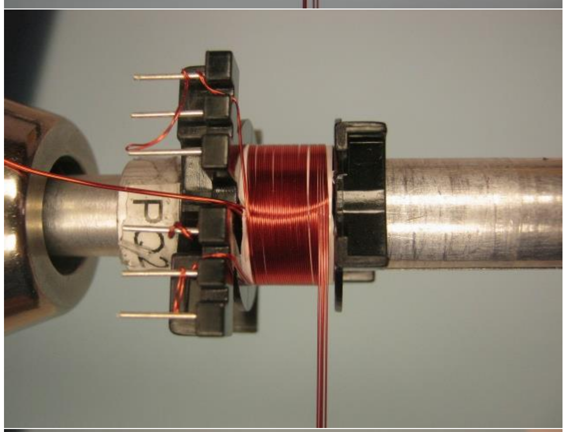
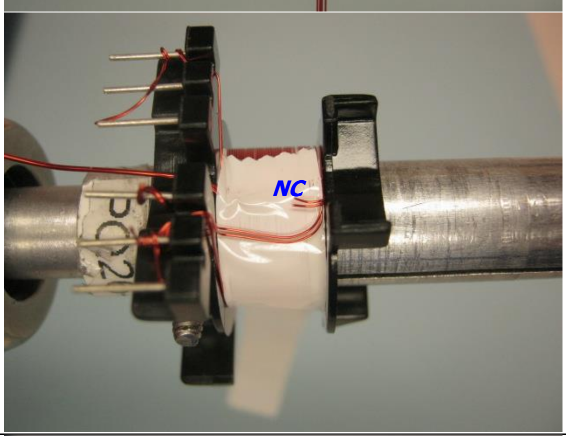
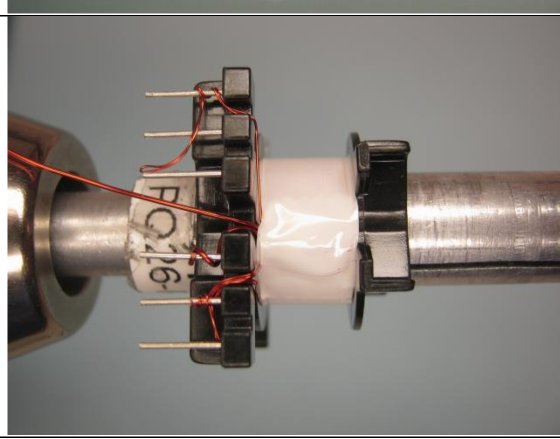
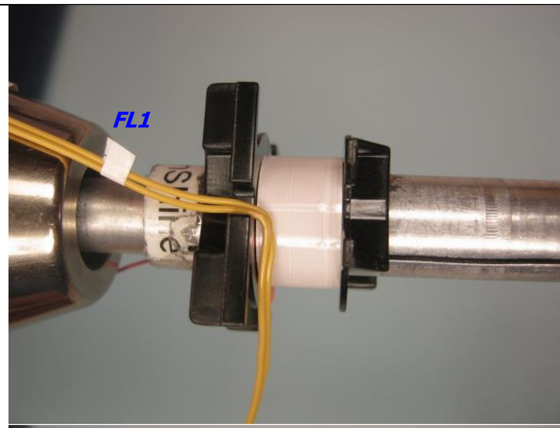
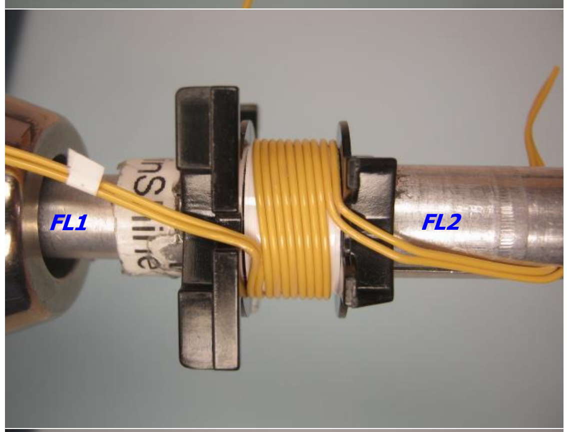
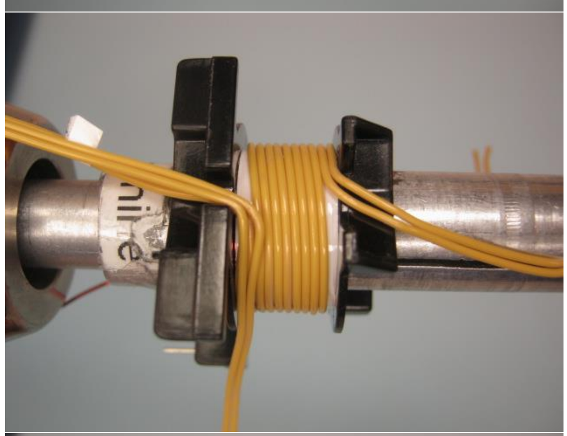
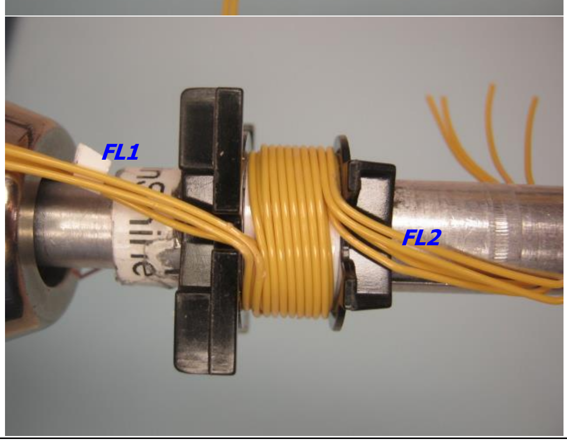
	  	
Insulation		1 layer of tape Item [7].

WD4 **Secondary**	   	Start at left slot of secondary side, use 2 wires Item [5], leaving ~40.0 mm floating, and mark as FL1.Wind 5 bifilar turns in 1 layer, from left to right, at the last turn exit the wires at right slot, also leaving ~30.0 mm floating, and mark FL2. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2.

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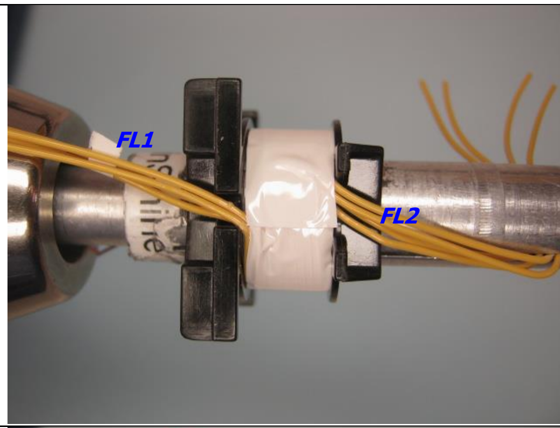
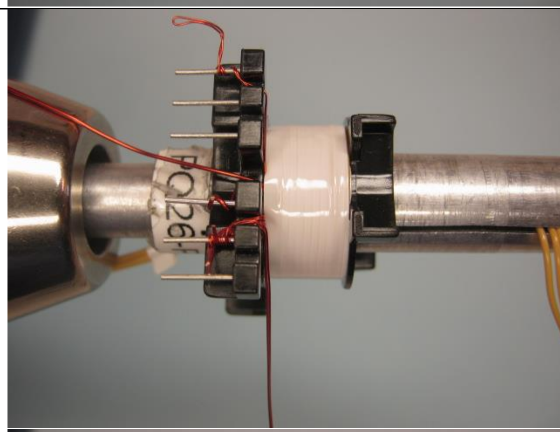
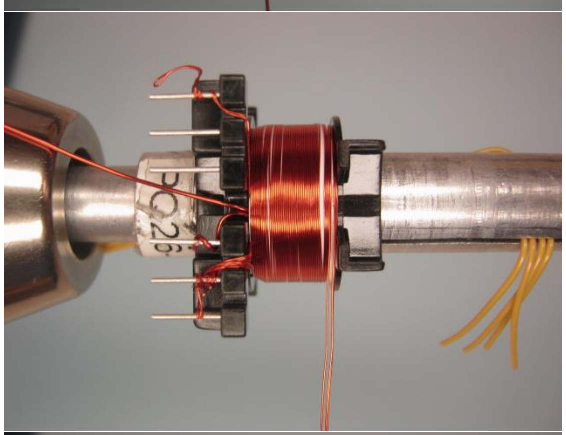
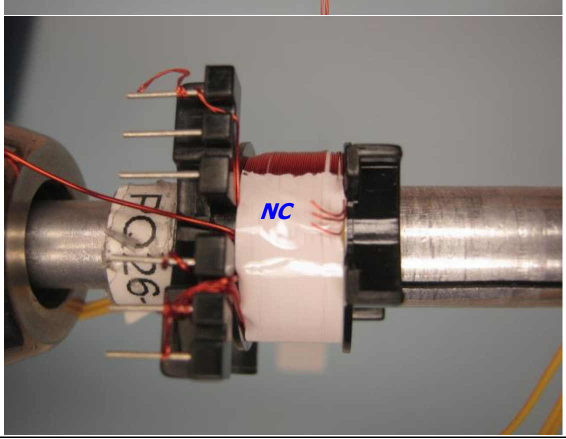
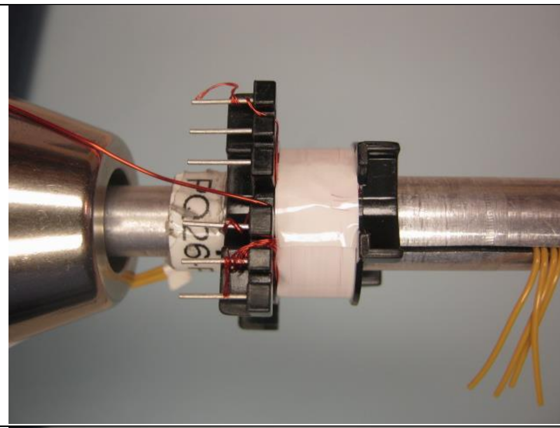
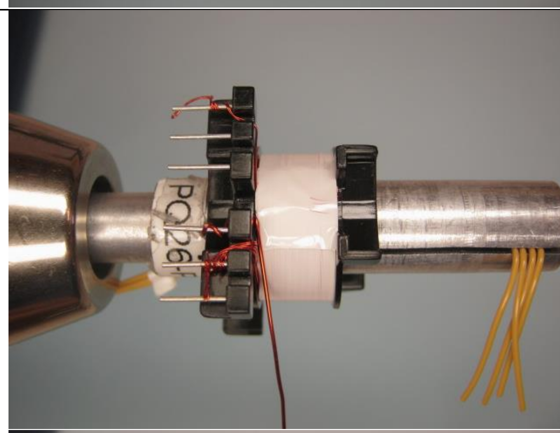
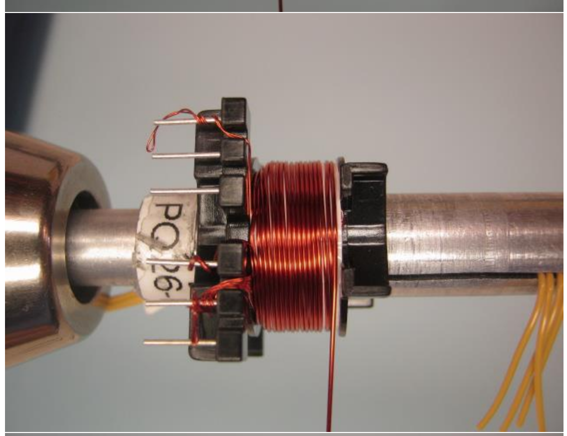
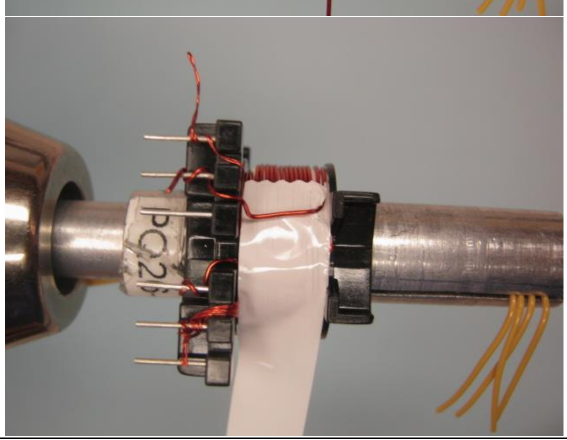
Insulation		3 layer of tape Item [7].
WD5 **Shield2**		Start at pin 5, wind 14 tri-filar turns of wire Item [4], from left to right. At the last turn, cut short to leave as No-Connect.

Insulation		1 layer of tape Item [7].
WD6 **2nd Primary**	  	Use floating wire from WD1-1st Primary, wind 17 turns from right to left and finish at pin 2.

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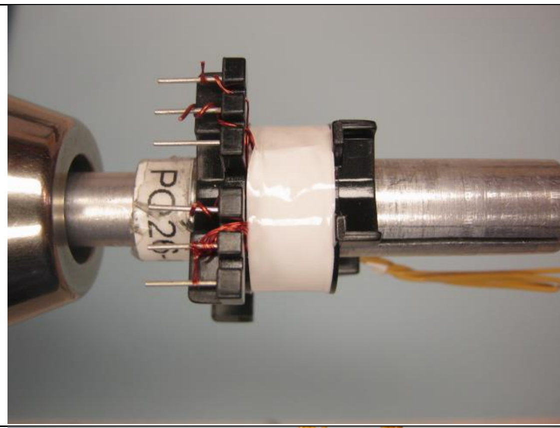
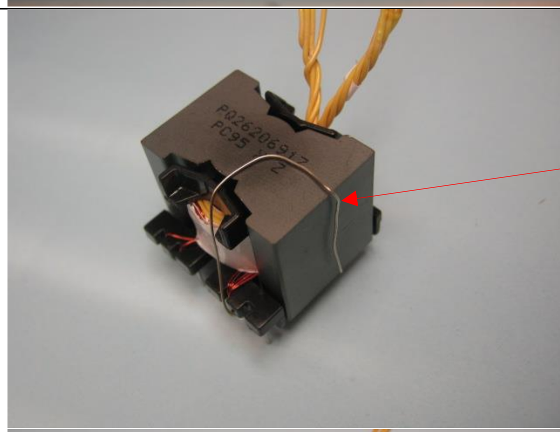
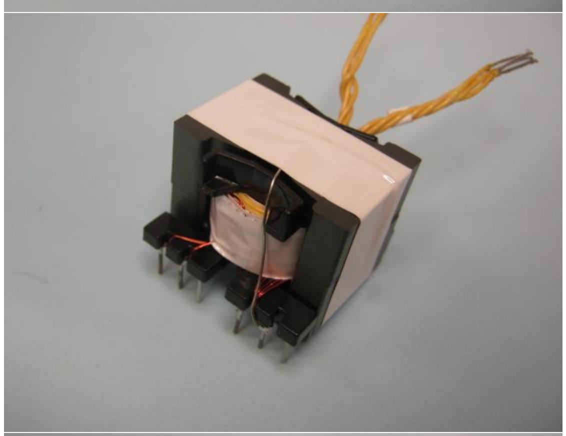
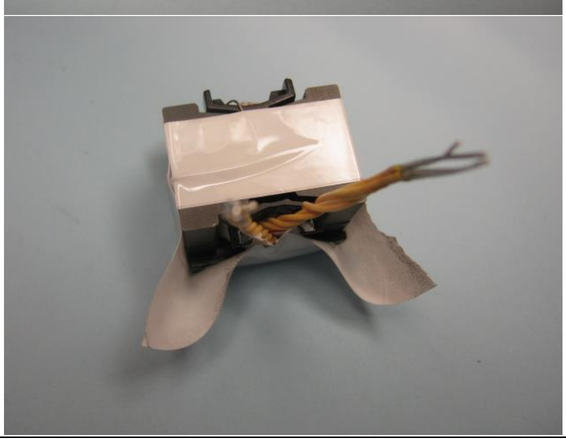
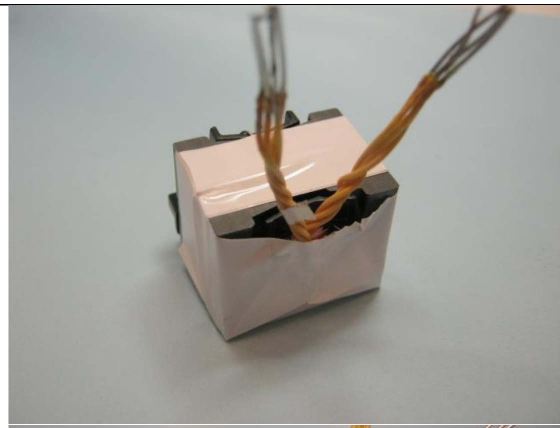
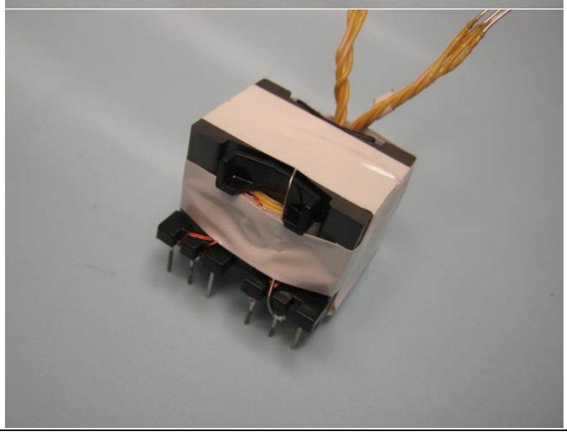
Insulation		1 layer of tape Item [7].
Finish	  	Bring 4 wires marked as FL1 to the right and secure with 2 layers of tape Item [7]. Gap core halves to get 548 μH. Solder pin 5 with bus-wire Item [6] then lean along core halves and secure with tape. Varnish with Item [9]. Place 2 layers of tape Item [8] at the bottom then wrap up to the body of transformer, and tape around 1 layer of tape Item [8]. (*See pictures beside*).

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11 Common Mode Choke Specifications

11.1 *250* uH *Common Mode Choke (L1)*

11.1.1 Electrical Diagram

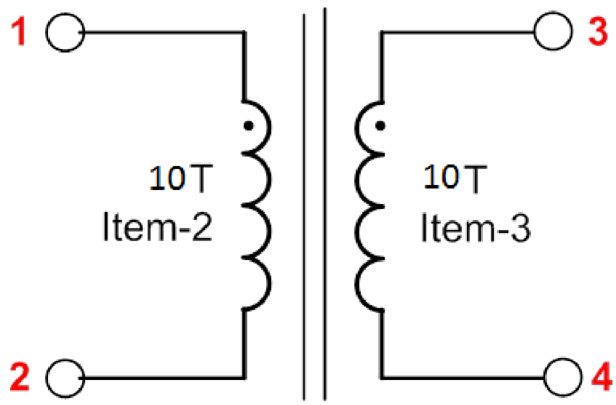


Figure 17 – Inductor Electrical Diagram.

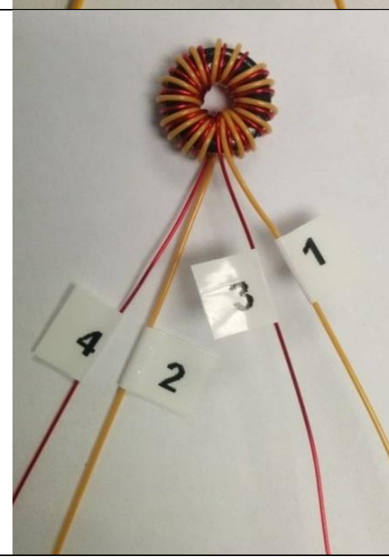
11.1.2 Electrical Specifications

Inductance	Pins 1-2 measured at 100 kHz, 0.4 RMS.	250 µH ±20%
Primary Leakage Inductance	Pins 1-2, with 3-4 shorted.	1 µH

11.1.3 Material List

Item	Description
[1]	Toroid: FERRITE INDUCTOR TOROID .415" O.D.; Mfg Part number: 35T0375-10H. Dim: 9.53 mm O.D. x 4.75 mm I.D. x 3.18 mm L.
[2]	Magnet Wire: #27 AWG.
[3]	Triple Insulated Wire #27 AWG.

11.1.4 Common Mode Choke Construction

Mark the start end of the winding as 1 and wind 10 turns of Item [2] on Item [1]. Mark the end of this winding as 2	
Repeat the same procedure as above for the other winding using Item [3], making sure that the start/end and the direction of winding is the same as the first winding. Varnish using Item [4]. Mark the start of this winding as 3 and the end as 4.	

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11.2 ***18 mH Common Mode Choke (L2)***

11.2.1 Electrical Diagram

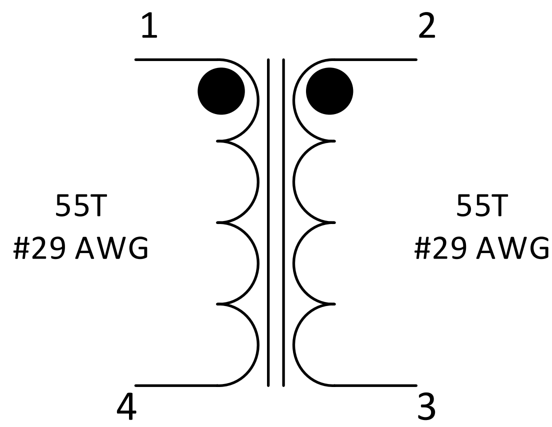

Figure 18 – Inductor Electrical Diagram.

11.2.2 Electrical Specifications

Inductance	Pins 1 - 4 and pins 2 - 3 measured at 100 kHz, 0.4 RMS.	18 mH ±25%
Core effective Inductance Index		5950 nH/N^2
Leakage Inductance	Pins 1 - 4, with pins 2 - 3 shorted.	80 µH ±10%

11.2.3 Material List

Item	Description
[1]	Toroid: FERRITE INDUCTOR TOROID T14 x 8 x 5.5, PI#: 32-00286-00.
[2]	Divider: Cable Tie, Panduit - Fish Paper, Insulating Cotton Rag, 0.010" Thick, PI#: 66-00042-00.
[3]	Magnet Wire: #29 AWG Heavy Nyleze.
[4]	Epoxy: Devon, 5mins Epoxy; or Equivalent.

11.2.4 Winding Instructions

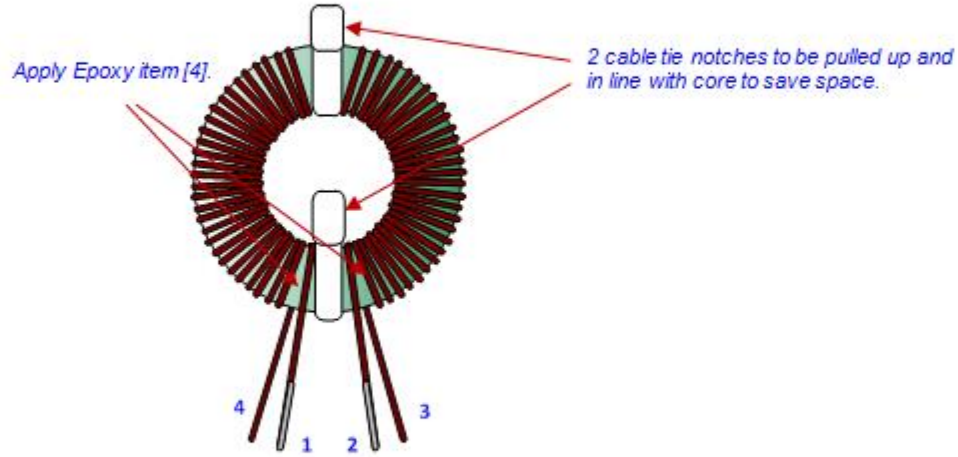

Figure 19 – 18 mH CMC Illustration Image.

- Place 2 pieces of cable tie Item [2] on to toroid Item [1] to divide 2 equal sections.
- Use 4 ft of wire Item [3], start as 1, wind 55 turns in 2 layers in a half section of toroid, and end as 4.
- Do the same for another half of Toroid, start as 2 and end as 3.
- Pull up 2 notches of cable ties to be in line with toroid body (to save space), and apply Epoxy Item [4] where leads floating.

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12 Adapter Case and Heat Spreader Assembly

12.1 *Materials*

Item	Qty	Description	Thickness	Material	PI#
[1A]	2	Thermal pad: for Bridge Rectifiers BR1 BR2.	0.5 mm	EYG-T7070A5A	61-00252-00
[1B]	1	Thermal pad: for PI device PFS7628C.	0.5 mm	EYG-T7070A5A	61-00253-00
[1C]	1	Thermal pad: for PI device INN3370C.	0.5 mm	EYG-T7070A5A	61-00254-00
[2]	1	Thermal pad: for SRFETs Q2 Q3.	1.0 mm	EYG-T7070A10A	61-00255-00
[3A]	1	Thermal pad: for copper section above PFS7628C.	2 mm	COH3114LVC-200-20	61-00257-00
[3B]	1	Thermal pad: for copper section below PFS7628C.	2 mm	COH3114LVC-200-20	61-00258-00
[3C]	1	Thermal pad: for copper section above INN3370C.	2 mm	COH3114LVC-200-20	61-00259-00
[3D]	2	Thermal pad: for PFC inductor core top and bottom.	2 mm	COH3114LVC-200-20	61-00260-00
[4]	1	Insulator: Mylar, Teijin.	3 mils	DuPont Mylar WC Film	61-00263-00
[5]	1	Heat spreader: Aluminum Sheet	25 mils	Aluminum 3003	61-00262-00
[6]	1	Thermal pad: for heat spreader inner-bottom.	1.5 mm	3M 5549S 1.5mm	61-00261-00
[7]	2	Thermal pad: for heat spreader outside-top and outside-bottom	1.0 mm	COH-3114LVC-200-10	61-00256-00
[8]		Tape: 3M 1350F-1 Polyester Film, 9.3 mm wide.	1 mil	Polyester Film	
[9]		Tape: 3M 1350F-1 Polyester Film, 33.0 mm wide.	1 mil	Polyester Film	
[10]		Tape: 3M 1350F-1 Polyester Film, 12.5 mm wide.	1 mil	Polyester Film	
[11]	1	DER-805 Enclosure – top		Polycarbonate, 3D print	07-00010-00
[12]	1	DER-805 Enclosure – bottom		Polycarbonate, 3D print	07-00011-00

12.2 ***Adapter Case Dimensions***

12.2.1 Enclosure - Top

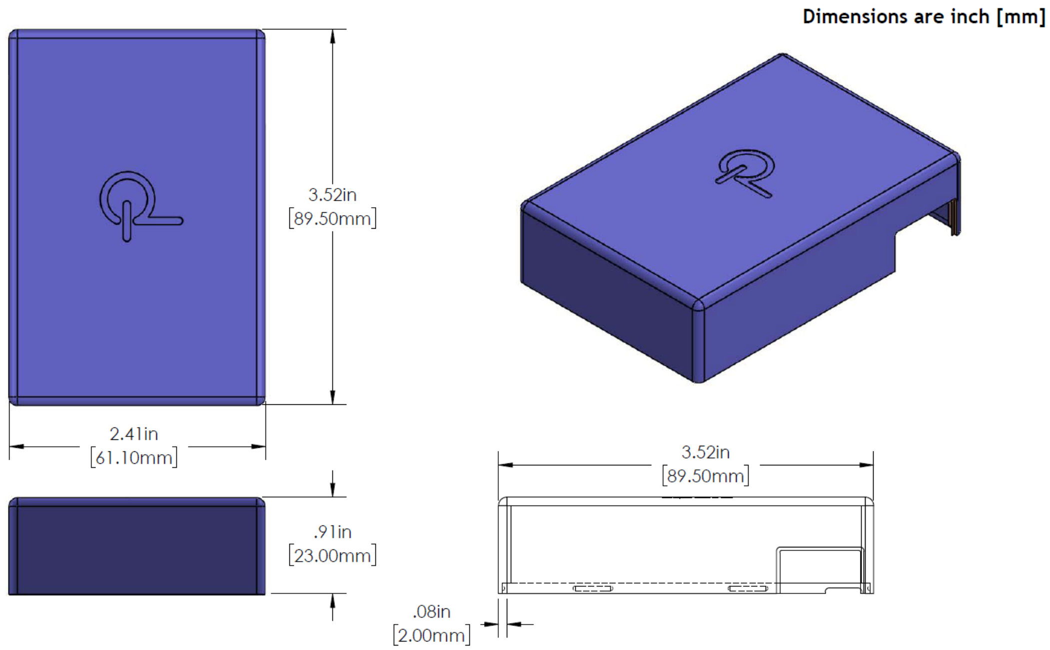

Figure 20 – Adapter Enclosure – Top Dimensions.

12.2.2 Enclosure - Bottom

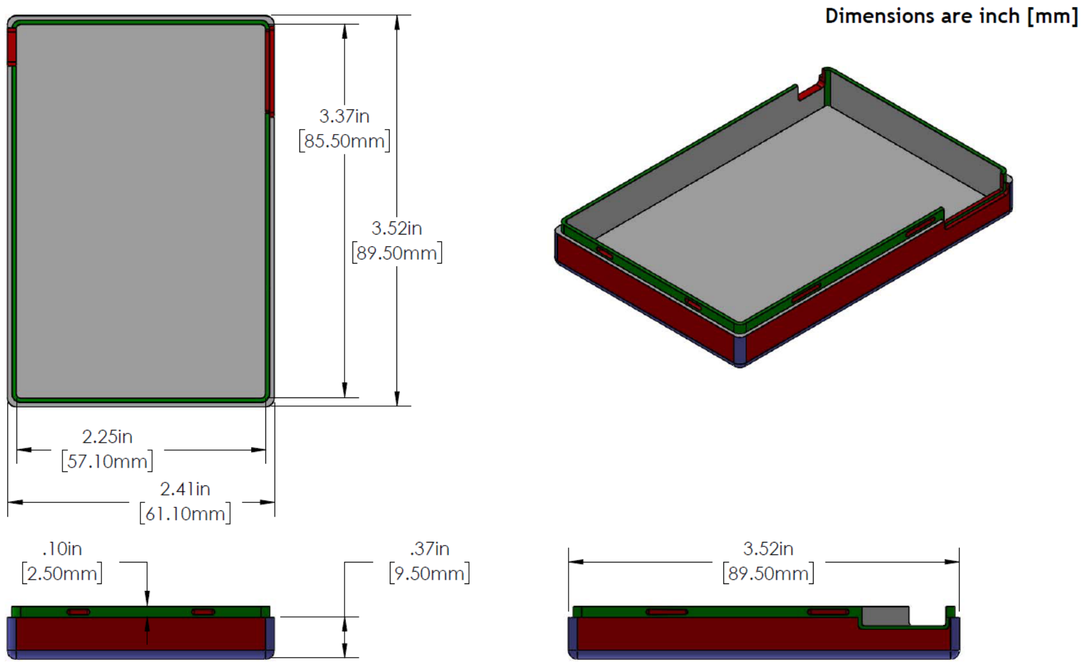

Figure 21 – Adapter Enclosure – Bottom Dimensions.

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12.3 ***Heat Spreader Dimensions***

12.3.1 Aluminum Sheet

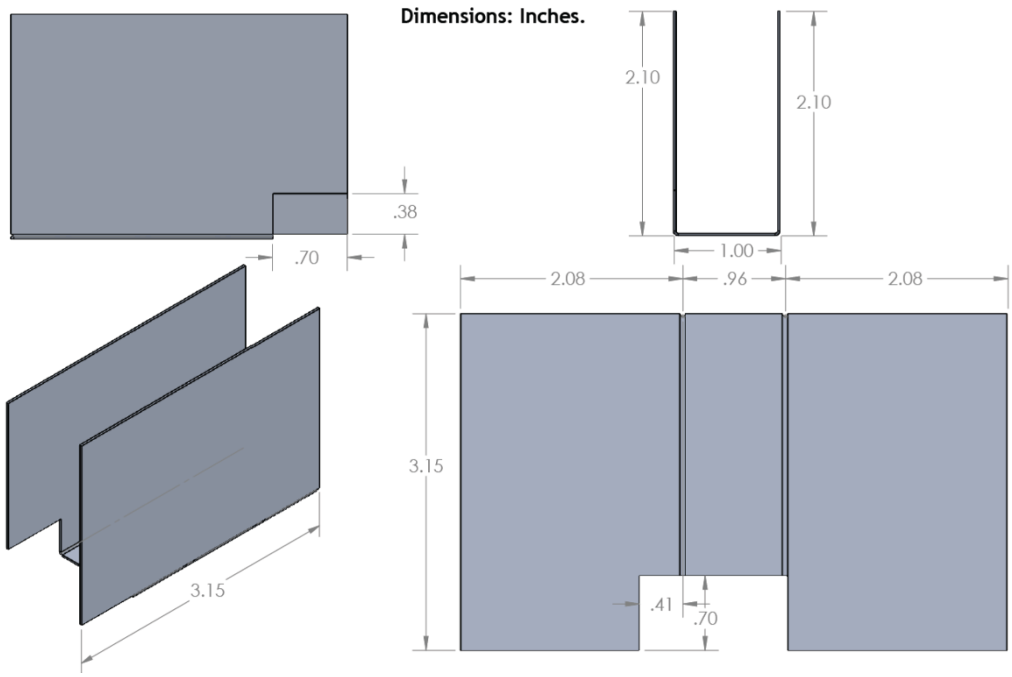

Figure 22 –Aluminum 3003 Sheet (25 mils thick) Dimensions.

12.4 ***Thermal Pad Dimensions***

12.4.1.1 For Bridge Rectifiers

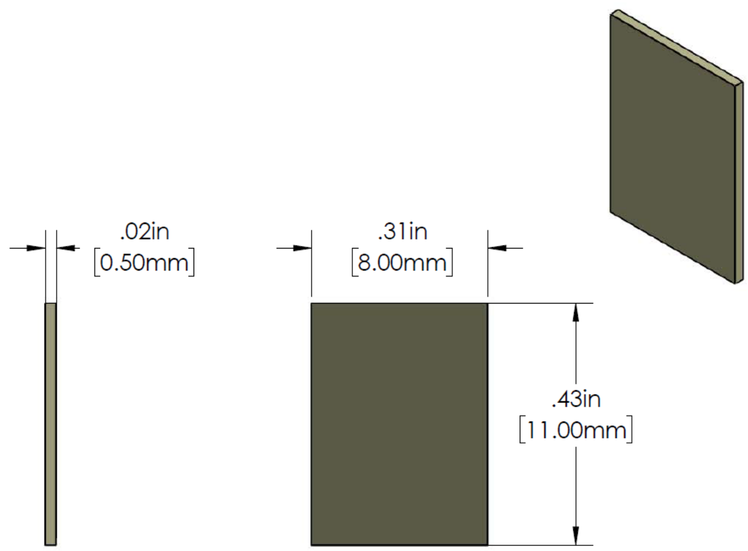

Figure 23 – Thermal Pad for Bridge Rectifiers (Material: EYG-T7070A5A, 0.5 mm).

12.4.1.2 For PFS7628C

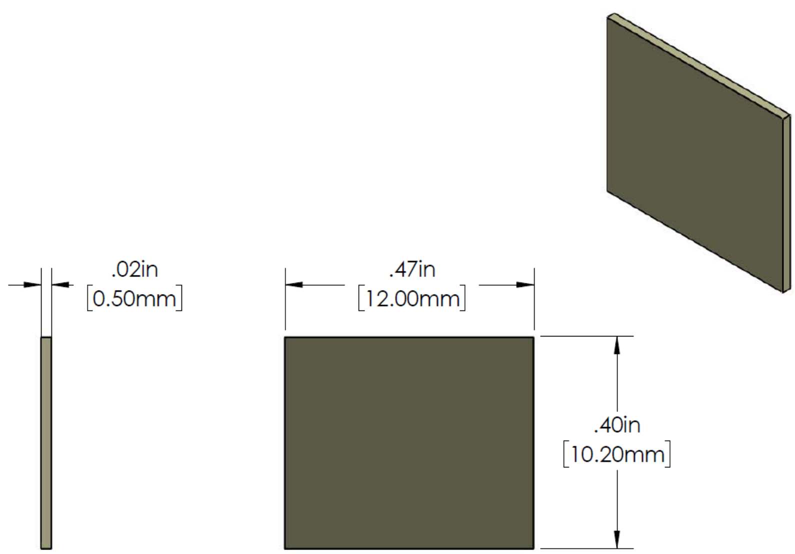

Figure 24 – Thermal Pad for PFS7628C (Material: EYG-T7070A5A, 0.5 mm).

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12.4.1.3 For INN3370C

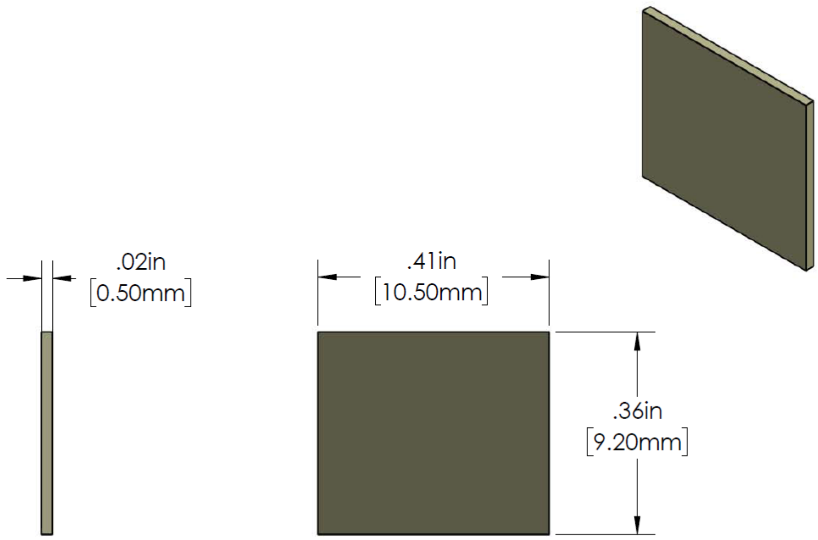

Figure 25 – Thermal Pad for INN3370C (Material: EYG-T7070A5A, 0.5 mm).

12.4.1.4 For SRFETs

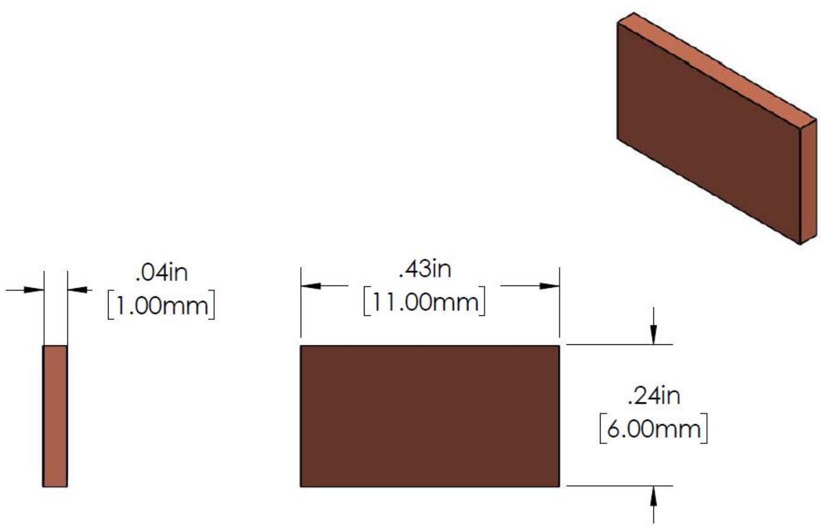

Figure 26 – Thermal Pad for SRFETs (Material: EYG-T7070A10A, 1.0 mm).

12.4.1.5 For Copper Section Above PFS7628C

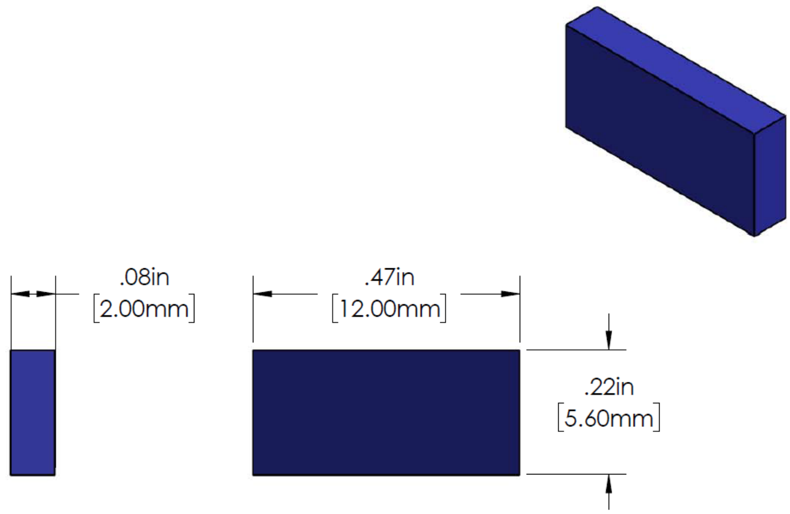

Figure 27 – Thermal Pad for Copper Section Above PFS7628C (Material: COH3114LVC-200-20, 2.0 mm).

12.4.1.6 For Copper Section Below PFS7628C

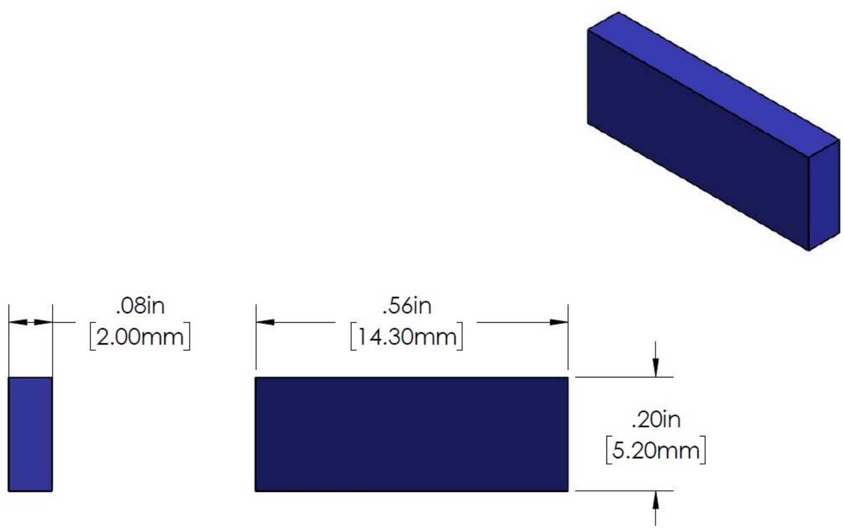

Figure 28 – Thermal Pad for Copper Section Below PFS7628C (Material: COH3114LVC-200-20, 2.0 mm).

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12.4.1.7 For Copper Section Above INN3370C

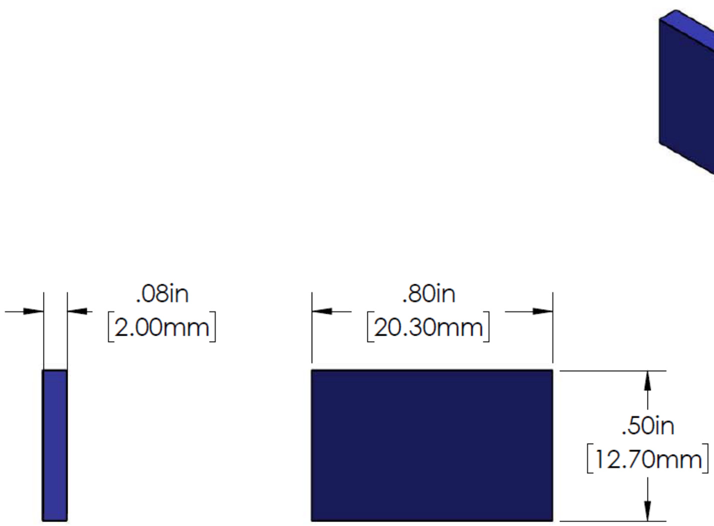

Figure 29 – Thermal Pad for Copper Section Above INN3370C (Material: COH3114LVC-200-20, 2.0 mm).

12.4.1.8 For PFC Inductor Core Top and Bottom

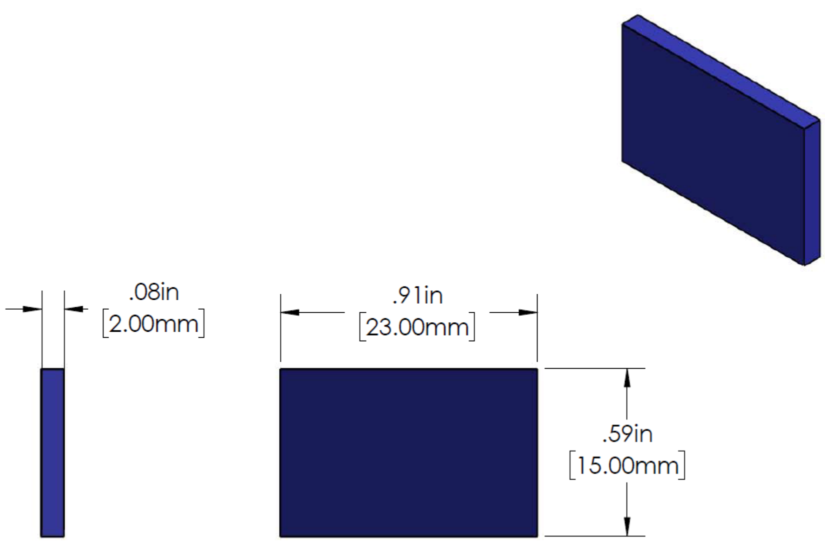

Figure 30 – Thermal Pad for PFC Inductor Top and Bottom (Material: COH3114LVC-200-20, 2.0 mm).

12.4.1.9 For Heat Spreader Inner-Bottom

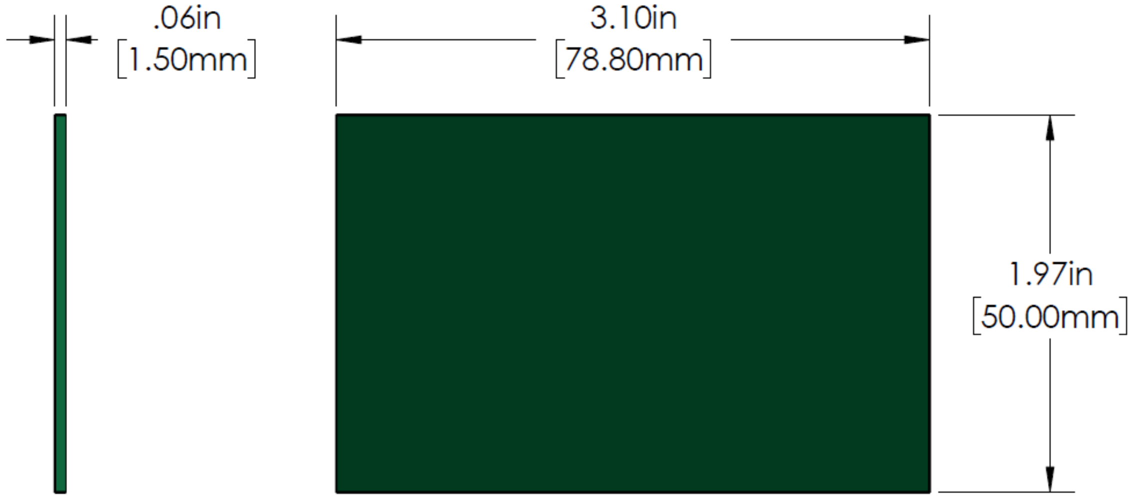

Figure 31 – Thermal Pad for Heat Spreader Inner-Bottom (Material: 3M 5549S, 1.5 mm).

12.4.1.10 For Heat Spreader Outside-Top and Outside-Bottom

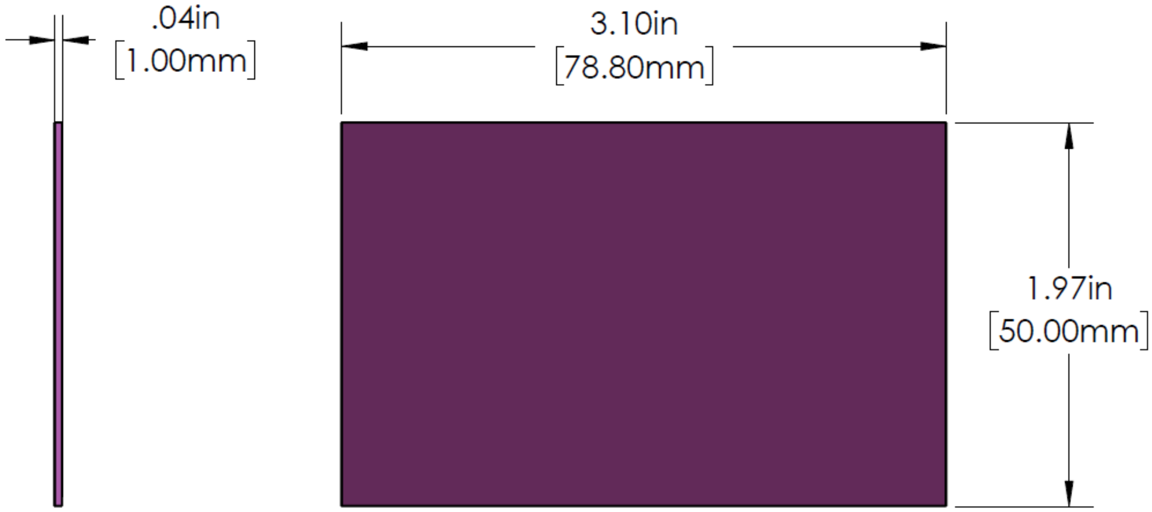

Figure 32 – Thermal Pad for Heat Spreader Outside-Top and Outside-Bottom (Material: COH3114LVC-200-10, 1.0 mm).

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12.5 *Mylar Insulator Dimensions*

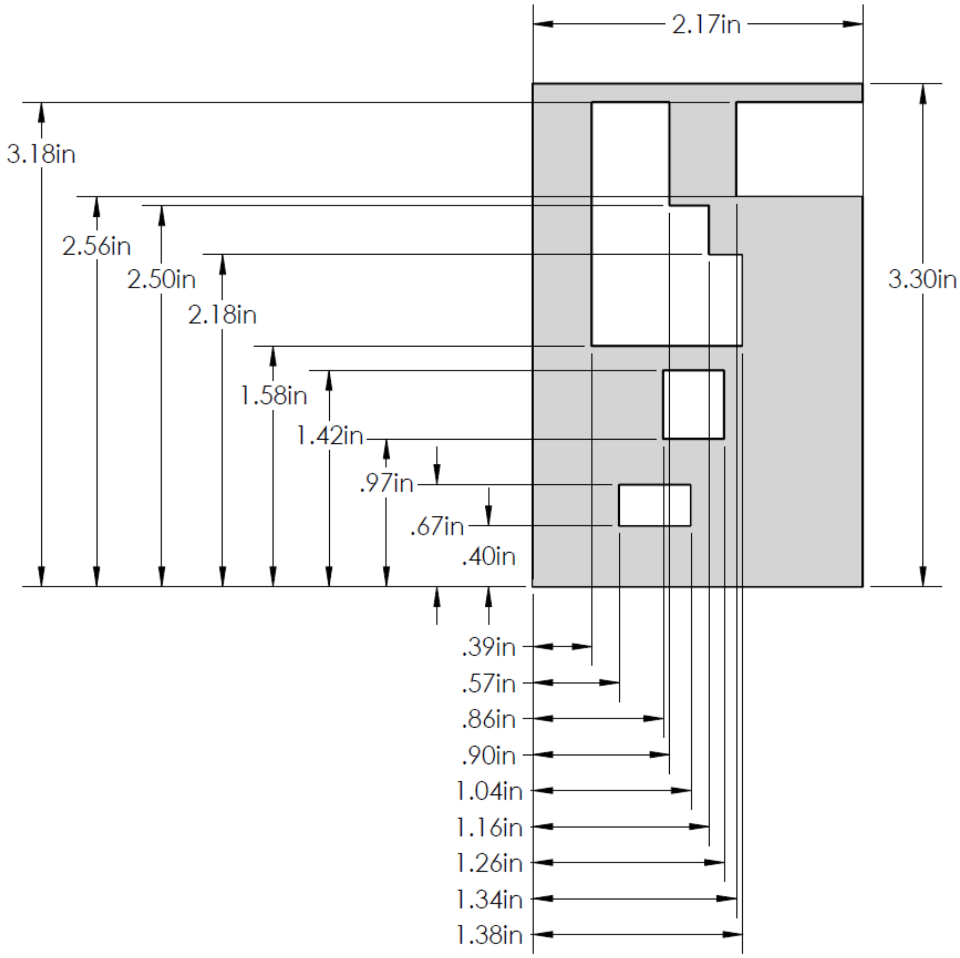
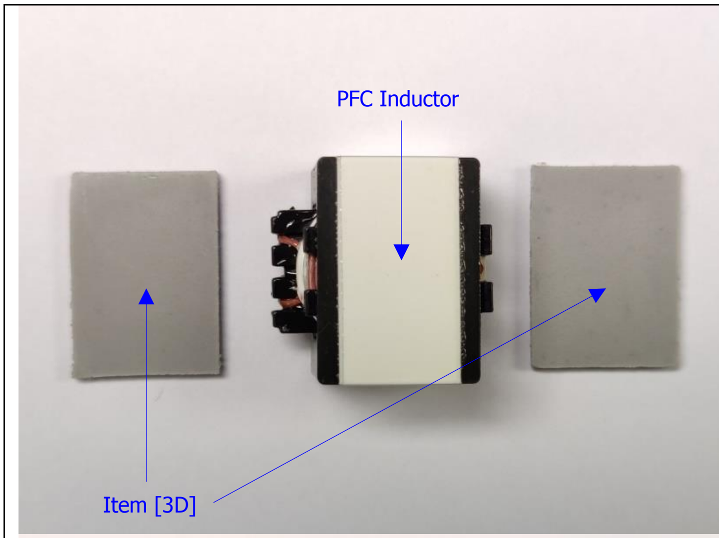
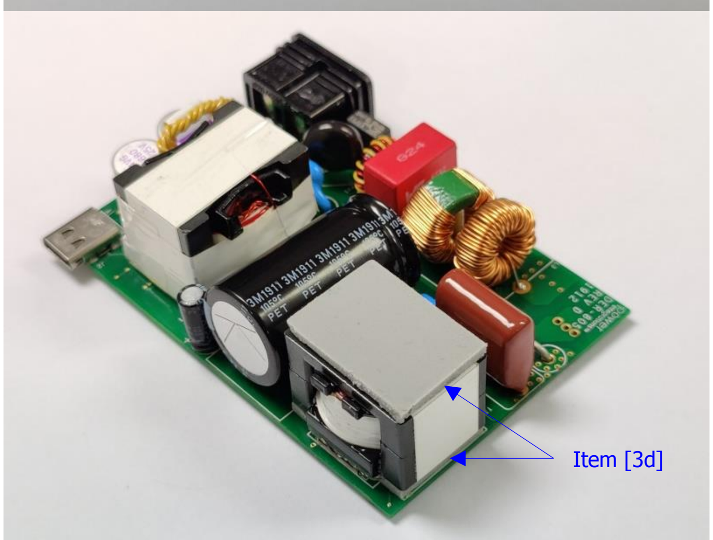
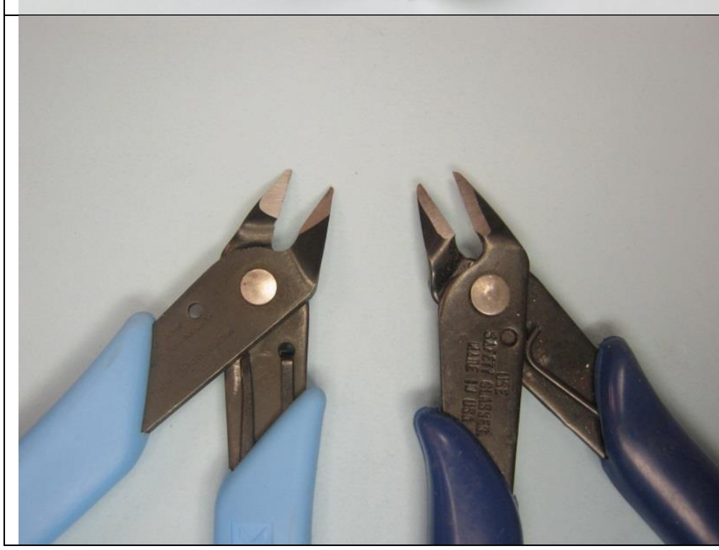


Figure 33 – Mylar Insulator Sheet (Material: DuPont Mylar WC Film, 3 mil).

12.6 *Assembly Illustrations*

	Prepare 2 pcs thermal pad Item [3D] and attach to PFC inductor core top and bottom sides.
	Solder PFC inductor into the PCB with the bottom thermal pad completely in contact with the PCB.
	Use proper flush cutters such as shown in this picture to have pins of the PCB to be flush cut in order to avoid any pins poking into the thermal pads (see next image for reference).

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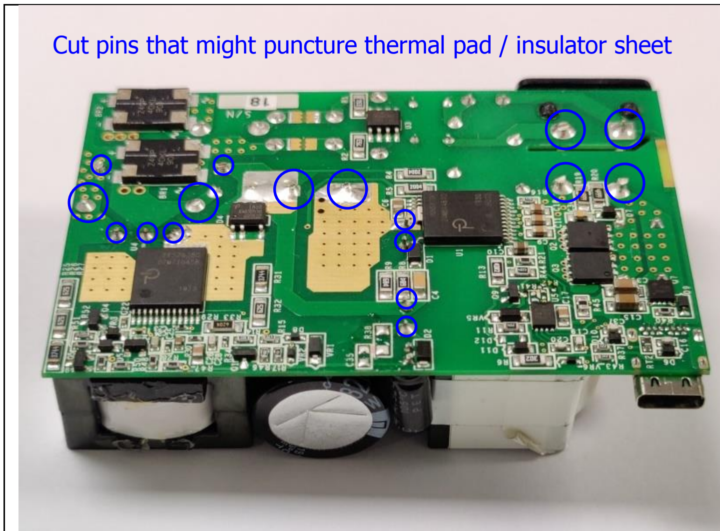
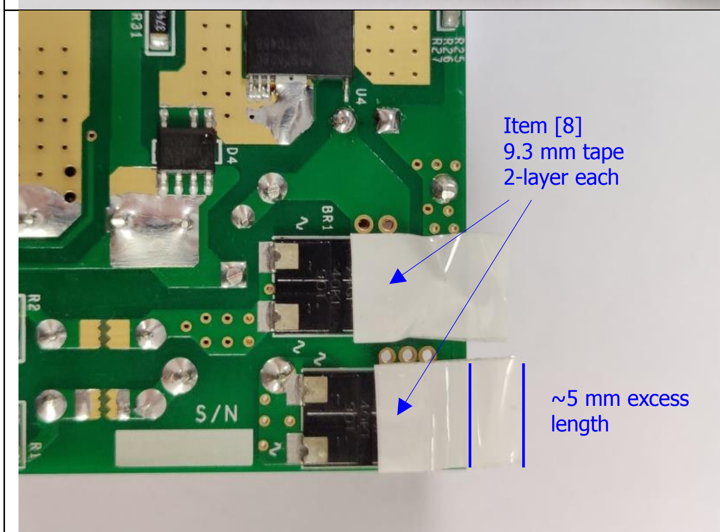
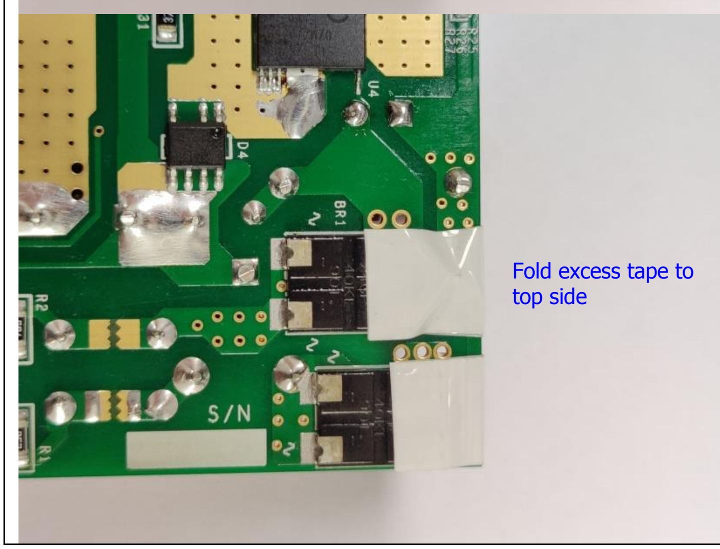
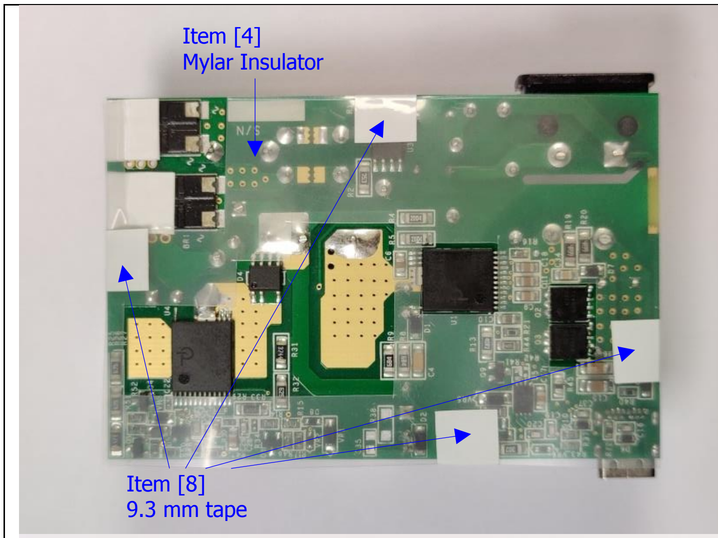
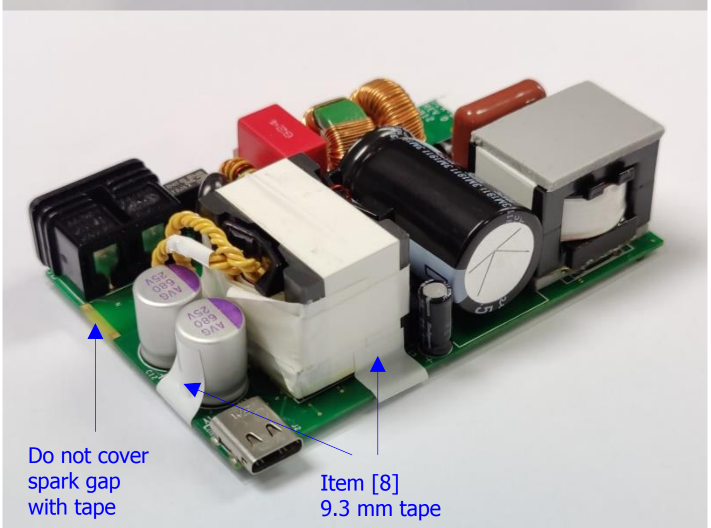
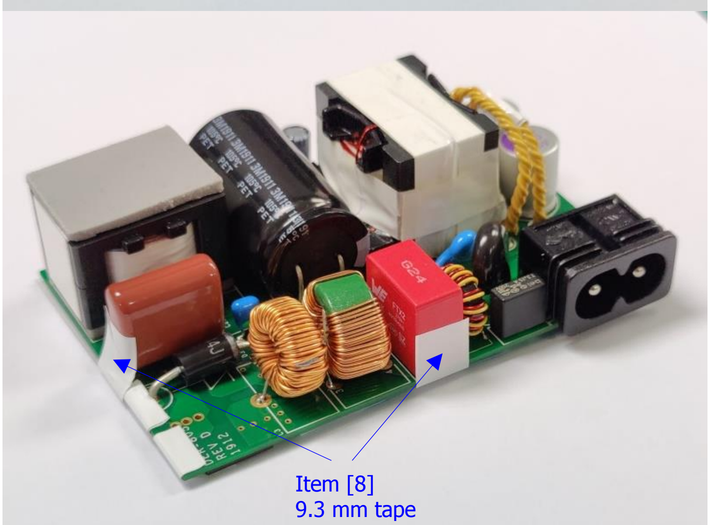
	
	Cover the two pads of BR1 and BR2 with tape Item [8], 2-layer tape for each component.
	Fold excess tape into PCB top side.







Place insulator Item [4] over PCB bottom side and secure with tape Item [8] at locations shown in the images on left.

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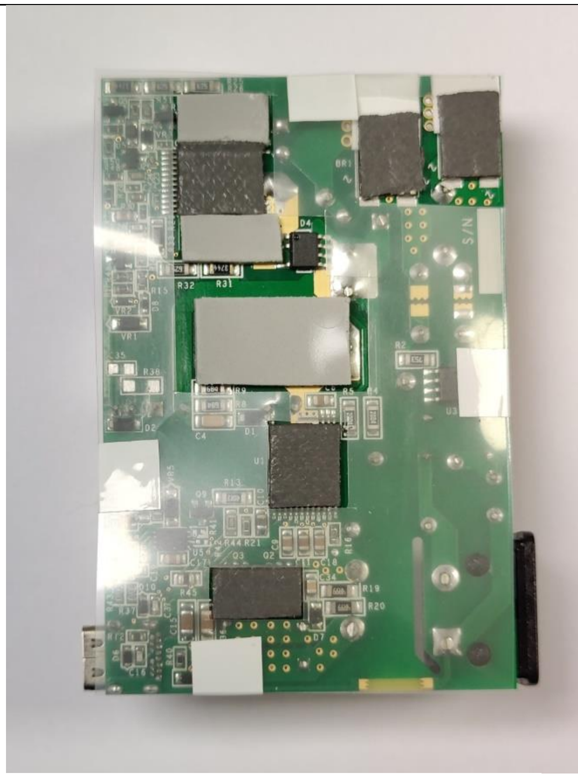
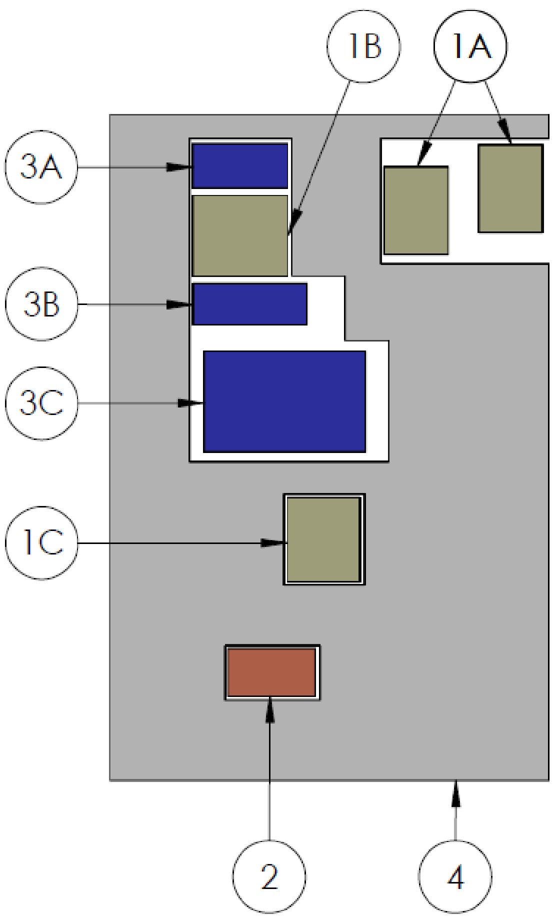
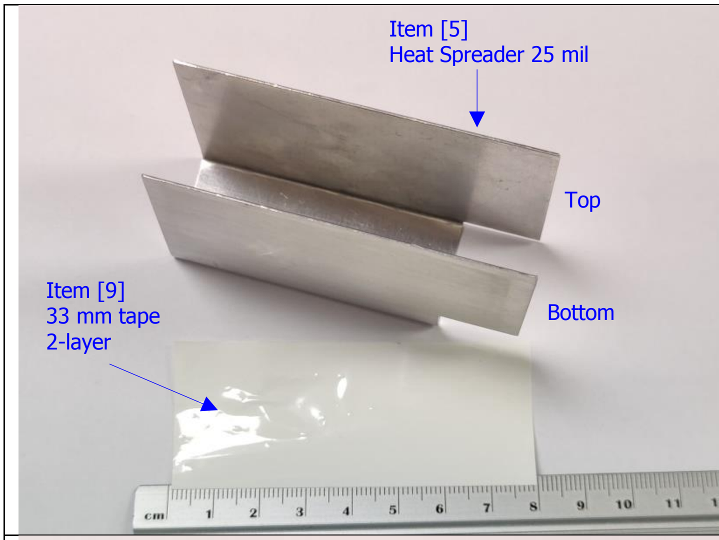
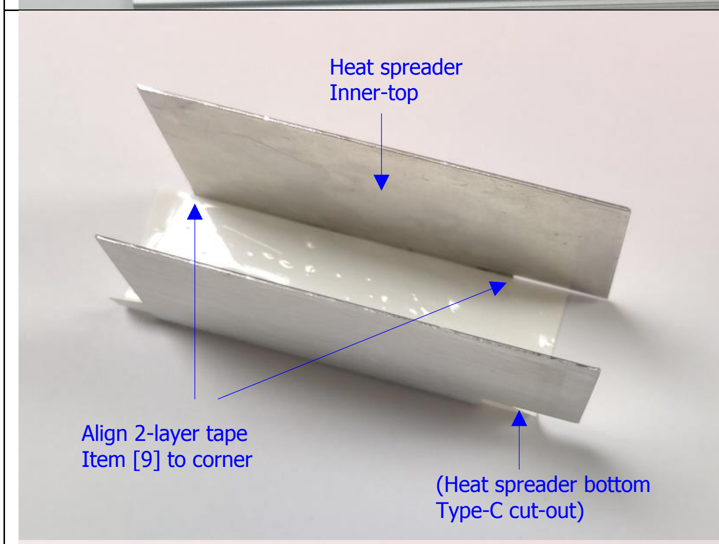
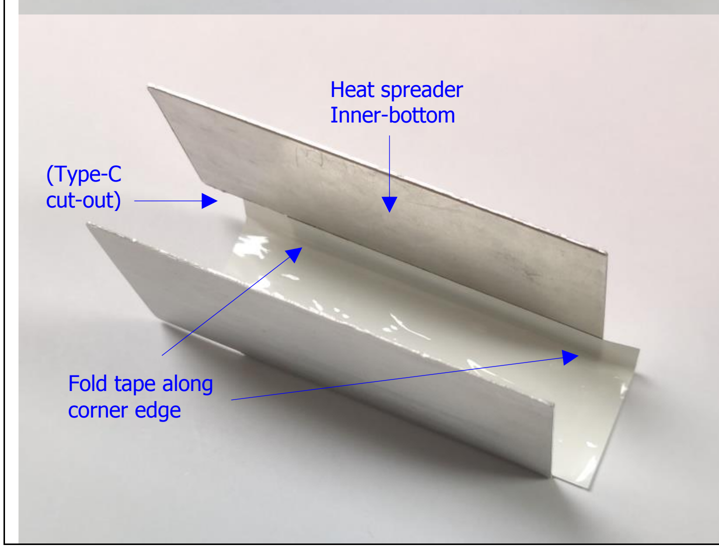
	Prepare thermal pad Items [1A], [1B], [1C], [2], [3A], [3B], and [3C].
 	Remove adhesive covers (top and bottom) and place the thermal pads to their respective locations as illustrated by the images on the left. Once done, set aside the PCB assembly and prepare aluminum heat spreader Item [5].

	Prepare heat spreader Item [5] and tape Item [9] (2-layer, ~80 mm length)
 	Place the tape inside the heat spreader as illustrated by the images on the left.

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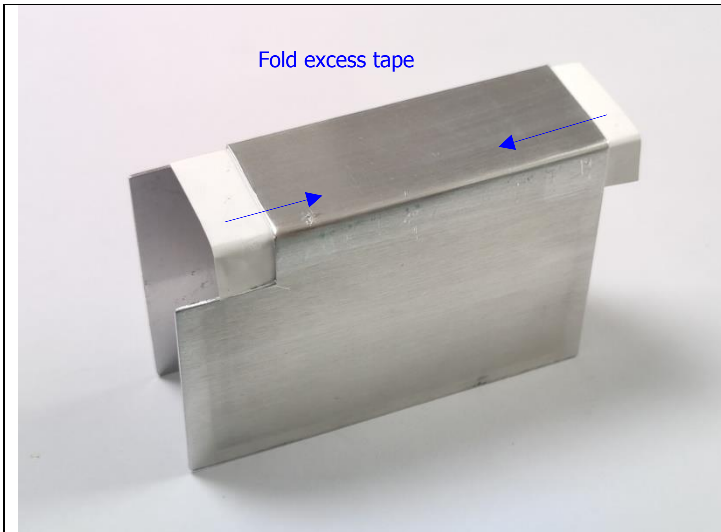
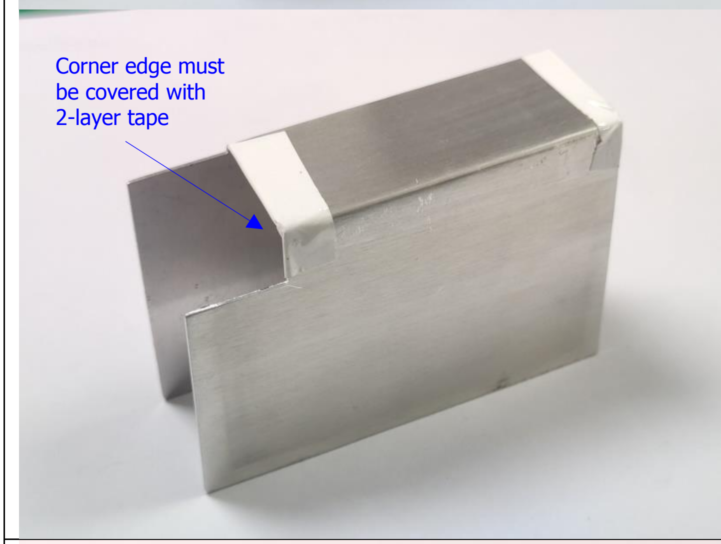
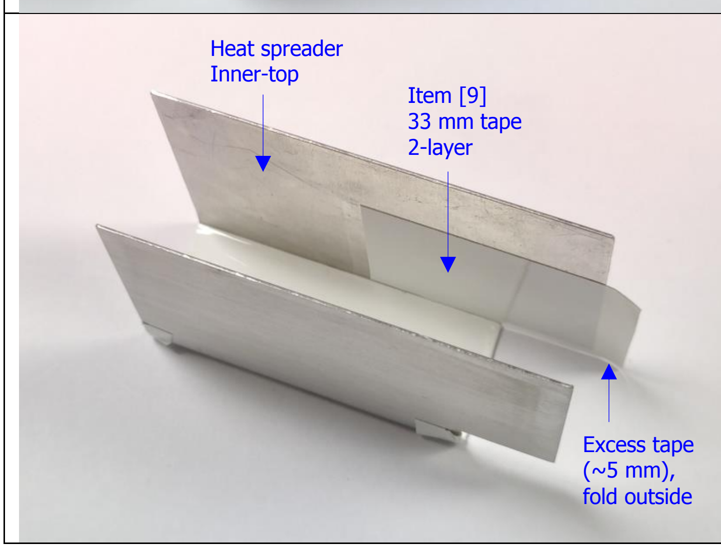
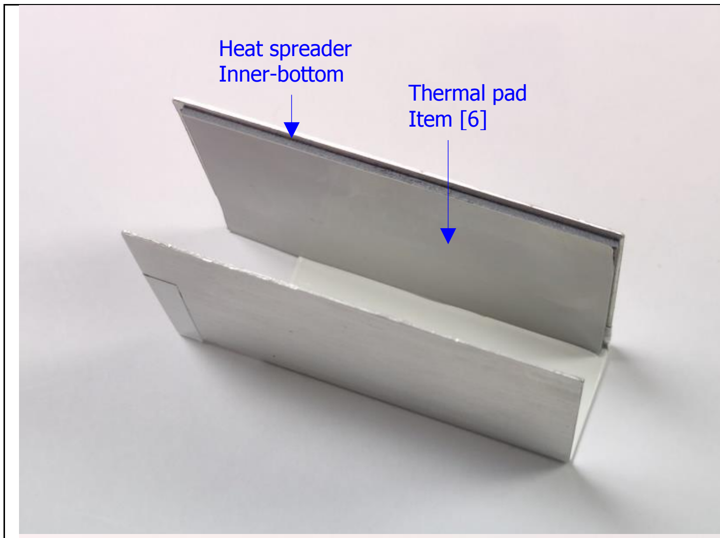
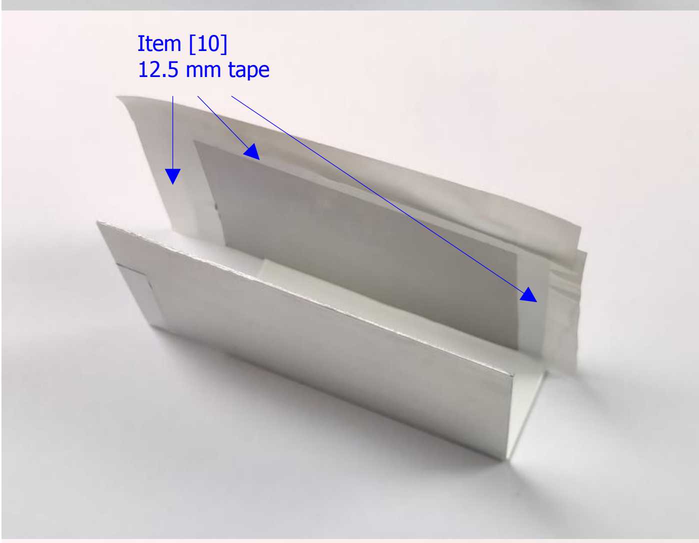
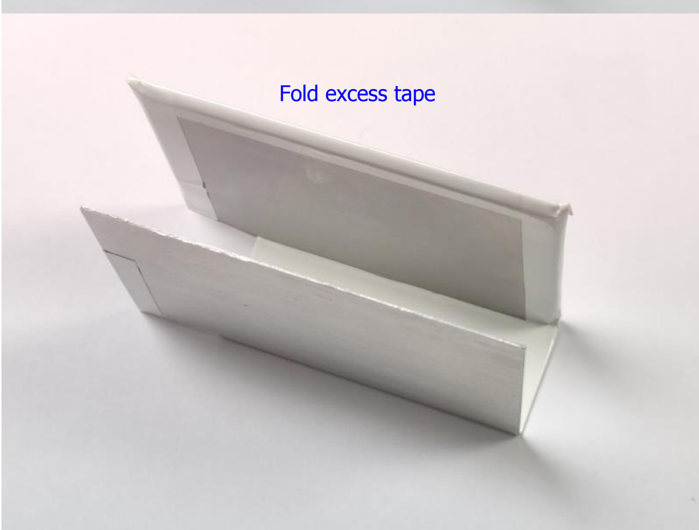
	Fold excess tape outside the heat spreader.
	Ensure that the corner near the Type-C cutout is completely covered by the 2-layer tape.
	Use tape Item [9] (2-layer, ~80 mm length) to cover portion of heat spreader inner-top. This will insulate the heat spreader from the flyback transformer core. Fold excess tape to the other side.

	Place thermal pad Item [6] to heat spreader inner-bottom.
	Secure all three edges using tape Item [10].
	

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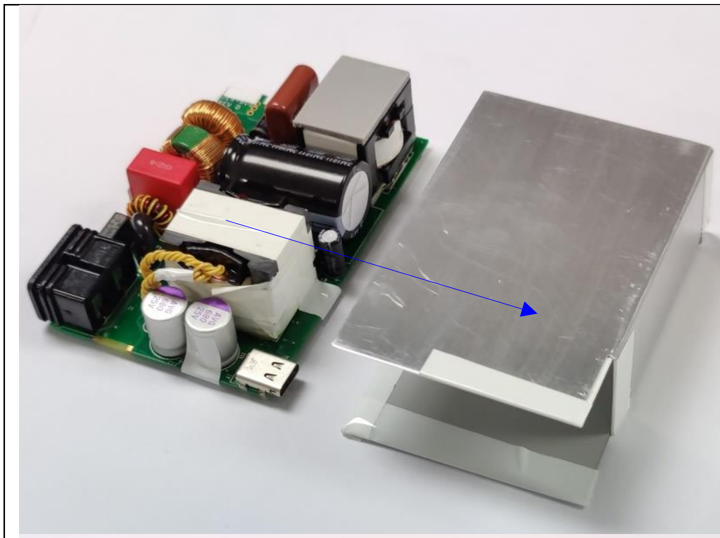
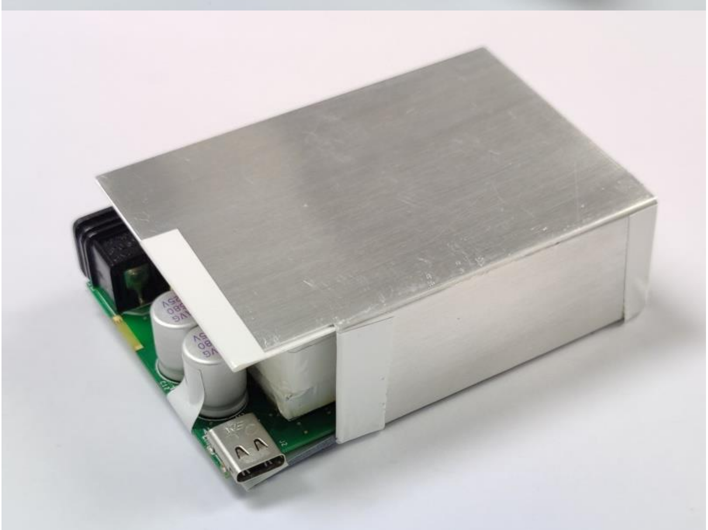
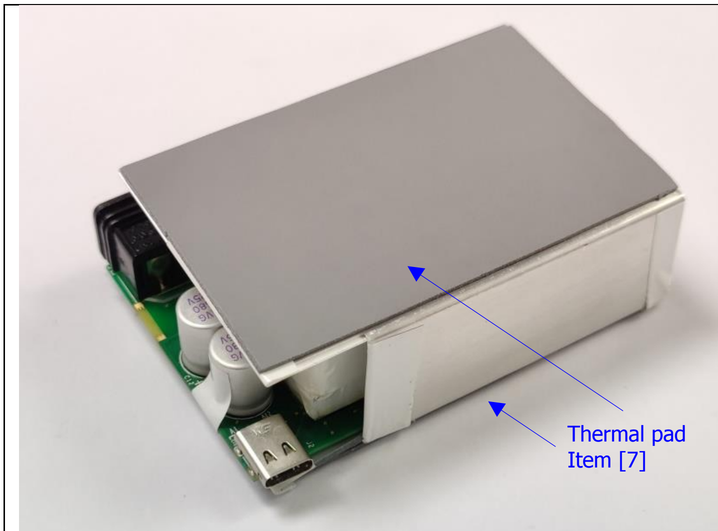
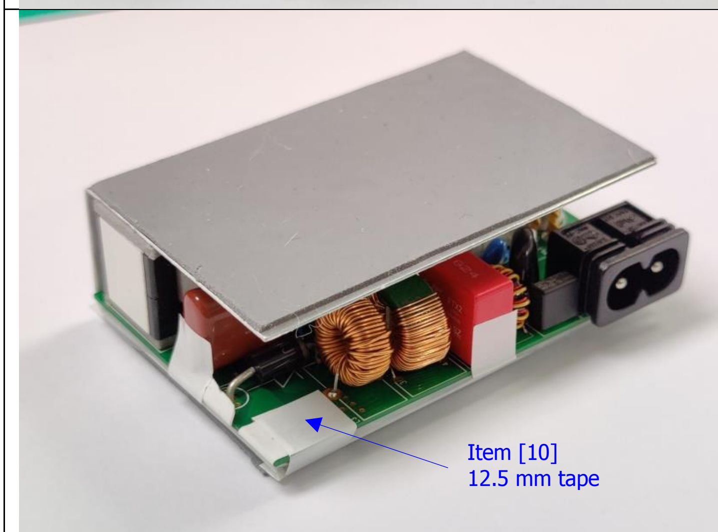
 	Insert the PCB assembly with thermal pads and mylar insulator into the heat spreader assembly.
	Prepare 2 pcs thermal pad Item [7].



Place Item [7] on heat spreader outside-top and outside-bottom.



Place tape Item [10] as illustrated by the image on the left to improve contact between thermal pad [1A] of BR2 and the heat spreader.

Place the entire assembly into enclosure – bottom Item [11], and then complete with enclosure – top Item [12].

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 	Finish assembly.

13 Performance Data

All the performance data have been taken on the board unless otherwise specifically mentioned.

Note: Some power supply designs are made with enclosures and/or heat spreaders to achieve the desired form factor. In such situations, these designs are tested with enclosure and any additional heat spreaders as indicated in the report. Although the DER boards are shipped without any enclosures and /or heat spreaders, the report should be reviewed carefully regarding test conditions used for assessment of performance. Unless otherwise specified, the DER boards can be evaluated without enclosures or heat spreaders though some performance results such as EMI, temperature rise of components and efficiency may vary.

13.1 *Efficiency vs. Line*

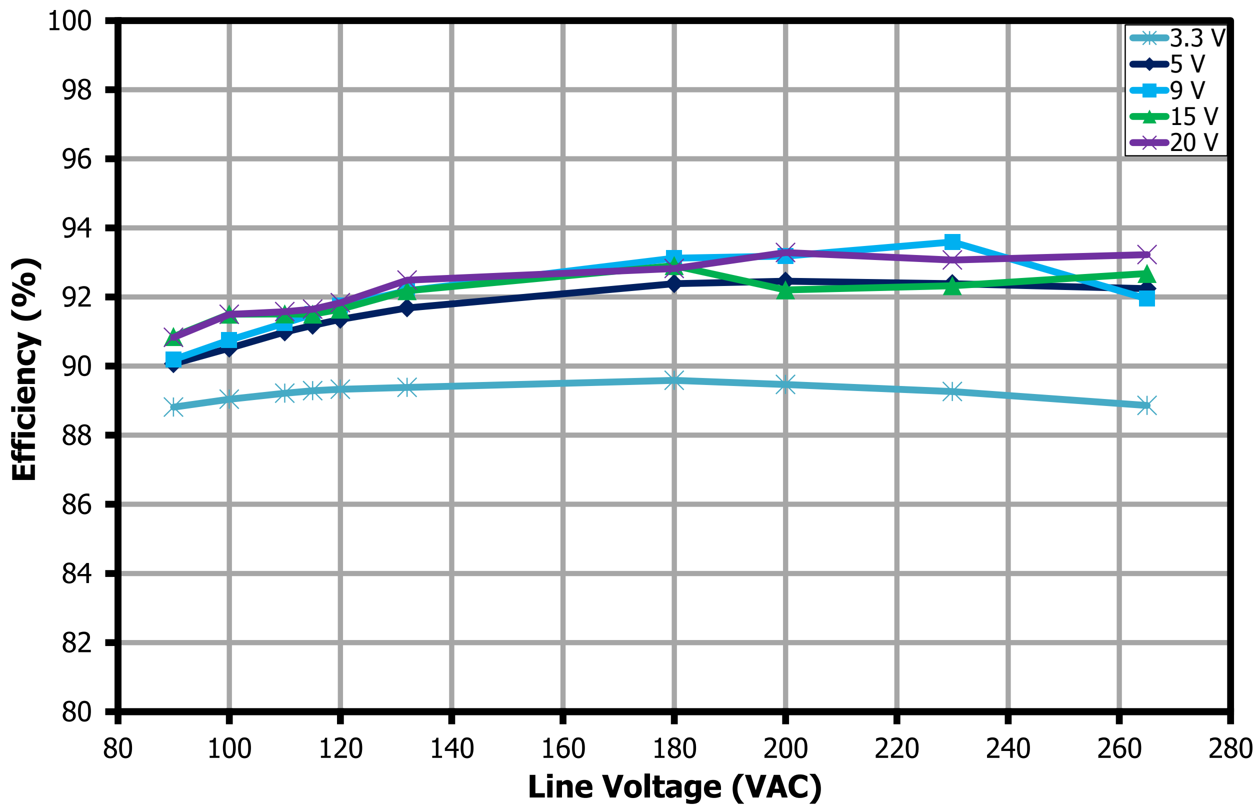

Figure 34 – Efficiency vs. Line, Room Ambient.

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13.2 No-Load Input Power at 5 V_{OUT}

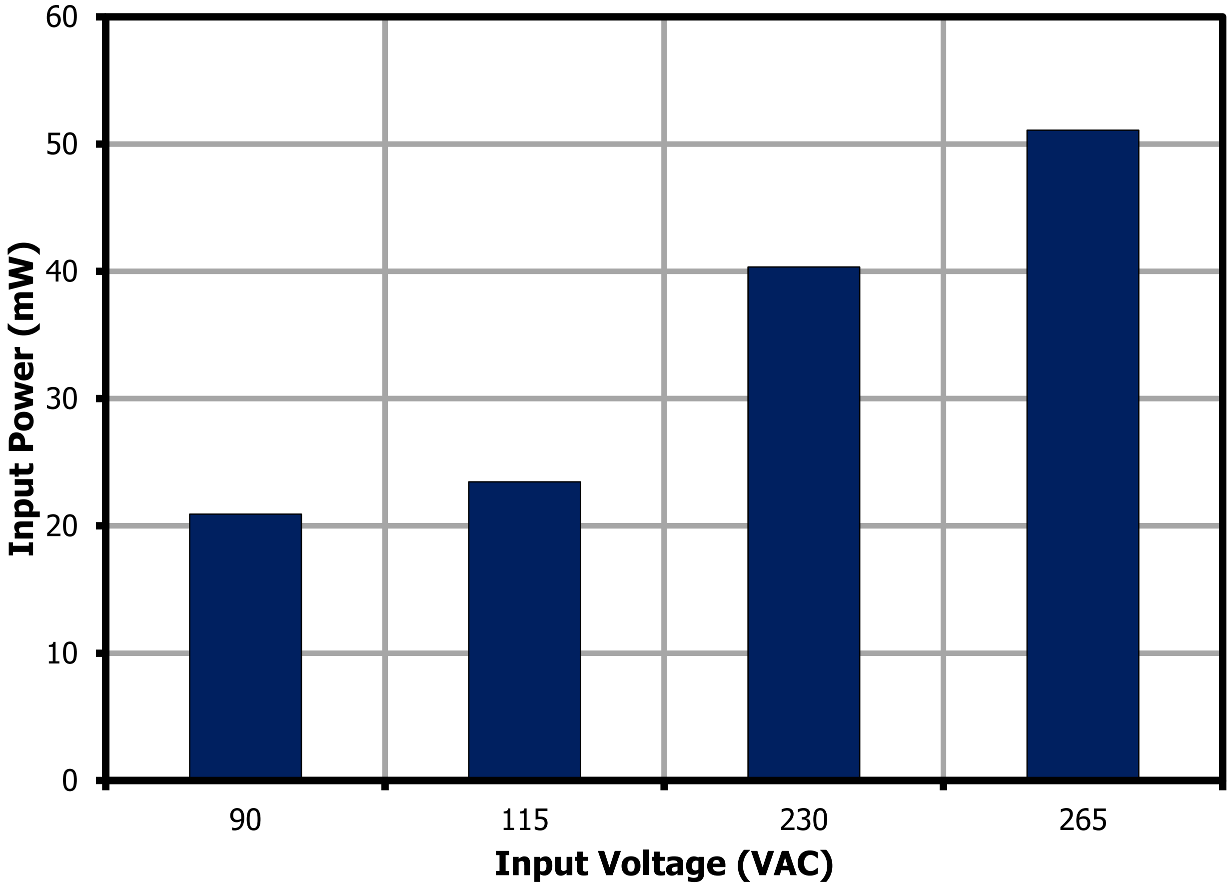

Figure 35 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

13.3 Average Efficiency Requirements

Output Voltage (V)	Model (V)	Test Power [W]	Average DOE6 Limit (%)	Average CoC v5 Tier 1 (%)	Average CoC v5 Tier 2 (%)	10% Load CoC v5 Tier 1 (%)	10% Load CoC v5 Tier 2 (%)
3.3	<6	16.5	82.47	79.8	82.47	70.2	73.08
5	<6	25	84.25	82.9	85.0	73.18	75.47
9	>6	45	87.73	88.43	88.8	78.43	78.85
15	>6	75	88.00	89.00	89.00	79.00	79.00
20	>6	100	88.00	89.00	89.00	79.00	79.00

13.4 Average and 10% Efficiency at 115 VAC Input

13.4.1 V_{OUT} = 3.3 V

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	16.31	89.57	89.33
75	12.31	90.01	
50	8.22	89.63	
25	4.12	88.10	
10	1.64	84.38	

13.4.2 V_{OUT} = 5 V

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	24.73	91.22	91.53
75	18.65	91.37	
50	12.43	92.04	
25	6.22	91.51	
10	2.48	89.87	

13.4.3 V_{OUT} = 9 V

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	45.00	91.56	91.96
75	33.89	91.90	
50	22.56	92.30	
25	11.29	92.10	
10	4.49	89.75	

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13.4.4 V_{OUT} = 15 V

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	74.80	91.51	90.8
75	56.35	91.53	
50	37.44	91.18	
25	18.72	88.99	
10	7.45	83.62	

13.4.5 V_{OUT} = 20 V

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	99.64	91.66	91.09
75	74.96	91.54	
50	49.82	91.30	
25	24.92	89.85	
10	9.90	83.51	

13.5 **Average and 10% Efficiency at 230 VAC Input**

13.5.1 V_{OUT} = 3.3 V

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	16.40	89.31	87.14
75	12.34	88.36	
50	8.24	87.16	
25	4.13	83.74	
10	1.64	78.66	

13.5.2 V_{OUT} = 5 V

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	24.83	92.42	91.49
75	18.69	91.77	
50	12.44	91.59	
25	6.23	90.18	
10	2.48	87.69	

13.5.3 V_{OUT} = 9 V

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	45.00	93.08	92.59
75	33.90	92.94	
50	22.54	92.81	
25	11.27	91.55	
10	4.49	87.83	

13.5.4 V_{OUT} = 15 V

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	74.84	92.35	90.48
75	56.37	91.79	
50	37.45	90.83	
25	18.73	86.93	
10	7.45	79.19	

13.5.5 V_{OUT} = 20 V

% Load	P_{OUT} (W)	Efficiency (%)	Average Efficiency (%)
100	99.70	93.02	91.17
75	75.00	92.40	
50	49.84	91.47	
25	24.93	87.78	
10	9.90	79.23	

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13.6 Line Regulation

13.6.1 V_{OUT} = 3.3 V

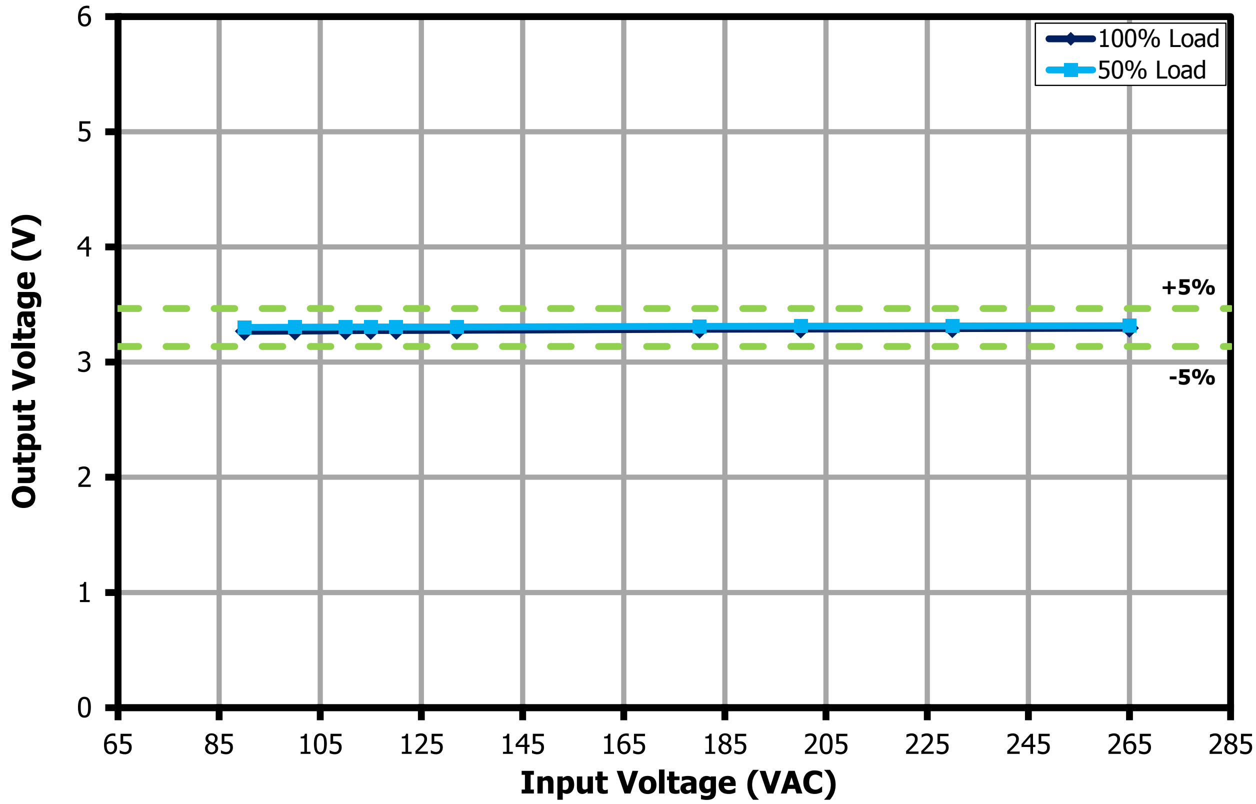

Figure 36 – Output Voltage vs. Input Voltage, Room Temperature.

13.6.2 V_{OUT} = 5 V

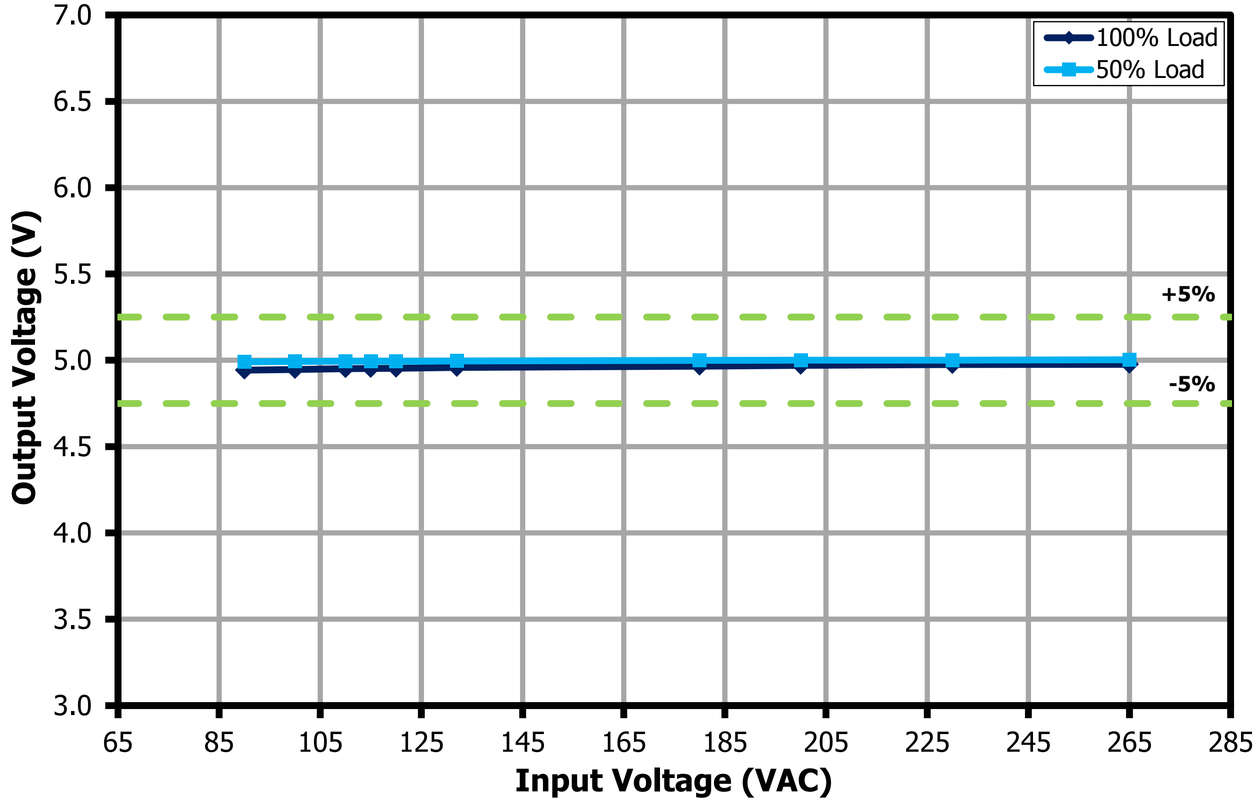

Figure 37 – Output Voltage vs. Input Voltage, Room Temperature.

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13.6.3 V_{OUT} = 9 V

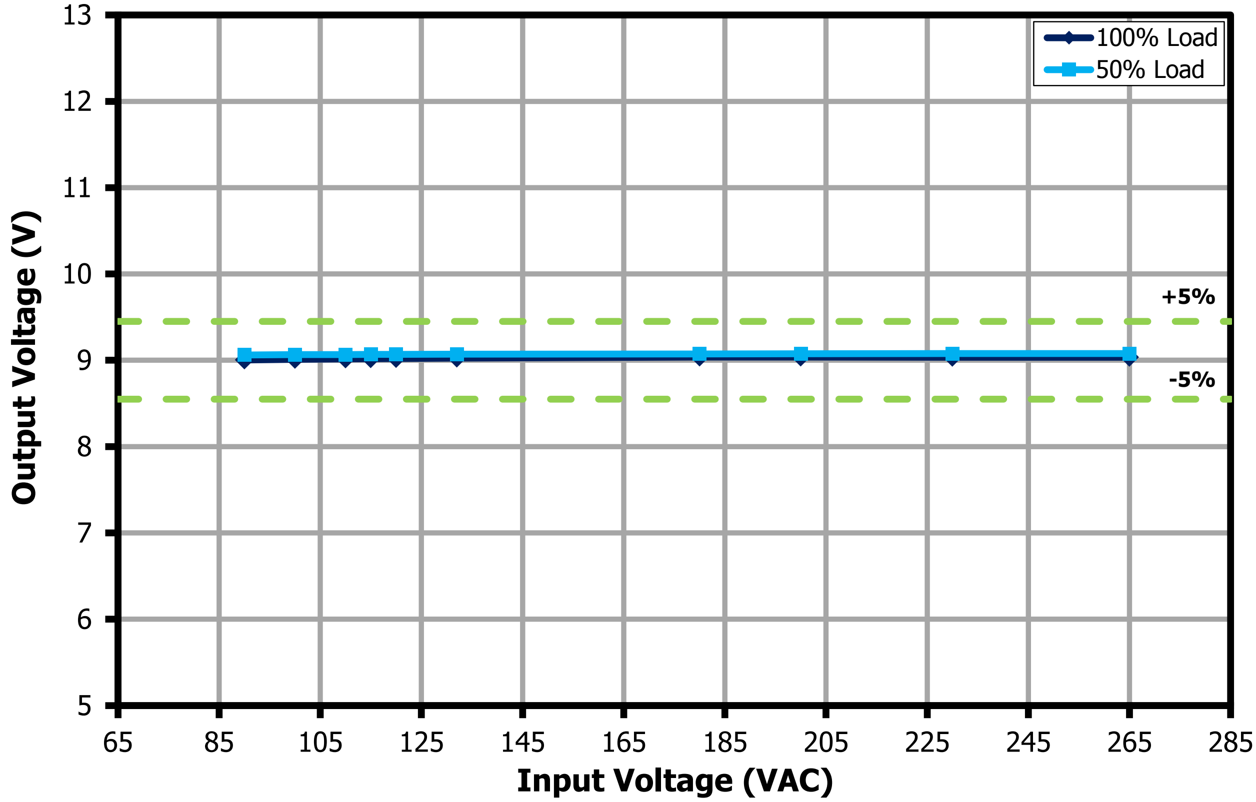

Figure 38 – Output Voltage vs. Input Voltage, Room Temperature.

13.6.4 V_{OUT} = 15 V

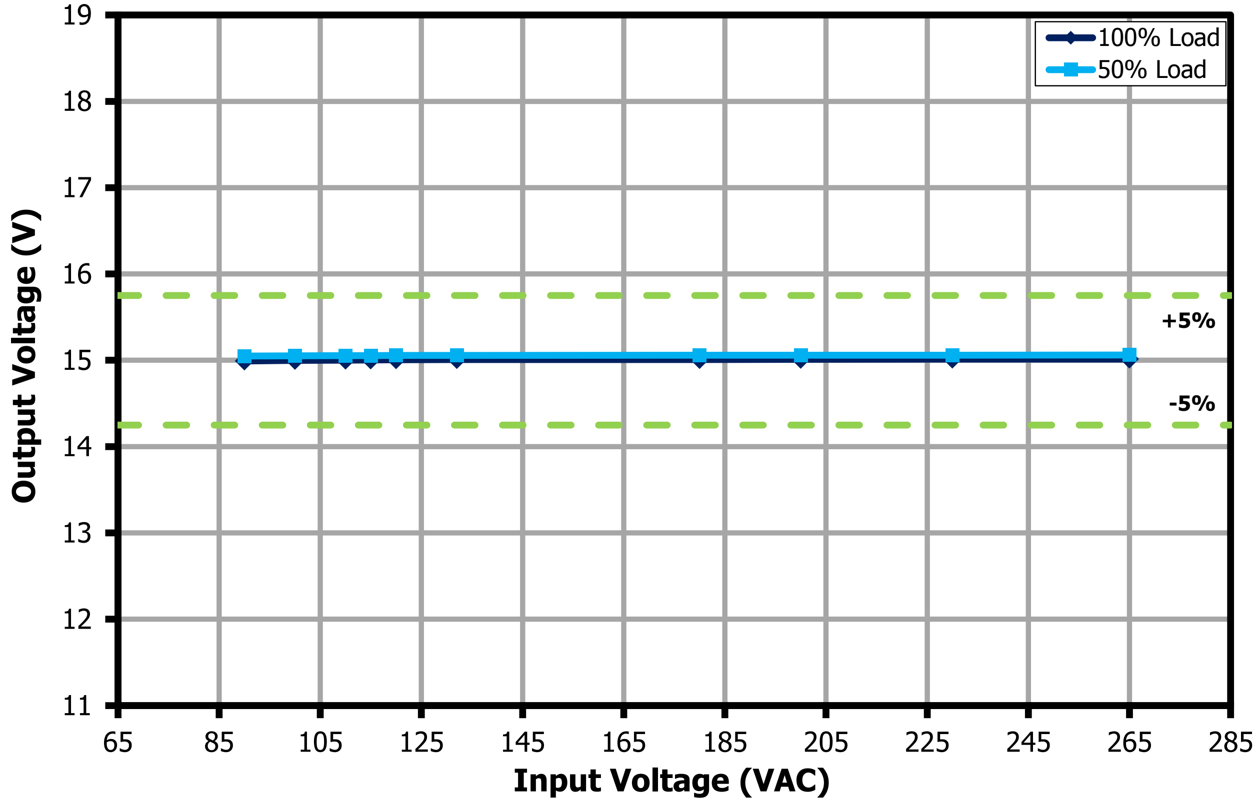

Figure 39 – Output Voltage vs. Input Voltage, Room Temperature.

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13.6.5 V_{OUT} = 20 V

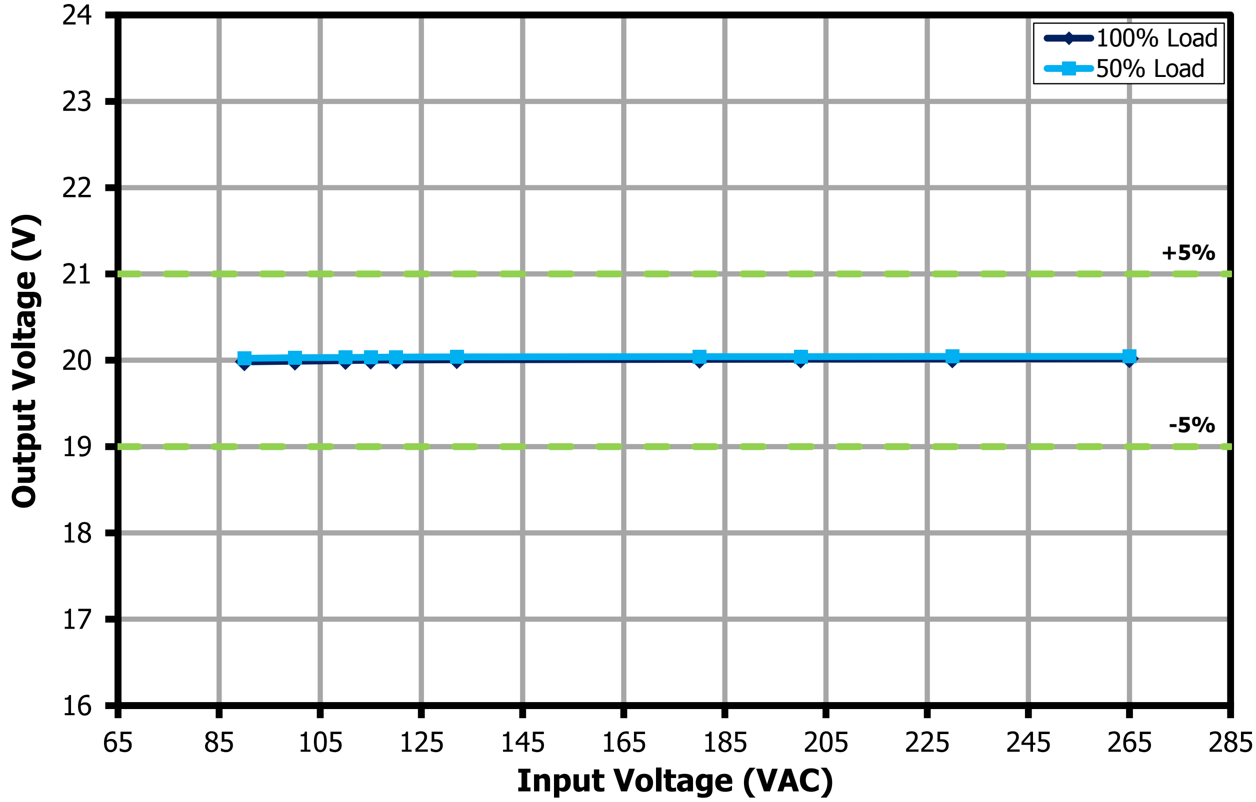

Figure 40 – Output Voltage vs. Input Voltage, Room Temperature.

13.7 Load Regulation

Load regulation data was captured on board.

13.7.1 V_{OUT} = 3.3 V

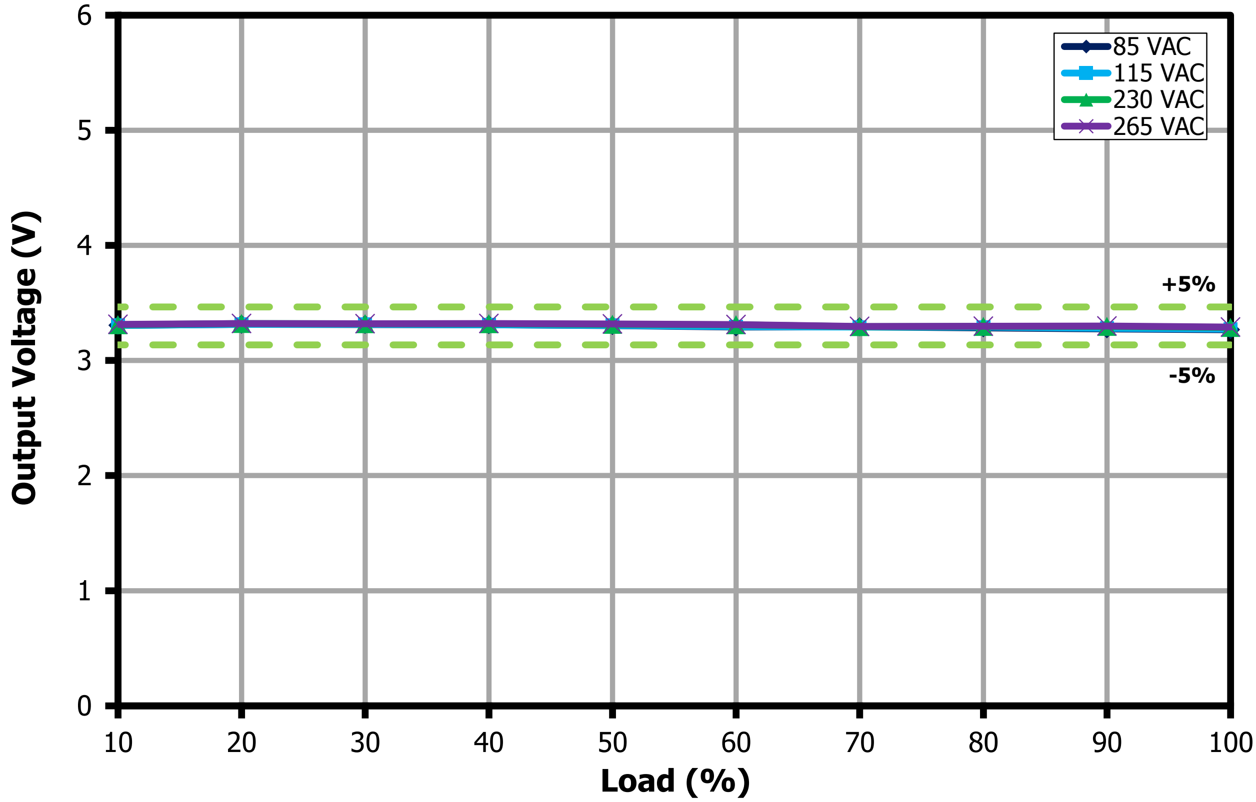

Figure 41 – Output Voltage vs. Load Current, Room Temperature.

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13.7.2 V_{OUT} = 5 V

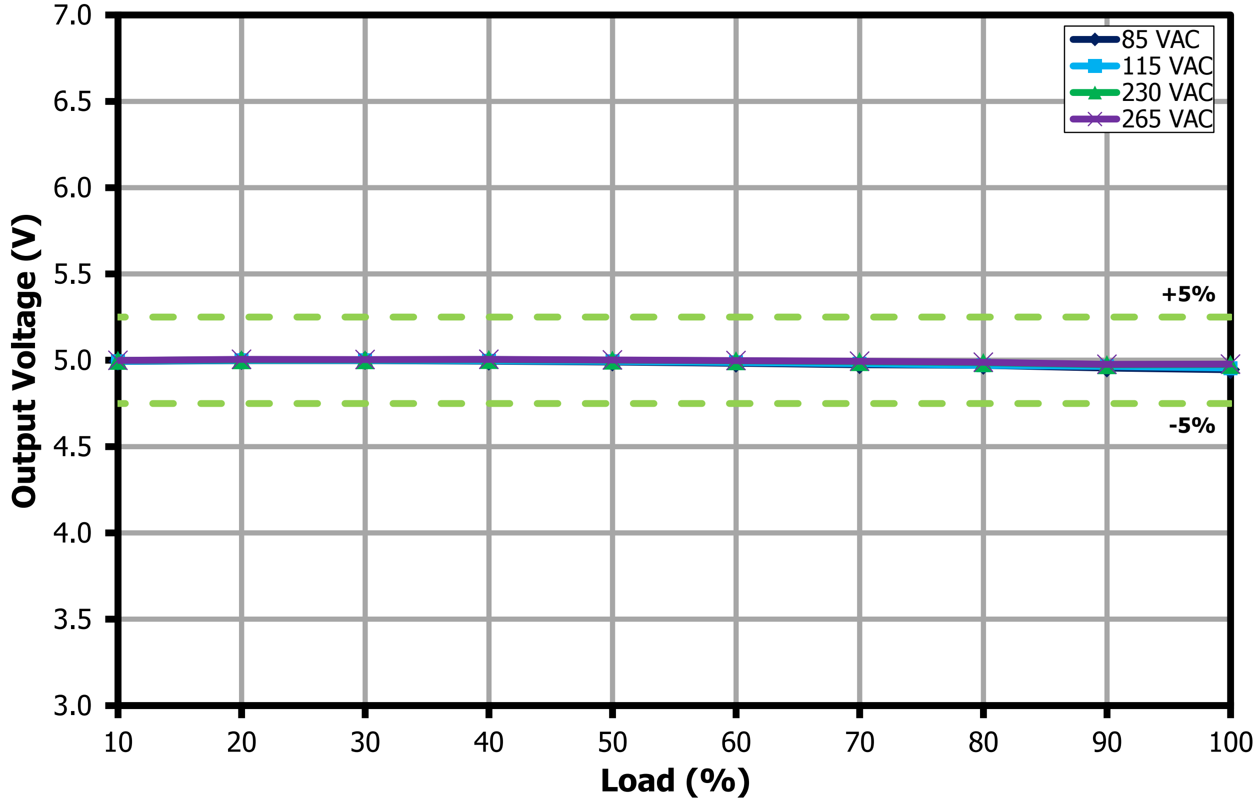

Figure 42 – Output Voltage vs. Load Current, Room Temperature.

13.7.3 V_{OUT} = 9 V

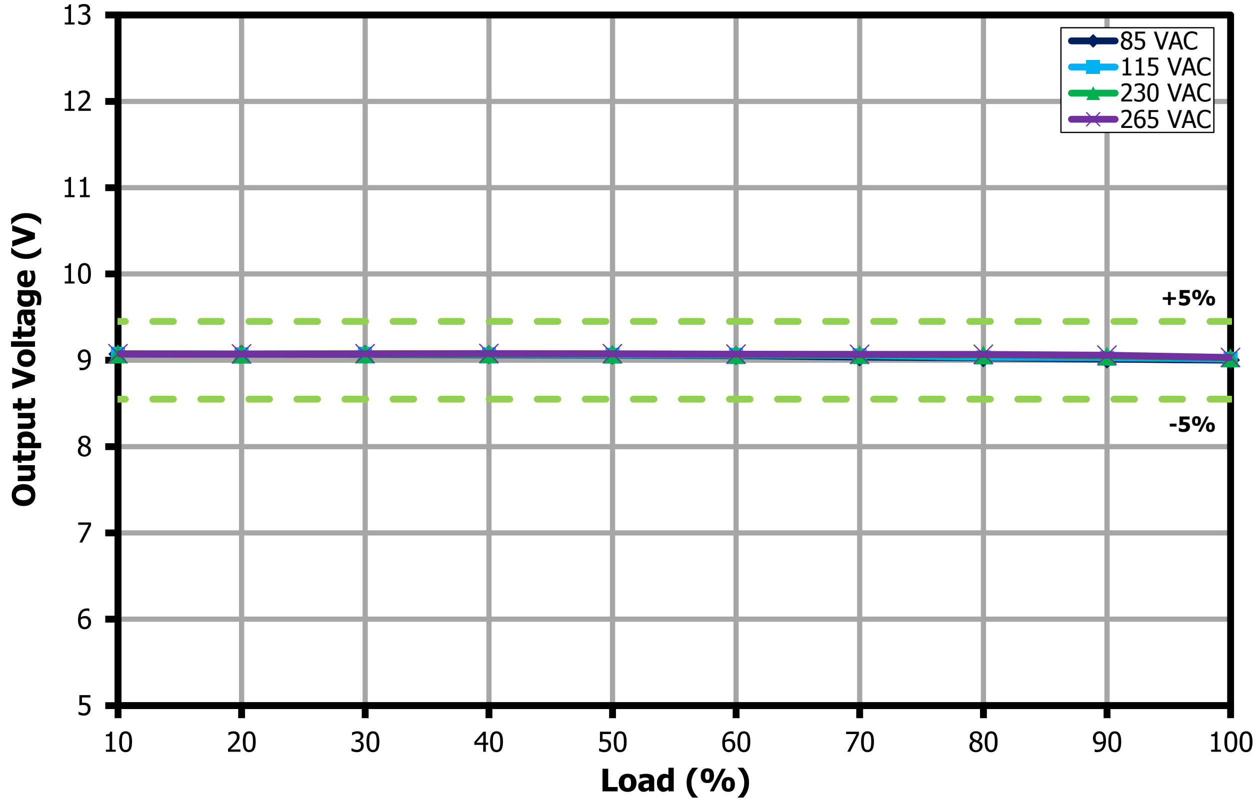

Figure 43 – Output Voltage vs. Load Current, Room Temperature.

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13.7.4 V_{OUT} = 15 V

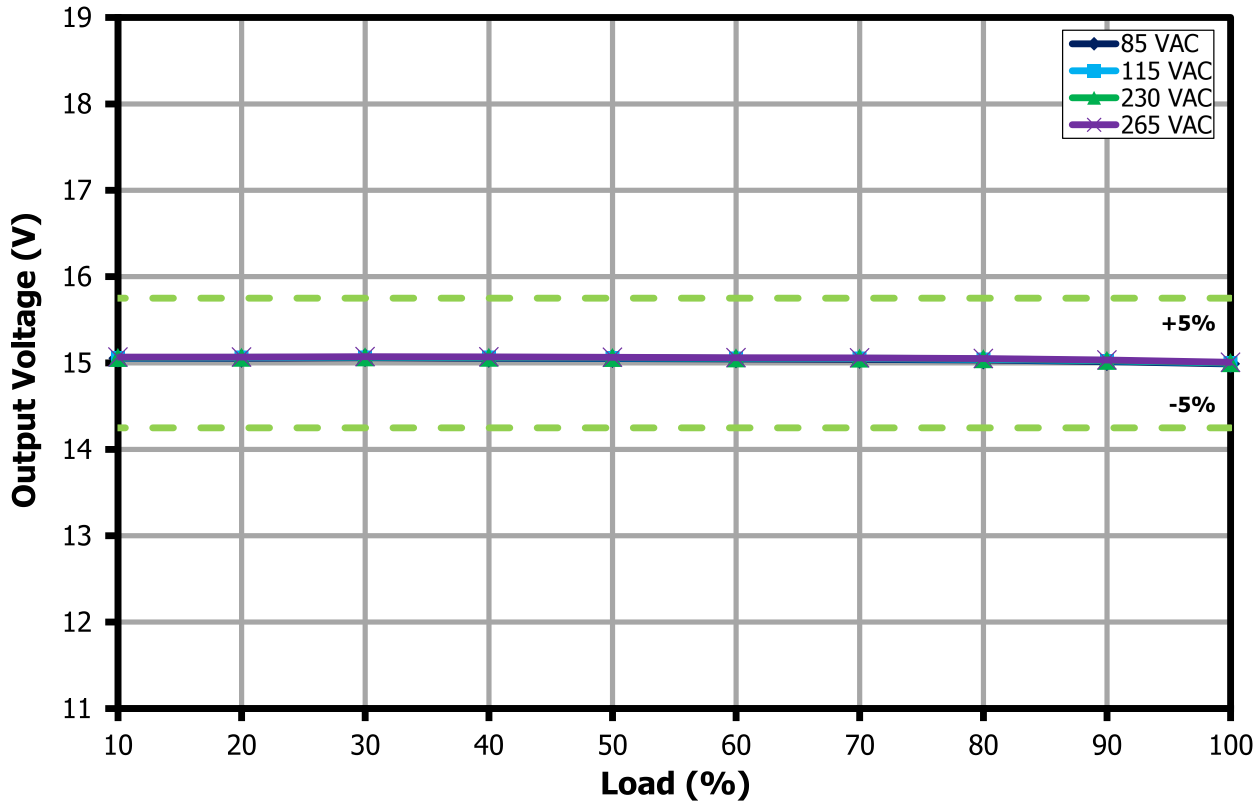

Figure 44 – Output Voltage vs. Load Current, Room Temperature.

13.7.5 V_{OUT} = 20 V

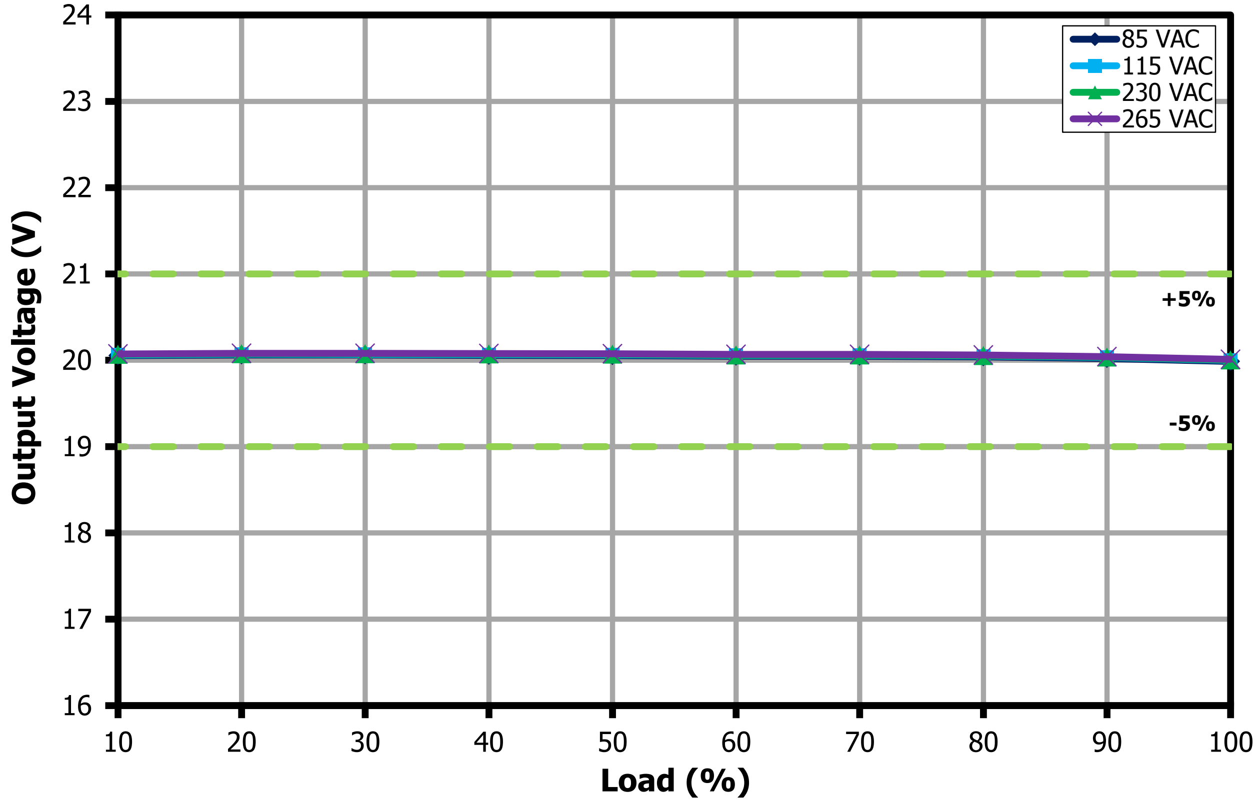

Figure 45 – Output Voltage vs. Load current, Room Temperature.

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13.8 ***CV/CC***

CV/CC characteristic was captured on board.

13.8.1 V_{OUT} = 3.3 V

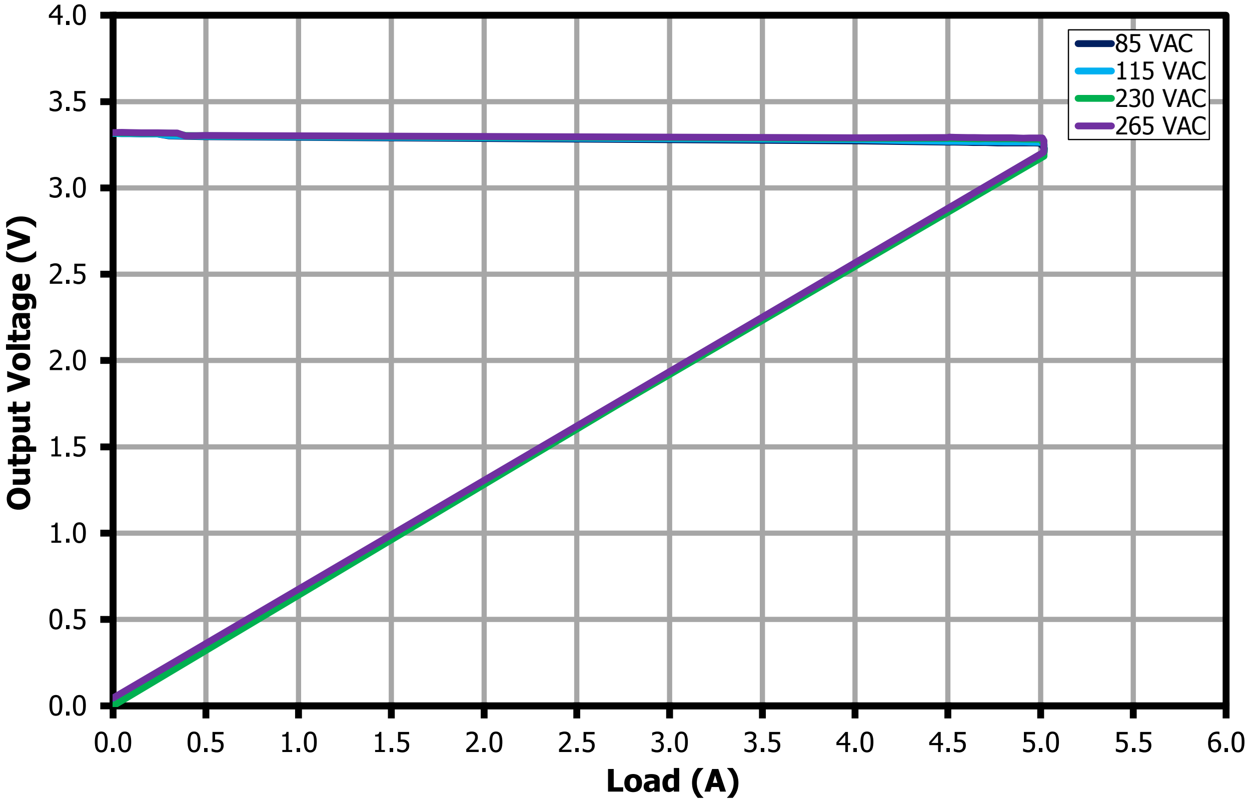

Figure 46 – Output Voltage vs. Output Current Across AC Input Voltage, Room Temperature, 3.3 V.

13.8.2 V_{OUT} = 5 V

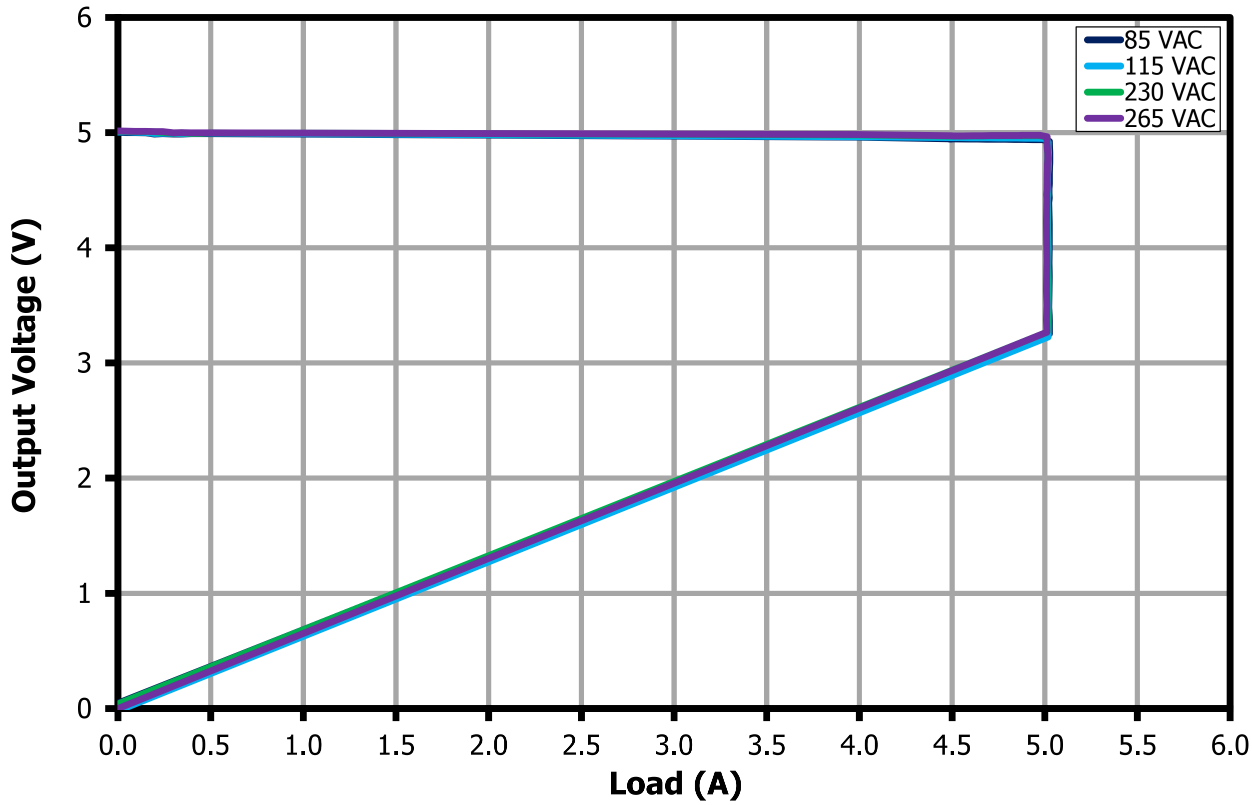

Figure 47 – Output Voltage vs. Output Current Across AC Input Voltage, Room Temperature, 5 V.

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13.8.3 V_{OUT} = 9 V

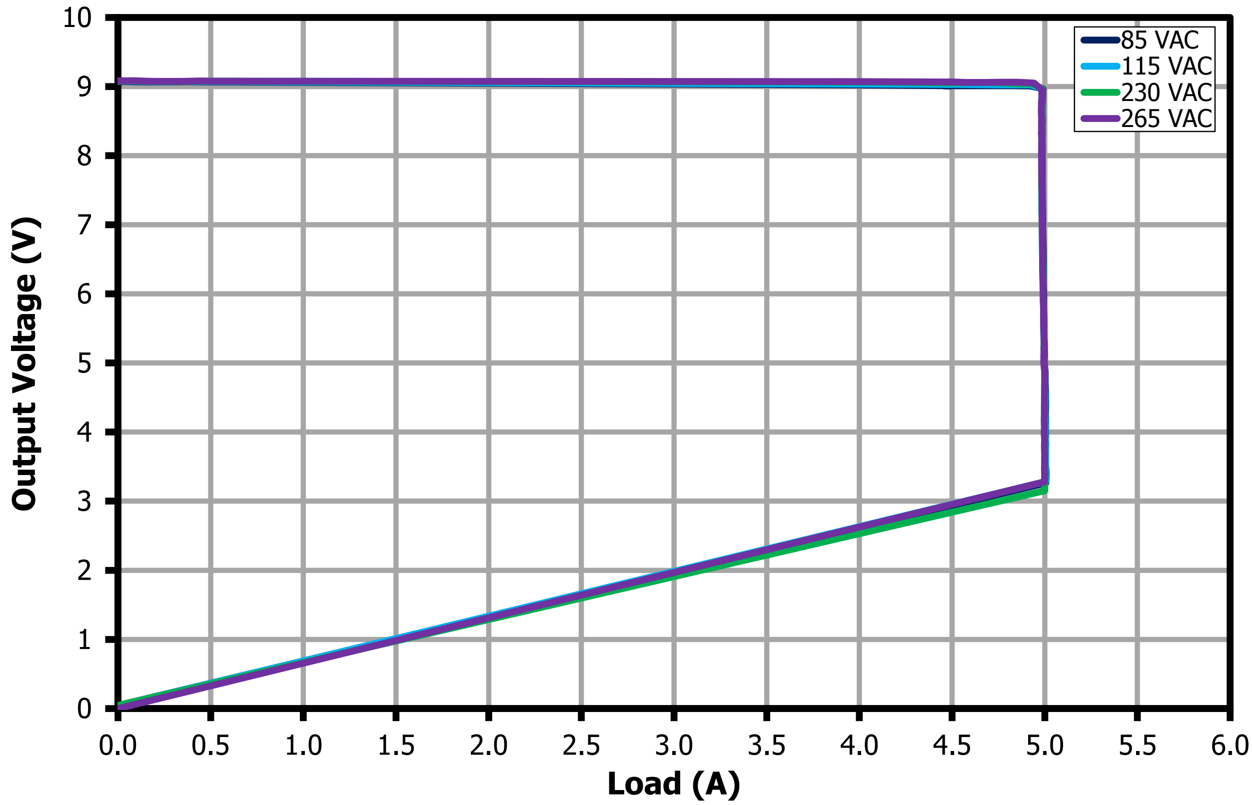

Figure 48 – Output Voltage vs. Output Current Across AC Input Voltage, Room Temperature, 9 V.

13.8.4 V_{OUT} = 15 V

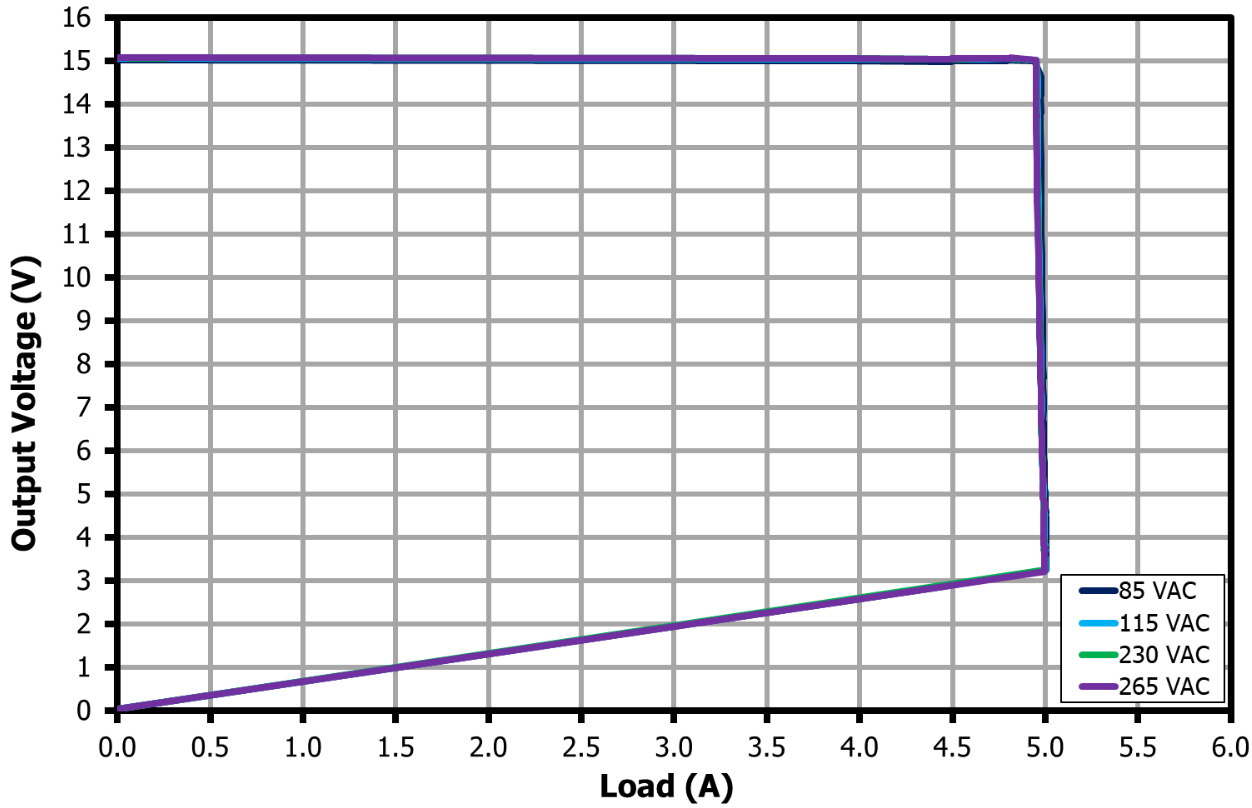

Figure 49 – Output Voltage vs. Output Current Across AC Input Voltage, Room Temperature, 15 V.

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13.8.5 V_{OUT} = 20 V

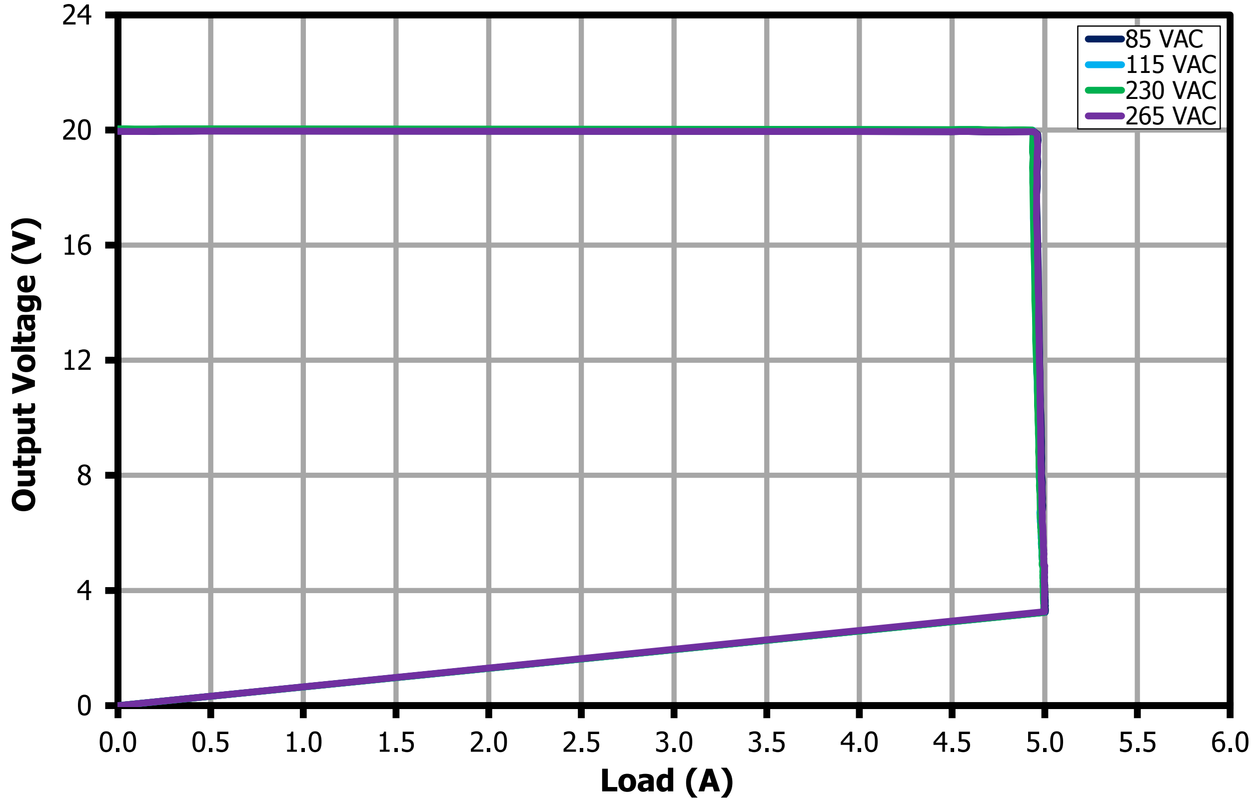

Figure 50 – Output Voltage vs. Output Current Across AC Input Voltage, Room Temperature, 20 V.

14 Thermal Performance

Thermal performance is measured room temperature.

14.1 *90 VAC, 20 V / 5 A Load*

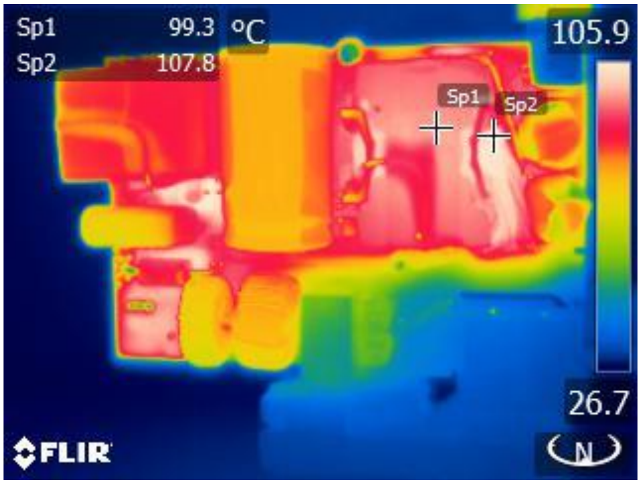

Figure 51 – Top Side. 90 VAC, Full Load.

	Meas.	ºC
Ambient		31
Transformer Core (T1)	Sp1	99.3
Transformer Winding (T1)	Sp2	107.8

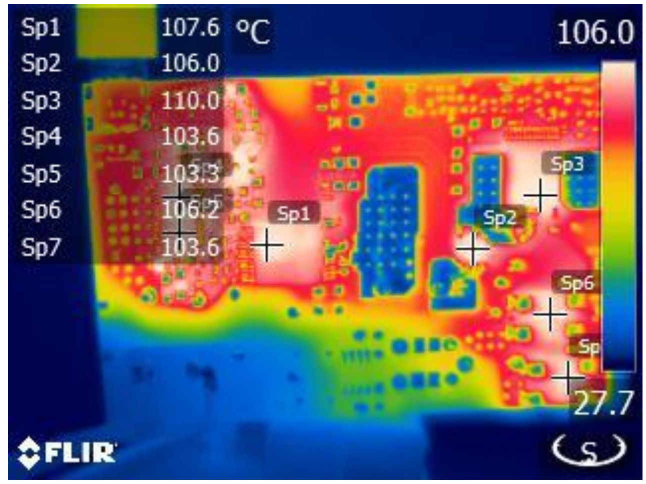

Figure 52 – Bottom Side. 90 VAC, Full Load.

	Meas.	ºC
Ambient		31
InnoSwitch3-Pro (U1)	Sp1	107.6
Boost Diode (D4)	Sp2	106
PFS Device (U4)	Sp3	110
SR FET (Q2)	Sp4	103.6
SR FET (Q3)	Sp5	103.3
Bridge (BR1)	Sp6	106.2
Bridge (BR2)	Sp7	103.6

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14.2 ***265 VAC, 20 V / 5 A Load***

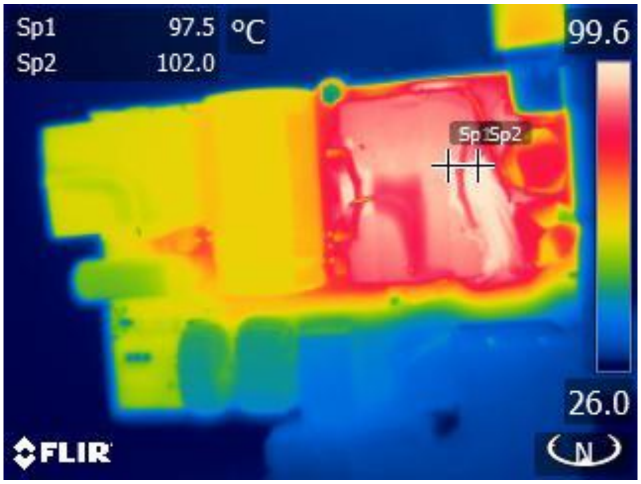

Figure 53 – Top Side. 265 VAC, Full Load.

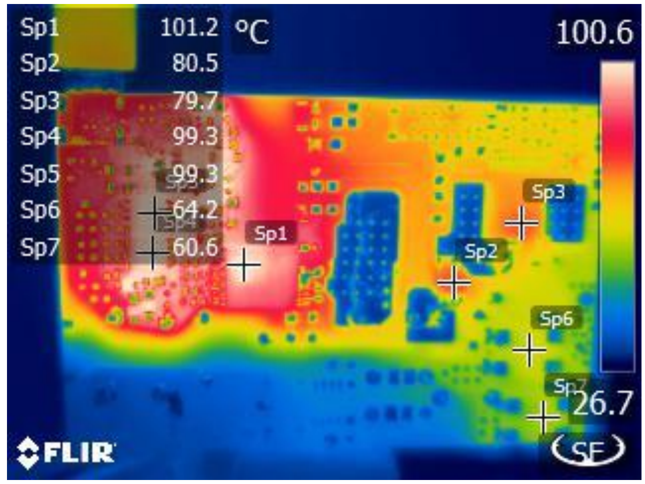

Figure 54 – Bottom Side. 265 VAC, Full Load.

	Meas.	ºC
Ambient		31
Transformer Core (T1)	Sp1	97.5
Transformer Winding (T1)	Sp2	102

	Meas.	ºC
Ambient		31
InnoSwitch3-Pro (U1)	Sp1	101.2
Boost Diode (D4)	Sp2	80.5
PFS Device (U4)	Sp3	79.7
SR FET (Q2)	Sp4	99.3
SR FET (Q3)	Sp5	99.3
Bridge (BR1)	Sp6	64.2
Bridge (BR2)	Sp7	60.6

14.3 *90 VAC, 20 V / 5 A Load (Enclosed Thermal Performance)*

No.	Location	Temperature
1	Heat Spreader	92.5
2	Ambient	45
3	SR1	105.6
4	InnoSwitch Source	102.8
5	Boost Diode	108.6
6	PFS	105.8
7	Bridge1	106.4
8	Bridge2	107.6
9	CMC	109.7
10	TR Core	99.5
11	Output Capacitor	97
12	PFC Inductor Core	90.2
13	Bulk Capacitor	96.4
14	PFC Inductor Winding	93.2
15	TR Winding	106.7
16	Case Internal	88.4
17	Case External	75.3

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15 Waveforms

15.1 *Input Voltage and Current Waveforms*

15.1.1 Output: 15 V / 5 A

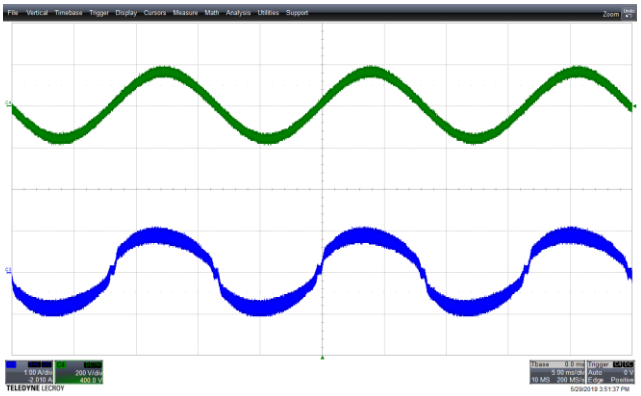

Figure 55 – Input Voltage and Current.
115 VAC, 15.0 V, 5 A Load.
C4: V_{IN}, 200 V / div.
C3: I_{IN}, 1 A / div., 5 ms / div.

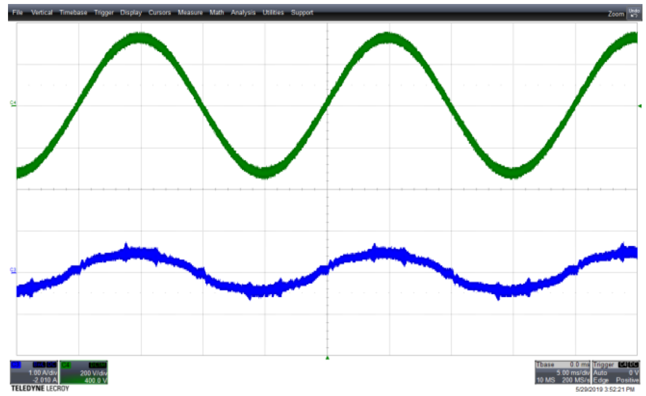

Figure 56 – Input Voltage and Current.
230 VAC, 15.0 V, 5 A Load.
C4: V_{IN}, 200 V / div.
C3: I_{IN}, 1 A / div., 5 ms / div.

15.1.2 Output: 20 V / 5 A

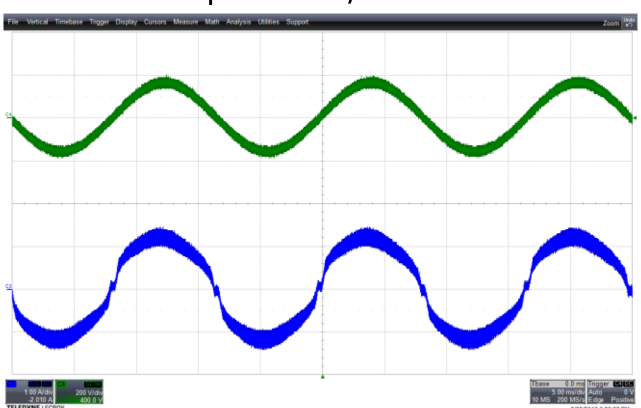

Figure 57 – Input Voltage and Current.
115 VAC, 20.0 V, 5 A Load.
C4: V_{IN}, 200 V / div.
C3: I_{IN}, 1 A / div., 5 ms / div.

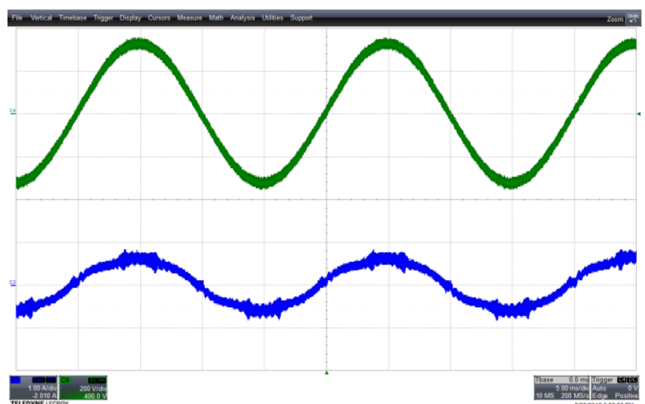

Figure 58 – Input Voltage and Current.
230 VAC, 20.0 V, 5 A Load.
C4: V_{IN}, 200 V / div.
C3: I_{IN}, 1 A / div., 5 ms / div.

15.2 *PFC Inductor Current and Drain Voltage Waveforms*

15.2.1 Output: 15 V / 5 A

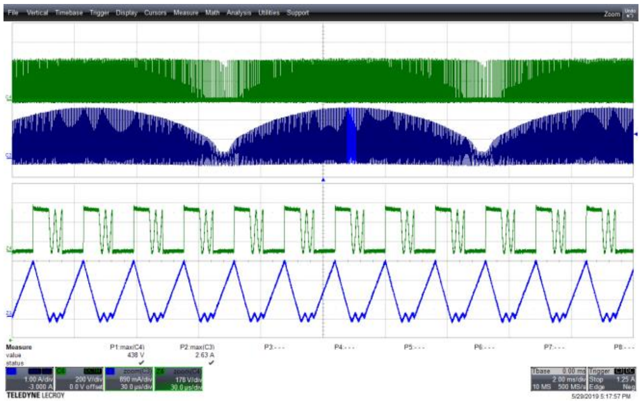

Figure 59 – PFC Inductor Current and Drain Voltage.
115 VAC, 15.0 V, 5 A Load.
C4: PFC V_{DS}, 200 V / div., 438 V_{MAX}.
C3: PFC I_{IND}, 1 A / div., 2.63 A_{MAX}.
2 ms / div.

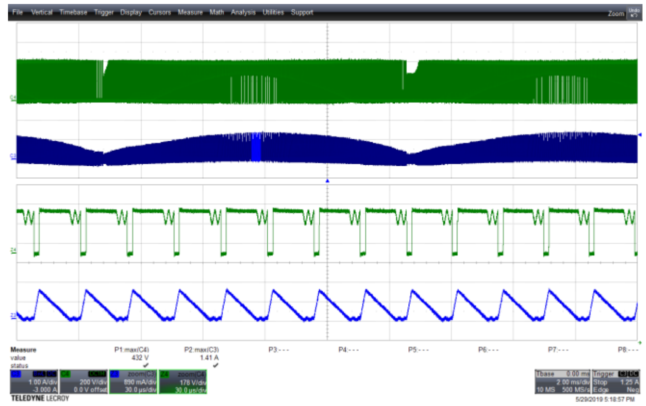

Figure 60 – PFC Inductor Current and Drain Voltage.
230 VAC, 15.0 V, 5 A Load.
C4: PFC V_{DS}, 200 V / div., 432 V_{MAX}.
C3: PFC I_{IND}, 1 A / div., 1.41 A_{MAX}.
2 ms / div.

15.2.2 Output: 20 V / 5 A

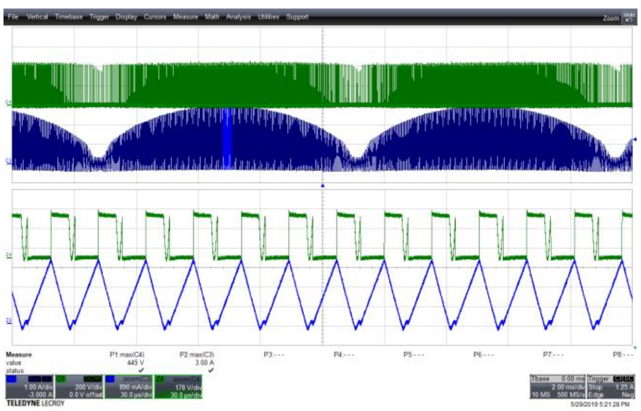

Figure 61 – PFC Inductor Current and Drain Voltage.
115 VAC, 20.0 V, 5 A Load.
C4: PFC V_{DS}, 200 V / div., 445 V_{MAX}.
C3: PFC I_{IND}, 1 A / div., 3 A_{MAX}
2 ms / div.

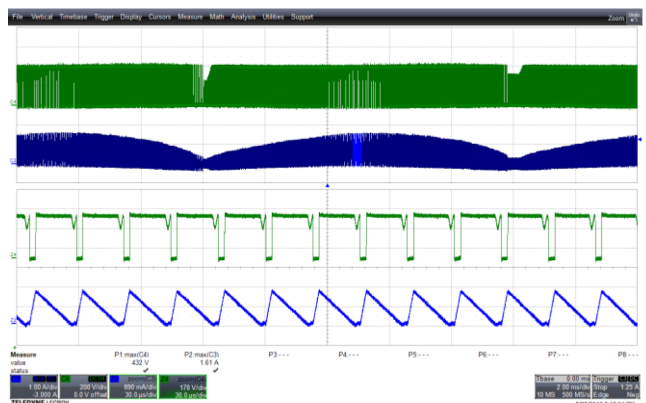

Figure 62 – PFC Inductor Current and Drain Voltage.
230 VAC, 20.0 V, 5 A Load.
C4: PFC V_{DS}, 200 V / div., 432 V_{MAX}.
C3: PFC I_{IND}, 1 A / div., 1.61 A_{MAX}
2 ms / div.

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15.3 Load Transient Response (on the board)

15.3.1 Output: 3.3 V

Figure 63 – Transient Response.
90 VAC, 3.3 V, 0 –1.25 A Load Step.
$V_{MIN:}$ 3.306 V, V_{MAX}: 3.439 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

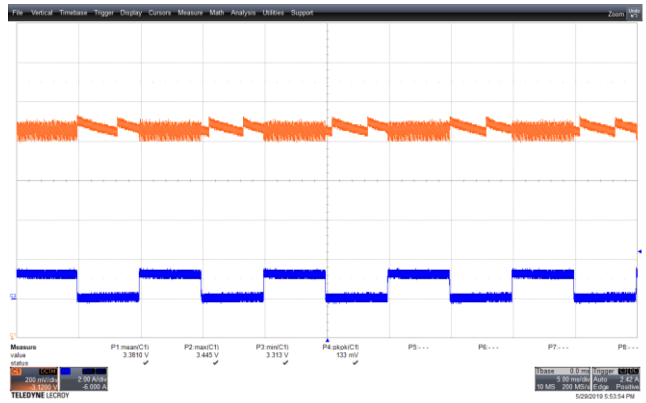

Figure 64 – Transient Response.
265 VAC, 3.3 V, 0 – 1.25 A Load Step.
V_{MIN} : 3.313 V, V_{MAX}: 3.445 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

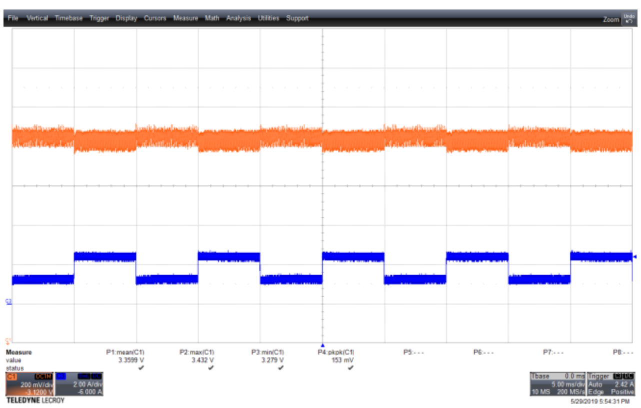

Figure 65 – Transient Response.
90 VAC, 3.3 V, 1.25 – 2.5 A Load Step.
$V_{MIN:}$ 3.279 V, V_{MAX}: 3.432 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

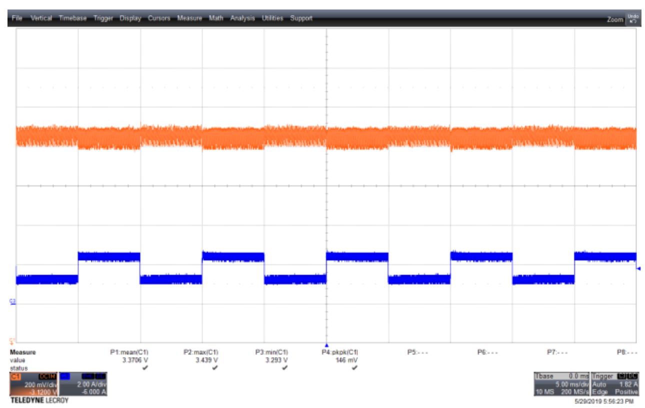

Figure 66 – Transient Response.
265 VAC, 3.3 V, 1.25 – 2.5 A Load Step.
$V_{MIN:}$ 3.293 V, V_{MAX}: 3.439 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

Figure 67 – Transient Response.
90 VAC, 3.3 V, 2.5 – 3.75 A Load Step.
V_{MIN}: 3.24 V, V_{MAX}: 3.412 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

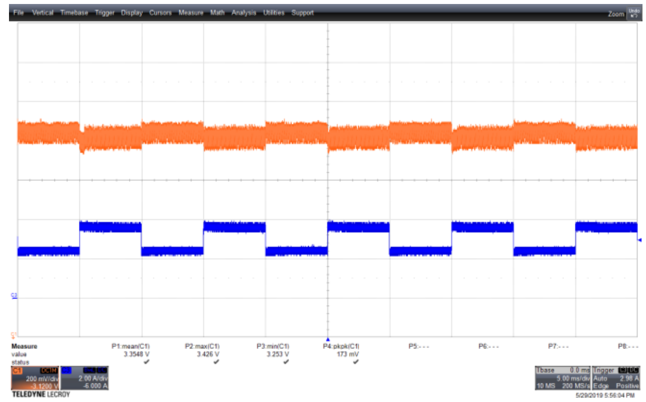

Figure 68 – Transient Response.
265 VAC, 3.3 V, 2.5 – 3.75 A Load Step.
V_{MIN}: 3.253 V, V_{MAX}: 3.426 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

Figure 69 – Transient Response.
90 VAC, 3.3 V, 3.75 – 5 A Load Step.
V_{MIN}: 3.226 V, V_{MAX}: 3.399 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

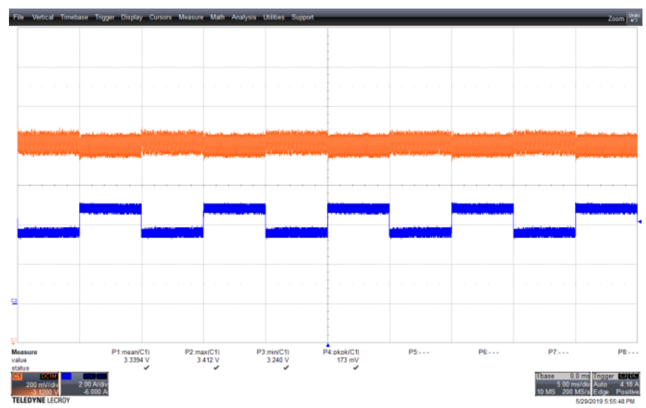

Figure 70 – Transient Response.
265 VAC, 3.3 V, 3.75 – 5 A Load Step.
V_{MIN}: 3.240 V, V_{MAX}: 3.412 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

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15.3.2 Output: 5 V

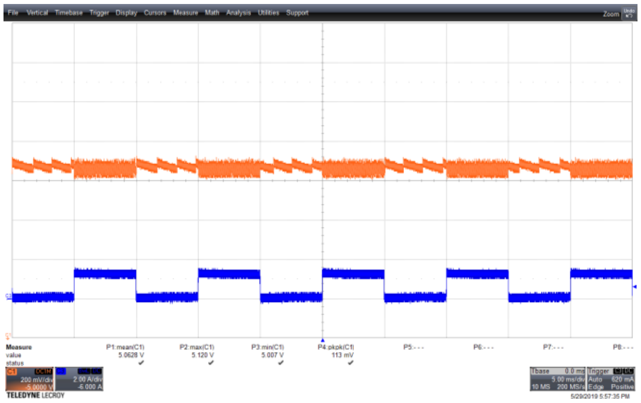

Figure 71 – Transient Response.
90 VAC, 5 V, 0 – 1.25 A Load Step.
$V_{MIN:}$ 5.007 V, V_{MAX}: 5.12 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

Figure 72 – Transient Response.
265 VAC, 5 V, 0 – 1.25 A Load Step.
V_{MIN} : 5 V, V_{MAX}: 5.126 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

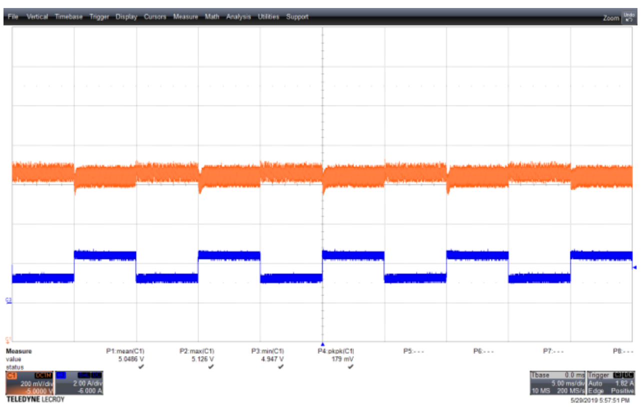

Figure 73 – Transient Response.
90 VAC, 5 V, 1.25 – 2.5 A Load Step.
$V_{MIN:}$ 4.947 V, V_{MAX}: 5.126 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

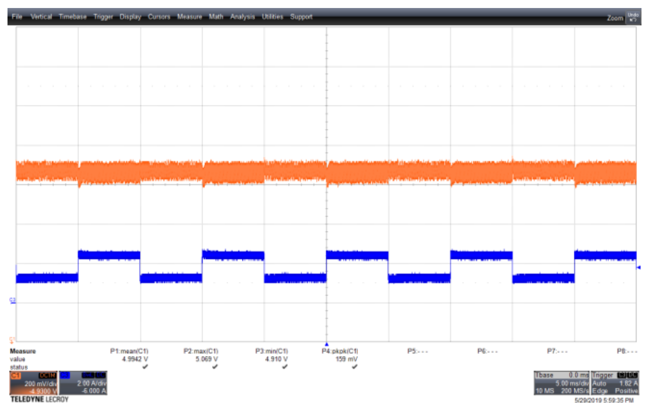

Figure 74 – Transient Response.
265 VAC, 5 V, 1.25 – 2.5 A Load Step.
$V_{MIN:}$ 4.91 V, V_{MAX}: 5.069 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

Figure 75 – Transient Response.
90 VAC, 5 V, 2.5 – 3.75 A Load Step.
$V_{MIN:}$ 4.934 V, V_{MAX}: 5.106 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

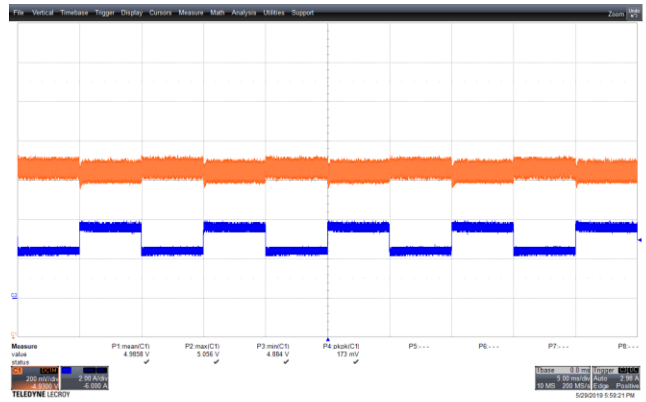

Figure 76 – Transient Response.
265 VAC, 5 V, 2.5 – 3.75 A Load Step.
$V_{MIN:}$ 4.884 V, V_{MAX}: 5.056 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

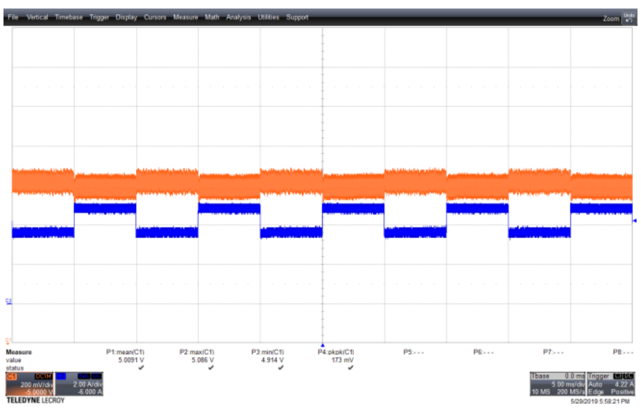

Figure 77 – Transient Response.
90 VAC, 5 V, 3.75 - 5 A Load Step.
$V_{MIN:}$ 4.914 V, V_{MAX}: 5.086 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

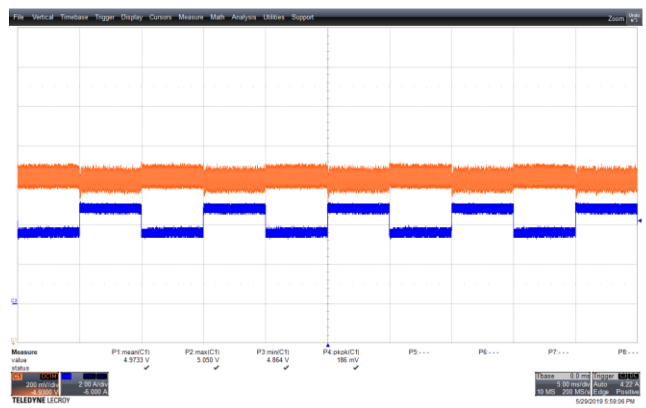

Figure 78 – Transient Response.
265 VAC, 5 V, 3.75 - 5 A Load Step.
$V_{MIN:}$ 4.864 V, V_{MAX}: 5.05 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

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15.3.3 Output: 9 V

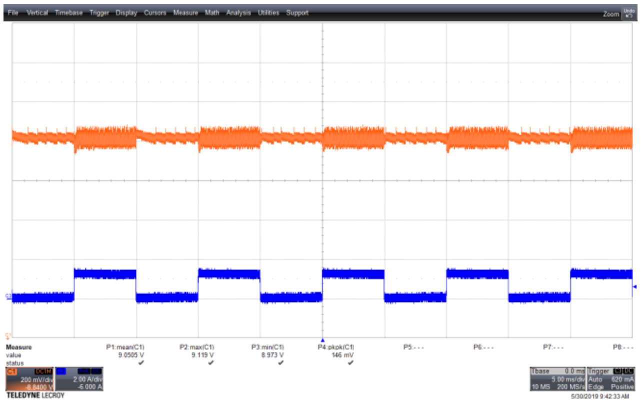

Figure 79 – Transient Response.
90 VAC, 9 V, 0 – 1.25 A Load Step.
V_{MIN}: 8.973 V, V_{MAX}: 9.119 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

Figure 80 – Transient Response.
265 VAC, 9 V, 0 – 1.25 A Load Step.
V_{MIN} : 9.006 V, V_{MAX}: 9.132 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

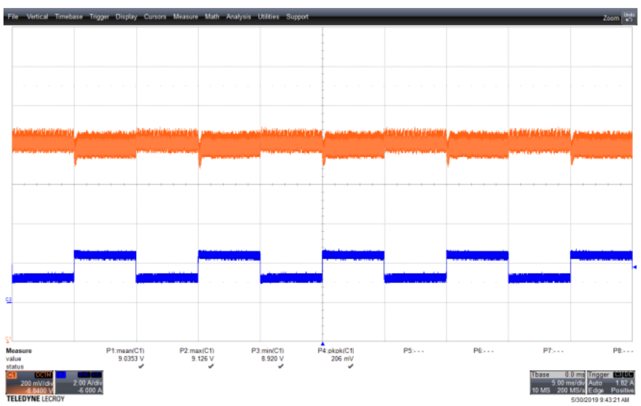

Figure 81 – Transient Response.
90 VAC, 9 V, 1.25 – 2.5 A Load Step.
V_{MIN}: 8.92 V, V_{MAX}: 9.126 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

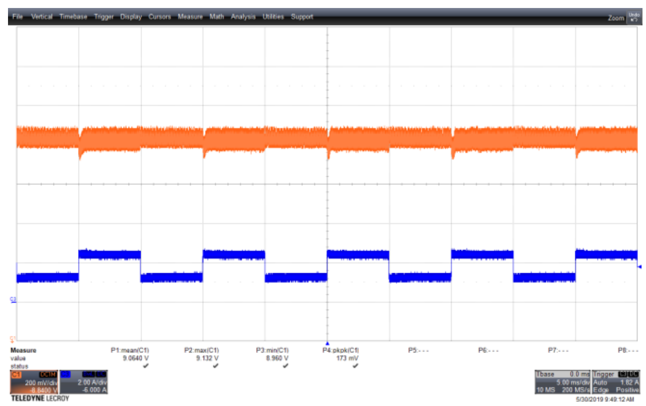

Figure 82 – Transient Response.
265 VAC, 9 V, 1.25 – 2.5 A Load Step.
V_{MIN}: 8.96 V, V_{MAX}: 9.132 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

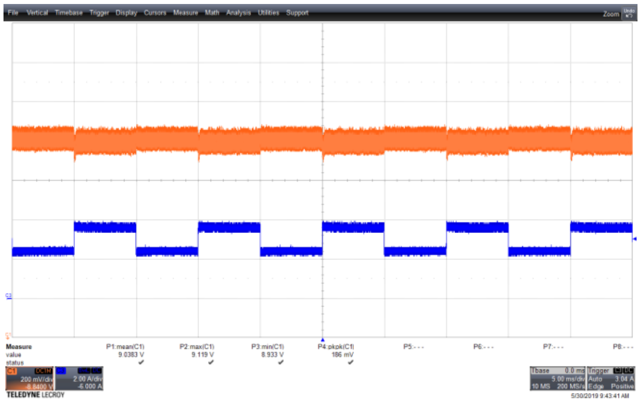

Figure 83 – Transient Response.
90 VAC, 9 V, 2.5 – 3.75 A Load Step.
V_{MIN}: 8.933 V, V_{MAX}: 9.119 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

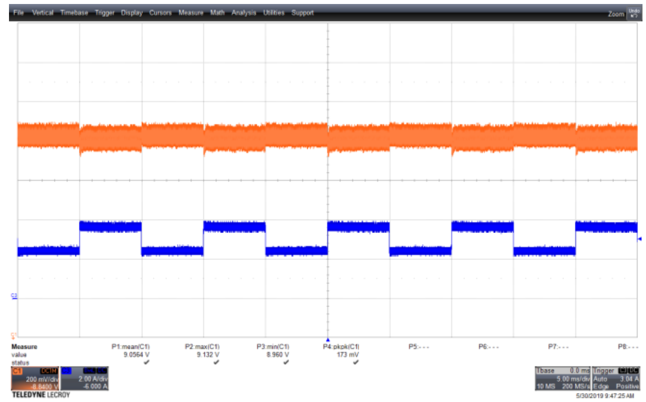

Figure 84 – Transient Response.
265 VAC, 9 V, 2.5 – 3.75 A Load Step.
V_{MIN}: 8.96 V, V_{MAX}: 9.132 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

Figure 85 – Transient Response.
90 VAC, 9 V, 3.75 – 5 A Load Step.
V_{MIN}: 8.92 V, V_{MAX}: 9.119 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

Figure 86 – Transient Response.
265 VAC, 9 V, 3.75 – 5 A Load Step.
V_{MIN}: 8.933 V, V_{MAX}: 9.132 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

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15.3.4 Output: 15 V

Figure 87 – Transient Response.
90 VAC, 15 V, 0 – 1.25 A Load Step.
V_{MIN}: 14.936 V, V_{MAX}: 15.109 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

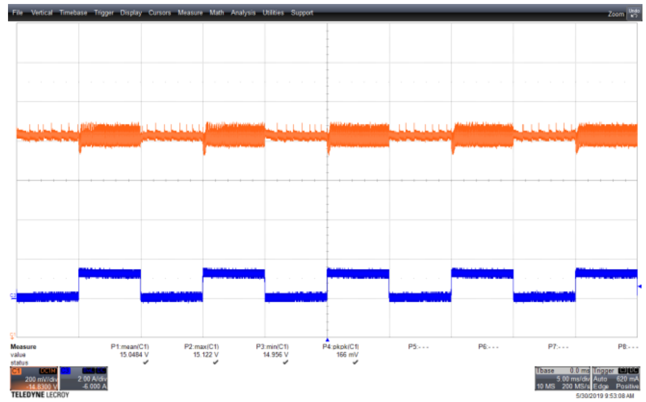

Figure 88 – Transient Response.
265 VAC, 15 V, 0 – 1.25 A Load Step.
V_{MIN} : 14.956 V, V_{MAX}: 15.122 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

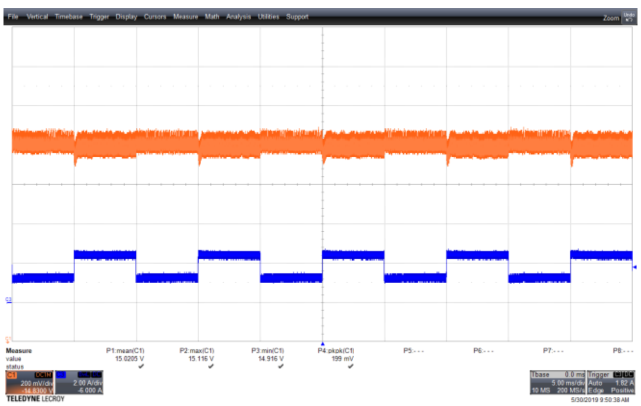

Figure 89 – Transient Response.
90 VAC, 15 V, 1.25 – 2.5 A Load Step.
V_{MIN}: 14.916 V, V_{MAX}: 15.116 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

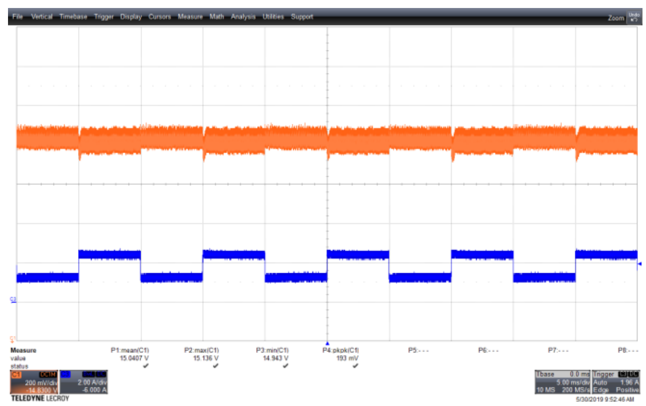

Figure 90 – Transient Response.
265 VAC, 5 V, 1.25 – 2.5 A Load Step.
V_{MIN}: 14.943 V, V_{MAX}: 15.136 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

Figure 91 – Transient Response.
90 VAC, 15 V, 2.5 – 3.75 A Load Step.
V_{MIN}: 14.91 V, V_{MAX}: 15.122 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

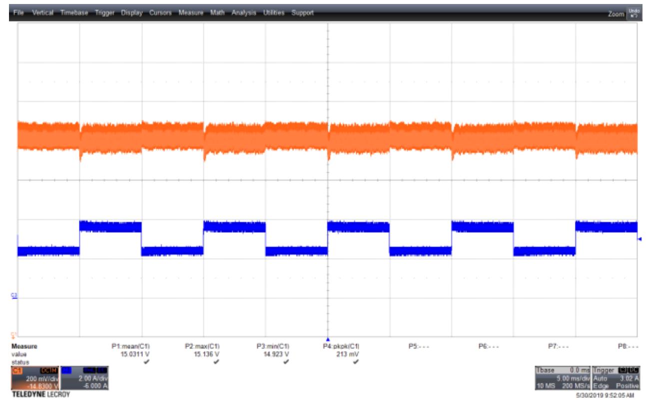

Figure 92 – Transient Response.
265 VAC, 15 V, 2.5 – 3.75 A Load Step.
V_{MIN}: 14.923 V, V_{MAX}: 15.136 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

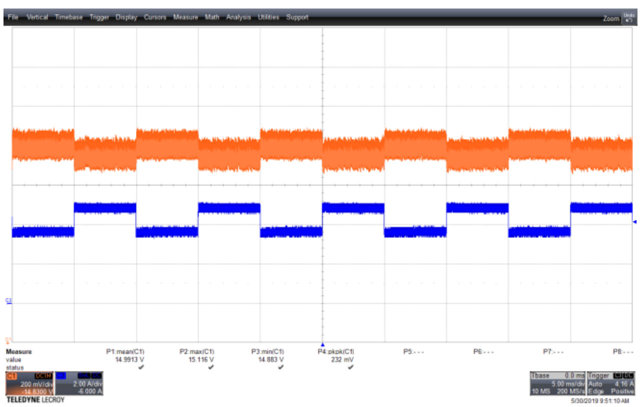

Figure 93 – Transient Response.
90 VAC, 15 V, 3.75 – 5 A Load Step.
V_{MIN}: 14.883 V, V_{MAX}: 15.116 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

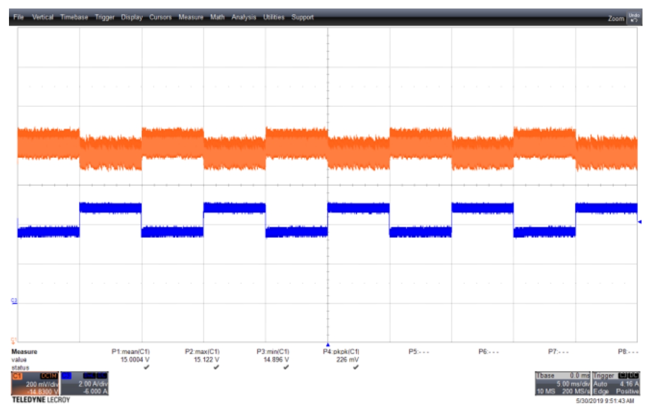

Figure 94 – Transient Response.
265 VAC, 3.3 V, 3.75 – 5 A Load Step.
V_{MIN}: 14.896 V, V_{MAX}: 15.122 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

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15.3.5 Output: 20 V

Figure 95 – Transient Response.
90 VAC, 20 V, 0 – 1.25 A Load Step.
V_{MIN}: 19.9 V, V_{MAX}: 20.106 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

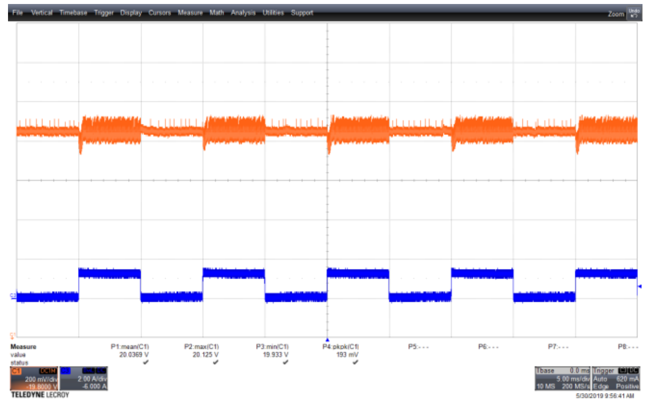

Figure 96 – Transient Response.
265 VAC, 20 V, 0 – 1.25 A Load Step.
V_{MIN} : 19.933 V, V_{MAX}: 20.125 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

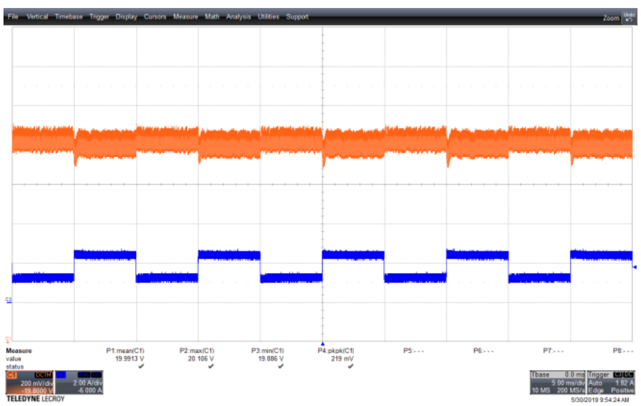

Figure 97 – Transient Response.
90 VAC, 20 V, 1.25 – 2.5 A Load Step.
V_{MIN}: 19.886 V, V_{MAX}: 20.106 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

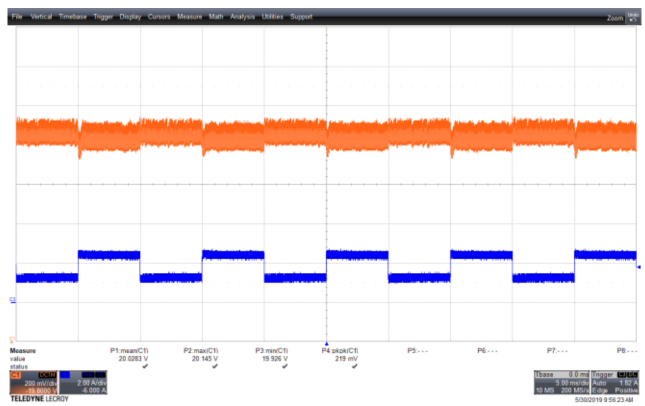

Figure 98 – Transient Response.
265 VAC, 20 V, 1.25 – 2.5 A Load Step.
V_{MIN}: 19.926 V, V_{MAX}: 20.145 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

Figure 99 – Transient Response.
90 VAC, 20 V, 2.5 – 3.75 A Load Step.
V_{MIN}: 19.88 V, V_{MAX}: 20.106 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

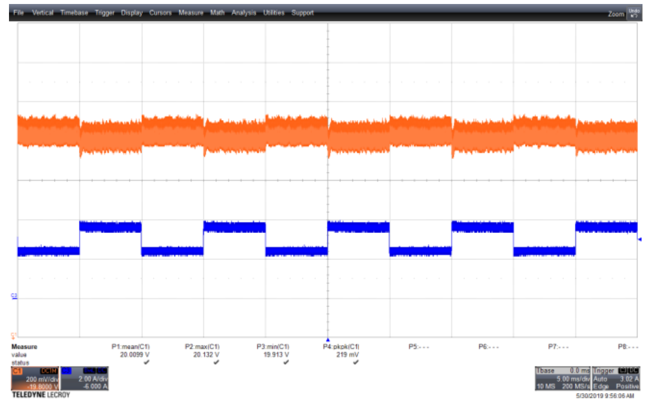

Figure 100 – Transient Response.
265 VAC, 20 V, 2.5 – 3.75 A Load Step.
V_{MIN}: 19.913 V, V_{MAX}: 20.132 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

Figure 101 – Transient Response.
90 VAC, 20 V, 3.75 – 5 A Load Step.
V_{MIN}: 19.853 V, V_{MAX}: 20.119 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

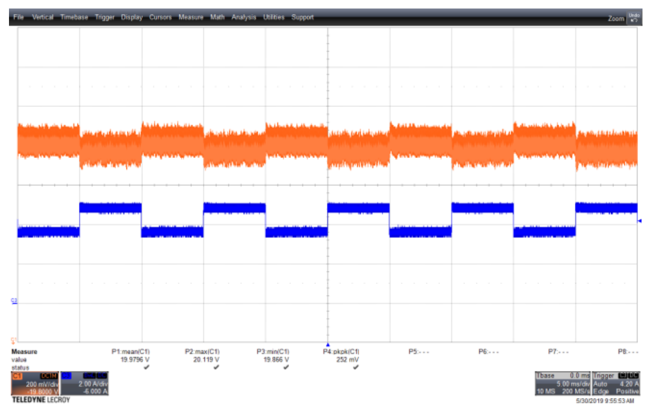

Figure 102 – Transient Response.
265 VAC, 20 V, 3.75 – 5 A Load Step.
V_{MIN}: 19.866 V, V_{MAX}: 20.119 V.
Upper: V_{OUT}, 0.2 V / div., 5 ms / div.
Lower: I_{LOAD}, 2 A / div.

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15.4 ***Switching Waveforms***

15.4.1 Primary Drain Voltage and Current

15.4.1.1 Output: 3.3 V / 5 A

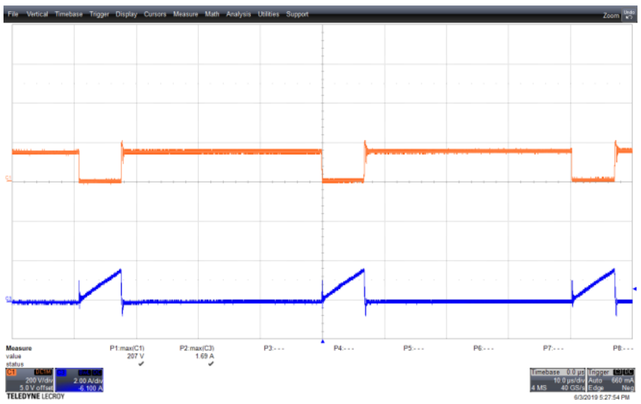

Figure 103 – Drain Voltage and Current Waveforms.
90 VAC, 3.3 V, 5 A Load, (207 V_{MAX}).
Upper: V_{DRAIN}, 200 V /div
Lower: I_{DRAIN}, 2 A / div, 10 μs / div.

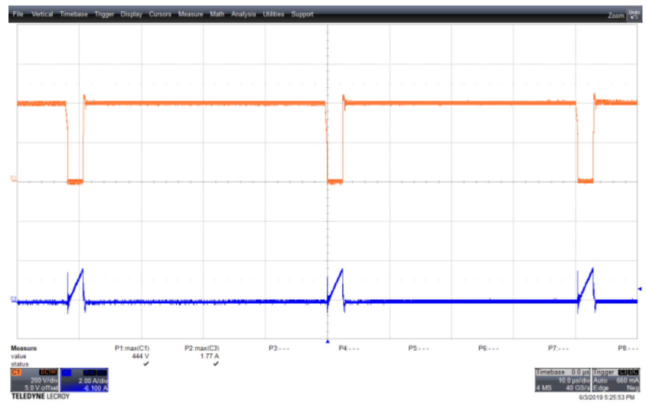

Figure 104 – Drain Voltage and Current Waveforms.
265 VAC, 3.3 V, 5 A Load, (444 V_{MAX}).
Upper: V_{DRAIN}, 200 V /div
Lower: I_{DRAIN}, 2 A / div, 10 μs / div.

15.4.1.2 Output: 5 V / 5 A

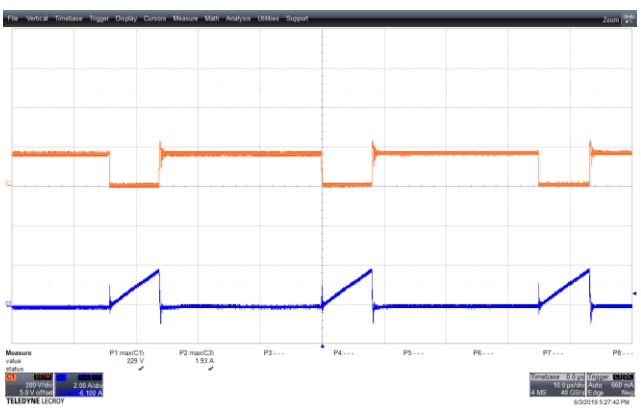

Figure 105 – Drain Voltage and Current Waveforms.
90 VAC, 5.0 V, 5 A Load, (229 V_{MAX}).
Upper: V_{DRAIN}, 200 V /div
Lower: I_{DRAIN}, 2 A / div, 10 μs / div.

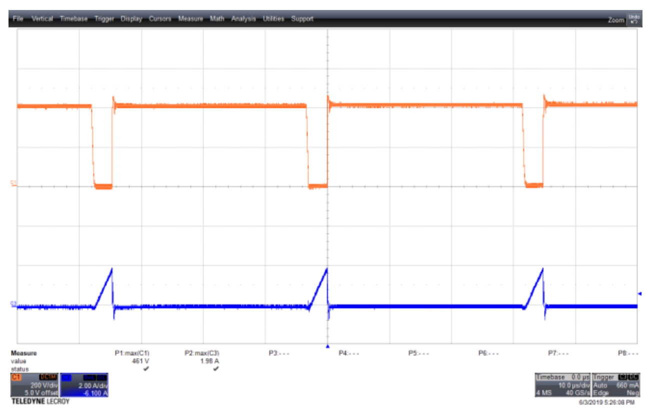

Figure 106 – Drain Voltage and Current Waveforms.
265 VAC, 5.0 V, 5 A Load, (461 V_{MAX}).
Upper: V_{DRAIN}, 200 V /div
Lower: I_{DRAIN}, 2 A / div, 10 μs / div.

15.4.1.3 Output: 9 V / 5 A

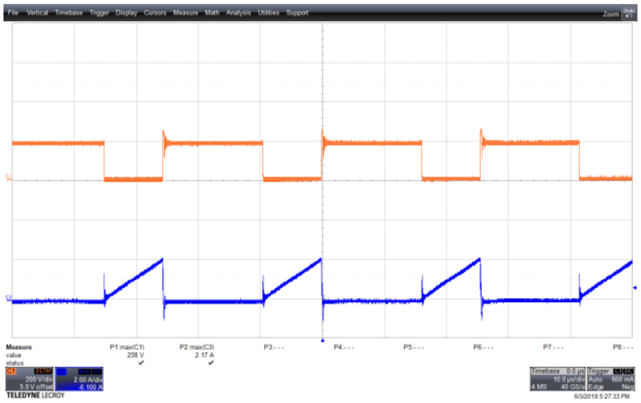

Figure 107 – Drain Voltage and Current Waveforms.
90 VAC, 9.0 V, 5 A Load, (258 V_{MAX}).
Upper: V_{DRAIN}, 200 V /div
Lower: I_{DRAIN}, 2 A / div, 10 μs / div.

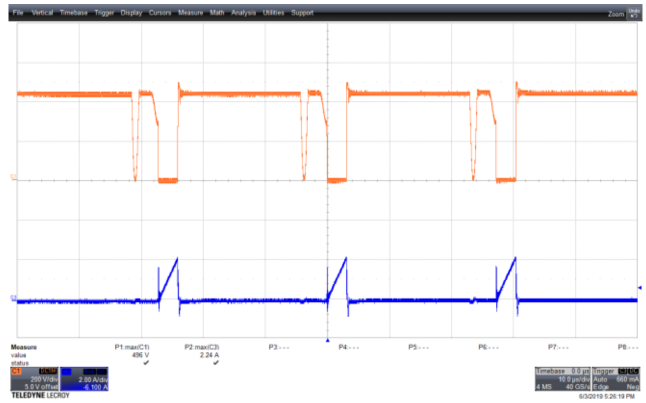

Figure 108 – Drain Voltage and Current Waveforms.
265 VAC, 9.0 V, 5 A Load, (496 V_{MAX}).
Upper: V_{DRAIN}, 200 V /div
Lower: I_{DRAIN}, 2 A / div, 10 μs / div.

15.4.1.4 Output: 15 V / 5 A

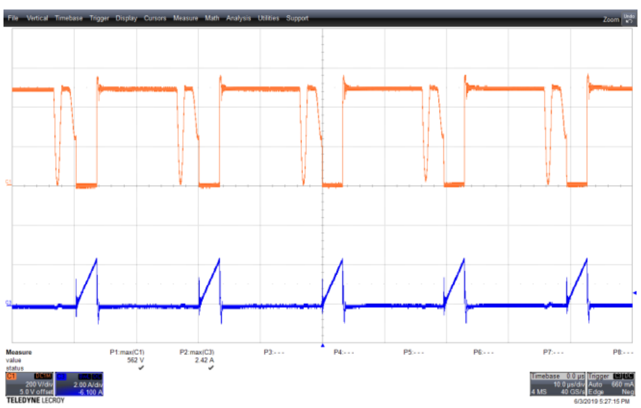

Figure 109 – Drain Voltage and Current Waveforms.
90 VAC, 15 V, 5 A Load, (562 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 2 A / div., 10 μs / div.

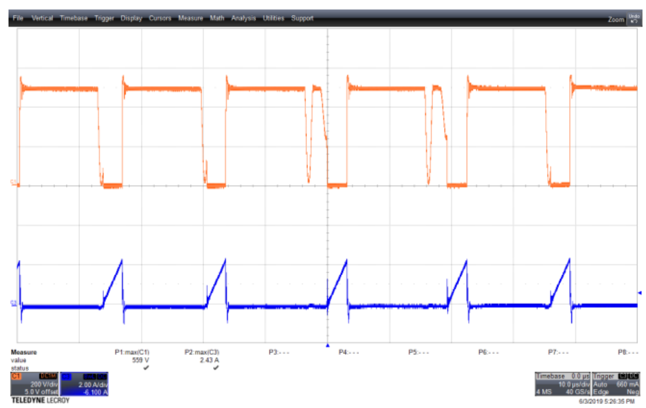

Figure 110 – Drain Voltage and Current Waveforms.
265 VAC, 15 V, 5 A Load, (559 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 2 A / div., 10 μs / div.

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15.4.1.5 Output: 20 V / 5 A

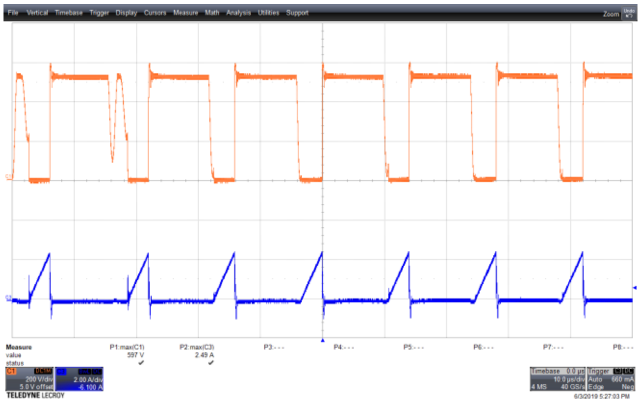

Figure 111 – Drain Voltage and Current Waveforms.
90 VAC, 20 V, 5 A Load, (597 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 2 A / div., 10 µs / div.

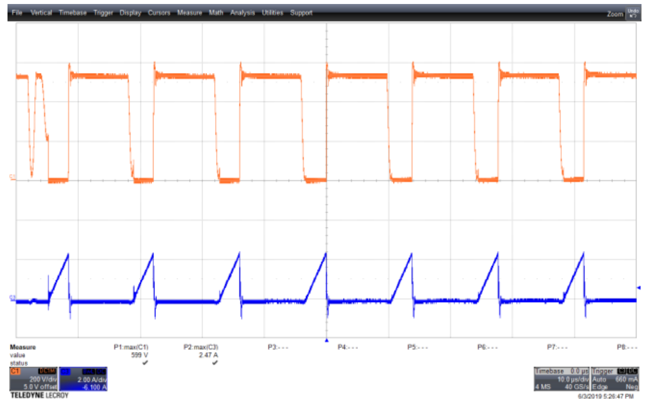

Figure 112 – Drain Voltage and Current Waveforms.
265 VAC, 20 V, 5A Load, (599 V_{MAX}).
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 2 A / div., 10 µs / div.

15.4.2 SR FET Voltage

15.4.2.1 Output: 3.3 V / 5 A

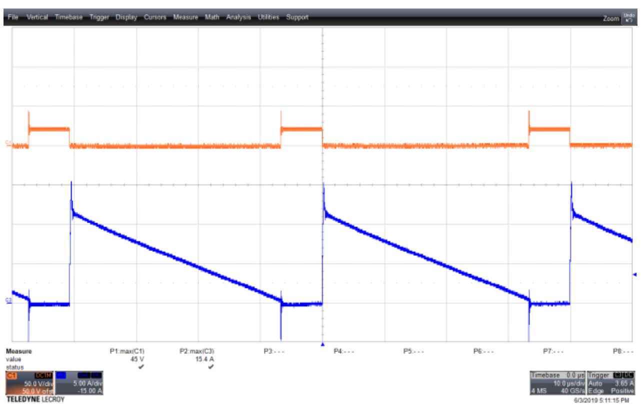

Figure 113 – SR FET Voltage Waveforms.
90 VAC, 3.3 V, 5 A Load, (45 V_{MAX}).
Upper: SR_V_{DRAIN}, 50 V / div., 10 µs / div.
Lower: SR_I_{DRAIN}, 5 A / div.

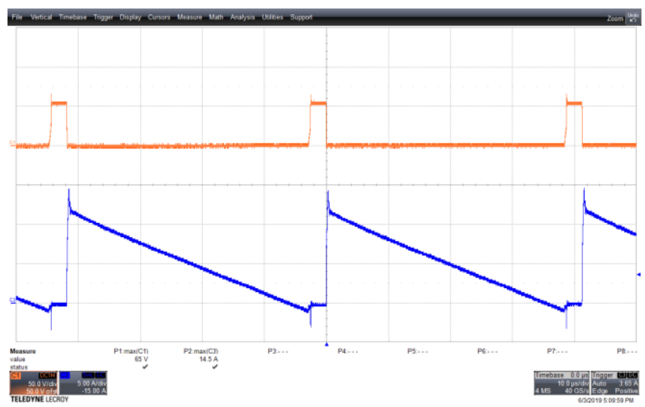

Figure 114 – SR FET Voltage Waveforms.
265 VAC, 3.3 V, 5 A Load, (65 V_{MAX}).
Upper: SR_V_{DRAIN}, 50 V / div., 10 µs / div.
Lower: SR_I_{DRAIN}, 5 A / div.

15.4.2.2 Output: 5 V / 5 A

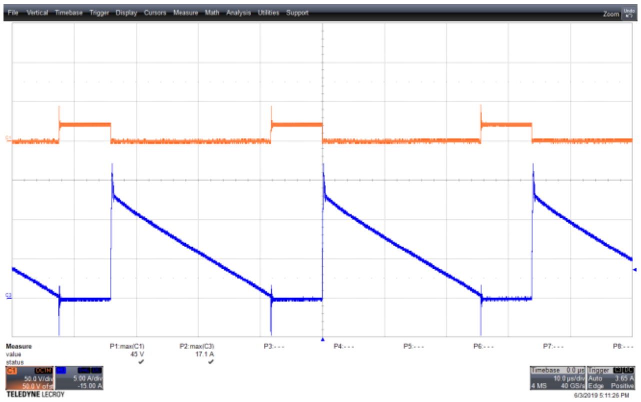

Figure 115 – SR FET Voltage Waveforms.
90 VAC, 5 V, 5 A Load, (45 V_{MAX}).
Upper: SR_V_{DRAIN}, 50 V / div., 10 μs / div.
Lower: SR_I_{DRAIN}, 5 A / div.

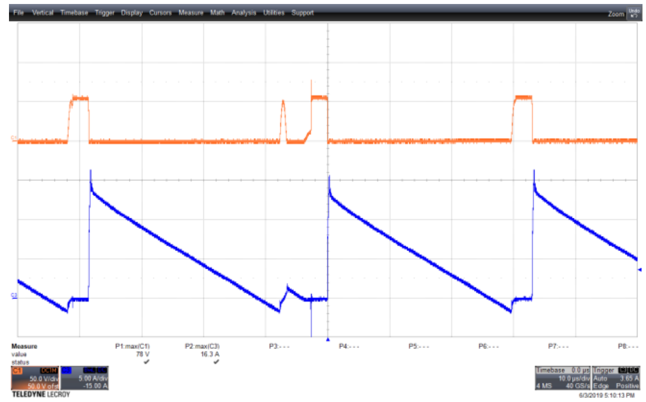

Figure 116 – SR FET Voltage Waveforms.
265 VAC, 5 V, 5 A Load, (78 V_{MAX}).
Upper: SR_V_{DRAIN}, 50 V / div., 10 μs / div.
Lower: SR_I_{DRAIN}, 5 A / div.

15.4.2.3 Output: 9 V / 5 A

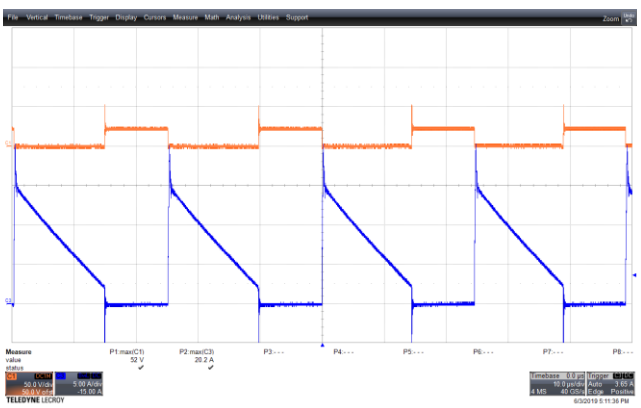

Figure 117 – SR FET Voltage Waveforms.
90 VAC, 9 V, 5 A Load, (52 V_{MAX}).
Upper: SR_V_{DRAIN}, 50 V / div., 20 μs / div.
Lower: SR_I_{DRAIN}, 5 A / div.

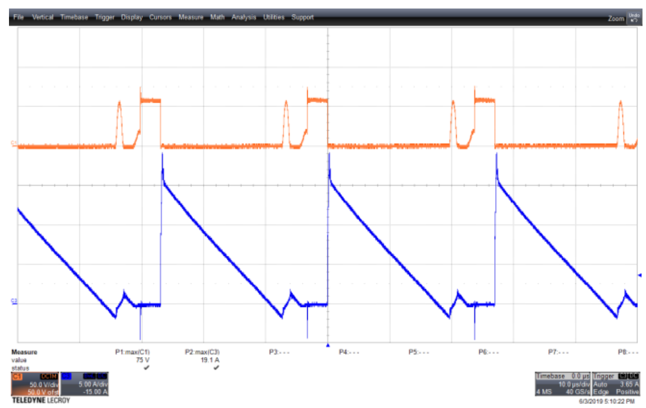

Figure 118 – SR FET Voltage Waveforms.
265 VAC, 9 V, 5 A Load, (75 V_{MAX}).
Upper: SR_V_{DRAIN}, 50 V / div., 20 μs / div.
Lower: SR_I_{DRAIN}, 5 A / div.

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15.4.2.4 Output: 15 V / 5 A

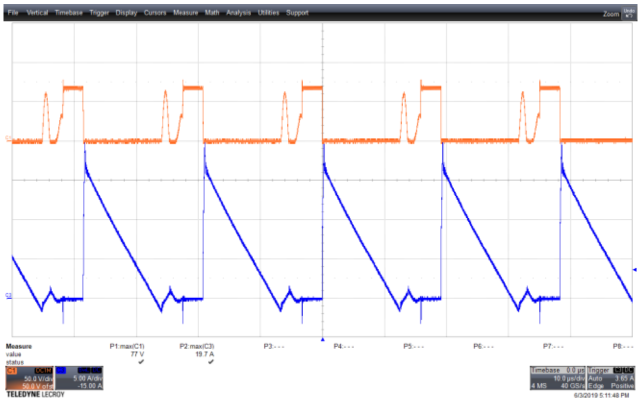

Figure 119 – SR FET Voltage Waveforms.
90 VAC, 15 V, 5 A Load, (77 V_{MAX}).
Upper: SR_V_{DRAIN}, 50 V / div., 20 μs / div.
Lower: SR_I_{DRAIN}, 5 A / div.

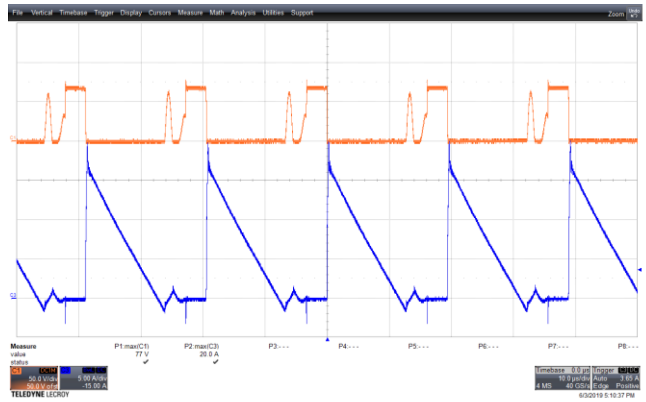

Figure 120 – SR FET Voltage Waveforms.
265 VAC, 15 V, 5 A Load, (77 V_{MAX})
Upper: SR_V_{DRAIN}, 50 V / div., 20. μs / div.
Lower: SR_I_{DRAIN}, 5 A / div.

15.4.2.5 Output: 20 V / 5 A

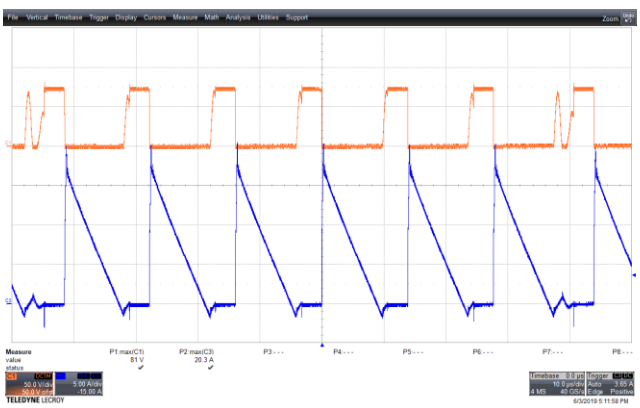

Figure 121 – SR FET Voltage Waveforms.
90 VAC, 20 V, 5 A Load, (81 V_{MAX}).
Upper: SR_V_{DRAIN}, 50 V / div., 20 μs / div.
Lower: SR_I_{DRAIN}, 5 A / div.

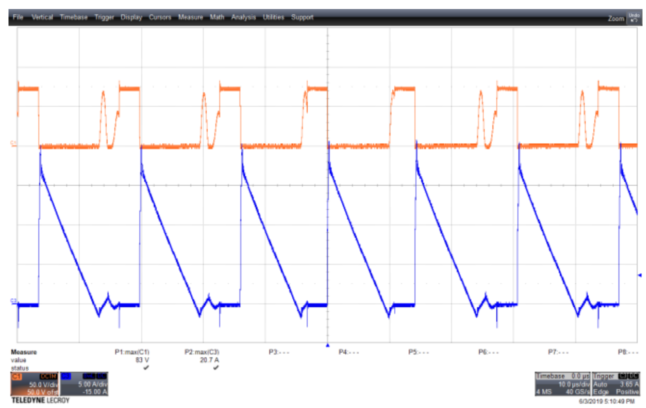

Figure 122 – SR FET Voltage Waveforms.
265 VAC, 20 V, 5 A Load, (83 V_{MAX}).
Upper: SR_V_{DRAIN}, 50 V / div., 20 μs / div.
Lower: SR_I_{DRAIN}, 5 A / div.

15.5 ***Output Ripple Measurements***

15.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

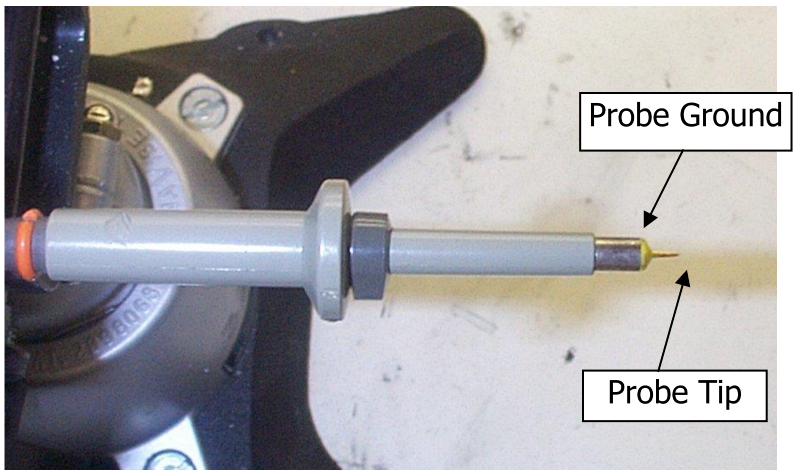

Figure 123 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

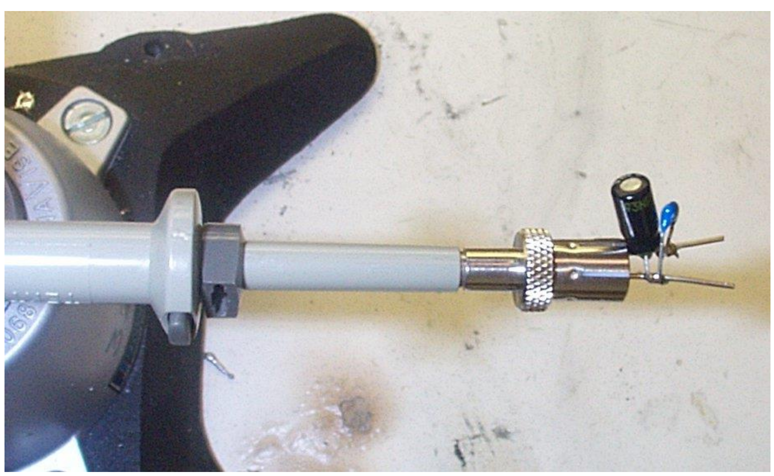

Figure 124 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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15.5.2 Ripple Amplitude vs. Load

15.5.2.1 Output: 3.3 V

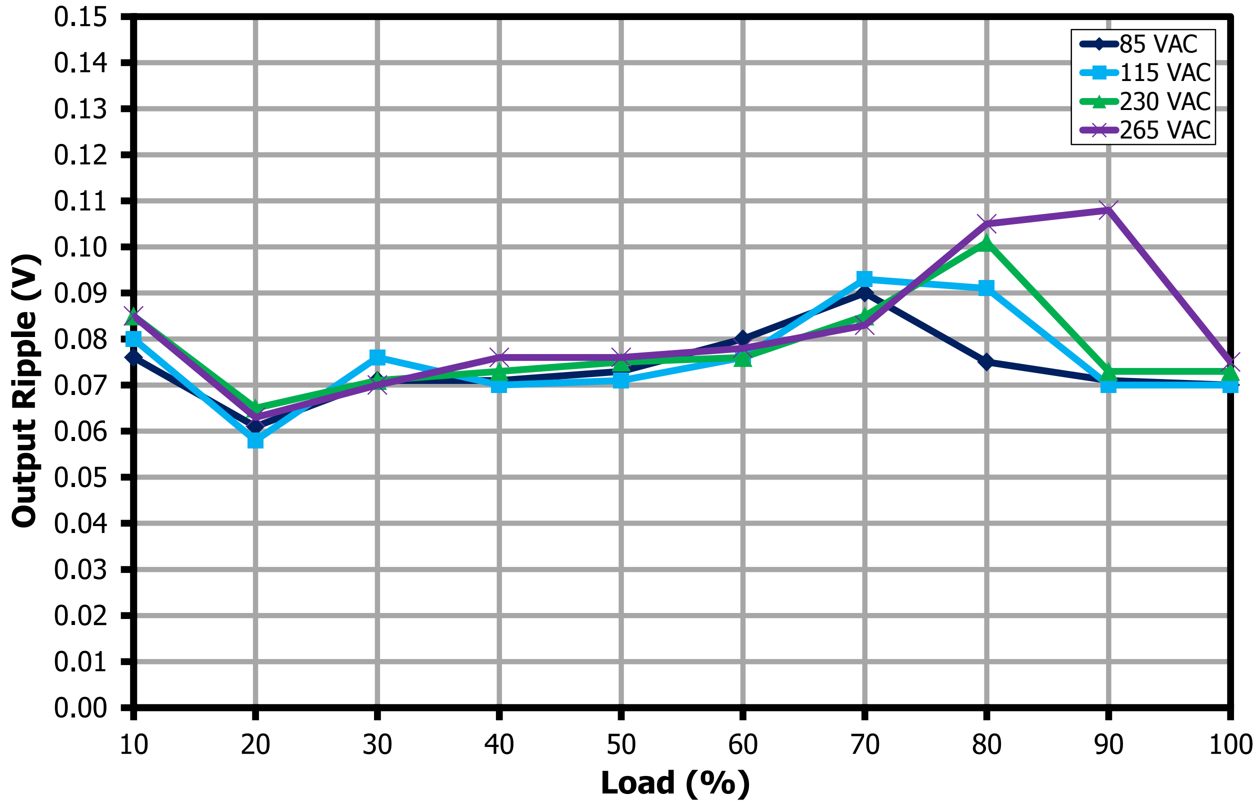

Figure 125 – 3.3 V Ripple Amplitude vs. Load.

15.5.2.2 Output: 5 V

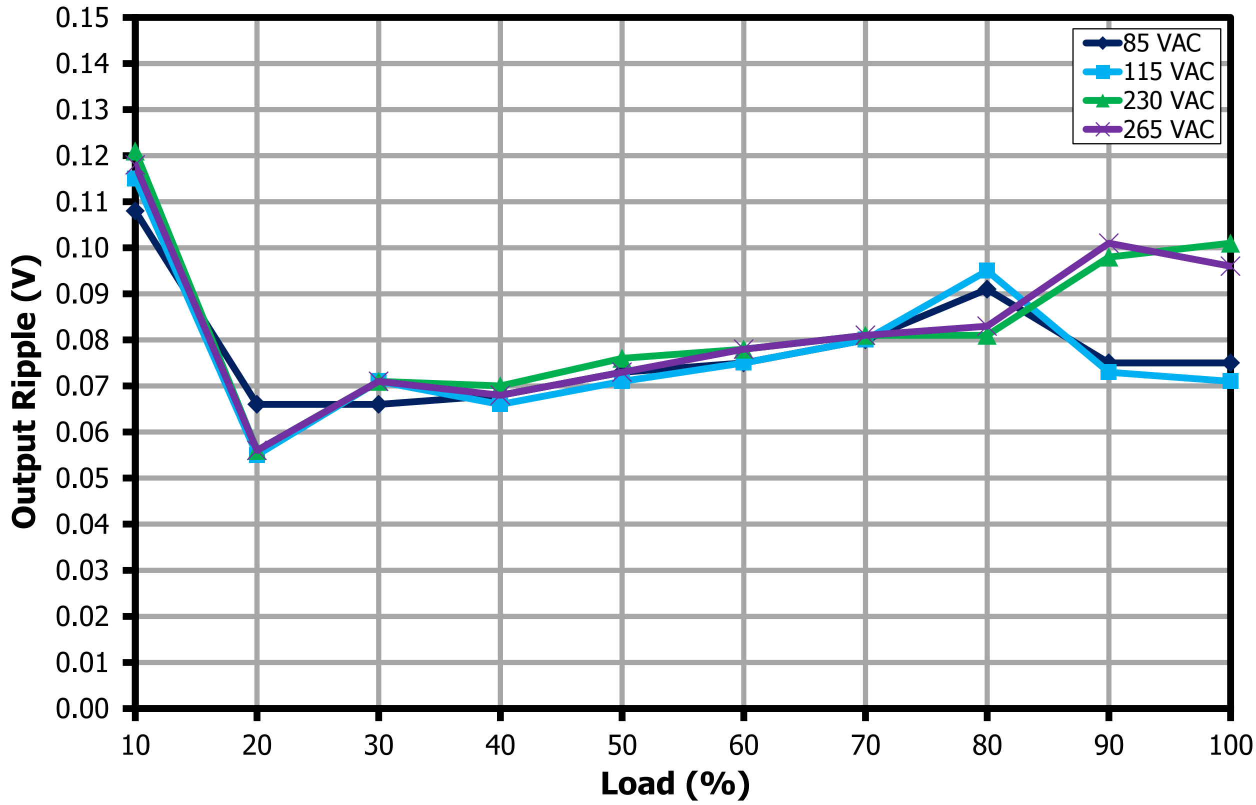

Figure 126 – 5 V Ripple Amplitude vs. Load.

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15.5.2.3 Output: 9 V

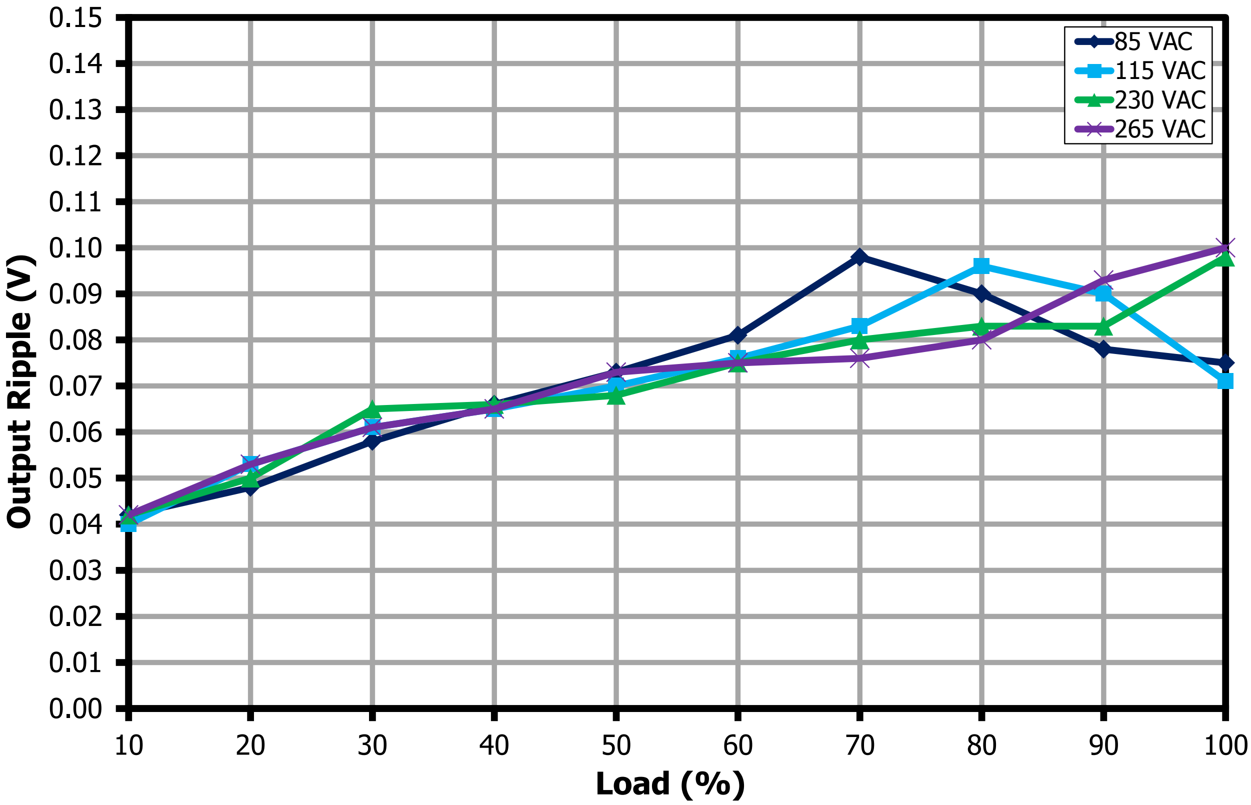

Figure 127 – 9 V Ripple Amplitude vs. Load.

15.5.2.4 Output: 15 V

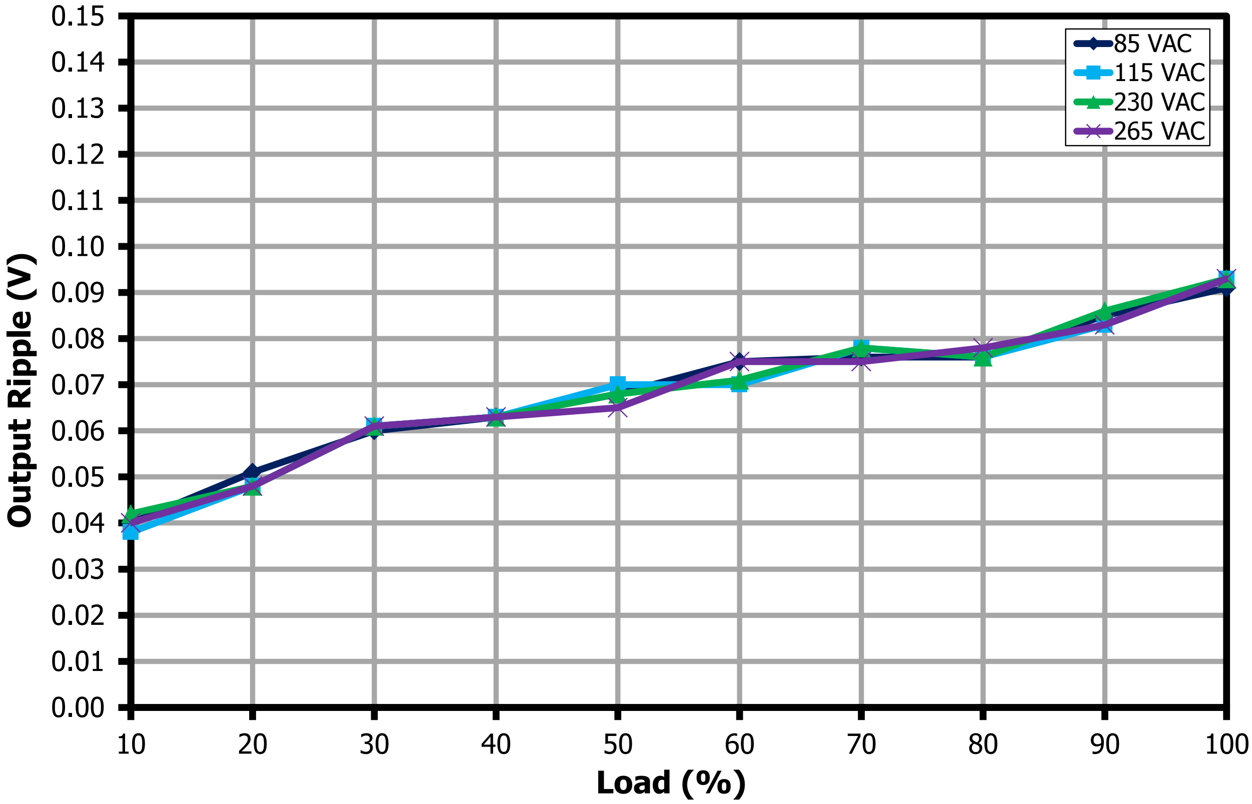

Figure 128 – 15 V Ripple Amplitude vs. Load.

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15.5.2.5 Output: 20 V

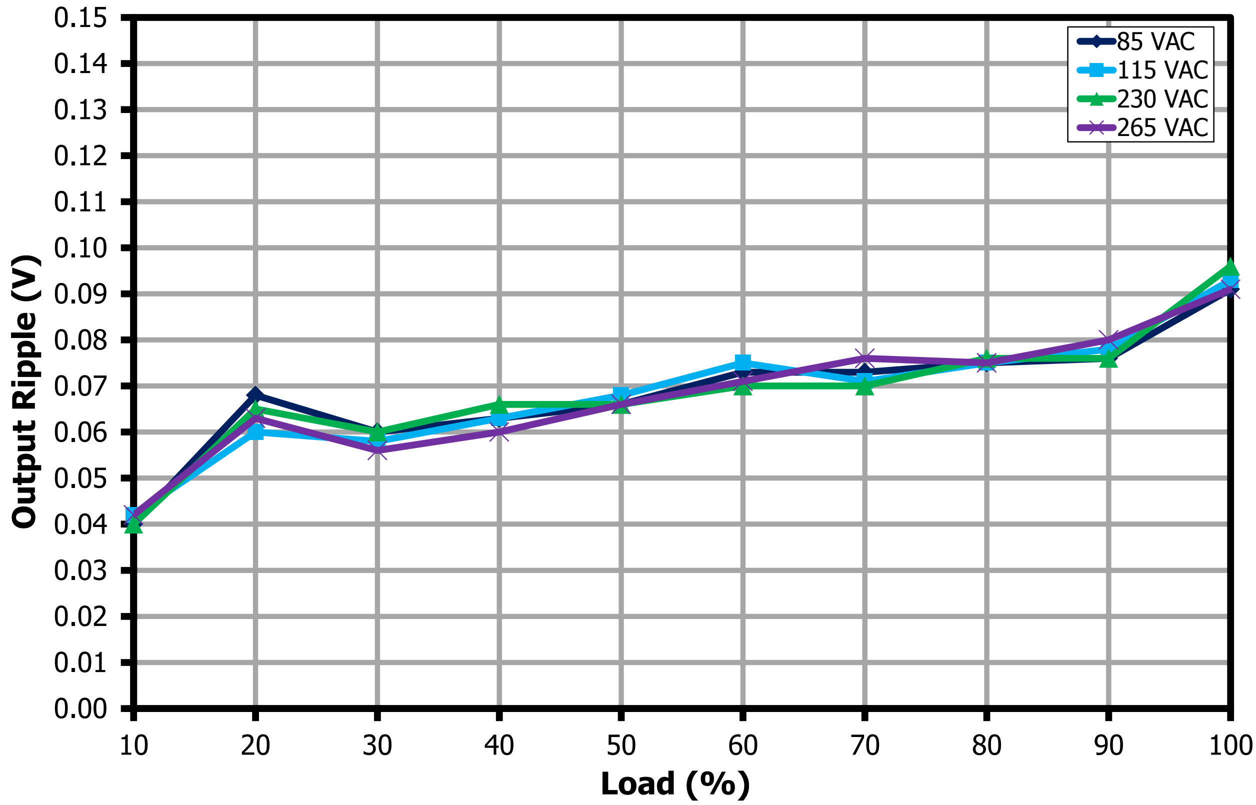

Figure 129 – 20 V Ripple Amplitude vs. Load.

15.5.3 Ripple Waveforms

15.5.3.1 3.3 V Ripple Waveforms

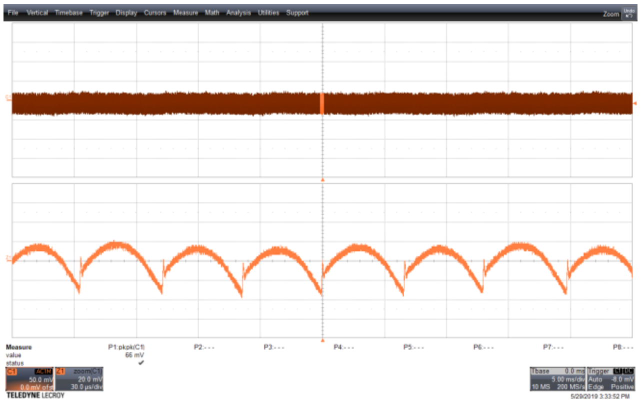

Figure 130 – Output Ripple. (PK-PK – 66 mV)
90 VAC Input 3.3 V, 5 A Load.
V_{OUT}, 50 mV / div., 66 mV_{PK-PK}
5 ms / div.

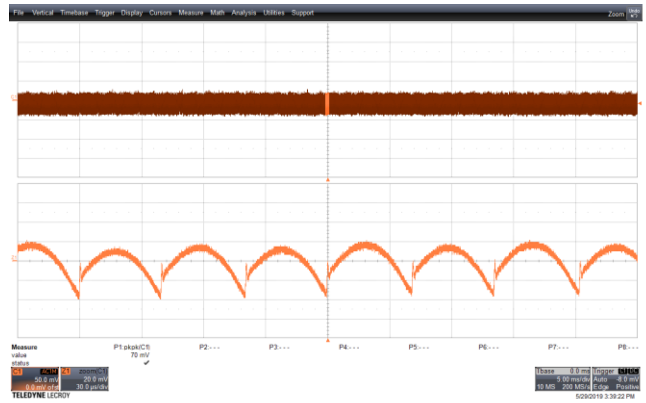

Figure 131 – Output Ripple. (PK-PK – 70 mV)
265 VAC Input 3.3 V, 5 A Load.
V_{OUT}, 50 mV / div., 70 mV_{PK-PK}
5 ms / div.

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15.5.3.2 5 V Ripple Waveforms

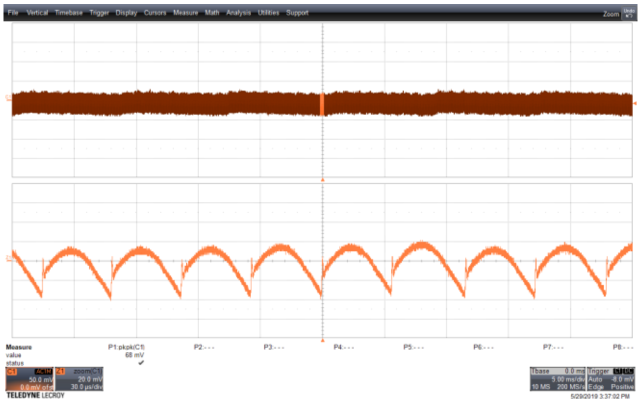

Figure 132 – Output Ripple. (PK-PK – 68 mV)
90 VAC Input 5 V, 5 A Load.
V_{OUT}, 50 mV / div., 68 mV_{PK-PK}
5 ms / div.

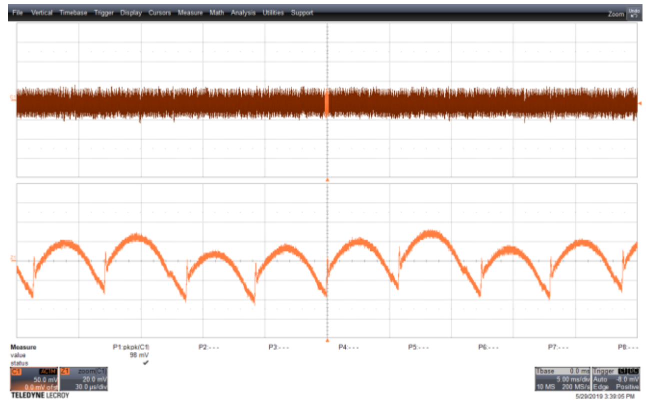

Figure 133 – Output Ripple. (PK-PK – 98 mV)
265 VAC Input 5 V, 5 A Load.
V_{OUT}, 50 mV / div., 98 mV_{PK-PK}
5 ms / div.

15.5.3.3 9 V Ripple Waveforms

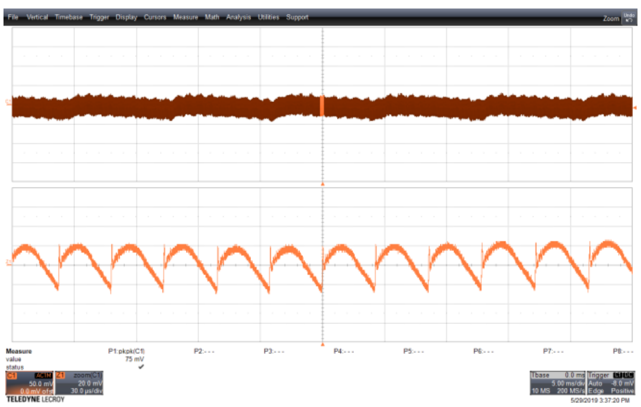

Figure 134 – Output Ripple. (PK-PK – 75 mV)
90 VAC Input 9 V, 5 A Load.
V_{OUT}, 50 mV / div., 75 mV_{PK-PK}
5 ms / div.

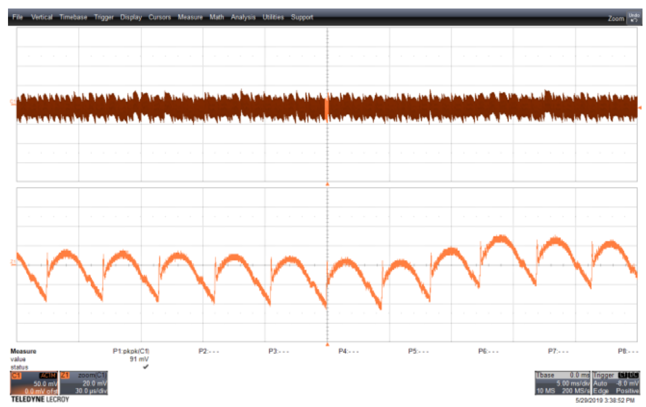

Figure 135 – Output Ripple. (PK-PK – 91 mV)
265 VAC Input 9 V, 5 A Load.
V_{OUT}, 50 mV / div., 91 mV_{PK-PK}
5 ms / div.

15.5.3.4 15 V Ripple Waveforms

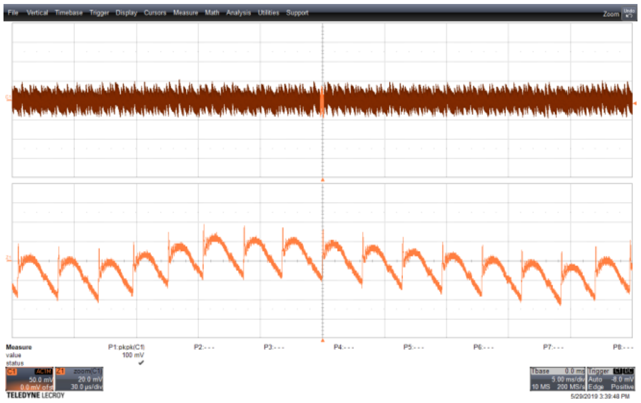

Figure 136 – Output Ripple. (PK-PK – 100 mV)
90 VAC Input 15 V, 5 A Load.
V_{OUT}, 50 mV / div., 5 ms / div.

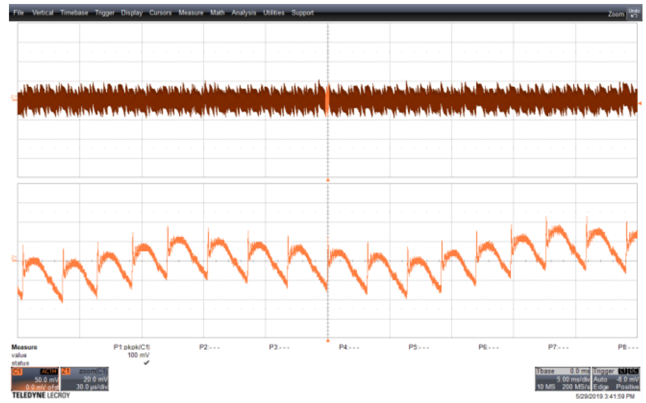

Figure 137 – Output Ripple. (PK-PK – 100 mV)
265 VAC Input 15 V, 5 A Load.
V_{OUT}, 50 mV / div., 5 ms / div.

15.5.3.5 20 V Ripple Waveforms

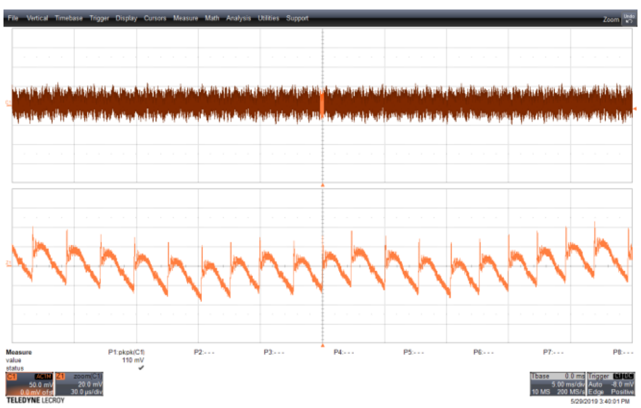

Figure 138 – Output Ripple. (PK-PK – 110 mV)
90 VAC Input 20 V, 5 A Load.
V_{OUT}, 50 mV / div., 5 ms / div.

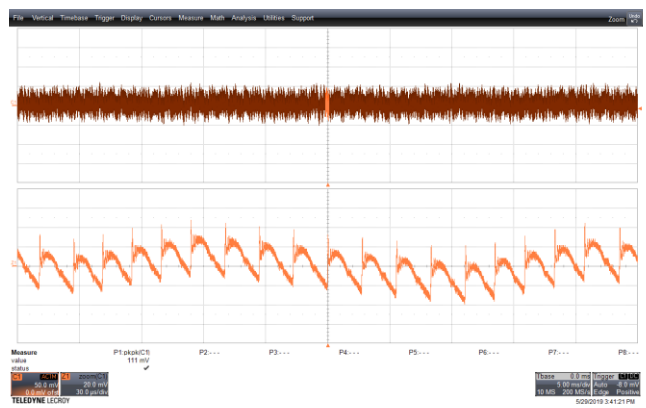

Figure 139 – Output Ripple. (PK-PK – 111 mV)
265 VAC Input 20 V, 5 A Load.
V_{OUT}, 50 mV / div., 5 ms / div.

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16 Voltage and Current Step Test using Quadramax and Total Phase Analyzer

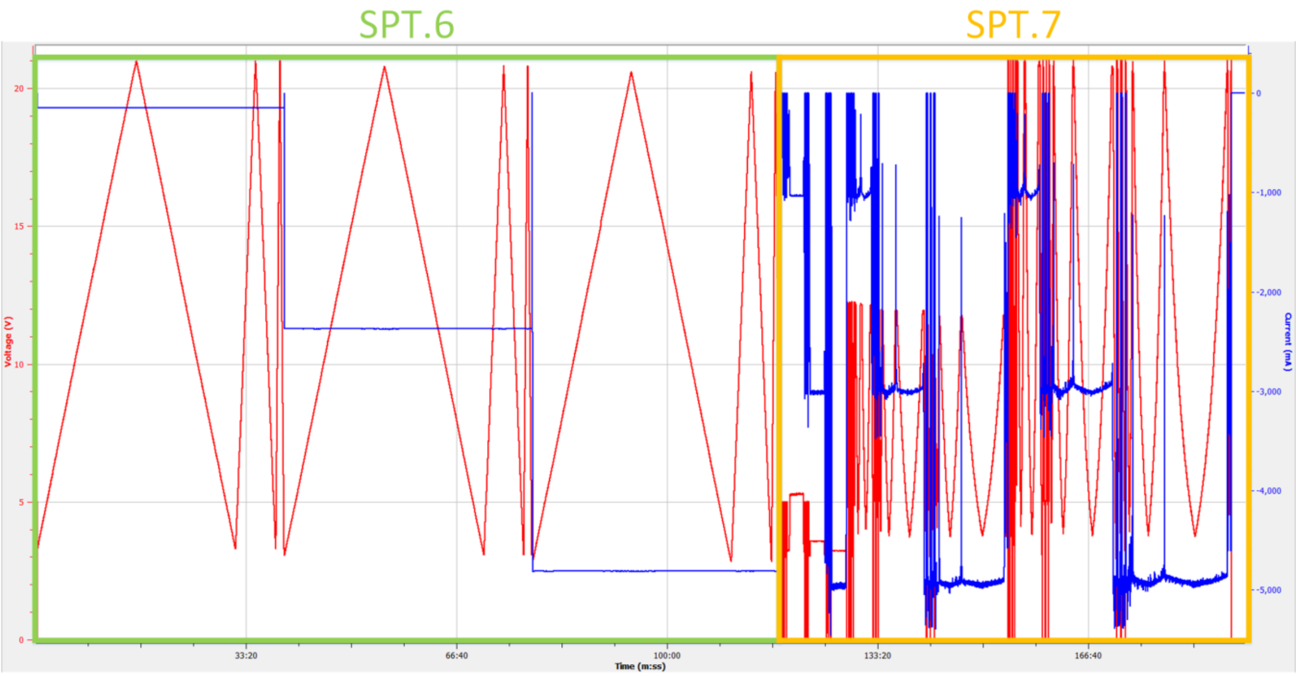

Figure 140 – Plot of SPT.6 VST Test and SPT.7 CLT Test from Total Phase Analyzer.

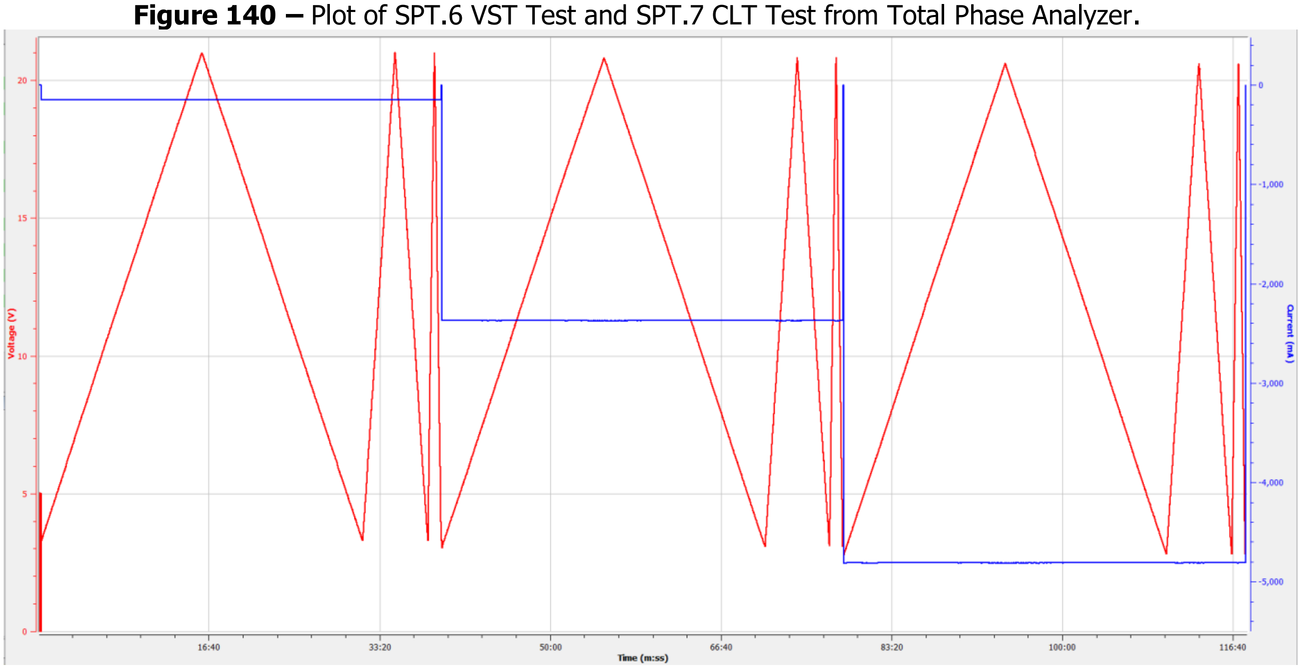

Figure 141 – Plot of SPT.6 VST Test from Total Phase Analyzer.

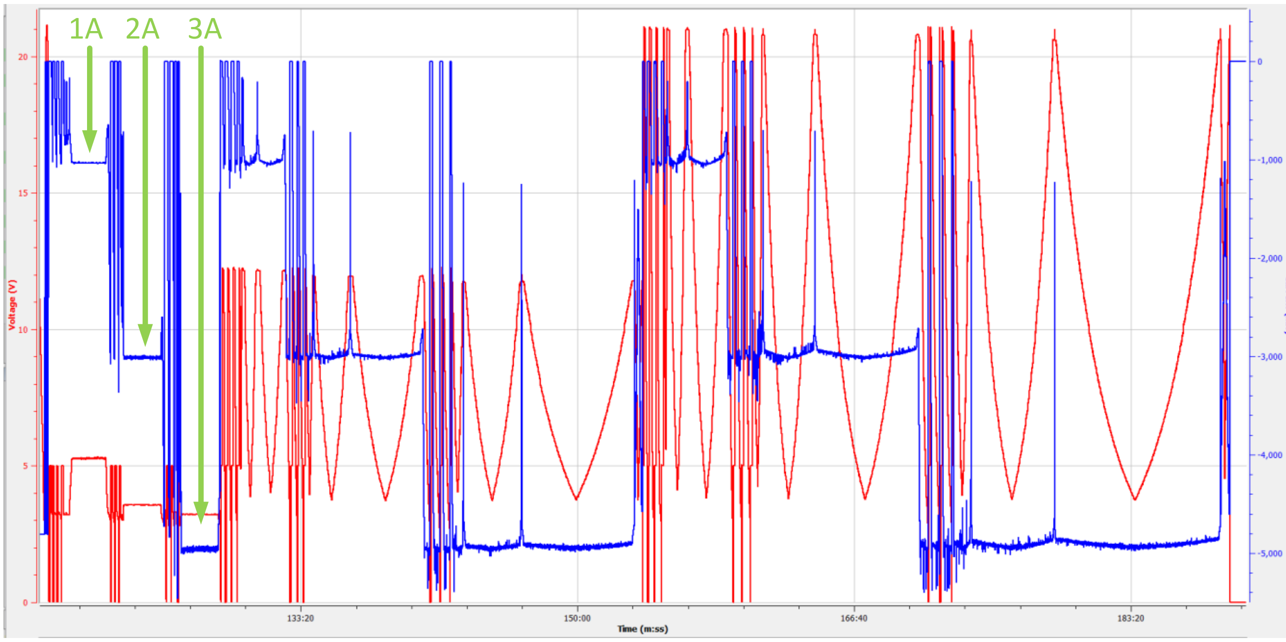

Figure 142 – Plot of SPT.7 CLT Test from Total Phase Analyzer.

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17 Conducted EMI

17.1 Floating (PK / AV)

17.1.1 5 V, 5 A

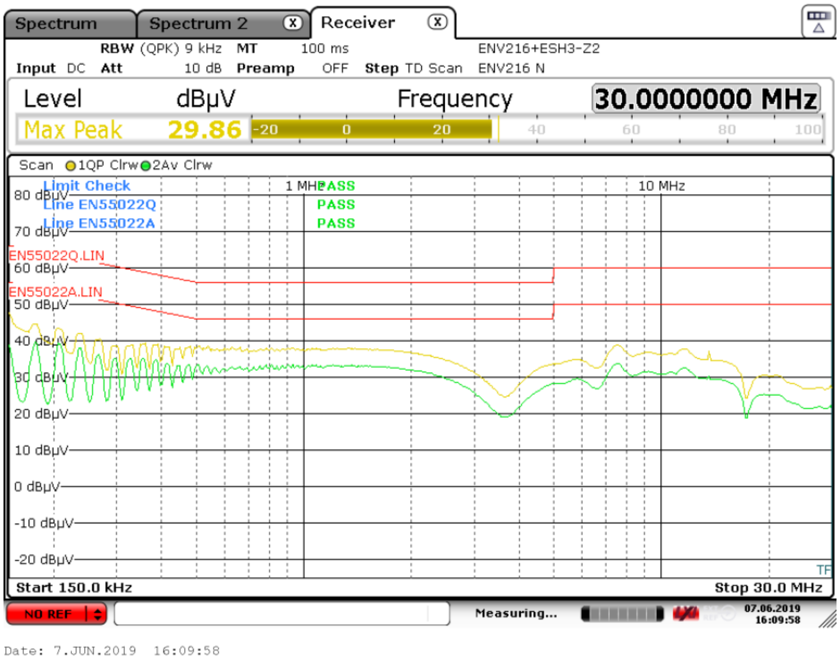

Figure 143 – Floating EMI, 5 V / 5 A Load for 115 VAC.

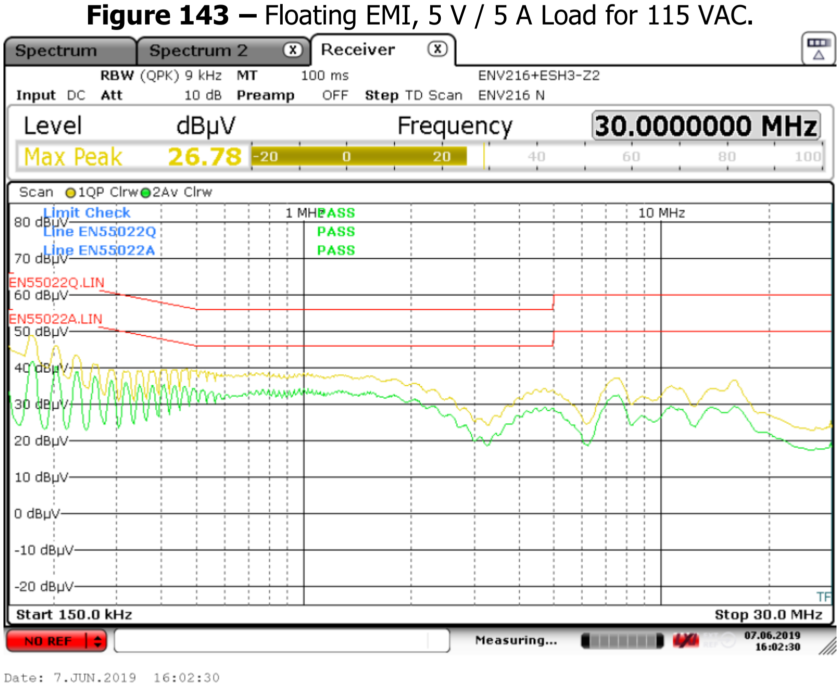

Figure 144 – Floating EMI, 5 V / 5 A Load for 230 VAC.

17.1.2 9 V, 5 A

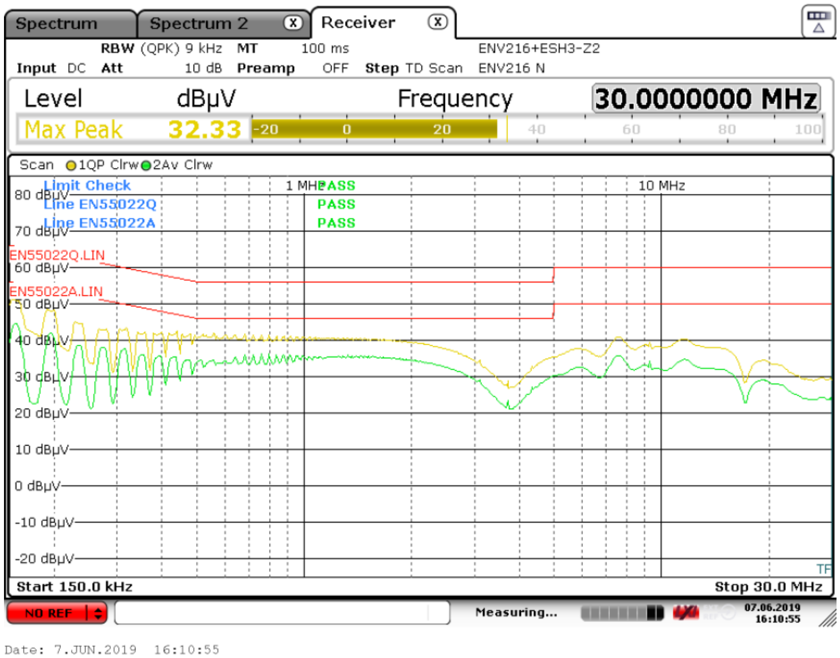

Figure 145 – Floating EMI, 9 V / 5 A Load for 115 VAC.

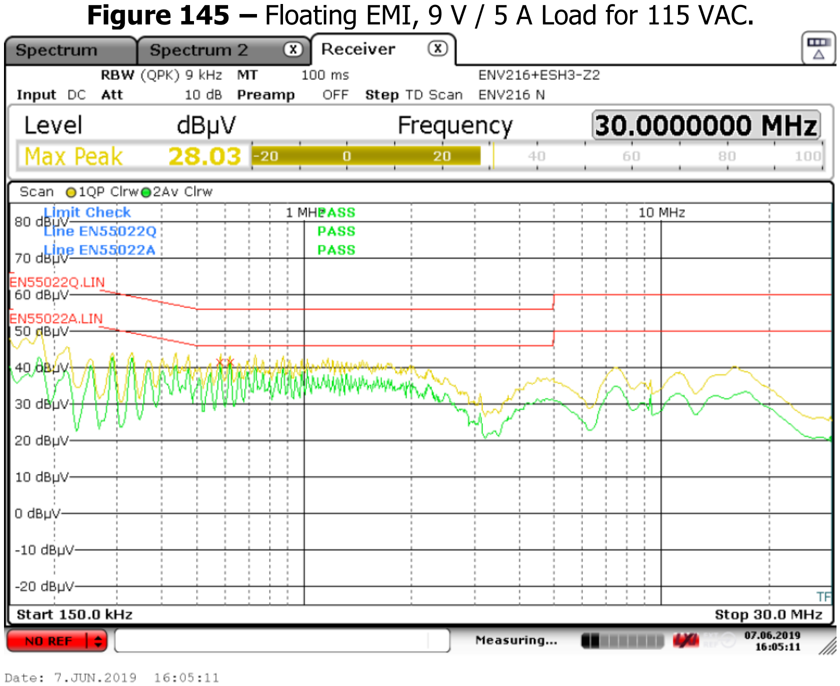

Figure 146 – Floating EMI, 9 V / 5 A Load for 230 VAC.

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17.1.3 15 V, 5 A

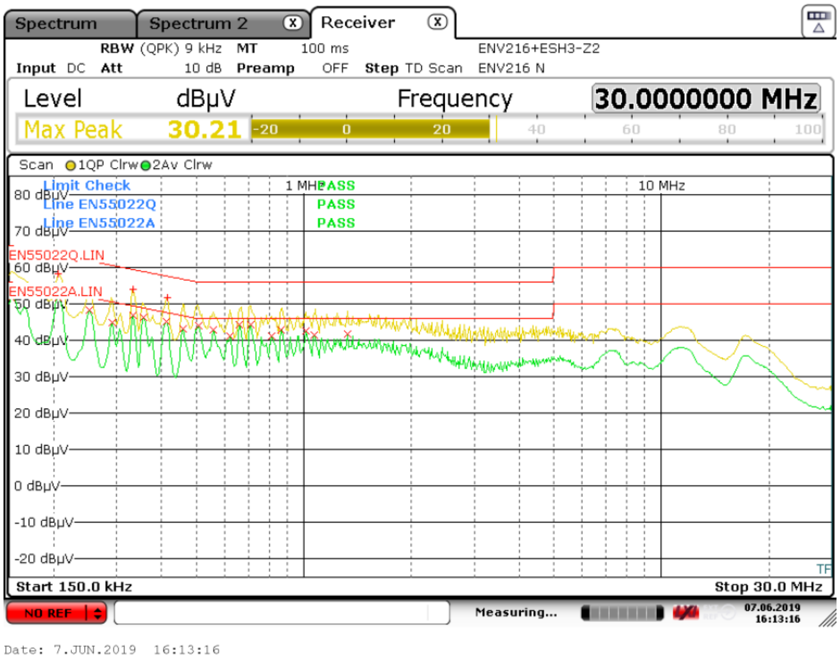

Figure 147 – Floating EMI, 15 V / 5 A Load for 115 VAC.

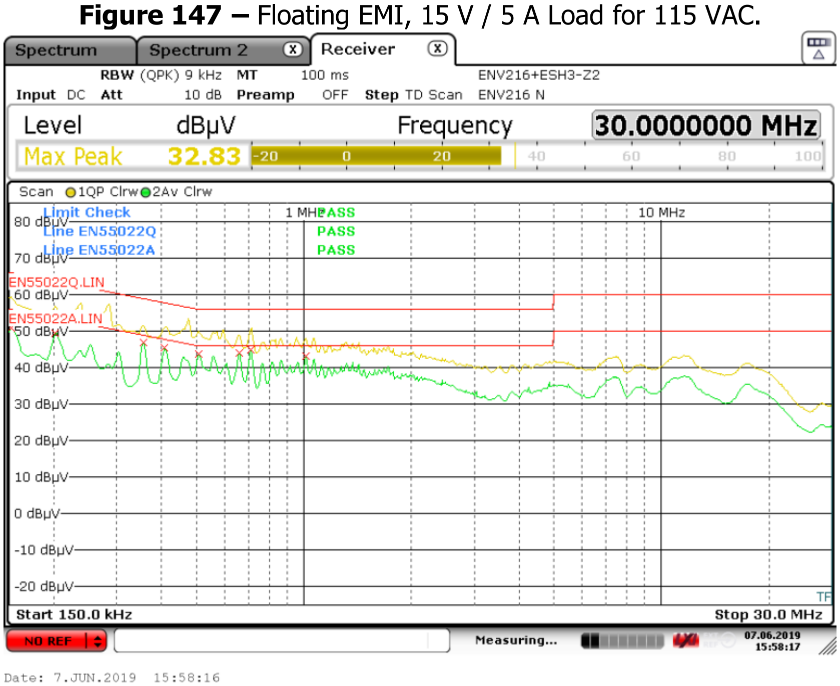

Figure 148 – Floating EMI, 15 V / 5 A Load for 230 VAC.

17.1.4 20 V, 5 A

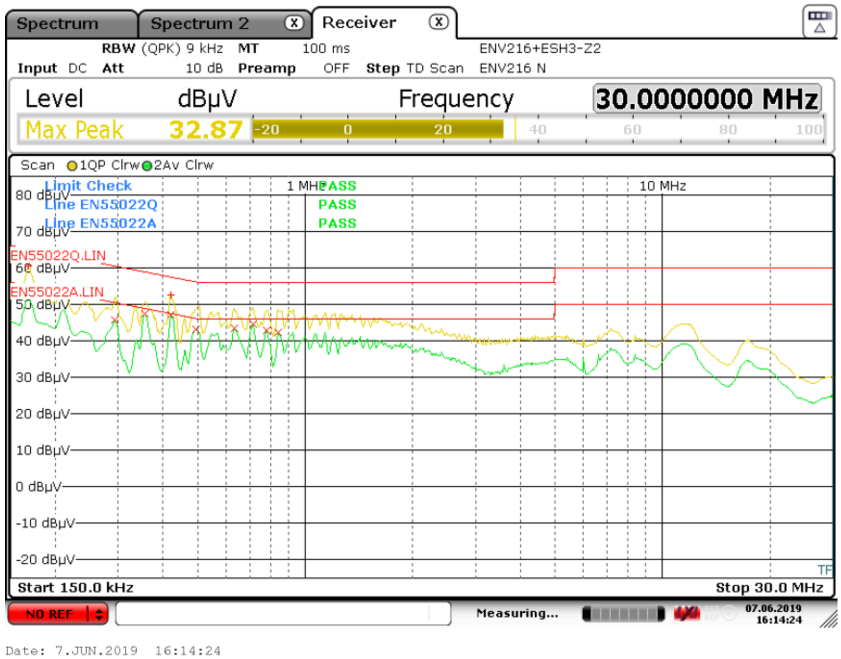

Figure 149 – Floating EMI, 20 V / 5 A Load for 115 VAC.

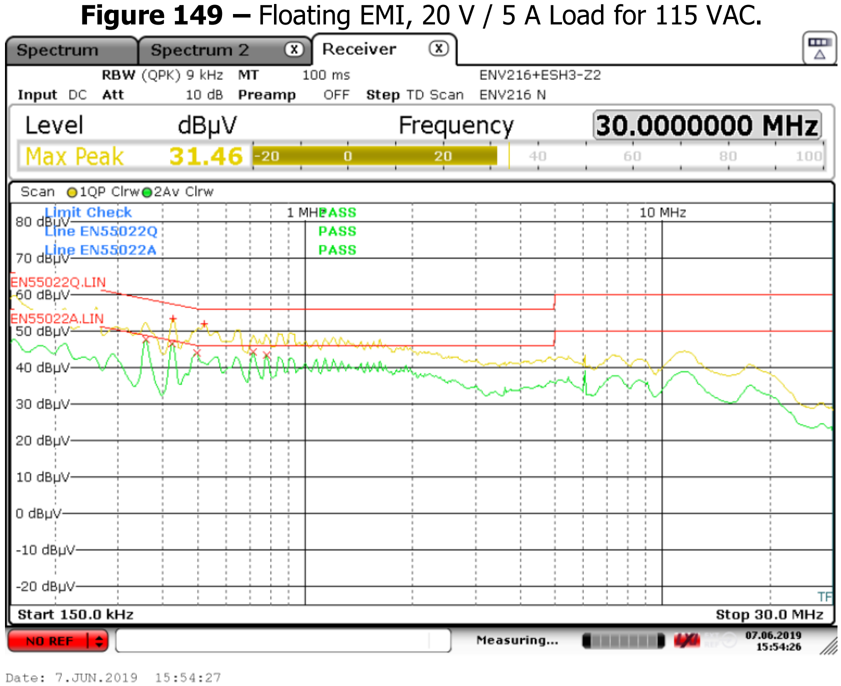

Figure 150 – Floating EMI, 20 V / 5 A Load for 230 VAC.

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18 Line Surge

18.1 *Combination Wave Differential Mode Test*

±1 kV. L-N Pass

Surge Voltage (kV)	Phase Angle (°)	Injection Location (2 Ω Impedance)	Number of Strikes	Test Result
+1	0	L-N	10	Pass
+1	90	L-N	10	Pass
+1	270	L-N	10	Pass
-1	0	L-N	10	Pass
-1	90	L-N	10	Pass
-1	270	L-N	10	Pass

Note: Input line OVP gets triggered when the DC bus voltages crosses line OV threshold.

18.2 *Combination Wave Common Mode Test*

Surge Voltage (kV)	Phase Angle (°)	Injection Location (12 Ω Impedance)	Number of Strikes	Test Result
+2	0	L-PE	10	PASS
+2	90	L-PE	10	PASS
+2	270	L-PE	10	PASS
-2	0	L-PE	10	PASS
-2	90	L-PE	10	PASS
-2	270	L-PE	10	PASS
+2	0	N-PE	10	PASS
+2	90	N-PE	10	PASS
+2	270	N-PE	10	PASS
-2	0	N-PE	10	PASS
-2	90	N-PE	10	PASS
-2	270	N-PE	10	PASS
+2	0	L,N-PE	10	PASS
+2	90	L,N-PE	10	PASS
+2	270	L,N-PE	10	PASS
-2	0	L,N-PE	10	PASS
-2	90	L,N-PE	10	PASS
-2	270	L,N-PE	10	PASS

Note: Input line OVP gets triggered when the DC bus voltages crosses line OV threshold.

19 ESD

ESD test is done on both VBUS and GND pin.

Air Discharge (kV)	Number of Strikes	Strike Location	Test Result
+16.5	10	VBUS	Pass
-16.5	10	VBUS	Pass
+16.5	10	GND	Pass
-16.5	10	GND	Pass

Contact Discharge (kV)	Number of Strikes	Strike Location	Test Result
+8	10	VBUS	Pass
-8	10	VBUS	Pass
+8	10	GND	Pass
-8	10	GND	Pass

Note: ESD test is performed at the end of 1 meter cable.

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20 Revision History

Date	Author	Revision	Description & Changes	Reviewed
24-Jul-19	JC	1.0	Initial Release.	Apps & Mktg
06-Sep-19	JC	1.1	Update Case Information. Updated Figure 46.	Apps & Mktg
25-Nov-19	KM	1.2	Updated U4 part number in BOM.	Apps & Mktg
11-Mar-20	KM	1.3	Added 2^{nd} source for D6, D10 and VR6.	Apps & Mktg
16-Sep-20	KM	1.4	Converted to RDR.	Apps & Mktg
17-Sep-20	DB	1.5	Updated / added info to following sections: BOM, PFC Inductor and Transformer Specifications, Transformer Design Spreadsheet, Adapter Case and Heat Spreader Assembly section.	Apps & Mktg

For the latest updates, visit our website: www.power.com

Patent Information

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