Title	***Reference Design report for a 300 W 3-Phase Inverter Using BridgeSwitch™ BRD1265C with Current Reconstruction in FOC Operation***
Specification	180 VAC – 265 VAC Input; 300 W Continuous Three-Phase Inverter Output Power, 0.98 A_{RMS} Continuous Motor Phase Current
Application	High-Voltage Brushless DC (BLDC) Motor Drive
Author	Applications Engineering Department
Document Number	RDR-964
Date	October 20, 2022
Revision	2.0

Summary and Features

- BridgeSwitch – high-voltage half-bridge motor driver
- Integrated 600 V FREDFETs with ultra-soft, fast recovery diodes
- No heat sink
- Fully self-biased operation – simplifies auxiliary power supply but can also support external bias operation as needed
- High-side and low-side cycle-by-cycle current limit
- Two level device over-temperature protection
- High-voltage bus monitor with four undervoltage threshold and one overvoltage threshold
- System level temperature monitor
- Single wire status update communication bus
- Supports any microcontroller (MCU) for sensorless field-oriented control (FOC) through the signal interface
- Instantaneous phase current output signal for each BridgeSwitch
- Fault reporting for each device through the FAULT BUS pin on the interface
- No op-amps for current signal conditioning – not needed when using IPH current reconstruction
- No current sense resistors – not needed when using IPH current reconstruction.

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PATENT INFORMATION

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Table of Contents

1 Introduction....5
2 Inverter Specification....6
3 Schematic....7
4 Circuit Description....10
4.1 Three-Phase BridgeSwitch Inverter....10
4.2 Input Stage....10
4.3 BridgeSwitch Bias Supply....10
4.4 PWM Input....10
4.5 Cycle-by-Cycle Current Limit....11
4.6 System Undervoltage (UV) and Overvoltage (OV) Protection....11
4.7 System Level Temperature and Monitoring....11
4.8 Fault Bus....11
4.9 Device ID....11
4.10 Microcontroller (MCU) Interface....11
4.11 External Supply....12
4.12 Three-Phase Motor Interface....12
4.13 Auxiliary Power Supply Circuit....12
5 Printed Circuit Board Layout....13
6 Bill of Materials....15
7 Performance Data....16
7.1 Start-Up Operation....16
7.1.1 Motor Start-Up Waveforms....16
7.2 Steady-State Operation....17
7.2.1 Phase Voltages (Drain-to-Source) During Steady-State....17
7.2.2 High-Side Drain-to-Source Voltage Slew Rate....18
7.2.3 Phase Currents During Steady-State....19
7.2.4 INL and /INH Signals....20
7.2.5 BPL and BPH during Steady-State....21
7.3 Thermal Performance....22
7.3.1 100 W Loading Condition (340 mA Average Motor Phase Current)....23
7.3.2 200 W Loading Condition (670 mA Average Motor Phase Current)....23
7.3.3 300 W Loading Condition (930 mA Average Motor Phase Current)....24
7.3.4 Thermal Scan Summary Table....24
7.3.4.1 Self Supply Mode 24
7.3.4.2 External Supply Mode 24
7.4 No-Load Input Power Consumption....25
7.5 Efficiency....26
7.5.1 Efficiency Table at Self Supply Mode....27
7.5.2 Efficiency Table at External Supply Mode....27
7.6 Device and System Level Protection / Monitoring....28
7.6.1 Overcurrent Protection (OCP)....28
7.6.2 Thermal Warning....29
7.6.3 Thermal Shutdown....30

7.6.4 Undervoltage (UV) 31
7.6.5 Overvoltage (OV) 33
7.6.6 System Thermal Fault 34
7.7 Abnormal Motor Operation Test 35
7.7.1 Operation Under Stalled (Motor) Conditions 35
7.7.2 Operation with One Motor Phase / Winding Disconnected 36
7.7.3 Running Overload Test 38
8 Appendix 39
8.1 Board Quick Reference 39
8.1.1 The Microcontroller (MCU) Interface Contains the Following Pins/Signals 39
8.1.2 J1 Connector Pin Designation 40
8.2 Recommended Start-up Sequence 41
8.3 Status Word Encoding 42
8.4 Suggested Microcontroller Actions to BridgeSwitch Fault Conditions 43
8.5 Inverter Output Power Measurement 44
8.6 Current Capability vs. Ambient Temperature 45
8.7 Efficiency Curves at Different Switching Frequencies 46
8.8 Operation with One Motor Phase / Winding Disconnected (with FAULT BUS Processing) 47
8.9 Running Overload Test (with FAULT BUS Processing) 48
8.10 Operation with Two Motor Phases / Windings Shorted 49
8.11 Dynamic Loading Operation Test 50
8.12 Test Bench Set-up 54
8.12.1 Equipment Used 55
8.13 Sensorless FOC Algorithm with IPH Reconstruction 56
8.14 Motor-Expert Suite 58
8.14.1 Motion Scope 59
8.14.2 Terminal Emulator 60
8.15 Hardware Changes/Improvements 61
9 Revision History 62

Important Note:

During operation, the reference design board is subject to hazards including high voltages, rotating parts, bare wires, and hot surfaces. Energized DC bus capacitors require time to discharge after DC input disconnection.

All testing should use an isolation transformer to provide the DC input to the board.

1 Introduction

This document describes a 300 W, 97% efficient, three-phase inverter for high-voltage brushless DC (BLDC) motor application using three BridgeSwitch BRD1265C devices. The design shows the device performance, internal level monitoring, system level monitoring, and fault protection facilitated by the high level of integration of the BridgeSwitch half-bridge motor driver IC. A high-voltage, low component count buck converter employing a LinkSwitch-TN2 LNK3204D device optionally provides external bias for the BridgeSwitch devices.

In addition, this document contains the inverter specification, schematic, bill of materials, printed circuit board (PCB) layout, performance data, and test setup. The provided waveforms along with the design performance are based on a sensorless field-oriented control (FOC) method employing Space Vector Modulation (SVM) scheme commonly referred to as three-phase modulation in this document.

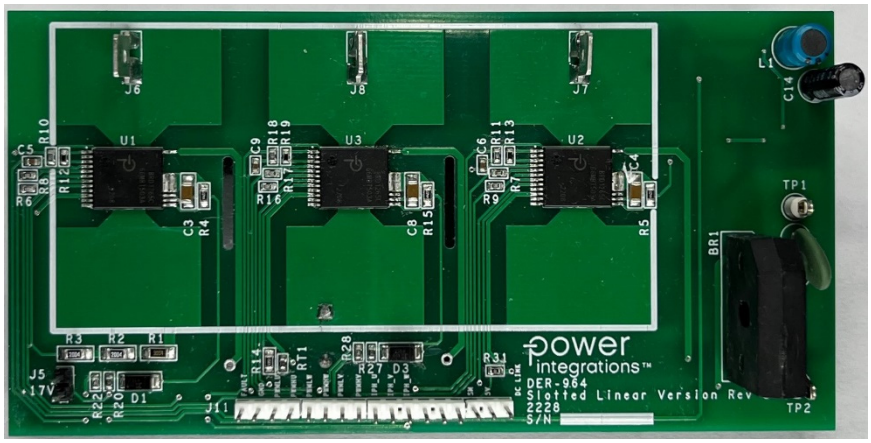


Figure 1 – Populated Circuit Board Top View.

Note: More information about the sensorless field-oriented control algorithm are discussed in the appendix including the Motor-Expert™ Suite.

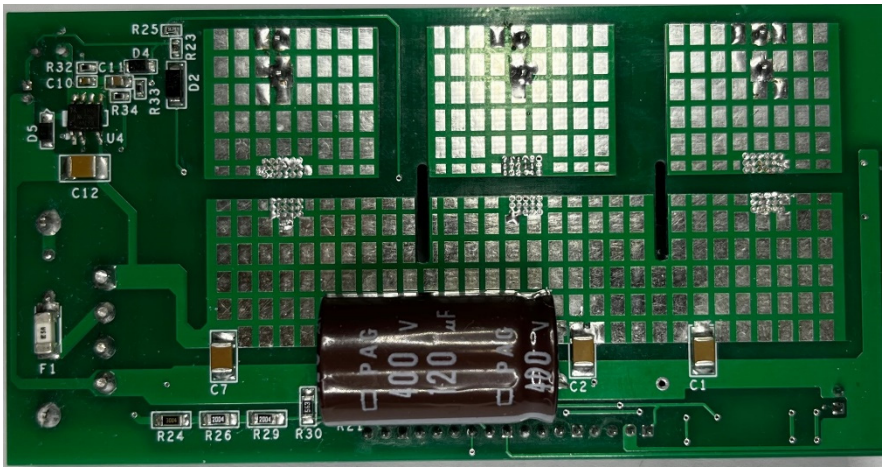


Figure 2 – Populated Circuit Board Bottom View.

2 Inverter Specification

The table below provides the electrical specification of the three-phase inverter design. The result section provides actual performance data.

Description	Symbol	Min	Typ	Max	Unit	Comment
Input						
Voltage	V_{IN}	180	240	265	VAC	2-Wire – No P.E.
Current	I_{IN}		0.91		A_{RMS}	RMS
Power	P_{IN}		309		W	At Efficiency = 97%.
Output						
Power	P_{OUT}		300		W	Inverter Output Power
Motor Phase Current	$I_{MOT(RMS)}$		0.98		A_{RMS}	Continuous RMS per Phase.
Inverter Peak Output Current	$I_{INT(PK)}$		3		A	Inverter Peak Current.
PWM Carrier Frequency[1]	f_{PWM}	5	12	16	kHz	Three-Phase FOC Modulation.
Efficiency	η		97		%	Self-Supplied Operation.
Output Speed	ω		5000		RPM	Motor Speed at 300 W Inverter Output.
Environmental						
Ambient Temperature	T_{AMB}	-20	28	65	°C	Average Ambient Temperature. Closed-case. Free Convection.
Device Case Temperature	$T_{PACKAGE}$		85	124	°C	Average Case Temperature at 0.98 A_{RMS} Phase Current in Self-Supplied Operation.
System Level Monitoring						Reported through Status Communication Bus (FAULT Pin).
DC Bus Sensing						
OV Threshold	V_{OV}		422		V	
1st UV Threshold	V_{UV100}		247		V	
2nd UV Threshold	V_{UV85}		212		V	
3rd UV Threshold	V_{UV60}		177		V	
4th UV Threshold	V_{UV55}		142		V	
Over Current Protection[2]	I_{OCP}		3		A_{PK}	At XL/XH = 44.2 kΩ
System Warning Temperature[3]	T_{SYS}		90		°C	

Notes:
1. 20 kHz is the maximum recommended PWM frequency with self-supply or with external supply.
2. This can be manually configured by adjusting the value of the XL/XH resistors. For BRD1265C, the maximum current protection level is 3 A_{PK} at an XL/XH resistance of 44.2 kΩ.
3. Sensed through an external thermistor, the temperature threshold depends on the chosen NTC and its location (requires verification in final application).

Table 1 – Inverter Specification.

3 Schematic

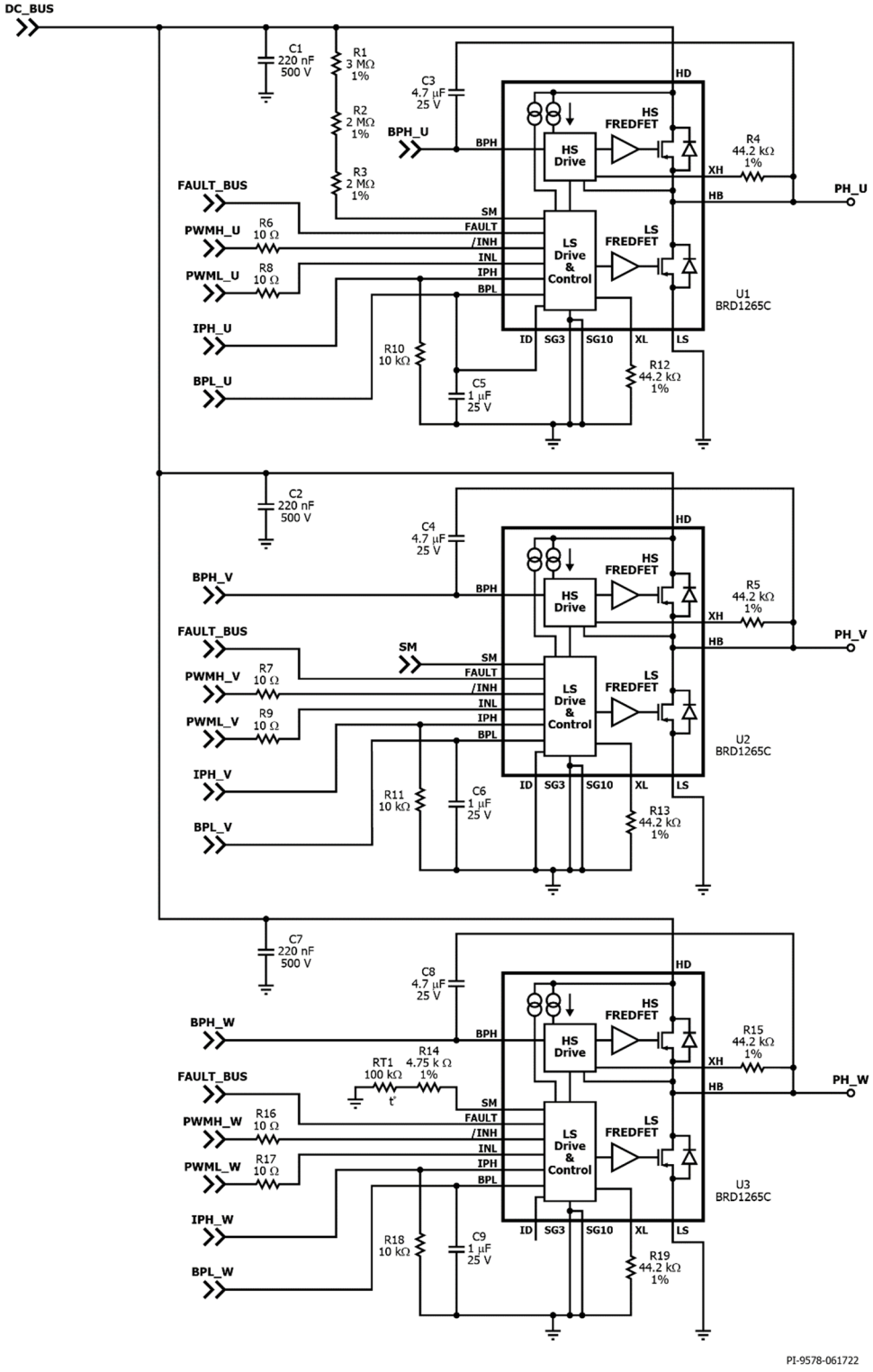


Figure 3 – BridgeSwitch Three-Phase Inverter Circuit Schematic.

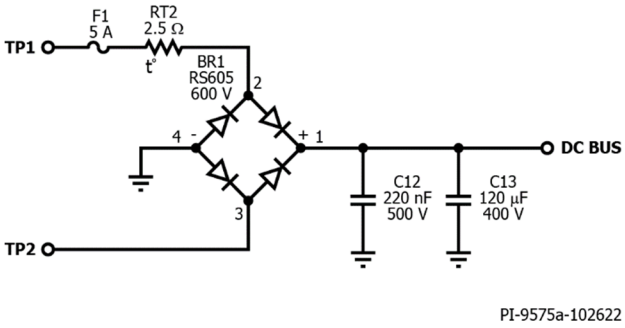


Figure 4 – AC Input.

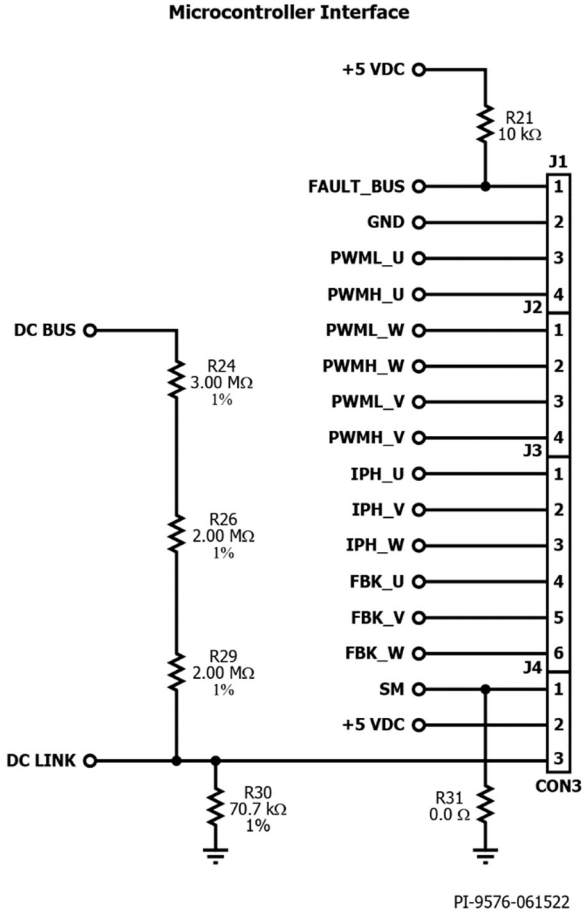


Figure 5 – Microcontroller Interface Schematic.

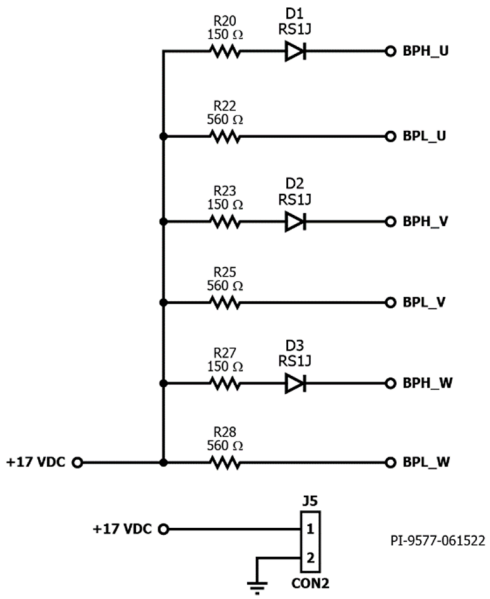


Figure 6 – External Supply Schematic.

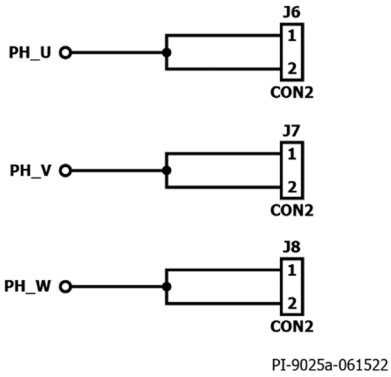


Figure 7 –Three-Phase Motor Interface Schematic.

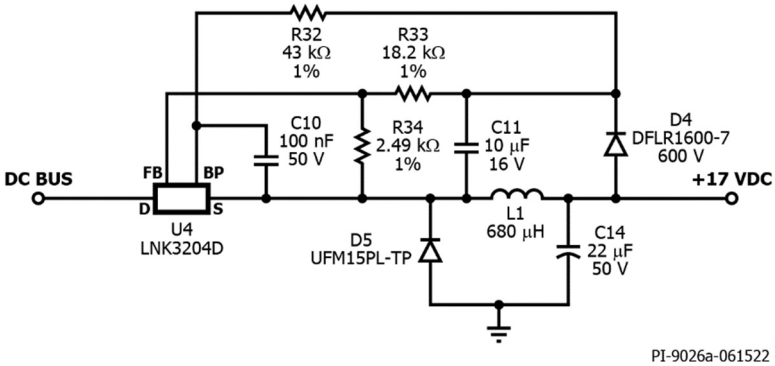


Figure 8 – Auxiliary Circuit Schematic.

4 Circuit Description

The overall schematic shows a three-phase inverter utilizing three BridgeSwitch BRD1265C devices. The circuit design drives a high-voltage, three-phase, brushless DC (BLDC) motor utilizing field-oriented control (FOC) for driving the motor. The BridgeSwitch IC combines two 600 V, N-channel power FREDFETs with their corresponding gate drivers into a low profile surface mount package. The BridgeSwitch power FREDFET features an ultra-soft, fast recovery diode ideally suited for inverter drives. Both drivers are fully self-supplied eliminating the need for the system power supply to provide gate drive power.

A LinkSwitch-TN2 LNK3204D device in a high-voltage buck converter configuration provides an optional +17 V supply for the BridgeSwitch device (external bias).

In addition, the BridgeSwitch IC incorporates internal fault protection and system level monitoring. Internal fault protection includes cycle-by-cycle current limit for both FREDFETs and a two level thermal overload protection. On the other hand, system level monitoring includes high-voltage DC bus sensing with multi-level undervoltage thresholds and one overvoltage threshold. The BridgeSwitch IC can also be configured using external sensors such as a thermistor for system temperature monitoring. A single wire open drain bus communicates all detected fault or change of status to the system microcontroller.

4.1 Three-Phase BridgeSwitch Inverter

The three BridgeSwitch devices U1, U2, and U3 form the three-phase inverter. The output of the inverter connects to the three-phase BLDC motor through connectors J6, J7, and J8.

4.2 Input Stage

The input stage consists of terminals TP1 and TP2, input bridge diode BR1, and bulk capacitors C12 and C13. Terminals TP1 (AC line) and TP2 (AC neutral) serve as connectors for the high-voltage AC or DC bus. The bulk capacitor C13 minimizes the path for the high-voltage DC input from the supply to the board.

4.3 BridgeSwitch Bias Supply

Capacitors C5, C6, and C9 provide self-supply decoupling for the integrated low-side controller and gate driver. An internal high-voltage current source recharges these capacitors as soon as the voltage level starts to dip. On the other hand, capacitors C3, C4, and C8 provide self-supply decoupling for the integrated high-side controller and gate driver. Internal high-voltage current sources recharge these capacitors whenever the half-bridge point of the respective device drops to the low-side source voltage level (i.e., the low-side FREDFET turns on).

4.4 PWM Input

Input PWM signals PWML_U, PWMH_U, PWML_V, PWMH_V, PWML_W, PWMH_W, control the switching state of the integrated high-side and low-side power FREDFETs. The system microcontroller provides the required PWM signal and desired switching frequency.

4.5 Cycle-by-Cycle Current Limit

Resistors R4, R12, R5, R13, R15, and R19 set the cycle-by-cycle current limit level for the integrated low-side and high-side power FREDFETs. A selected value of 44.2 kΩ set the current limit to 100% of the default level or 3 A_{PK}.

4.6 System Undervoltage (UV) and Overvoltage (OV) Protection

The BridgeSwitch device (U1) monitors the DC bus voltage through resistors R1 (3 MΩ), R2 (2 MΩ), and R3 (2 MΩ). The combined resistance of 7 MΩ sets the undervoltage thresholds to 247 V, 212 V, 177 V, and 142 V. The bus overvoltage threshold is at 422 V. The FAULT pin reports any detected bus voltage fault condition.

4.7 System Level Temperature and Monitoring

The BridgeSwitch device (U3) monitors the system temperature through thermistor RT1 connected to the SM pin. Resistor R14 tunes the threshold for a system level fault of 90 °C. The device reports a detected status change of the externally set system level temperature through the FAULT pin.

4.8 Fault Bus

The BridgeSwitch devices (U1, U2, and U3) reports any detected internal and system status change through pin 1 of connector J4. The system microcontroller can take action in accordance to the status update reported by the device. Such action could be for instance inverter shutdown, latch, restart, warning, etc.

4.9 Device ID

Each BRD1265C assigns itself a unique device ID through the connection of pin 11 (ID pin). The pin can be floating, connected to the SG pin, or connected to the BPL pin. The device ID allows the specific device flagging a fault to communicate its physical location to the system microcontroller.

4.10 Microcontroller (MCU) Interface

Connector J1, J2, J3, and J4 serve as an interface between the system microcontroller and the BridgeSwitch three-phase inverter which contains the following signals:

- **FAULT_BUS** – Pin dedicated for fault reporting of all BridgeSwitch devices.
- **GND** – Common ground interface between the microcontroller and the inverter board.
- **PWMH_U, PWML_U, PWMH_V, PWML_V, PWMH_W, and PWML_W** – PWM input signal interface from the system microcontroller to the BridgeSwitch device.
- **SM** – Configurable system monitoring pin for the BridgeSwitch device (U2).
- **IPH_U, IPH_V, IPH_W** – Instantaneous phase current information of the low-side power FREDFET Drain-to-Source current of each BridgeSwitch device coming from the IPH pin.

4.11 External Supply

Components R20, R22, R23, R25, R27, R28 and diodes D1, D2, and D3 are responsible for providing external supply to the BridgeSwitch BPL/BPH pin through device U4. External supply operation is optional for applications that require lower inverter no-load input power or operate at elevated ambient temperatures. Otherwise, these resistor and diode components can be depopulated. If depopulated, BPL/BPH supply will be drawn internally through the BridgeSwitch device (self-supply).

4.12 Three-Phase Motor Interface

Connectors J6, J7, and J8 are mechanical connectors that directly connect the BridgeSwitch three-phase inverter to the BLDC motor.

4.13 Auxiliary Power Supply Circuit

Device U4 (LNK3204D) is a high-side buck switcher IC responsible for providing optional +17 V supply for BPL/BPH (external bias). It directly steps down the high input DC voltage to the desired low output voltage. For more information about LNK3204D, please refer to the datasheet through the following link:

https://ac-dc.power.com/design-support/product-documents/data-sheets/linkswitch-tn2-data-sheet/

5 Printed Circuit Board Layout

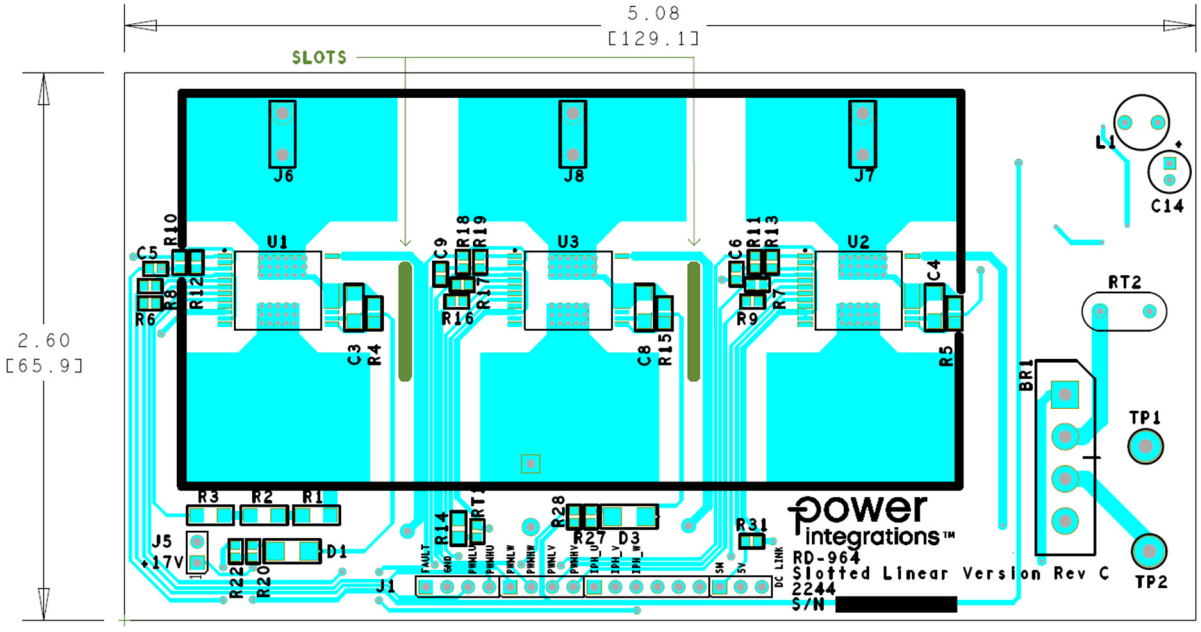


Figure 9 – Printed Circuit Board Layout (Top View).

Note:

1. The overall PCB dimension is 129mm X 66mm (L X W).
2. The inverter PCB dimension is 94mm x 47mm (L X W) – in black rectangle.
3. PCB Specifications:
   - Board thickness: 1.2 mm
   - Board material: FR4
   - Copper weight: 2 oz
   - No. of layers: 2

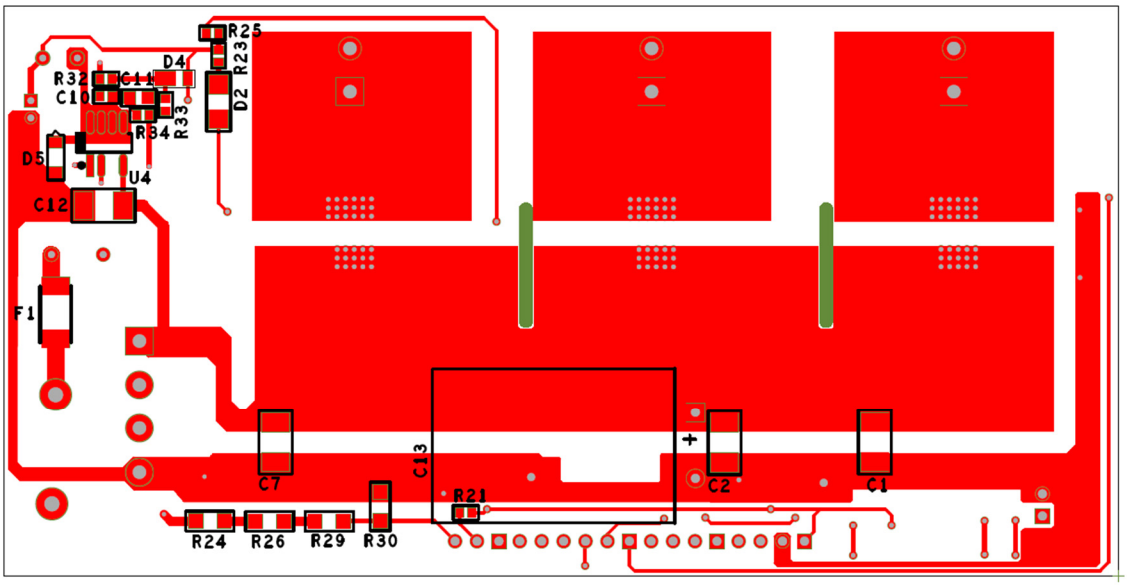


Figure 10 – Printed Circuit Board Layout (Bottom View).

Note:

1. The overall PCB dimension is 129mm X 66mm (L X W).
2. The inverter PCB dimension is 94mm x 47mm (L X W).
3. PCB Specifications:
    - Board thickness: 1.2 mm
    - Board material: FR4
    - Copper weight: 2 oz
    - No. of layers: 2

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	800 V, 6A, Bridge Rectifier, 1 Phase	GBU6K	ON Semi
2	4	C1, C2, C,7 C12	220 nF, ±10%, 500 V, X7R, Ceramic, SMT, MLCC 1812	C1812C224KCRACTU	KEMET
3	3	C3, C4, C8	4.7 μF, ±10%, 25 V, X7R, Ceramic, SMT, MLCC 1206	GCM31CR71E475KA55L	Murata Electronics
4	5	C5, C6, C9-C11	1 μF, ±10%, 25 V, X7R, Ceramic, SMT, MLCC 0603	CGA3E1X7R1E105K080AE	TDK
5	1	C13	100 μF, 20%, 400 V, Electrolytic	EPAG401ELL101ML30S	United Chemi-Con
6	1	C14	22 μF,20%, 25 V, Electrolytic	UVR1H220MDD1TD	Nichicon
7	3	D1-D3	600 V, 1 A, General Purpose, SMA	RS1J-13-F	Diodes, Inc.
8	1	D4	600 V, 1 A, Rectifier, Glass Passivated, POWERDI123	DFLR1600-7	Diodes, Inc.
9	1	D5	600 V, 1 A, Ultrafast Recovery, 75 ns, SOD-123	UFM15PL-TP	Micro Commercial
10	1	F1	FUSE FAST 250V 1245 5A	TR-1245UMFF5-R	Eaton
11	2	J1, J2	4 Pos (1 x 4) header, 0.1 pitch, Vertical	22032041	Molex
12	1	J3	6 Pos (1 x 6) header, 0.1 pitch, Vertical	22032061	Molex
13	1	J4	4 Pos (1 x 3) header, 0.1 pitch, Vertical	22284030	Molex
14	1	J5	2 Pos (1 x 2) header, 0.1 pitch, Vertical	22284020	Molex
15	3	J6-J8	CONN QC TAB 0.250 SOLDER	1287-ST	Keystone
16	1	L1	680 μH, 0.36 A	SBC2-681-211	KEMET
17	1	RT1	NTC Thermistor, 100 kΩ, 5%, 0603	NCU18WF104D60RB	Murata
18	1	RT2	NTC Thermistor, 2.5 Ω, 5 A	SCK102R55ALSY	Thinking Electronics
19	2	R1, R24	RES, 3 MΩ, 1%, 1/4 W, Thick Film, 1206	RC1206FR-073ML	Yageo
20	4	R2, R3, R26, R29	RES, 2 MΩ, 1%, 1/4 W, Thick Film, 1206	RC1206FR-072ML	Yageo
21	6	R4, R5, R12, R13, R15, R19	RES, 44.2 kΩ, 1%, 1/8 W, Thick Film, 0805	RC0805FR-0744K2L	Yageo
22	6	R6, R7, R8, R9, R16, R17	RES, 10 Ω, 5%, 1/10 W, Thick Film, 0603	RC0603FR-0710RL	Yageo
23	4	R10, R11, R18, R21	RES, 10 kΩ, 5%, 1/10 W, Thick Film, 0603	RC0603FR-0710KL	Yageo
24	1	R14	RES, 4.75 kΩ, 1%, 1/10 W, Thick Film, 0603	RC0603FR-074K75L	Yageo
25	3	R20, R23, R27	RES, 150 Ω, 5%, 1/10 W, Thick Film, 0603	RC0603JR-07150RL	Yageo
26	3	R22, R25, R28	RES, 560 Ω, 5%, 1/10 W, Thick Film, 0603	RC0603JR-07560RL	Yageo
27	1	R30	RES, 56.2 kΩ, 1%, 1/10 W, Thick Film, 0603	RC0603FR-0756K2L	Yageo
28	1	R31	RES, 0 Ω, JUMPER, 1/10W, Thick Film , 0603	RC0603JR-070RL	Yageo
29	1	R32	RES, 43 kΩ, 1%, 1/10 W, Thick Film, 0603	RC0603FR-0743KL	Yageo
30	1	R33	RES, 18.2 kΩ, 1%,1/10 W, Thick Film, 0603	RC0603FR-0718K2L	Yageo
31	1	R34	RES, 2.49 kΩ, 1%, 1/10 W, Thick Film, 0603	RC0603FR-072K49L	Yageo
32	1	TP1	Test Point, WHT, Thru-hole Mount	5012	Yageo
33	1	TP2	Test Point, BLK, Thru-hole Mount	5011	Yageo
34	3	U1, U2, U3	BridgeSwitch, BLDC Motor Current 5.5 A (DC)	BRD1265C	Power Integrations
35	1	U4	LinkSwitch-TN2, SO-8C	LNK3204D	Power Integrations

7 Performance Data

This section presents waveform plots and performance data of the BridgeSwitch inverter. The high voltage (VBUS) level of 340 VDC is applied directly across the input capacitor C12 unless stated otherwise. Additionally, the fuse F1, inrush thermistor RT2, and bridge diode BR1 were disabled during operation and measurement. An external supply of 17 VDC was connected to J5 to achieve an externally-supplied operation.

Light load measurements describe the inverter operating with no mechanical brake load applied to the motor. Full load operation describes the inverter operating at 300 W output power (refer to the Appendix for details on the method used to measure output power in a three-phase inverter). All measurements were performed at 12 kHz PWM frequency, 28 °C average ambient temperature, and three-phase field-oriented control (three-phase FOC) type of modulation using IPH current reconstruction.

7.1 Start-Up Operation

7.1.1 Motor Start-Up Waveforms

The waveforms below demonstrate the motor start-up of the BridgeSwitch FOC inverter at light load up to 300 W loading condition. The VBUS is set at 340 VDC and the motor maximum speed is set at 5000 RPM.

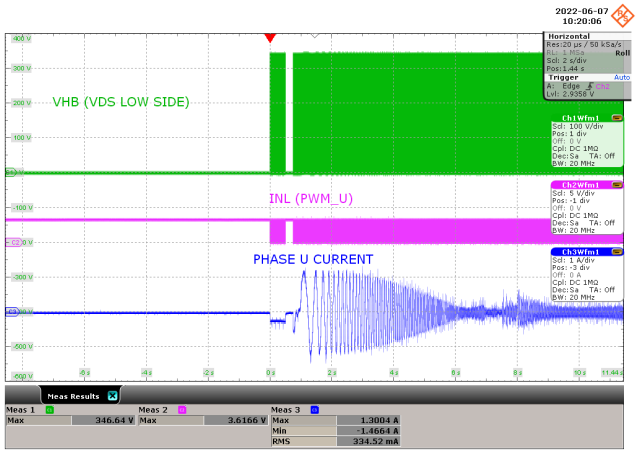


Figure 11 – Motor Start-up at Light Load.
CH1: V_{HB}, 100 V / div.
CH2: V_{INL}, 5 V / div.
CH3: $I_{PHASE\_CURRENT}$, 1 A / div.
Time Scale: 2 s / div.
Maximum Phase Peak Current = 1.46 A_{PK}.
Maximum VHB Peak Voltage = 346.64 V_{PK}.

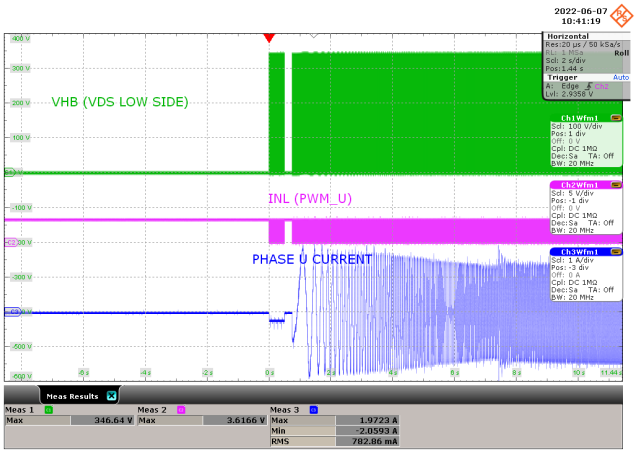


Figure 12 – Motor Start-up at 300 W Load.
CH1: V_{HB}, 100 V / div.
CH2: V_{INL}, 5 V / div.
CH3: $I_{PHASE\_CURRENT}$, 1 A / div.
Time Scale: 2 s / div.
Maximum Phase Peak Current = 2.05 A_{PK}.
Maximum VHB Peak Voltage = 346.64 V_{PK}.

7.2 Steady-State Operation

7.2.1 Phase Voltages (Drain-to-Source) During Steady-State

The waveforms below show the phase voltages of the BridgeSwitch (low-side drain-to-source voltage) three-phase inverter using field-oriented control. The maximum peak voltage was measured from light to full load (inverter load) during steady-state operation. The VBUS is 340 VDC and the motor speed is 5000 RPM.

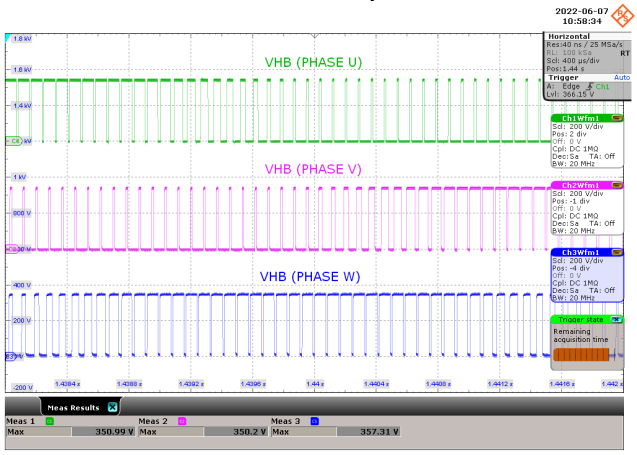


Figure 13 – Drain-to-Source Voltage at Light Load.
CH1: V_{HB_PHASEU}, 200 V / div.
CH2: V_{HB_PHASEV}, 200 V / div.
CH3: V_{HB_PHASEW}, 200 V / div.
Time Scale: 400 us / div.
Maximum Peak Voltage (U) = 350.99 V_{PK}.
Maximum Peak Voltage (V) = 350.20 V_{PK}.
Maximum Peak Voltage (W) = 357.31 V_{PK}.

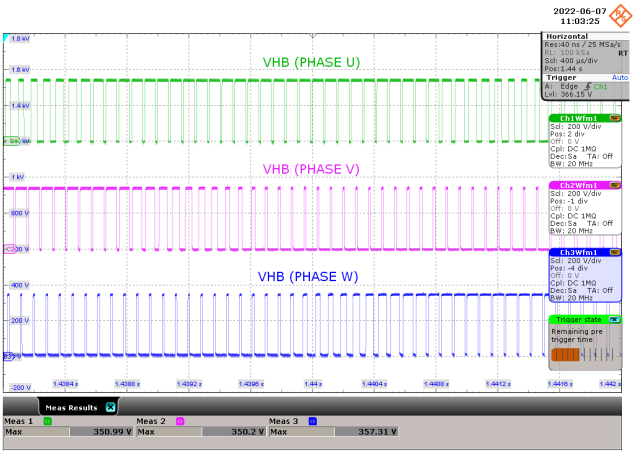


Figure 14 – Drain-to-Source Voltage at 300 W Load.
CH1: V_{HB_PHASEU}, 200 V / div.
CH2: V_{HB_PHASEV}, 200 V / div.
CH3: V_{HB_PHASEW}, 200 V / div.
Time Scale: 400 us / div.
Maximum Peak Voltage (U) = 350.99 V_{PK}.
Maximum Peak Voltage (V) = 350.20 V_{PK}.
Maximum Peak Voltage (W) = 357.31 V_{PK}.

7.2.2 High-Side Drain-to-Source Voltage Slew Rate

The waveforms below show the voltage slew rate at TURN ON and TURN OFF transitions of the high-side BridgeSwitch FREDFET. The measurements were taken at 340 VDC, 5000 RPM, 200 W and 300 W loading condition.

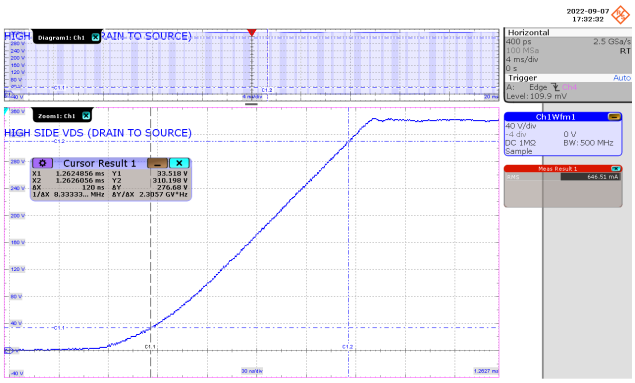


Figure 15 – TURN ON Slew Rate, 200 W Load.

CH1: $V_{DS\_HIGHSIDE}$, 40 V / div.
Time Scale: 4 ms / div.
Time Scale (Zoomed Area): 30 ns / div.
Measured Slew Rate = 2.3 V / ns.

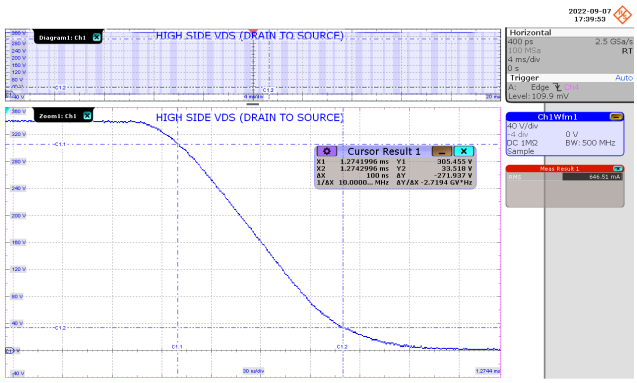


Figure 16 – TURN OFF Slew Rate, 200 W Load.

CH1: $V_{DS\_HIGHSIDE}$, 40 V / div.
Time Scale: 4 ms / div.
Time Scale (Zoomed Area): 30 ns / div.
Measured Slew Rate = 2.72 V / ns.

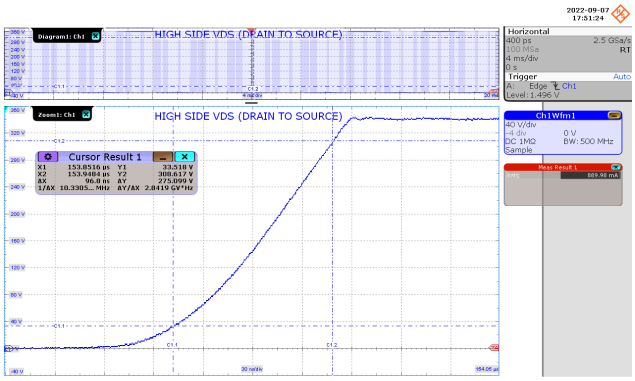


Figure 17 – TURN ON Slew Rate, 300 W Load.

CH1: $V_{DS\_HIGHSIDE}$, 40 V / div.
Time Scale: 4 ms / div.
Time Scale (Zoomed Area): 30 ns / div.
Measured Slew Rate = 2.84 V / ns.

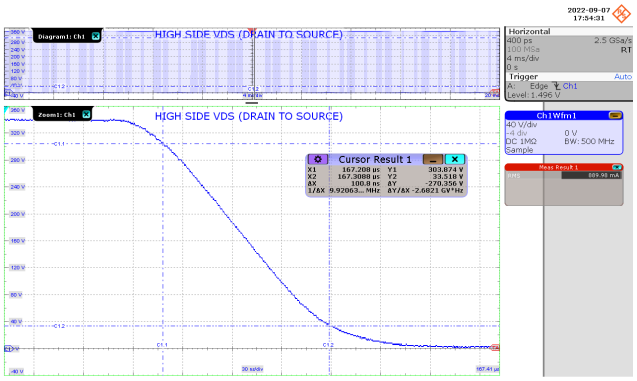


Figure 18 – TURN OFF Slew Rate, 300 W Load.

CH1: $V_{DS\_HIGHSIDE}$, 40 V / div.
Time Scale: 4 ms / div.
Time Scale (Zoomed Area): 30 ns / div.
Measured Slew Rate = 2.68 V / ns.

7.2.3 Phase Currents During Steady-State

The waveforms below show the phase currents of the BridgeSwitch three-phase inverter using field-oriented method of control (FOC). The maximum peak current was measured from light load to 300 W loading condition during steady-state operation.

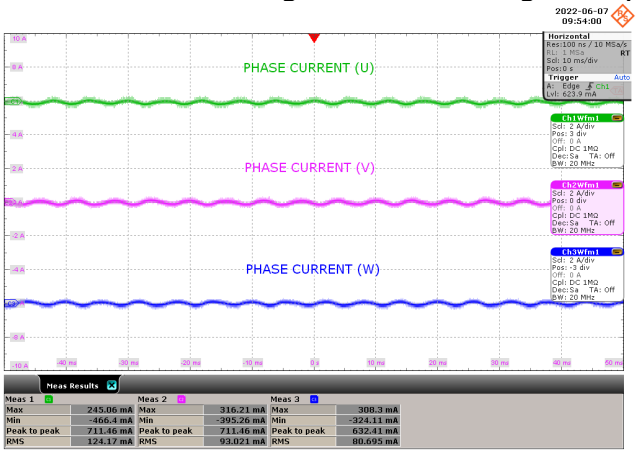


Figure 19 – Phase Current at Light Load.
CH1: I_{PHASEU}, 2 A / div.
CH2: I_{PHASEV}, 2 A / div.
CH3: I_{PHASEW}, 2 A / div.
Time Scale: 10 ms / div.
RMS Current (U) = 124 mA_{RMS}.
RMS Current (V) = 93 mA_{RMS}.
RMS Current (W) = 80 mA_{RMS}.

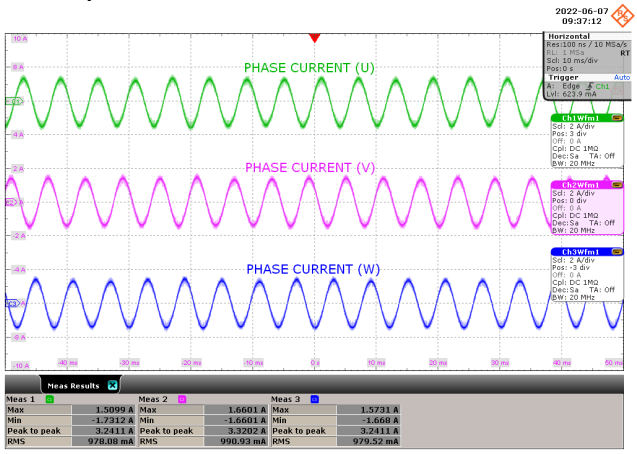


Figure 20 – Phase Current at 300 W Load.
CH1: I_{PHASEU}, 2 A / div.
CH2: I_{PHASEV}, 2 A / div.
CH3: I_{PHASEW}, 2 A / div.
Time Scale: 10 ms / div.
RMS Current (U) = 978 mA_{RMS}.
RMS Current (V) = 990 mA_{RMS}.
RMS Current (W) =979 mA_{RMS}.

7.2.4 INL and /INH Signals

The waveforms below show the low-side (INL) and high-side (/INH) input PWM signals during light load to full load condition at steady-state operation. The PWM frequency is set at 12 kHz with a constant motor speed of 5000 RPM.

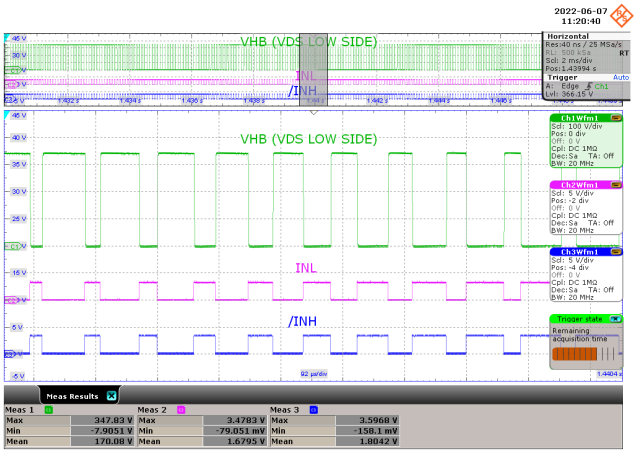


Figure 21 – INL and /INH Signal at Light Load.
CH1: V_{HB}, 100 V / div.
CH2: V_{INL}, 5 V / div.
CH3: V_{INH}, 5 V / div.
Time Scale: 2 ms / div.
Time Scale (Zoomed Area): 92 µs / div.

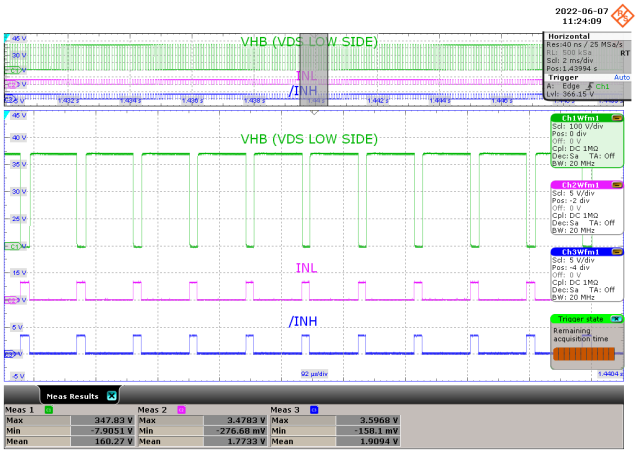


Figure 22 – INL and /INH Signal at 300 W Load.
CH1: V_{HB}, 100 V / div.
CH2: V_{INL}, 5 V / div.
CH3: V_{INH}, 5 V / div.
Time Scale: 2 ms / div.
Time Scale (Zoomed Area): 92 µs / div.

7.2.5 BPL and BPH during Steady-State

The waveforms below show the BPL and BPH (low-side and high-side self-supply bias level respectively) from light load to full load condition during steady-state operation.

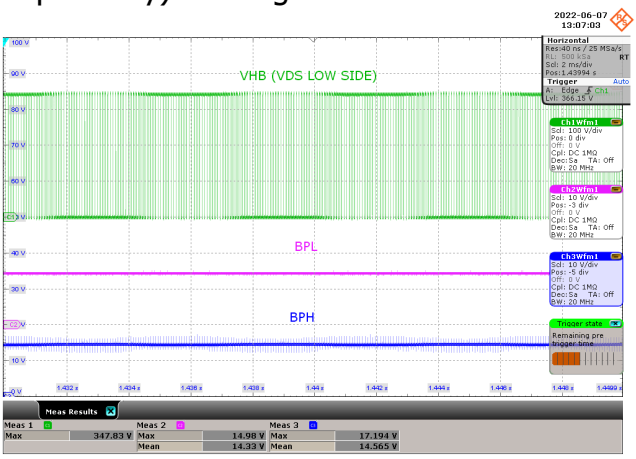


Figure 23 – BPL and BPH Signal at Light Load.
CH1: V_{HB}, 100 V / div.
CH2: V_{BPL}, 10 V / div.
CH3: V_{BPH}, 10 V / div.
Time Scale: 2 ms / div.
BPL Average Voltage = 14.33 V.
BPH Average Voltage = 14.56 V.

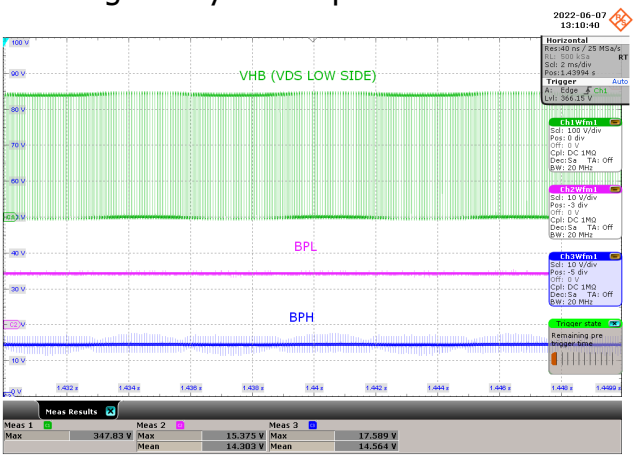


Figure 24 – BPL and BPH Signal at 300 W Load.
CH1: V_{HB}, 100 V / div.
CH2: V_{BPL}, 10 V / div.
CH3: V_{BPH}, 10 V / div.
Time Scale: 2 ms / div.
BPL Average Voltage = 14.30 V.
BPH Average Voltage = 14.56 V.

7.3 Thermal Performance

The thermal scans below depict on-board device thermal performance after 20 minutes each for 100 W, 200 W, and 300 W inverter output power running at a constant speed of 5000 RPM, 12 kHz PWM switching frequency, three-phase FOC modulation, BridgeSwitch device at self and external supply mode, with an average ambient temperature of 28 ºC measured three inches above the inverter board. An additional +17 VDC supply was used during external supply mode for the bypass pin supply. The inverter setup was enclosed in an acrylic case to minimize the effects of air flow on the thermal data.

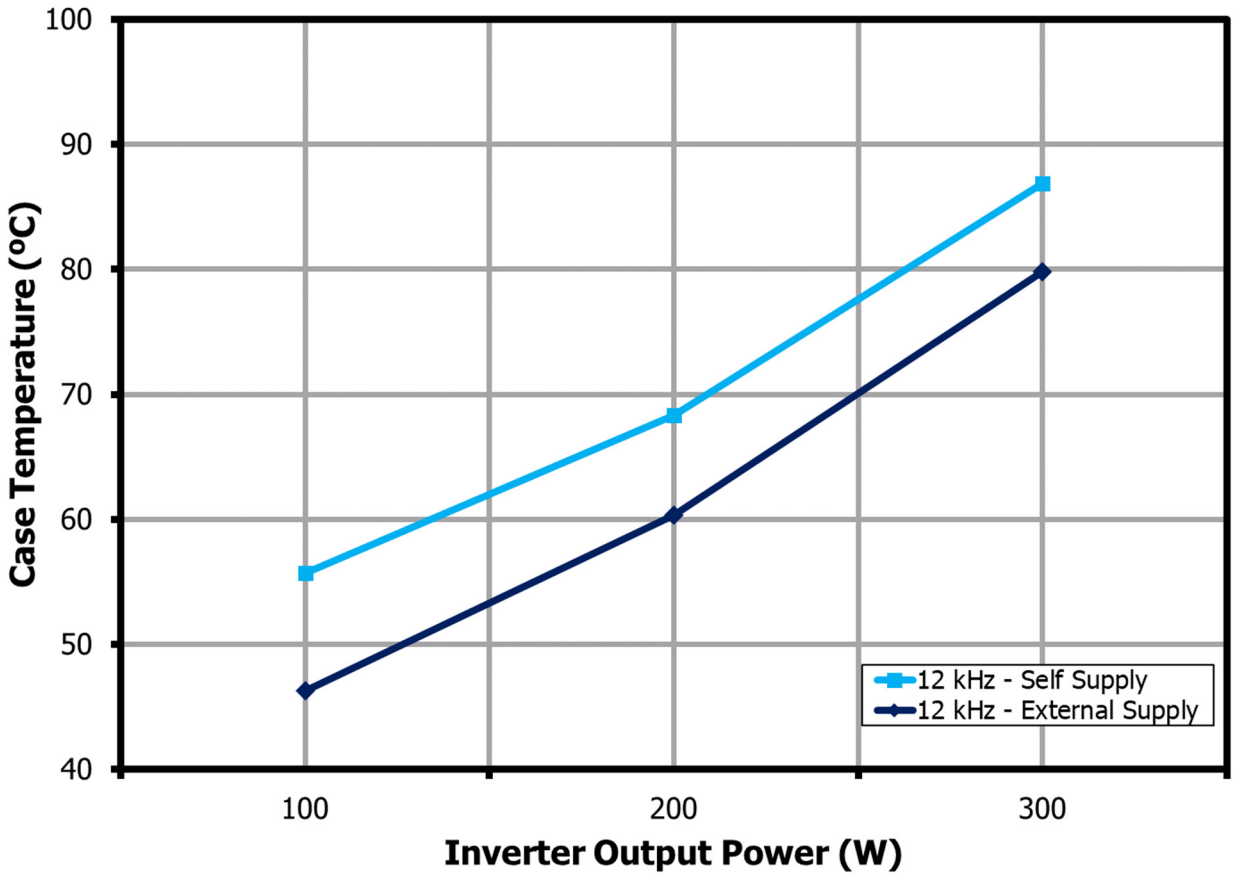


Figure 25 – Thermal Performance at Self and External Supply Mode.

7.3.1 100 W Loading Condition (340 mA Average Motor Phase Current)

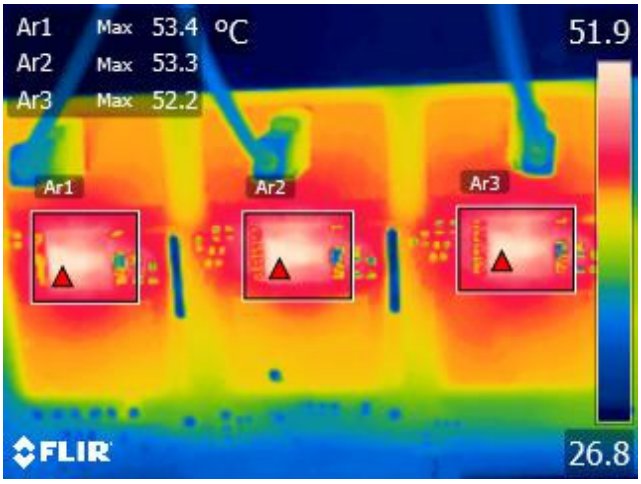


Figure 26 – BridgeSwitch Device Case Temperatures at 100 W Output Power (Self-Supply Mode).

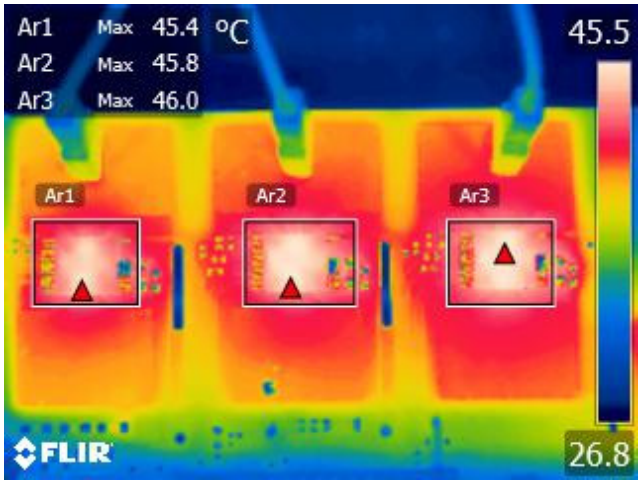


Figure 27 – BridgeSwitch Device Case Temperatures at 100 W Output Power (External Supply Mode).

7.3.2 200 W Loading Condition (670 mA Average Motor Phase Current)

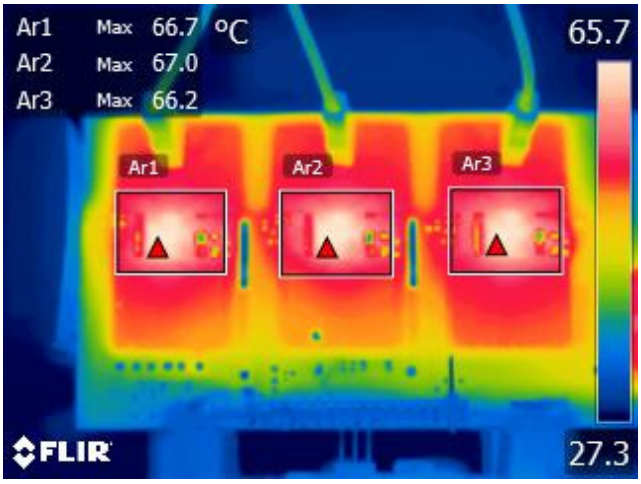


Figure 28 – BridgeSwitch Device Case Temperatures at 200 W Output Power (Self-Supply Mode).

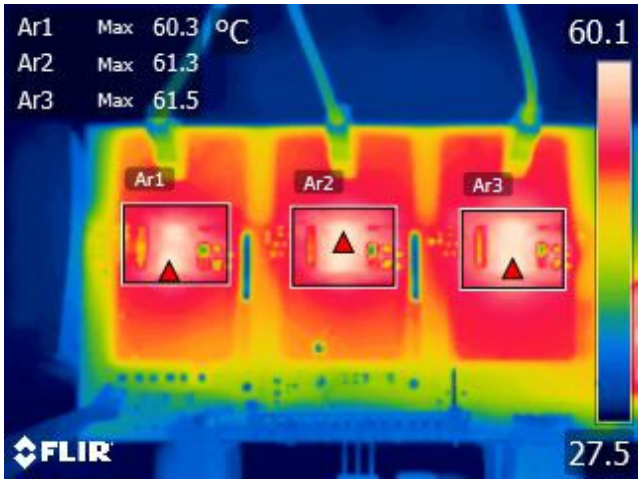


Figure 29 – BridgeSwitch Device Case Temperatures at 200 W Output Power (External Supply Mode).

7.3.3 300 W Loading Condition (930 mA Average Motor Phase Current)

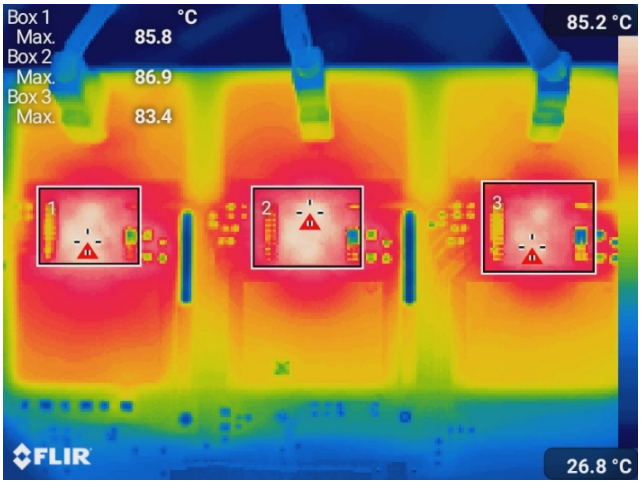


Figure 30 – BridgeSwitch Device Case Temperatures at 300 W Output Power (Self-Supply Mode).

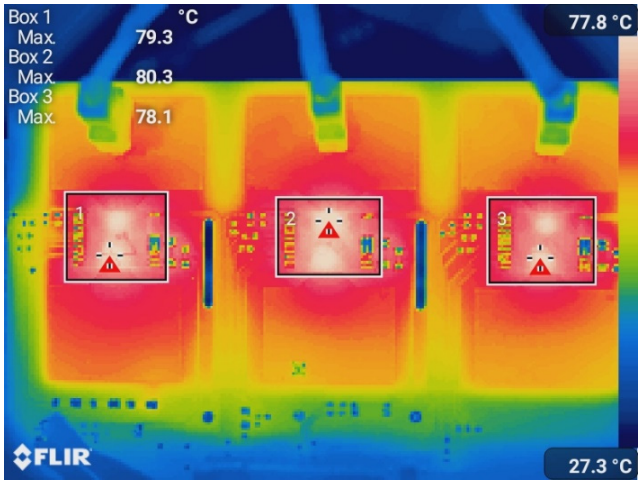


Figure 31 – BridgeSwitch Device Case Temperatures at 300 W Output Power (External Supply Mode).

7.3.4 Thermal Scan Summary Table

The tables below summarize the thermal measurement results collected at an average ambient temperature of 28 °C.

7.3.4.1 Self Supply Mode

Phase	Device	Inverter Output Power		
		100 W	200 W	300 W
U	U1	53.4	66.7	85.8
V	U2	53.3	67.0	86.9
W	U3	52.2	66.2	83.4
	Ave. Case Temp	**53.0**	**66.6**	**85.4**

7.3.4.2 External Supply Mode

Phase	Device	Inverter Output Power		
		100 W	200 W	300 W
U	U1	45.4	60.3	79.3
V	U2	45.8	61.3	80.3
W	U3	46.0	61.5	78.1
	Ave. Case Temp	**45.7**	**61.0**	**79.2**

7.4 No-Load Input Power Consumption

The graph below illustrates the BridgeSwitch three-phase inverter no-load input power measured at different input voltages. The voltage was measured directly at the positive input DC BUS of the inverter.

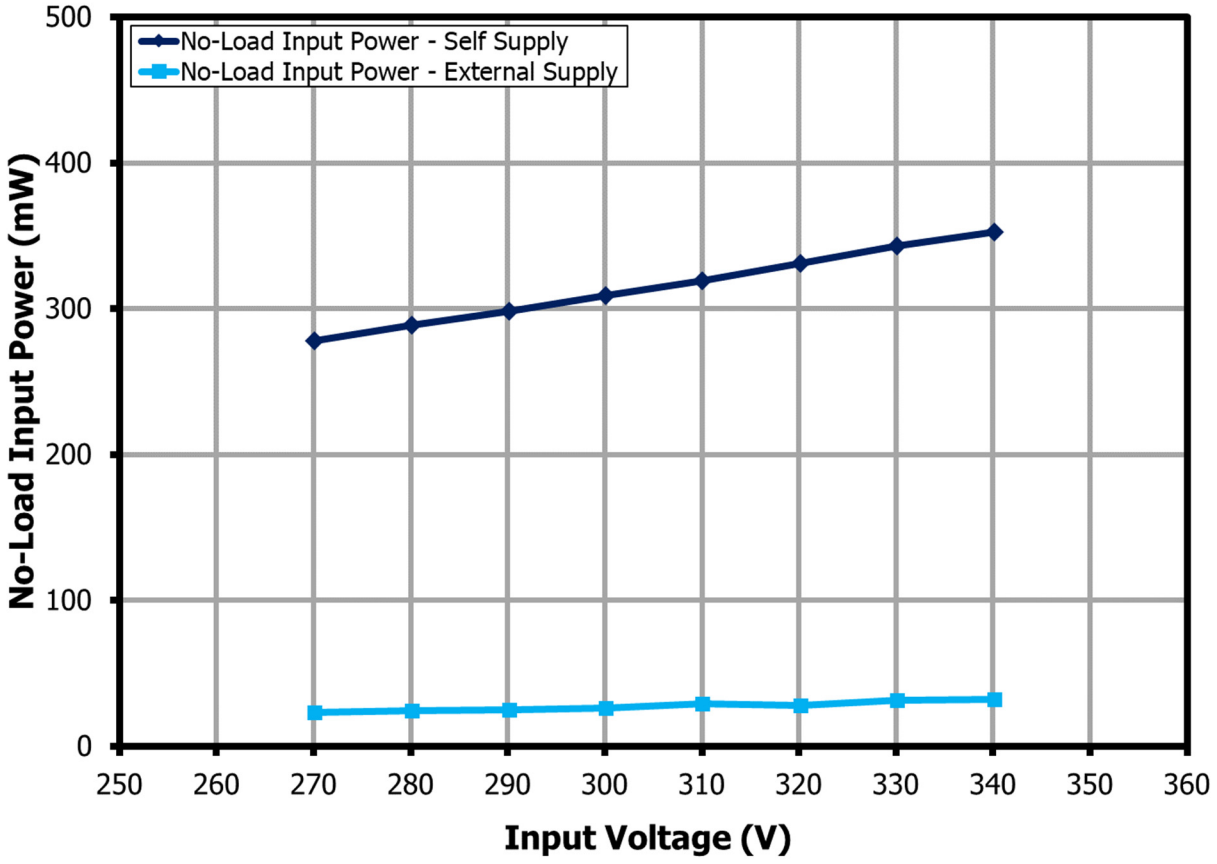


Figure 32 – No-Load Input Power.

7.5 Efficiency

The graph and table below displays the BridgeSwitch inverter efficiency at 340 VDC input, 12 kHz PWM switching frequency, a constant motor speed of 5000 RPM, three-phase FOC modulation, BridgeSwitch devices at self and external supply mode, and at an average ambient temperature of 28 °C. The auxiliary circuit was disabled for efficiency data accuracy. This was accomplished by measuring the input voltage directly at the positive input DC BUS of the inverter. An additional +17 VDC supply was used during external supply mode for the bypass pin supply.

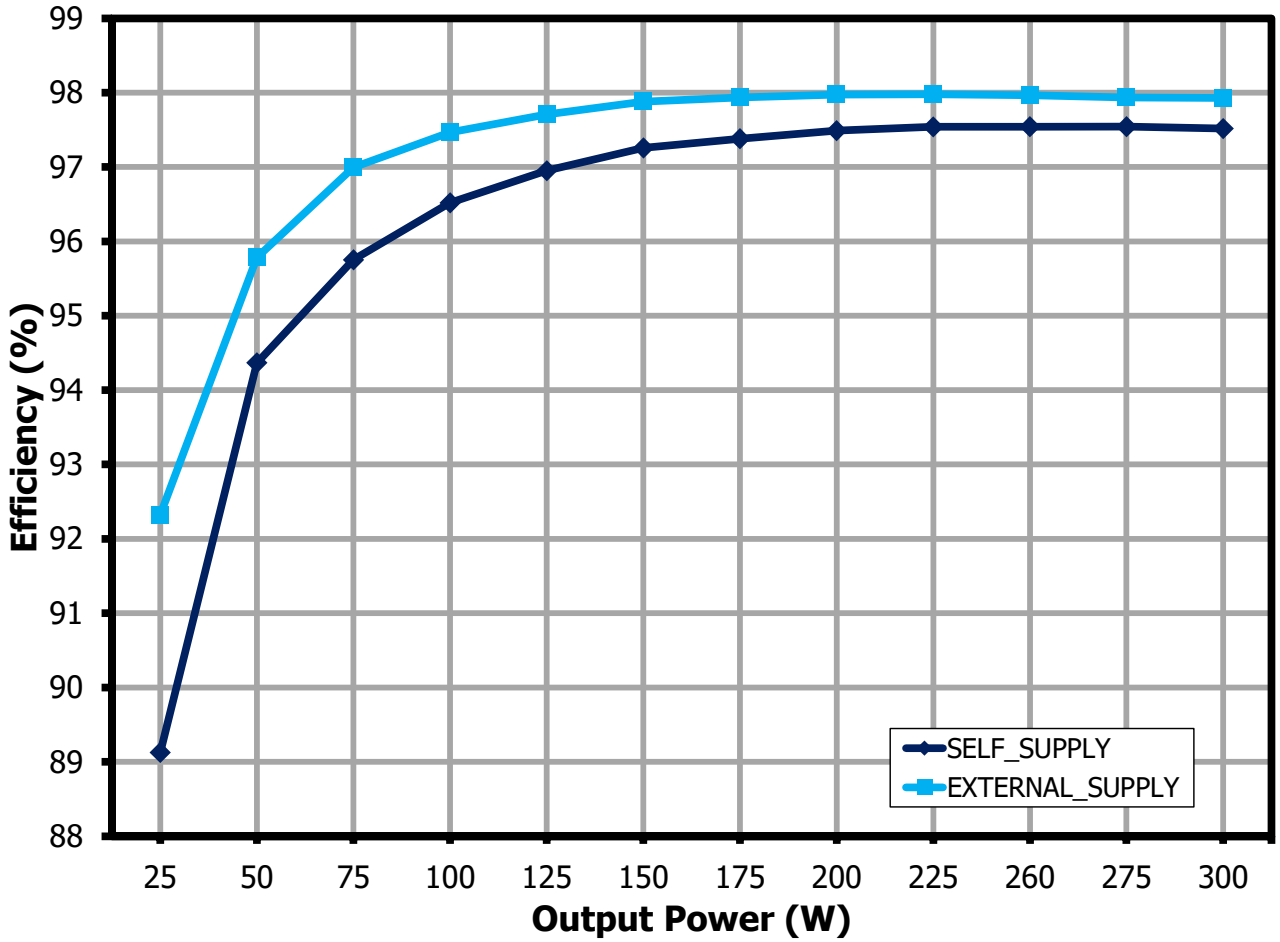


Figure 33 – Inverter Efficiency Graph.

7.5.1 Efficiency Table at Self Supply Mode

DC Input Voltage (V_{IN})	Input DC Current (mA)	Input Power (W)	$I_{RMS}U$ (mA)	$I_{RMS}V$ (mA)	$I_{RMS}W$ (mA)	Inverter Output Power (W)	Inverter Efficiency (%)
340	256	29.70	91	96	101	26.47	89.13
340	293	57.93	171	178	181	54.67	94.37
340	335	80.56	239	248	252	77.14	95.75
340	391	105.76	315	327	332	102.08	96.52
340	453	131.30	388	407	411	127.30	96.95
340	537	163.89	485	504	508	159.40	97.26
340	591	184.18	547	563	568	179.36	97.38
340	660	209.59	621	636	642	204.30	97.49
340	724	233.06	686	700	708	227.32	97.54
340	795	257.69	766	778	787	251.36	97.54
340	866	283.02	839	853	864	276.07	97.54
340	944	310.53	919	929	950	302.83	97.52

Table 2 – Efficiency Table (Self-Supply Mode).

7.5.2 Efficiency Table at External Supply Mode

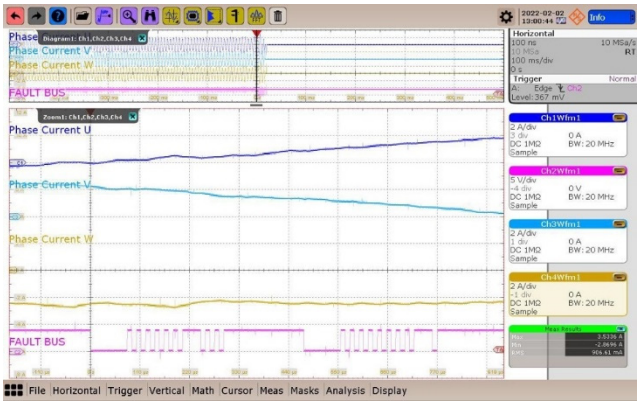
DC Input Voltage (V_{IN})	Input DC Current (mA)	Input Power (W)	$I_{RMS}U$ (mA)	$I_{RMS}V$ (mA)	$I_{RMS}W$ (mA)	Inverter Output Power (W)	Inverter Efficiency (%)
340	127	29.70	96	101	101	26.64	92.32
340	183	57.93	155	170	177	50.85	95.78
340	252	80.56	237	251	253	77.09	97.00
340	320	105.76	313	327	331	101.29	97.47
340	385	131.30	379	398	402	123.97	97.71
340	478	163.89	475	495	498	155.98	97.88
340	537	184.18	538	555	559	176.00	97.94
340	623	209.59	627	642	644	205.04	97.98
340	691	233.06	698	710	715	228.17	97.98
340	764	257.69	773	783	788	252.67	97.97
340	844	283.02	852	861	866	279.19	97.93
340	907	310.53	908	916	923	300.37	97.93

Table 3 – Efficiency Table (External Supply Mode).

7.6 Device and System Level Protection / Monitoring

7.6.1 Overcurrent Protection (OCP)

The waveforms below depict the current limit triggering of the BridgeSwitch device. For this test, the current set resistors R_{XL} and R_{XH} were set to 44.2 kΩ resulting in a current limit of approximately 3 A.



LS FET OCP FAULT DEVICE READY

Figure 34 – OCP and OCP Fault Clear ar R_{XL}/R_{XH} = 44.2 kO, I_{LIM} = 3 A.

CH1: $I_{PHASE}U$, 2 A / div.
CH3: $I_{PHASE}V$, 2 A / div.
CH4: $I_{PHASE}W$, 2 A / div.
CH2: VFAULT, 5 V / div.
Time Scale: 100 ms / div.
Time Scale (Zoomed Area): 100 μs / div. FAULT Flag Reading = 0000010.
Decoded FAULT = LS FET OCP.

CH1: $I_{PHASE}U$, 2 A / div.
CH3: $I_{PHASE}V$, 2 A / div.
CH4: $I_{PHASE}W$, 2 A / div.
CH2: VFAULT, 5 V / div.
Time Scale: 100 ms / div.
Time Scale (Zoomed Area): 100 μs / div. FAULT Flag Reading = 0000000.
Decoded FAULT = DEVICE READY.

7.6.2 Thermal Warning

The waveforms below depict the low-side FREDFET over-temperature warning. A localized external heat source was applied to the device to force temperature rise.

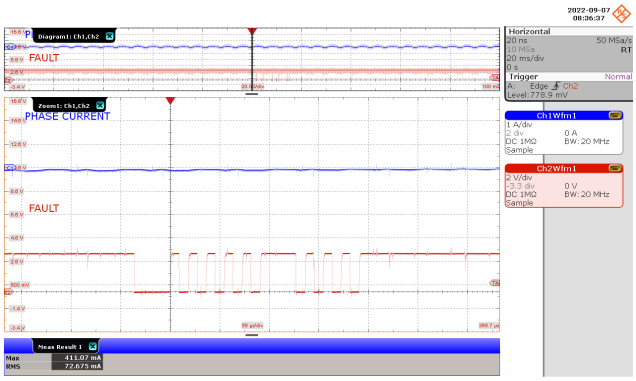


Figure 35 – Thermal Warning at Light Load.

CH1: I_{PHASE}, 1 A / div.
CH2: V_{FAULT}, 2 V / div.
Time Scale: 20 ms / div.
Time Scale (Zoomed Area): 55 µs / div. FAULT Flag/Reading = 00001**0**0.
Decoded FAULT = LS FET THERM. WARNING.

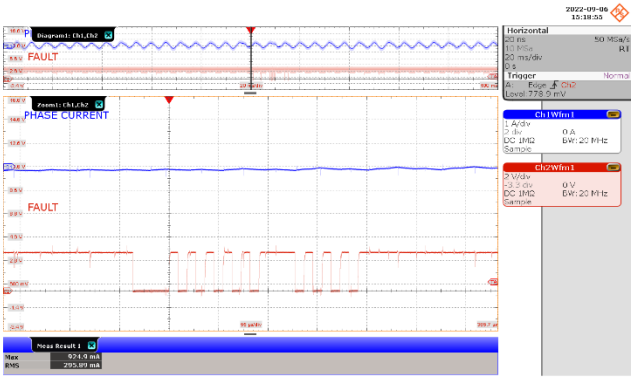


Figure 36 – Thermal Warning at 100 W.

CH1: I_{PHASE}, 1 A / div.
CH2: V_{FAULT}, 2 V / div.
Time Scale: 20 ms / div.
Time Scale (Zoomed Area): 55 µs / div. FAULT Flag/Reading = 00001**0**0.
Decoded FAULT = LS FET THERM. WARNING.

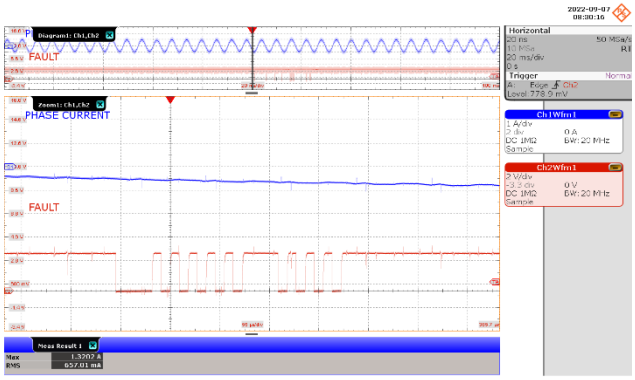


Figure 37 – Thermal Warning at 200 W.

CH1: I_{PHASE}, 1 A / div.
CH2: V_{FAULT}, 2 V / div.
Time Scale: 20 ms / div.
Time Scale (Zoomed Area): 55 µs / div. FAULT Flag/Reading = 00001**0**0.
Decoded FAULT = LS FET THERM. WARNING

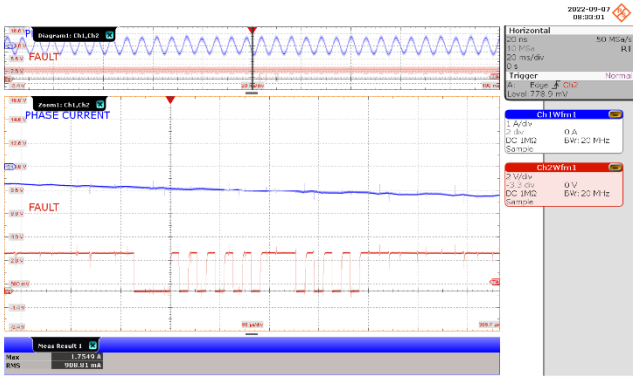


Figure 38 – Thermal Warning at 300 W.

CH1: I_{PHASE}, 1 A / div.
CH2: V_{FAULT}, 2 V / div.
Time Scale: 20 ms / div.
Time Scale (Zoomed Area): 55 µs / div. FAULT Flag/Reading = 00001**0**0.
Decoded FAULT = LS FET THERM. WARNING.

7.6.3 Thermal Shutdown

The waveform below depicts the low-side FREDFET over-temperature shutdown. A localized external heat source was applied to a single BridgeSwitch device (U1) to force temperature rise while the inverter is running at 100 W loading condition.

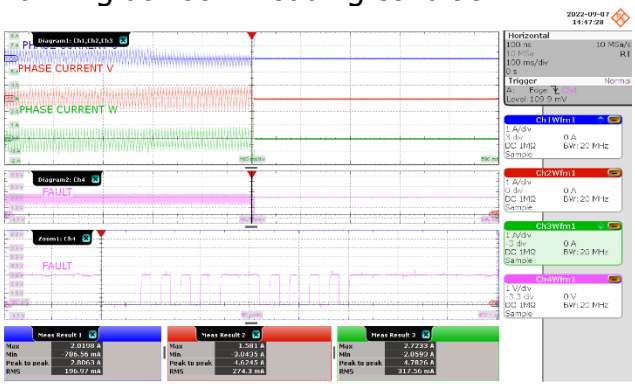


Figure 39 – Thermal Shutdown.

CH1: $I_{PHASE}U$, 1 A / div.
CH2: $I_{PHASE}V$, 1 A / div.
CH3: $I_{PHASE}W$, 1 A / div.
CH4: V_{FAULT}, 1 V / div.
Time Scale: 100 ms / div.
Time Scale (Zoomed Area): 50 μs / div.
FAULT Flag/Reading = 0001000.
Decoded FAULT = LS FET THERM. SHUTDOWN

7.6.4 Undervoltage (UV)

The test results below demonstrate the integrated bus UV monitoring function and status reporting through the communication bus (FAULT pin). Device U1 senses the bus voltage through resistors R24, R26, and R29. Switching resumes after the bus voltage level drops below the OV detection threshold.

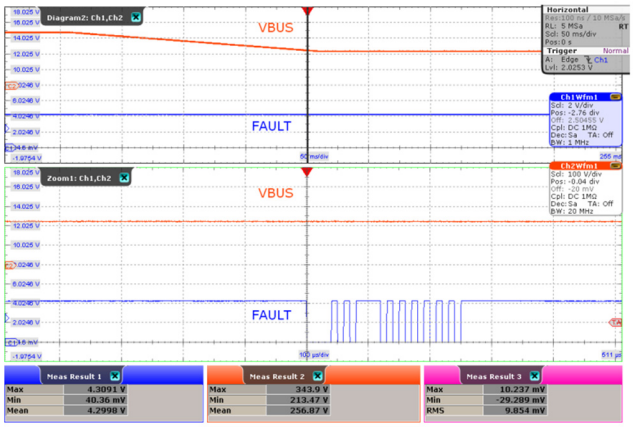


Figure 40 – UVP, 5000 RPM, No-Load, 340 V to 220V.

CH2: V_{BUS}, 100 V / div.
CH1: V_{FAULT}, 2 V / div.
Time Scale: 50 ms / div.
Time Scale (Zoomed Area): 100 µs / div.
Voltage Slew Rate = 0.5 V / msec.
UV Level = 100%.
FAULT Flag Reading = 0100000.
Decoded FAULT = HV bus UV 100%.

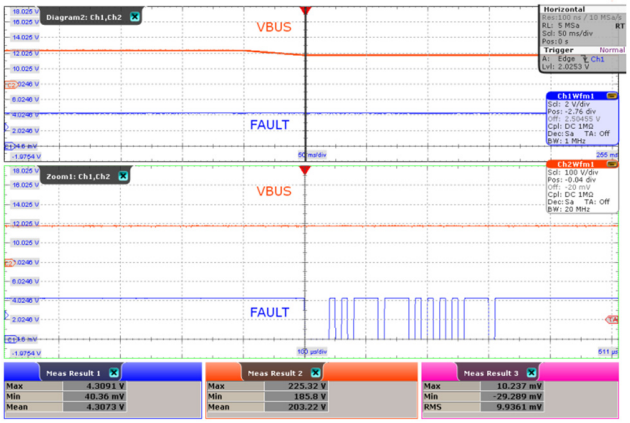


Figure 41 – UVP, 5000 RPM, No-Load, 220 V to 190 V.

CH2: V_{BUS}, 100 V / div.
CH1: V_{FAULT}, 2 V / div.
Time Scale: 50 ms / div.
Time Scale (Zoomed Area): 100 µs / div. Voltage Slew Rate = 0.5 V / msec.
UV Level = 85%.
FAULT Flag Reading = 0110000.
Decoded FAULT = HV bus UV 85%.

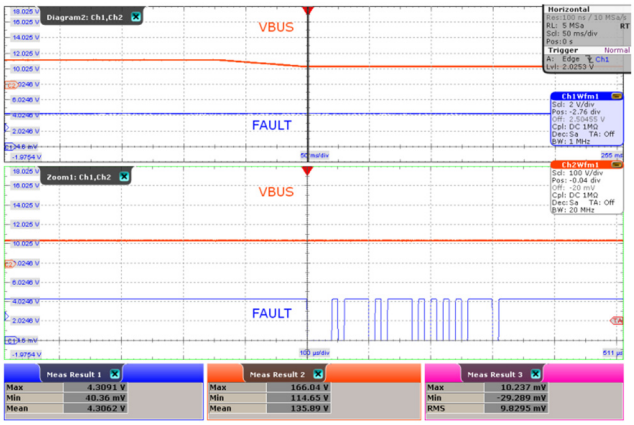


Figure 42 – UVP, 5000 RPM, No-Load, 190 V to 160 V.

CH2: V_{BUS}, 100 V / div.
CH1: V_{FAULT}, 2 V / div.
Time Scale: 50 ms / div.
Time Scale (Zoomed Area): 100 µs / div.
Voltage Slew Rate = 0.5 V / msec.
UV Level = 70%.
FAULT Flag Reading = 1000000.
Decoded FAULT = HV bus UV 70%.

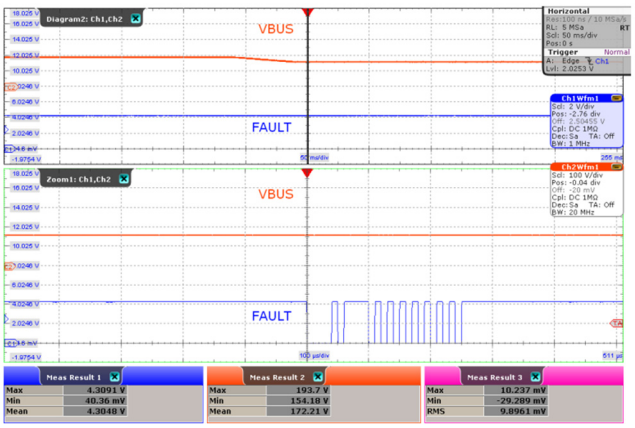


Figure 43 – UVP, 5000 RPM, No-Load, 160 V to 120 V.

CH2: V_{BUS}, 100 V / div.
CH1: V_{FAULT}, 2 V / div.
Time Scale: 50 ms / div.
Time Scale (Zoomed Area): 100 µs / div.
Voltage Slew Rate = 0.5 V / msec.
UV Level = 55%.
FAULT Flag Reading = 1010000.
Decoded FAULT = HV bus UV 55%.

7.6.5 Overvoltage (OV)

The waveforms below illustrate the bus OV monitoring feature. The bus sensing resistance is set at 7 MΩ (total value of R21, R22, and R23) giving an overvoltage (OV) level threshold of 422 VDC. The BridgeSwitch device stops switching and reports the OV fault condition as soon as the bus voltage exceeds the OV threshold.

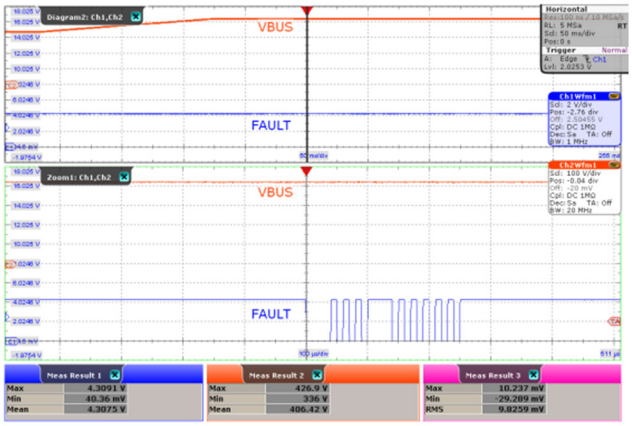


Figure 44 – OVP, 340 V to 425 V.

CH2: V_{BUS}, 100 V / div.
CH1: V_{FAULT}, 2 V / div.
Time Scale: 50 ms / div.
Time Scale (Zoomed Area): 100 µs / div.
Voltage Slew Rate = 0.5 V / msec.
Measured OVP Level = 426.90 V.
FAULT Flag/Reading = 0010000.
Decoded FAULT = HV bus OV.

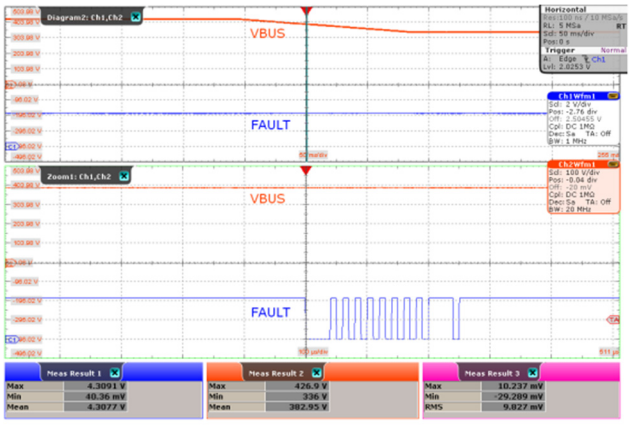


Figure 45 – OVP Clear, 425 V to 340 V.

CH2: V_{BUS}, 100 V / div.
CH1: V_{FAULT}, 2 V / div.
Time Scale: 50 ms / div.
Time Scale (Zoomed Area): 100 µs / div.
Voltage Slew Rate = 0.5 V / msec.
OV Fault Clear.
FAULT Flag/Reading = 0000000.
Decoded FAULT = OV FAULT Clear.

7.6.6 System Thermal Fault

The waveforms below show the system thermal warning flag of the BridgeSwitch device through an external thermistor RT1. The device checks the resistance connected to the SM pin every second for a period of 10 ms. The system temperature fault was simulated by applying a localized external heat to sense thermistor RT1 with the motor running at different loading conditions.

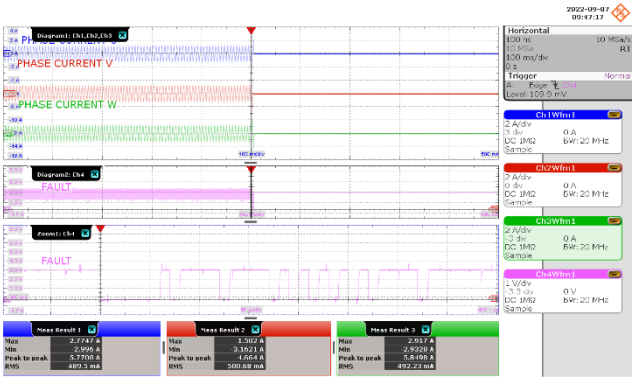


Figure 46 – System Thermal Fault, 5000 RPM, Light Load.

CH1: $I_{PHASE}U$, 1 A / div.
CH2: $I_{PHASE}V$, 1 A / div.
CH3: $I_{PHASE}W$, 1 A / div.
CH4: V_{FAULT}, 1 V / div.
Time Scale: 100 ms / div.
Time Scale (Zoomed Area): 50 µs / div.
FAULT Flag/Reading = 1101000.
Decoded FAULT = SYSTEM THERMAL FAULT.

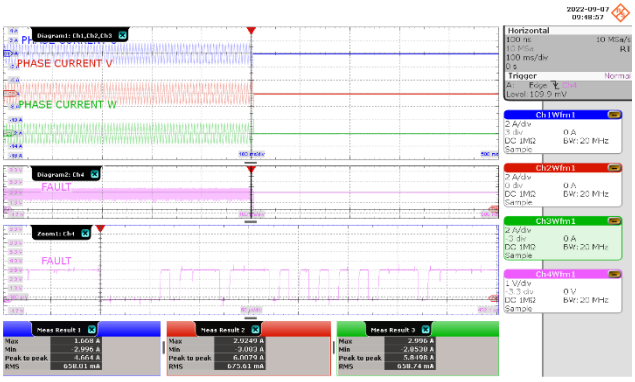


Figure 47 – System Thermal Fault, 5000 RPM, 100 W.

CH1: $I_{PHASE}U$, 1 A / div.
CH2: $I_{PHASE}V$, 1 A / div.
CH3: $I_{PHASE}W$, 1 A / div.
CH4: V_{FAULT}, 1 V / div.
Time Scale: 100 ms / div.
Time Scale (Zoomed Area): 50 µs / div.
FAULT Flag/Reading = 1101000.
Decoded FAULT = SYSTEM THERMAL FAULT.

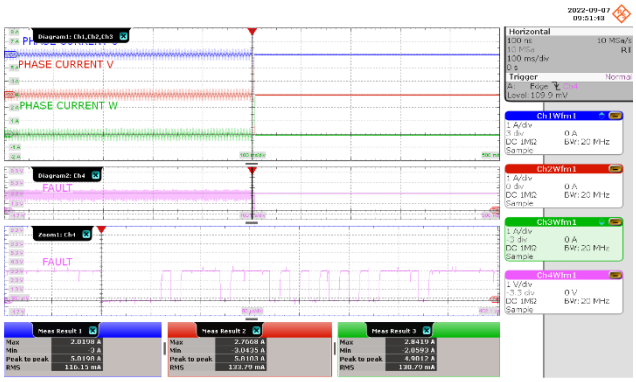


Figure 48 – System Thermal Fault, 5000 RPM, 200 W.

CH1: $I_{PHASE}U$, 1 A / div.
CH2: $I_{PHASE}V$, 1 A / div.
CH3: $I_{PHASE}W$, 1 A / div.
CH4: V_{FAULT}, 1 V / div.
Time Scale: 100 ms / div.
Time Scale (Zoomed Area): 50 µs / div.
FAULT Flag/Reading = 1101000.
Decoded FAULT = SYSTEM THERMAL FAULT.

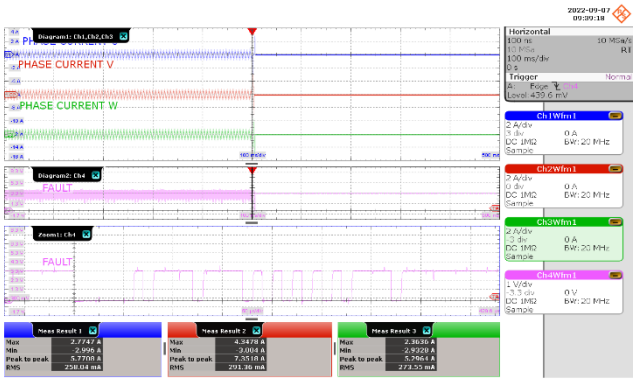


Figure 49 – System Thermal Fault, 5000 RPM, 300 W.

CH1: $I_{PHASE}U$, 1 A / div.
CH2: $I_{PHASE}V$, 1 A / div.
CH3: $I_{PHASE}W$, 1 A / div.
CH4: V_{FAULT}, 1 V / div.
Time Scale: 100 ms / div.
Time Scale (Zoomed Area): 50 µs / div.
FAULT Flag/Reading = 1101000.
Decoded FAULT = SYSTEM THERMAL FAULT.

7.7 Abnormal Motor Operation Test

This paragraph provides results during abnormal operation tests for appliances with motors as described in IEC 60335-1 (Safety of household and similar electrical appliances). The test includes:

- Operation under stalled motor conditions
- Operation with one motor winding disconnected
- Running overload test

The test results demonstrate the integrated protection features of the BridgeSwitch under such abnormal operations.

7.7.1 Operation Under Stalled (Motor) Conditions

For the motor stalled condition, the inverter is initially running at 340 VDC, 200 W and 300 W output load, and a motor speed of 5000 RPM. The load was then ramped up drastically to simulate sudden brake or sudden stoppage of motor rotation.

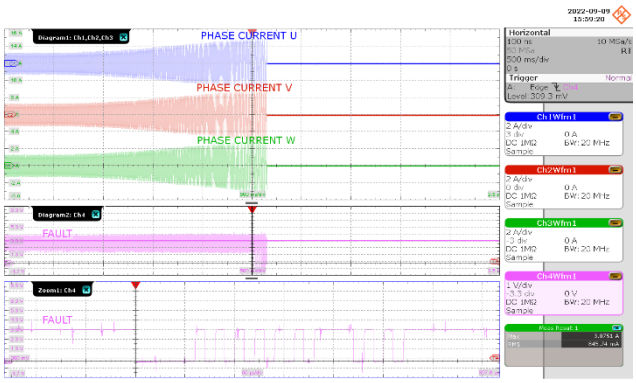


Figure 50 – At stalled condition, 200W Load
CH1: IPHASE, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
CH4: Hall Sensor, 5V / div.
Time Scale: 500 ms / div.
Time Scale (Zoomed): 50 μs / div.
1st FAULT = 0000010,
Decoded FAULT = LS FET OCP.

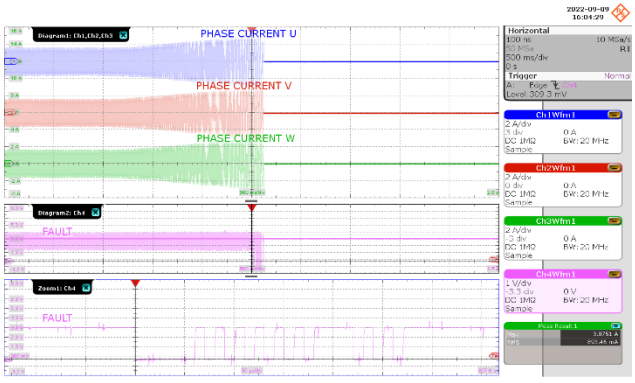


Figure 51 – At stalled condition, 300W Load
CH1: IPHASE, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
CH4: Hall Sensor, 5V / div.
Time Scale: 500 ms / div.
Time Scale (Zoomed): 50 μs / div.
1st FAULT = 0000010,
Decoded FAULT = LS FET OCP.

7.7.2 Operation with One Motor Phase / Winding Disconnected

The figures below depict the motor phase currents and fault flag during operation with one motor winding disconnected. One phase is disconnected during running condition at 200 W and 300 W load (at 340 VDC input, and a motor speed of 5000 RPM). Reconnection of phase was also tested per loading condition to determine the robustness of the BridgeSwitch inverter. No damage was incurred in the motor, as well as in the BridgeSwitch inverter during and after the test.

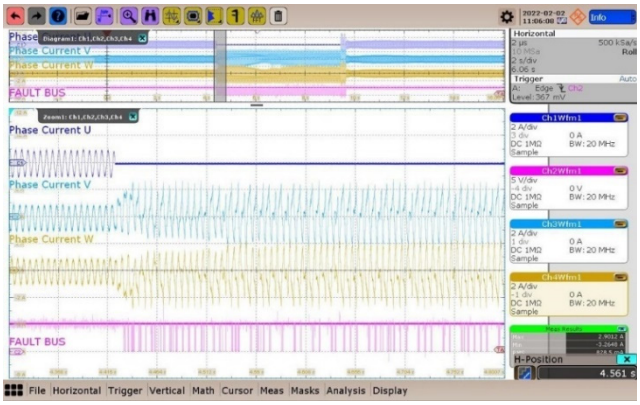


Figure 52 – One Phase Disconnected at 200W

CH1: $I_{PHASE}U$, 2 A / div.
CH3: $I_{PHASE}V$, 2 A / div.
CH4: $I_{PHASE}W$, 2 A / div.
CH2: V_{FAULT}, 5 V / div.
Time Scale: 2 s / div.
Time Scale (Zoomed): 50 ms / div.

Figure 53 – One Phase Reconnected at 200W

CH1: $I_{PHASE}U$, 2 A / div.
CH3: $I_{PHASE}V$, 2 A / div.
CH4: $I_{PHASE}W$, 2 A / div.
CH2: V_{FAULT}, 5 V / div.
Time Scale: 2 s / div.
Time Scale (Zoomed): 50 ms / div.

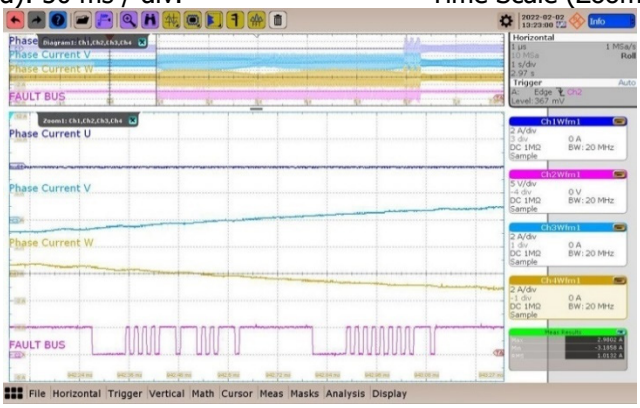


Figure 54 – FAULT Detail

CH1: $I_{PHASE}U$, 2 A / div.
CH3: $I_{PHASE}V$, 2 A / div.
CH4: $I_{PHASE}W$, 2 A / div.
CH2: V_{FAULT}, 5 V / div.
Time Scale: 2 s / div.
Time Scale (Zoomed FAULT): 100 µs / div.
FAULT Flag = 0001100
Decoded FAULT = HS DRIVER NOT READY.

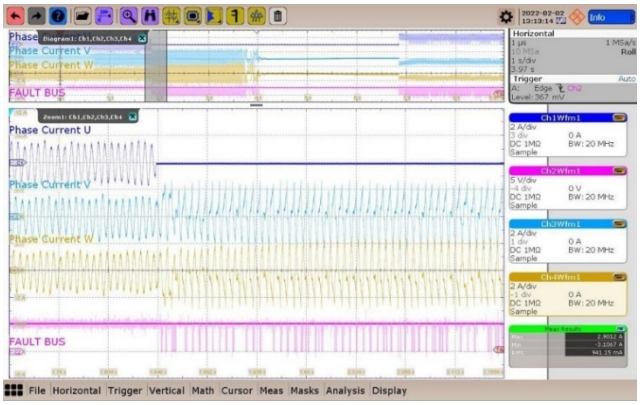


Figure 55 – One Phase Disconnected at 300W

CH1: $I_{PHASE}U$, 2 A / div.
CH3: $I_{PHASE}V$, 2 A / div.
CH4: $I_{PHASE}W$, 2 A / div.
CH2: V_{FAULT}, 5 V / div.
Time Scale: 2 s / div.
Time Scale (Zoomed): 50 ms / div.

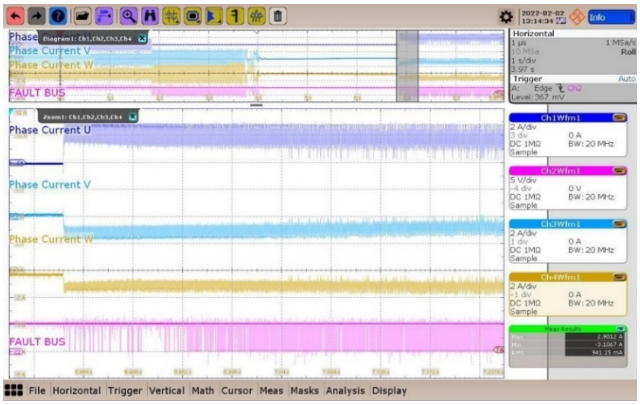


Figure 56 – One Phase Reconnected at 300W

CH1: $I_{PHASE}U$, 2 A / div.
CH3: $I_{PHASE}V$, 2 A / div.
CH4: $I_{PHASE}W$, 2 A / div.
CH2: V_{FAULT}, 5 V / div.
Time Scale: 2 s / div.
Time Scale (Zoomed): 50 ms / div.

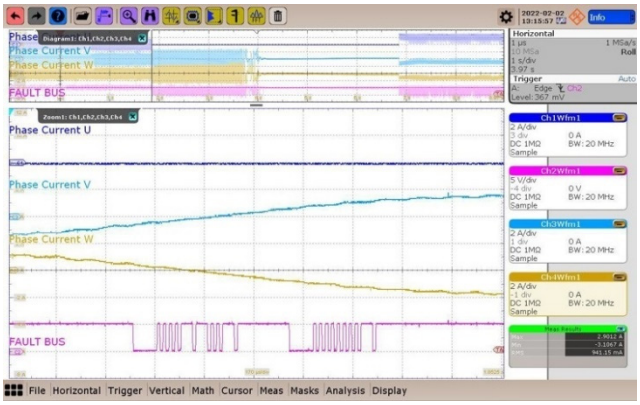


Figure 57 – FAULT Detail

CH1: $I_{PHASE}U$, 2 A / div.
CH3: $I_{PHASE}V$, 2 A / div.
CH4: $I_{PHASE}W$, 2 A / div.
CH2: V_{FAULT}, 5 V / div.
Time Scale: 2 s / div.
Time Scale (Zoomed): 100 µs / div.
FAULT Flag = 0001100
Decoded FAULT = HS DRIVER NOT READY.

7.7.3 Running Overload Test

The figures below depict the motor phase currents and status update flag during a running overload fault condition. During this test, the motor load is increased such that the current through the motor windings increases by 10% and until steady conditions are established. The load is then increased again and the test repeats until the BridgeSwitch protection engages or the motor stalls. During the overload condition, the motor is non-operational with no device or motor damage.

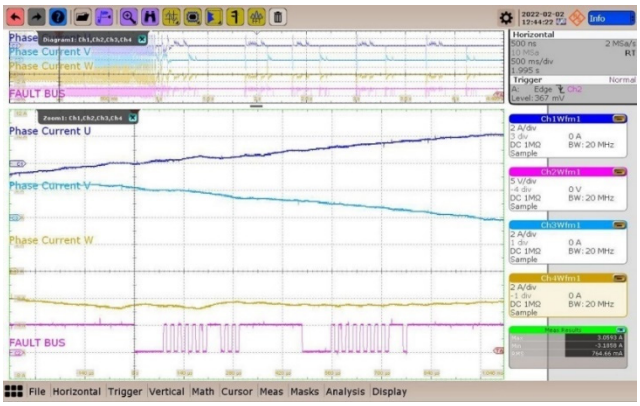


Figure 58 – Overload Test at Running Condition, 340 VDC Input

CH1: $I_{PHASE}U$, 2 A / div.
CH3: $I_{PHASE}V$, 2 A / div.
CH4: $I_{PHASE}W$, 2 A / div.
CH2: V_{FAULT}, 5 V / div.
Time Scale: 2 s / div.
Time Scale (Zoomed): 100 µs / div.
FAULT Flag = 0000010
Decoded FAULT = LS FET OCP.

Note: During overload condition, the motor stops rotating or remains in stalled condition.

8 Appendix

8.1 Board Quick Reference

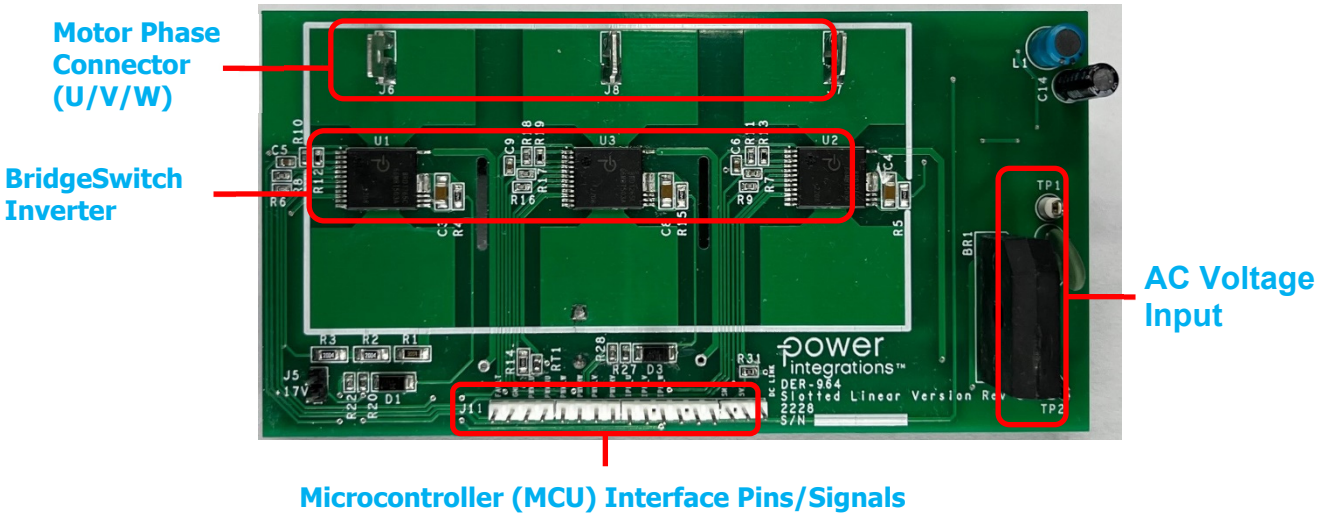


Figure 59 – RD-964 Board Quick Reference/Guide

8.1.1 The Microcontroller (MCU) Interface Contains the Following Pins/Signals

- **FAULT_BUS –** Pin dedicated for fault reporting of all BridgeSwitch devices.
- **GND –** Common ground interface between the microcontroller and the inverter board.
- **PWMH_U, PWML_U, PWMH_V, PWM_L_V, PWMH_W, PWML_W –** PWM input signal interface from the system microcontroller to the BridgeSwith device.
- **+5V –** Voltage supply pin for the FAULT BUS pull-up resistor (can be ignored MCU or controller has internal or external pull-up for FAULT BUS).
- **SM –** Configurable system monitoring pin for BridgeSwitch IC (U2).
- **IPH_U, IPH_V, IPH_W –** Instantaneous phase current information of the low-side-power FREDFET Drain-to-Source current of each BridgeSwitch device coming from the IPH pin.
- **DC_LINK –** DC bus voltage monitor for the microcontroller ADC input pin.

Note: On the RD board, proper labels for the pin designation of connectors are provided.

8.1.2 J1 Connector Pin Designation

Pin No.	Signal	Type	Comments
1	FAULT_BUS	Input/Output	Single wire, bi-directional fault communication bus.
2	GND	N/A	Ground reference for connector input and output signals.
3	PWMH_U	Input	Gate drive signal for high-side power FREDFET phase U.
4	PWML_U	Input	Gate drive signal for low-side power FREDFET phase U.
5	PWMH_W	Input	Gate drive signal for high-side power FREDFET phase W.
6	PWML_W	Input	Gate drive signal for low-side power FREDFET phase W.
7	PWMH_V	Input	Gate drive signal for high-side power FREDFET phase V.
8	PWML_V	Input	Gate drive signal for low-side power FREDFET phase V.
9	IPH_U	Output	Voltage signal proportional to the instantaneous phase low-side FREDFET Drain current of Phase U.
10	IPH_V	Output	Voltage signal proportional to the instantaneous phase low-side FREDFET Drain current of Phase V.
11	IPH_W	Output	Voltage signal proportional to the instantaneous phase low-side FREDFET Drain current of Phase W.
12	NC	N/A	Kept for backward compatibility.
13	NC	N/A	Kept for backward compatibility.
14	NC	N/A	Kept for backward compatibility.
15	SM	Input	External input for system sensing (i.e. can be connected to an external thermistor for system temperature monitor via status communication bus).
16	+5VDC	Input	Voltage supply pin for FAULT BUS pull-up resistor.
17	DC_LINK	Output	Voltage monitor pin for the microcontroller ADC pin.

Note: On the RD board, proper labels for the pin designation of connectors are provided.

8.2 Recommended Start-up Sequence

BridgeSwitch devices have internal self-supply supporting commutation PWM frequencies up to 20 kHz. To ensure sufficient supply voltage levels across the BPL pin capacitor and the BPH pin capacitor at inverter start-up, the system microcontroller (MCU) should follow the recommended power-up sequence as depicted below.

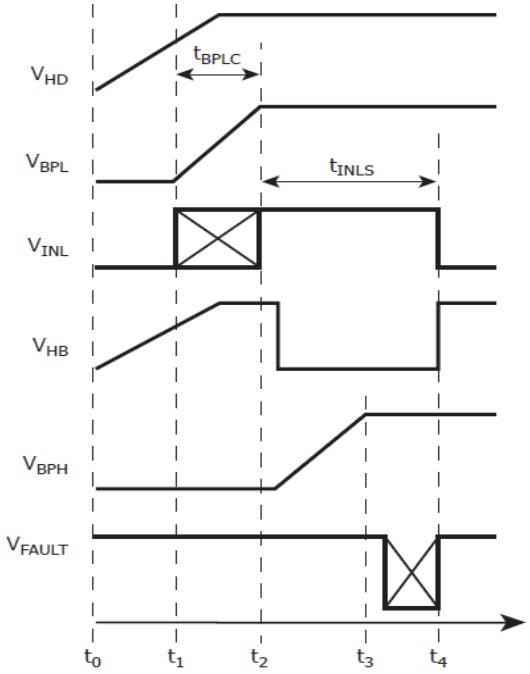


Figure 60 – Recommended Power-up Sequence with Self-Supplied Operation.

The table below lists activities occurring during the recommended power-up sequence.

Time Point	Activity
t_0	• High-voltage DC bus is applied
t_1	• Internal current source starts charging BPL pin capacitor once HD pin voltage reaches $V_{HD(START)}$ • System MCU may start setting low-side power-FREDFET control signal INL to high
t_2	• BPL pin voltage reaches V_{BPL} (typ. 14.5 V) • Device determines external device settings • Internal Gate drive logic turns on low-side power FREDFET after device setup completes and once INL becomes high or if it is already high • Internal current source charges BPH pin capacitor
t_3	• BPH pin voltage reaches V_{BPH} with respect to the HB pin (typically 14.5 V) • Device starts communicating successful power-up through fault pin Note: The device does not send a status update if the internal power-up sequence did not complete successfully
t_4	• BridgeSwitch is ready for state operation (indicated by communicated status update at time point t_3) • System MCU turns off low-side FREDFET

Table 4 – Power-up Sequence with Self-Supplied Operation.

8.3 Status Word Encoding

FAULT	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6
HV Bus OV	0	0	1				
HV Bus UV 100%	0	1	0				
HV Bus UV 85%	0	1	1				
HV Bus 70%	1	0	0				
HV Bus 55%	1	0	1				
System Thermal Fault	1	1	0				
LS Driver Not Ready	1	1	1				
LS FET Thermal Warning				0	1		
LS FET Thermal Shutdown				1	0		
HS Driver Not Ready				1	1		
LS FET Over-Current						1	
HS FET Over-Current							1
Device Ready (No Faults)	0	0	0	0	0	0	0

Notes:

1. Includes XL pin open-short circuit fault, IPH pin to XL pin short-circuit, and trim bit corruption
2. Includes HS-to-LS communication loss, V_{BPH} or internal 5 V rail out of range, and XH pin open/short-circuit fault

Table 5 – BridgeSwitch Fault Encoding.

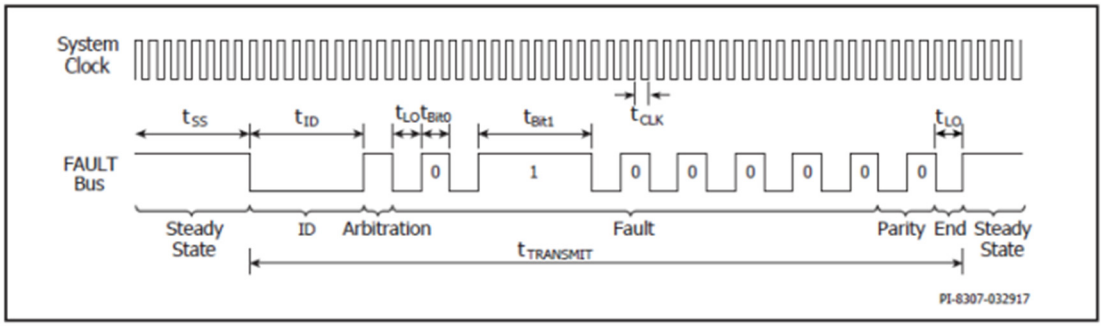


Figure 61 – Fault Status Communication Bit Stream.

8.4 Suggested Microcontroller Actions to BridgeSwitch Fault Conditions

Fault	Fault ID	Action/Decision
HV Bus Overvoltage	001xxxx	Shutdown
HV 100%	010xxxx	Warning
HV Bus 85%	011xxxx	Warning
HV Bus 70%	100xxxx	Warning
HV Bus 55%	101xxxx	Warning
System Thermal	110xxxx	Shutdown
LS Driver Not Ready	111xxxx	Shutdown
LS FET Thermal Warning	xxx010x	Warning
LS FET Thermal Shutdown	xxx10xx	Shutdown
LS FET Over-Current	xxxxx1x	Shutdown
HS Driver Not Ready	xxx11xx	Shutdown
HS FET Over-Current	xxxxxx1	Shutdown
Device Ready	0000000	None

8.5 Inverter Output Power Measurement

The three-phase inverter output power (P_{OUT}) measurement uses the "two-wattmeter" method as illustrated below.

$$P_{OUT} = P_{CH1} + P_{CH2}$$

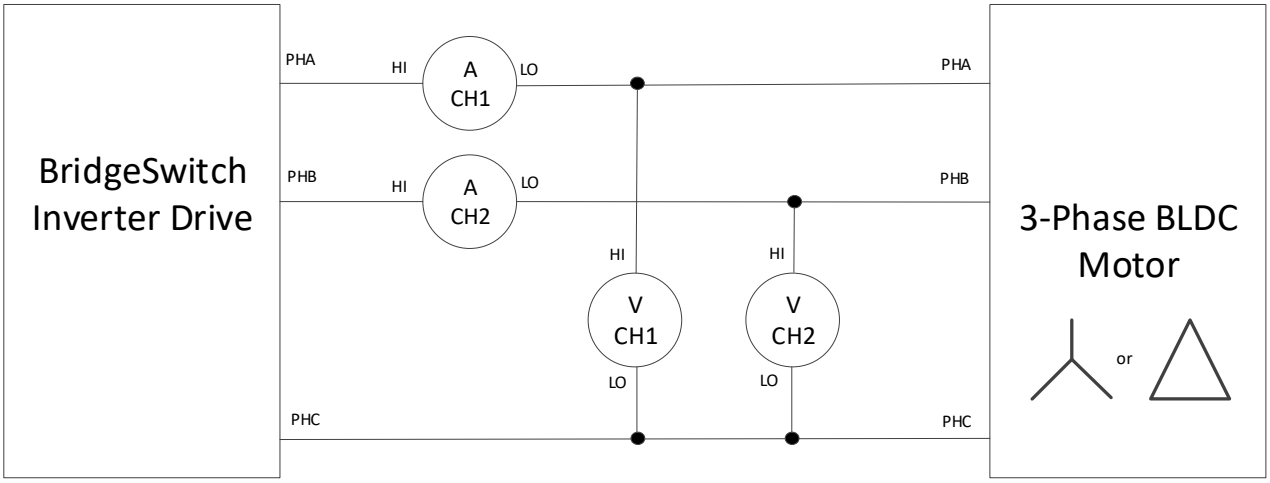


Figure 62 – Inverter Output Power Measurement.

8.6 Current Capability vs. Ambient Temperature

The figure below depicts the continuous RMS current capability of the RD-964 example design under different operation conditions: 5 kHz, 12 kHz, and 16 kHz PWM frequency and the three BRD1265C devices operating self-supplied or with external supply at their respective BPL and BPH pins. The DC bus voltage is 340 VDC and the motor is operating at a speed of 5000 RPM. The inverter board is enclosed in an acrylic case to minimize the effects of air flow to the thermal behavior of the BridgeSwitch devices. Each curve details the available continuous RMS current at different board ambient temperatures with a package temperature of 100 °C (average of all three devices).

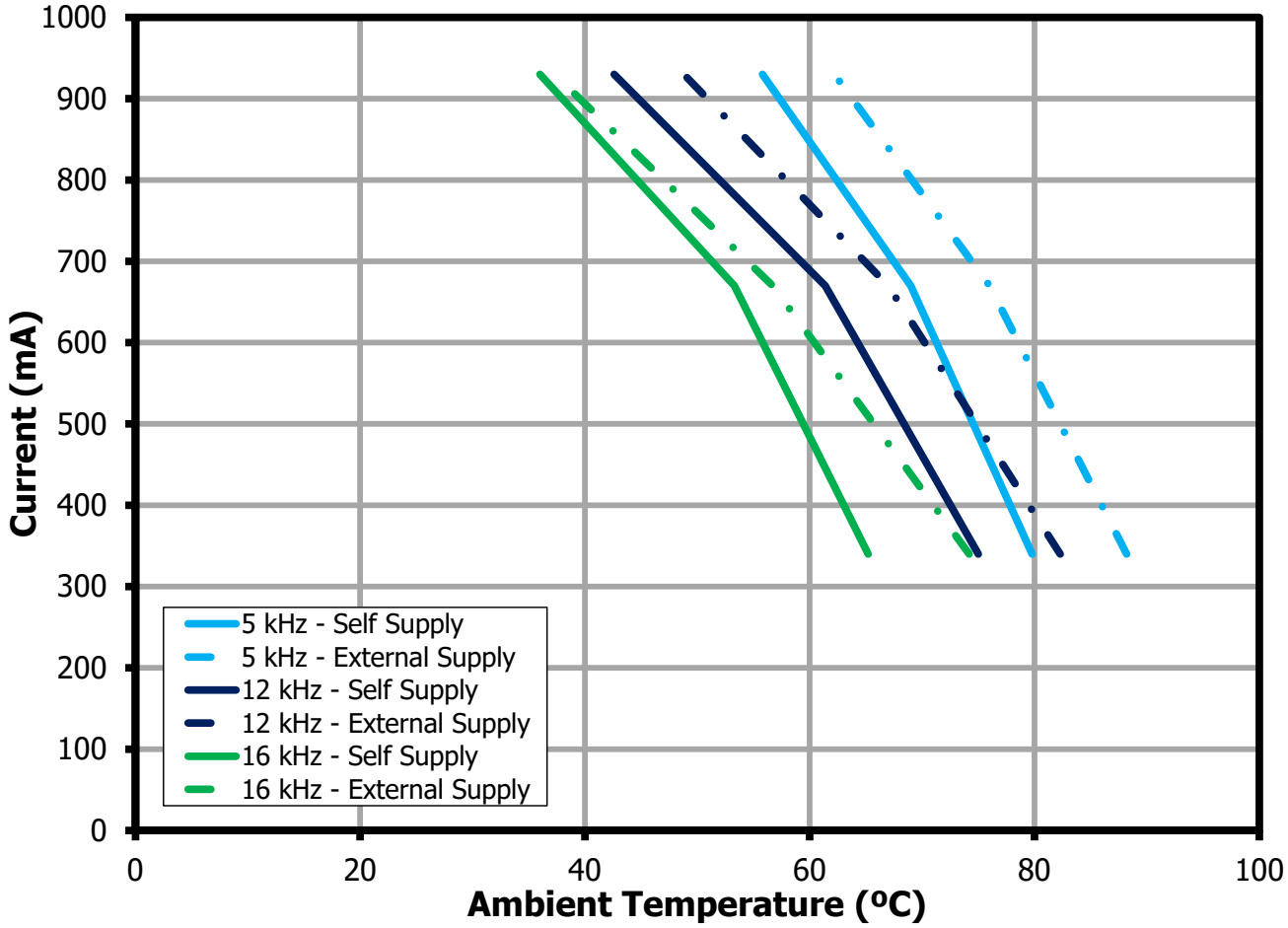


Figure 63 – Current Capability vs. Ambient Temperature (Max. 100 ºC Package Temperature)

8.7 Efficiency Curves at Different Switching Frequencies

The graph below shows the BridgeSwitch inverter efficiency at 340 VDC input, 5 kHz, 12 kHz, 16 kHz PWM switching frequencies, a constant motor speed of 5000 RPM, three-phase FOC modulation, BridgeSwitch devices at self and external supply mode, and at an average ambient temperature of 28 ºC. The bridge rectifier circuit, auxiliary power, and input diode were disabled for efficiency data accuracy. This was accomplished by measuring the input voltage directly at the positive input DC BUS of the inverter, and depopulating components BR1, F1, and RT2. An external +17 VDC supply was used during external supply mode for the bypass pin supply.

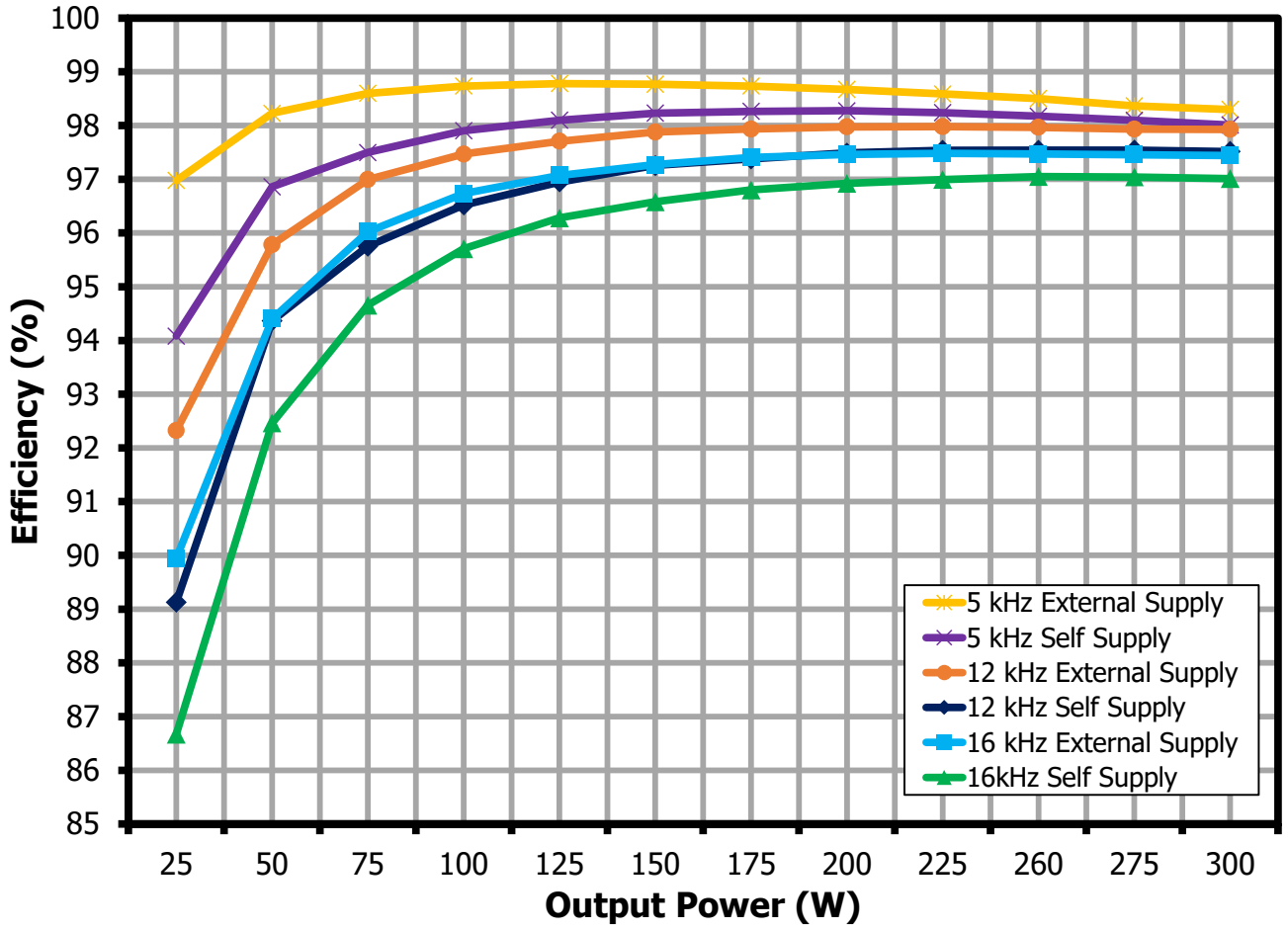


Figure 64 – Inverter Efficiency Graph.

8.8 Operation with One Motor Phase / Winding Disconnected (with FAULT BUS Processing)

Similar to 7.7.2, this section highlights an extra feature of the firmware to read and process the BridgeSwitch FAULT BUS pin. Depending on the type of fault, the firmware can be programmed to respond accordingly. These responses can be an ignore for low-level faults while a shutdown can be forced for critical statuses such as low-side FET over-current protection.

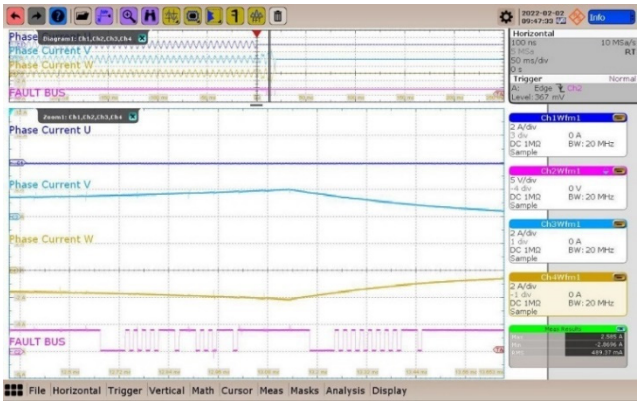


Figure 65 – One Phase Disconnected at 200 W.

CH1: $I_{PHASE}U$, 2 A / div.
CH3: $I_{PHASE}V$, 2 A / div.
CH4: $I_{PHASE}W$, 2 A / div.
CH2: V_{FAULT}, 5 V / div.
Time Scale: 50 ms / div.
Time Scale (Zoomed): 100 μs / div.
FAULT Flag = 0001100
Decoded FAULT = HS DRIVER NOT READY.

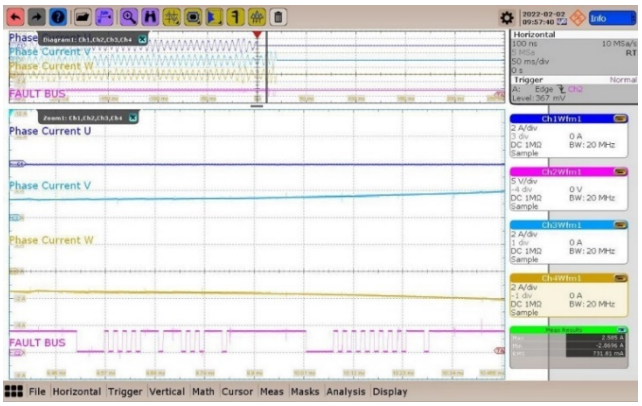


Figure 66 – One Phase Disconnected at 300 W.

CH1: $I_{PHASE}U$, 2 A / div.
CH3: $I_{PHASE}V$, 2 A / div.
CH4: $I_{PHASE}W$, 2 A / div.
CH2: V_{FAULT}, 5 V / div.
Time Scale: 50 ms / div.
Time Scale (Zoomed): 100 μs / div.
FAULT Flag = 0001100
Decoded FAULT = HS DRIVER NOT READY.

8.9 Running Overload Test (with FAULT BUS Processing)

As with Section 7.7.3, the overload run test was repeated with additional FAULT BUS processing by the firmware. Below is the oscilloscope capture of the phase currents at the overload event.

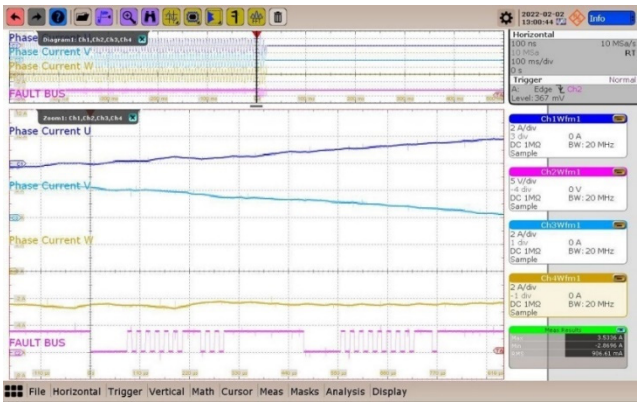


Figure 67 – Overload Test at Running Condition with FAULT BUS Processing, 340 VDC Input.

CH1: $I_{PHASE}U$, 2 A / div.
CH3: $I_{PHASE}V$, 2 A / div.
CH4: $I_{PHASE}W$, 2 A / div.
CH2: V_{FAULT}, 5 V / div.
Time Scale: 2 s / div.
Time Scale (Zoomed): 100 µs / div.
FAULT Flag = 0000010
Decoded FAULT = LS FET OCP.

8.10 Operation with Two Motor Phases / Windings Shorted

The figures below depict the motor phase currents and fault flag during operation with two motor windings shorted. The two phases are disconnected during running condition at 300 W load (at 340 VDC input, and a motor speed of 5000 RPM). For safety considerations, the phase short test was conducted only with the FAULT BUS processing* enabled. No damage was incurred in the motor, as well as in the BridgeSwitch inverter during and after the test.

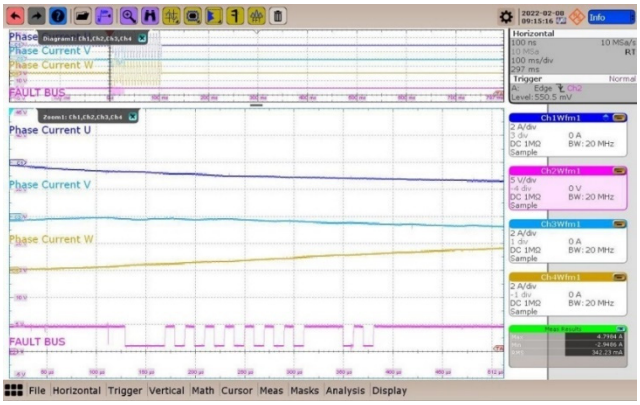


Figure 68 – Two Phases Shorted at 300 W.

CH1: $I_{PHASE}U$, 2 A / div.
CH3: $I_{PHASE}V$, 2 A / div.
CH4: $I_{PHASE}W$, 2 A / div.
CH2: V_{FAULT}, 5 V / div.
Time Scale: 2 s / div.
Time Scale (Zoomed): 100 µs / div.
FAULT Flag = 0000001
Decoded FAULT = HS FET OCP.

***Note:** Fault processing is done by the firmware by reading the status of the FAULT BUS.

8.11 Dynamic Loading Operation Test

The following waveforms show the system response to dynamic application of load. Power Integrations' current reconstruction firmware (FW) was tested under various loading conditions: 0-25, 0-50, 0-75, 0-100%, and vice versa. The loading condition is determined by the RMS phase current of the motor.

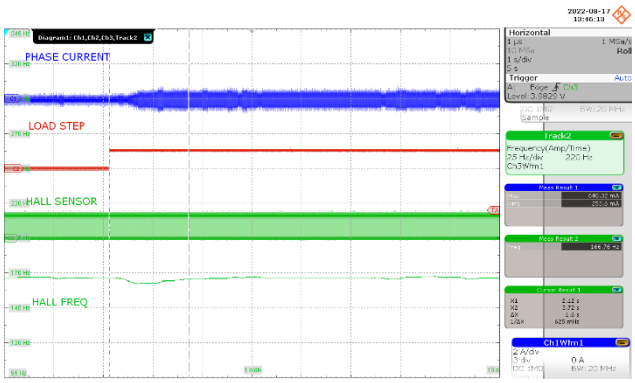


Figure 69 – 25% Load Application.

CH1: I_{PHASE}, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
T1: Hall Frequency Tracking.
Time Scale: 1 s / div.
Recovery Time: 1.6 seconds.

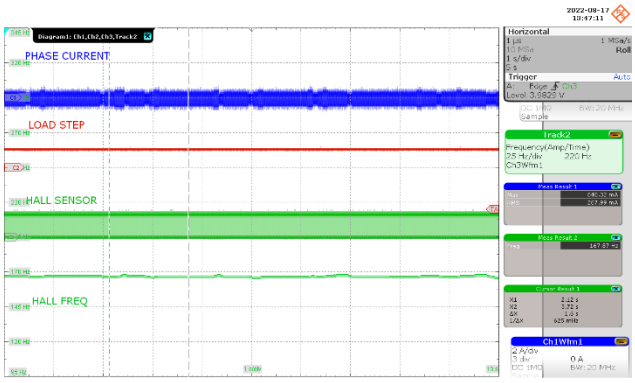


Figure 70 – 25% Load Steady-state.

CH1: I_{PHASE}, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
T1: Hall Frequency Tracking.
Time Scale: 1 s / div.
RMS Phase Current: 267 mA

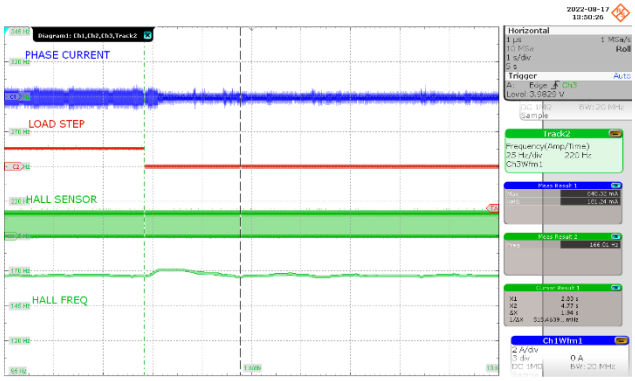


Figure 71 – 25% Load Removal.

CH1: I_{PHASE}, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
T1: Hall Frequency Tracking.
Time Scale: 1 s / div.
Recovery Time: 1.94 seconds.

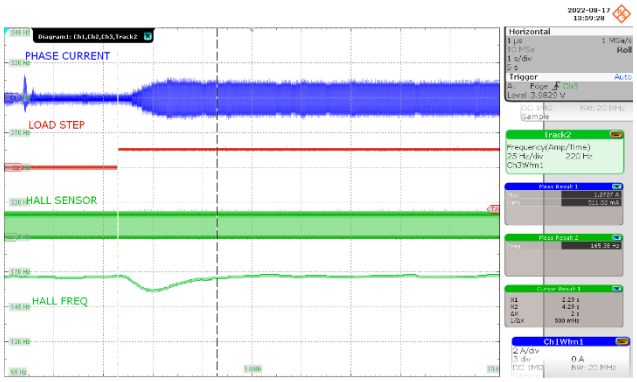


Figure 72 – 50% Load Application.

CH1: IPHASE, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
T1: Hall Frequency Tracking.
Time Scale: 1 s / div.
Recovery Time: 2 seconds.

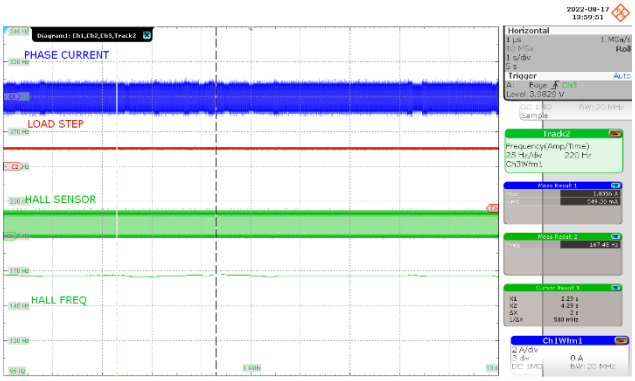


Figure 73 – 50% Load Steady-state.

CH1: IPHASE, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
T1: Hall Frequency Tracking.
Time Scale: 1 s / div.
RMS Phase Current: 549 mA.

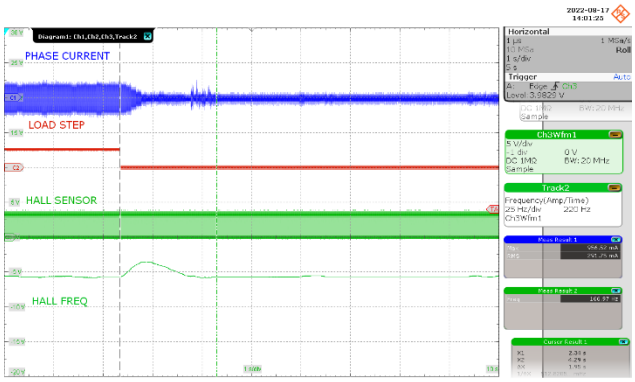


Figure 74 – 50% Load Removal.

CH1: IPHASE, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
T1: Hall Frequency Tracking.
Time Scale: 1 s / div.
Recovery Time: 1.95 seconds.

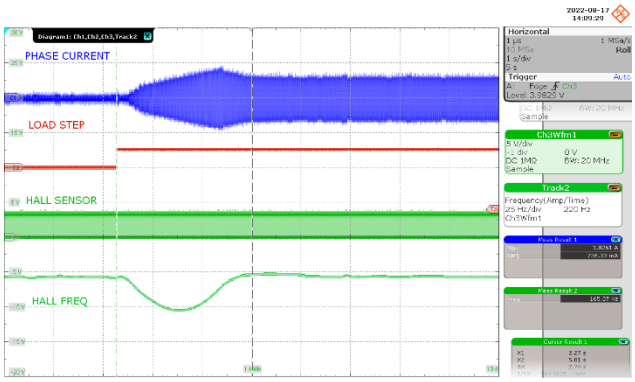


Figure 75 – 75% Load Application.

CH1: I_{PHASE}, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
T1: Hall Frequency Tracking.
Time Scale: 1 s / div.
Recovery Time: 2.74 seconds.

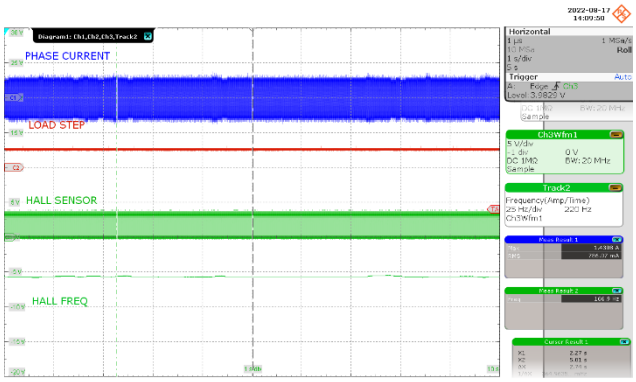


Figure 76 – 75% Load Steady-state.

CH1: I_{PHASE}, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
T1: Hall Frequency Tracking.
Time Scale: 1 s / div.
RMS Phase Current: 786 mA.

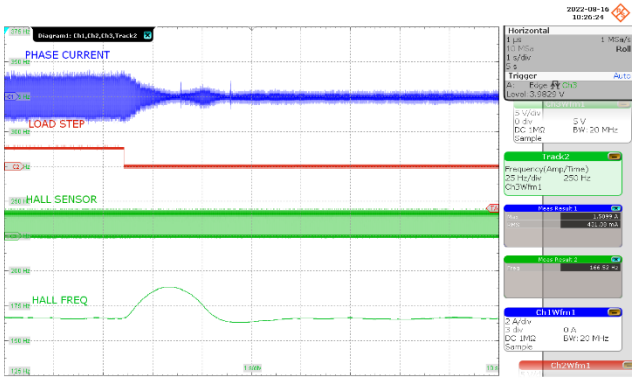


Figure 77 – 75% Load Removal.

CH1: I_{PHASE}, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
T1: Hall Frequency Tracking.
Time Scale: 1 s / div.
Recovery Time: 3.5 seconds.

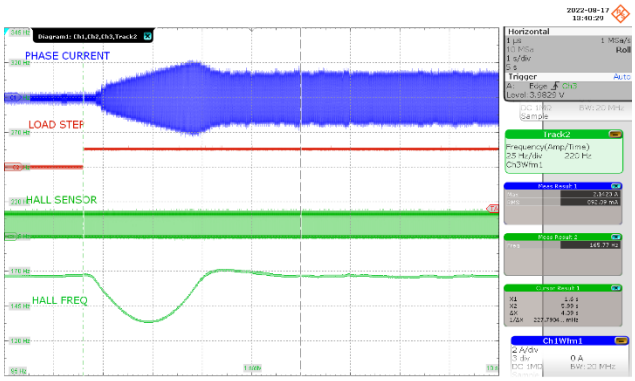


Figure 78 – 100% Load Application.

CH1: I_{PHASE}, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
T1: Hall Frequency Tracking
Time Scale: 1 s / div.
Recovery Time: 4.39 seconds.

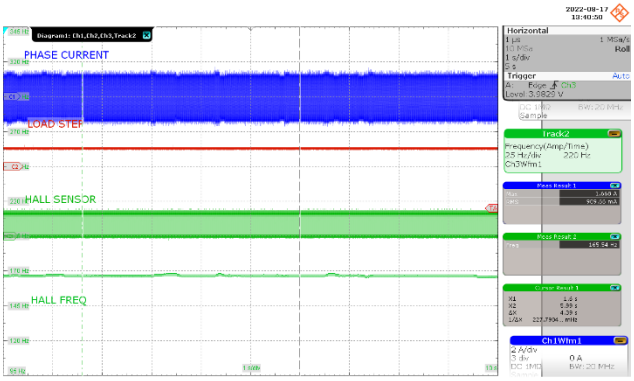


Figure 79 – 100% Load Steady-state.

CH1: I_{PHASE}, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
T1: Hall Frequency Tracking.
Time Scale: 1 s / div.
RMS Phase Current: 910 mA.

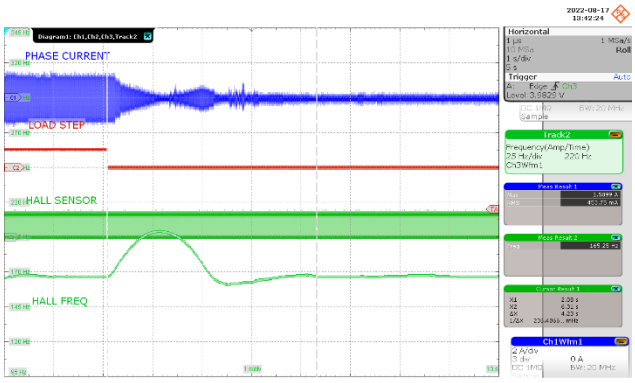


Figure 80 – 100% Load Removal.

CH1: I_{PHASE}, 2 A / div.
CH2: Load Step, 5 V / div.
CH3: Hall Sensor, 5V / div.
T1: Hall Frequency Tracking.
Time Scale: 1 s / div.
Recovery Time: 4.23 seconds.

8.12 Test Bench Set-up

This setup improves the accuracy of all thermal measurements. The inverter board is enclosed in an acrylic case to minimize the effects of air flow to the thermal behavior of the BridgeSwitch devices. A digital multimeter with a thermocouple probe placed three inches above the inverter board is used for ambient temperature monitoring.

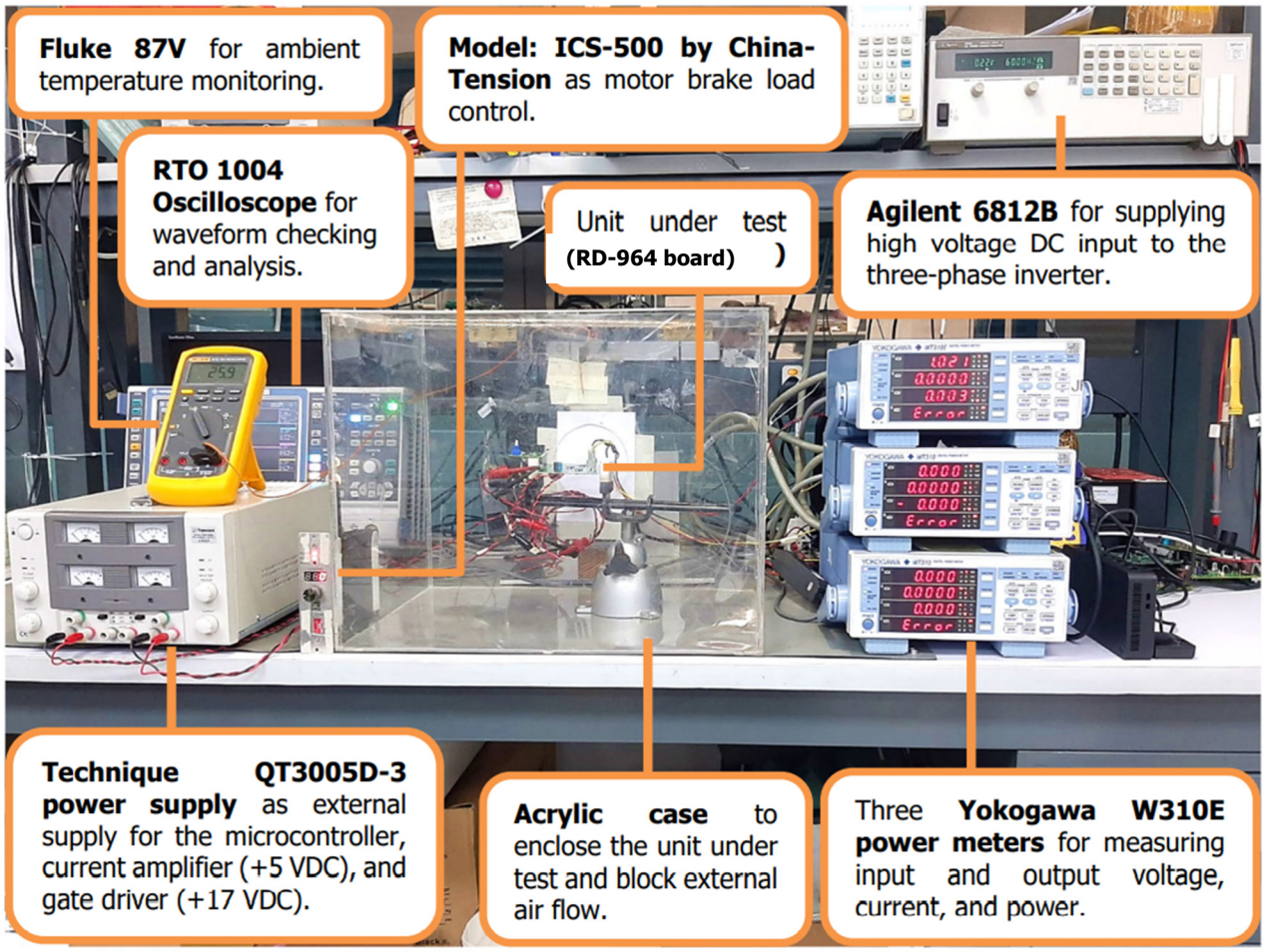


Figure 81 – Actual Bench Set-up for Thermal Performance Measurements.

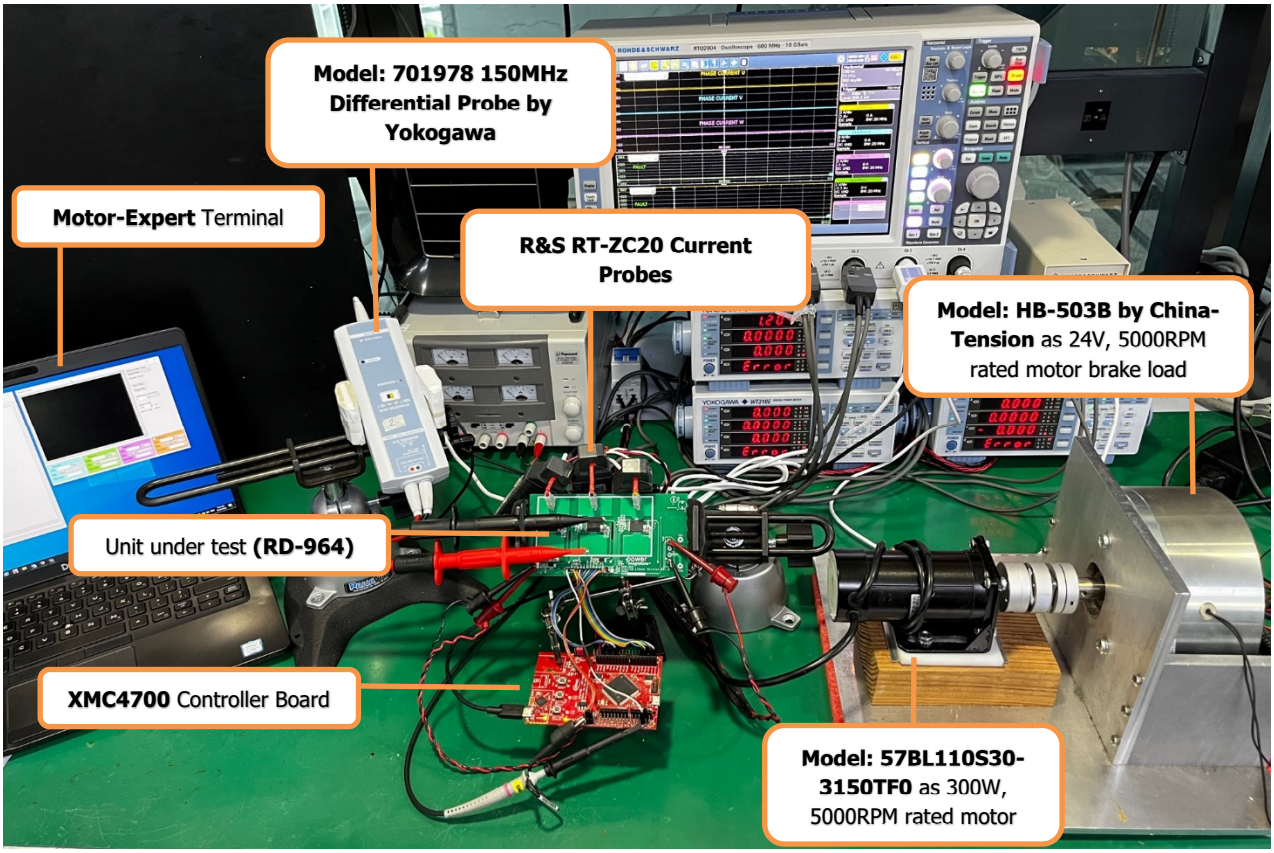


Figure 82 – Actual Bench Set-up for Inverter Efficiency Measurements.

8.12.1 Equipment Used

- **Motor (Model: 57BL110S30-3150TF0)** – as a 300W, 5000RPM, rated motor.
- **Motor brake load (Model: HB-503B by China-Tension) –** as a 24VDC, 300W rated brake load.
- **Brake load control (Model: ICS-500 by China-Tension) –** as a 24VDC, 500mA rated brake load control.
- **High-voltage DC source (Agilent 6812B) –** for supplying high-voltage DC input to the three-phase inverter.
- **Low-voltage DC source (Technique QT3005D-3) –** as external supply for the gate driver (+17VDC).
- **Oscilloscope (R&S RTO 1004/2004) –** for waveform checking and analysis.
- **Digital multimeter (Fluke 87V) –** for ambient temperature monitoring.
- **Current probes (R&S RT-ZC20) –** for capturing the inverter phase currents.
- **Differential probes (Yokogawa 701978) –** 150MHz differential probe for high-voltage measurements.
- **Power meter (Yokogawa WT310E) –** for measuring input and output voltage, current, and power.
- **XMC4700 development board –** as three-phase inverter controller programmed with three-phase field-oriented control with IPH phase current reconstruction.
- **Laptop –** as terminal for Motor-Expert Suite.

8.13 Sensorless FOC Algorithm with IPH Reconstruction

In order to highlight the use of BridgeSwitch IPH, Power Integrations developed its own sensorless field-oriented control algorithm. The algorithm makes use of the information taken from the IPH pin of all three BridgeSwitch devices in the inverter. Additionally, a proprietary algorithm to reconstruct the phase current was also developed and used together with the FOC algorithm.

The reconstructed phase currents (U, V, and W) are used to calculate the flux of the motor stator and rotor. This flux information then becomes the reference for the field-oriented control algorithm. Various Proportional-Integral observers are then utilized to implement speed and current control needed for FOC.

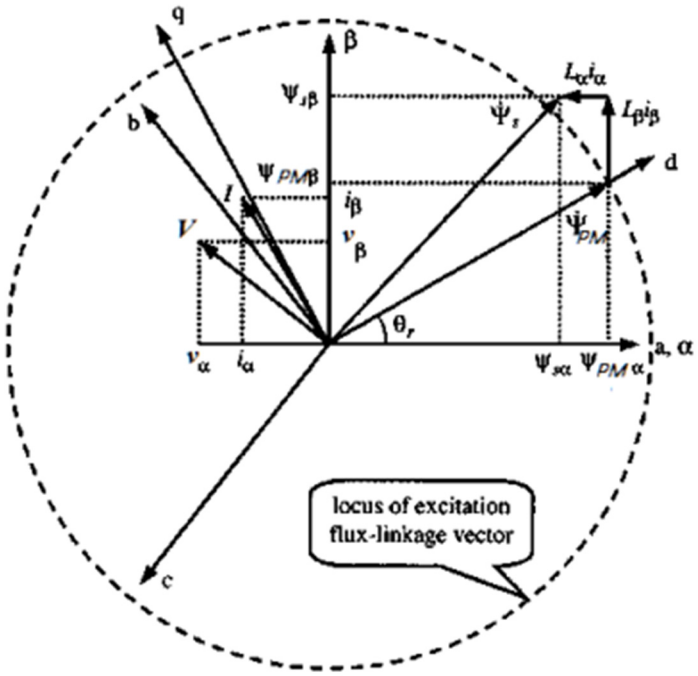


Figure 83 – Motor Flux Diagram.

Finally, to estimate the rotor position, a quadrature phase-locked loop (PLL) structure is put in place. The rationale for the QPLL is its resilience to noise and its simplicity. To further simplify angular calculations, a look-up table is also inserted into the current reconstruction library

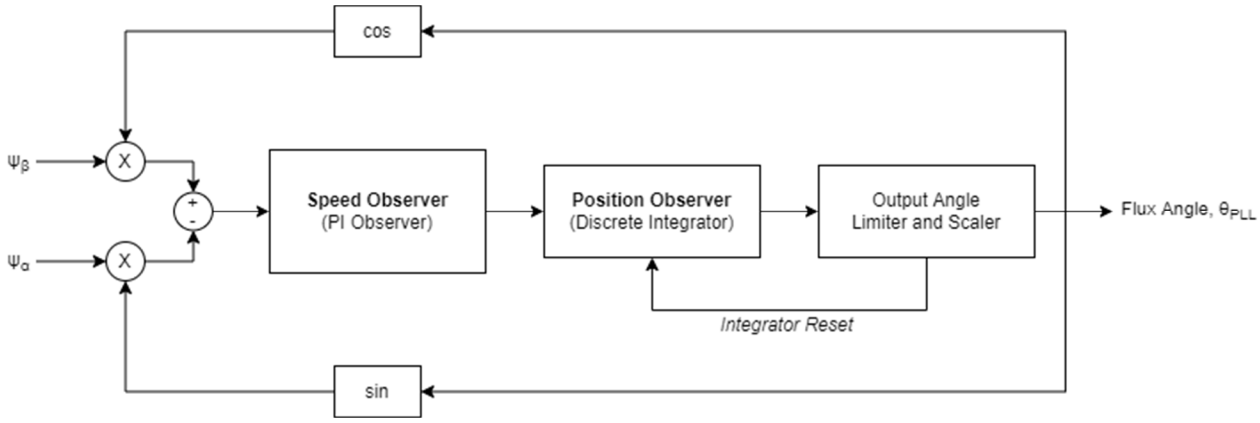


Figure 84 – QPLL Position Estimation Controller

The Motor-Expert Suite documentation discusses the specifics of the FOC algorithm as well as phase current reconstruction in more details.

8.14 Motor-Expert Suite

Motor-Expert Suite is an application designed and made by Power Integrations to aid the configuration, tuning, and diagnostic of the Power Integrations motor development kits. It provides graphical user interface to all parameters and commands as wells as terminal emulator for interacting with the motor controller in serial mode.

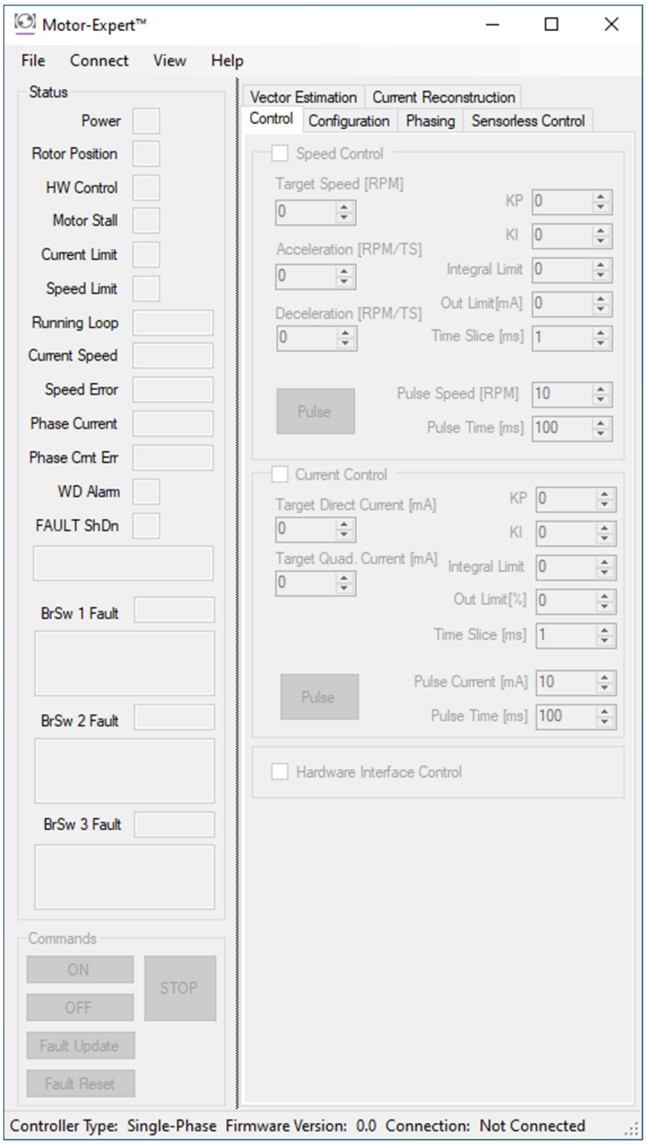


Figure 85 – Motor-Expert Graphical User Interface

To download the Motor-Expert Suite, follow the link below.

https://www.power.com/design-support/downloads/motor-expert-suite

8.14.1 Motion Scope

The Motor-Expert Suite comes with a digital parameters viewer called the Motion Scope. The Motion Scope can be configured, with its four channels similar to a digital storage oscilloscope, to visualize various motor control parameters during runtime that are normally not viewable by a physical or digital oscilloscope or test hardware. Communication is accomplished through the serial bus or UART.

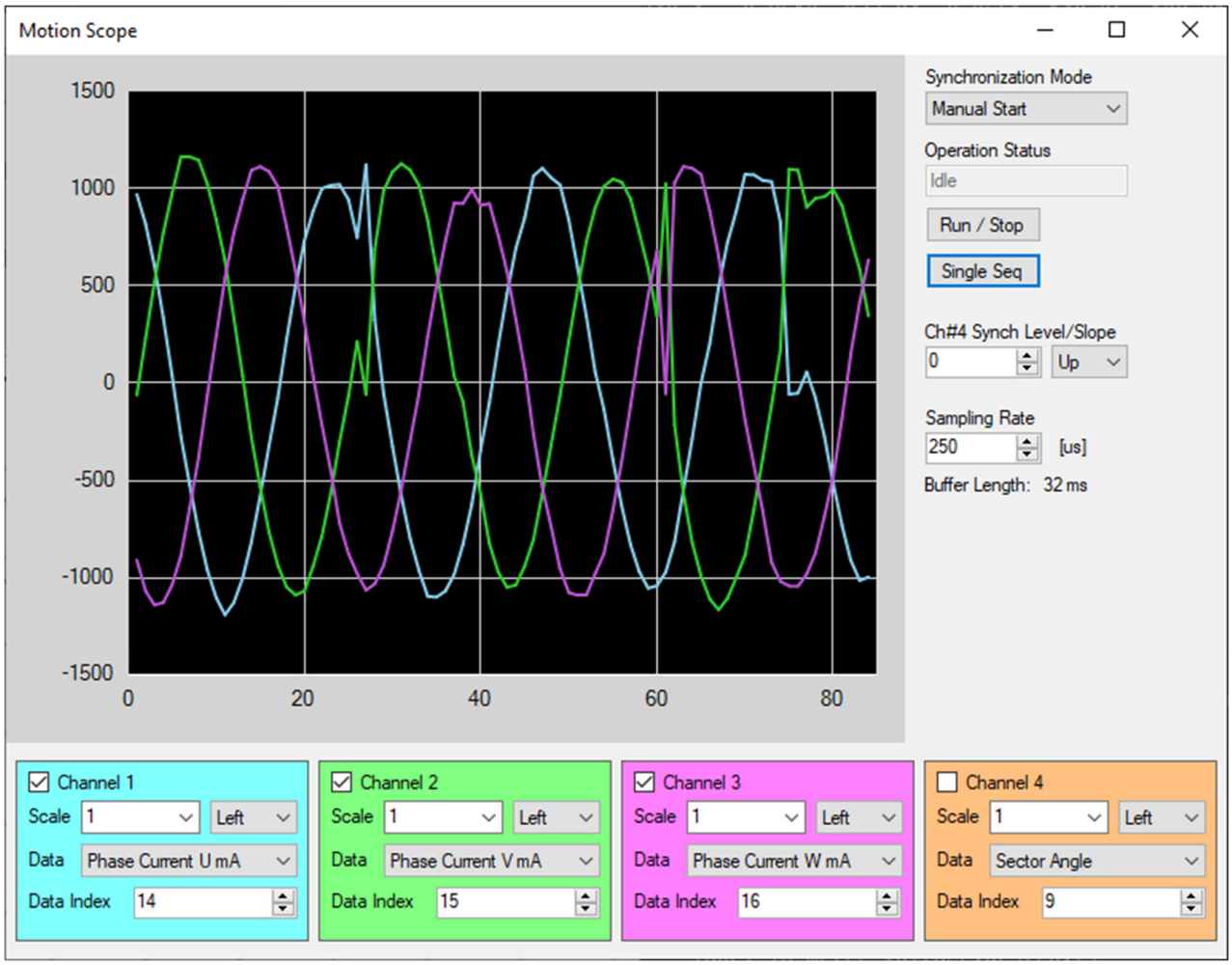


Figure 86 – Motion Scope Feature.

8.14.2 Terminal Emulator

In addition to the Motion Scope, the Motor-Expert Suite also comes with a terminal emulator. This emulator can be used to send and receive serial commands to the attached controller. BridgeSwitch FAULT BUS messages can also be seen from the terminal emulator during runtime.

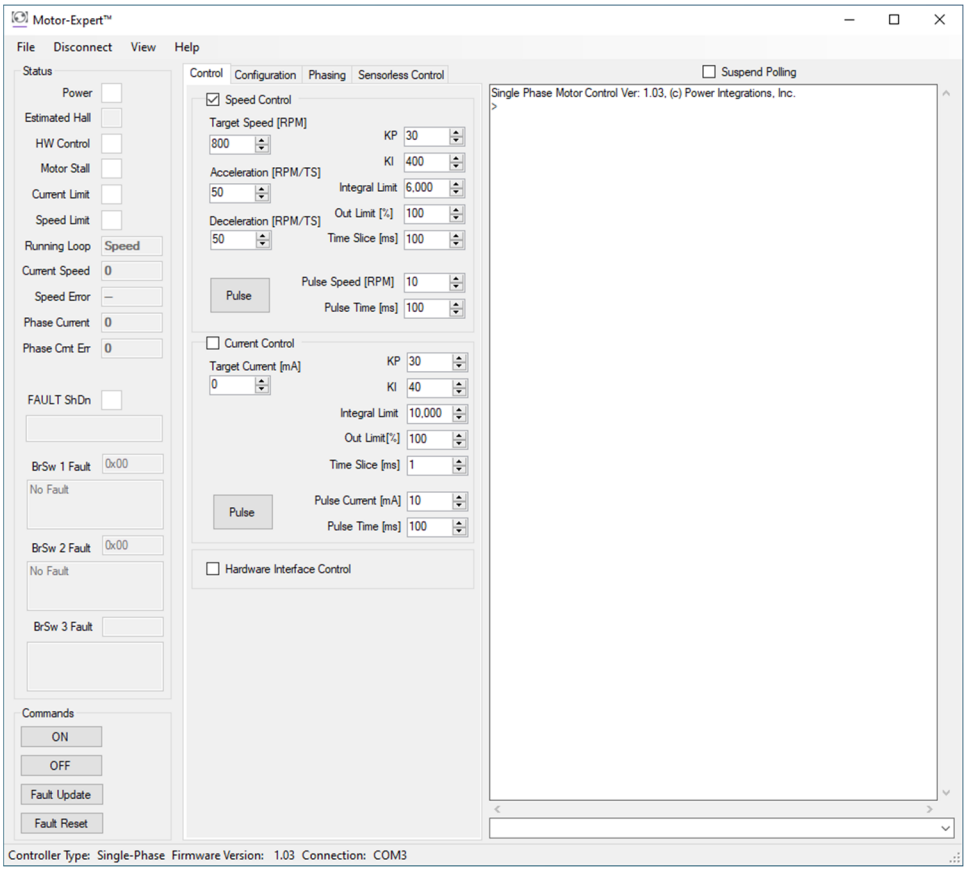


Figure 87 – Terminal Emulator.

Note: All user manuals, getting started documents, and references for the Motor-Expert Suite are available from www.power.com.

8.15 Hardware Changes/Improvements

The main highlight of RDR-964 is the use of BridgeSwitch IPH pins in combination to the three-phase field-oriented control firmware with IPH phase current reconstruction. As a result, a number of passive and active components have been replaced by a resistor connected to the IPH pin of each BridgeSwitch devices.

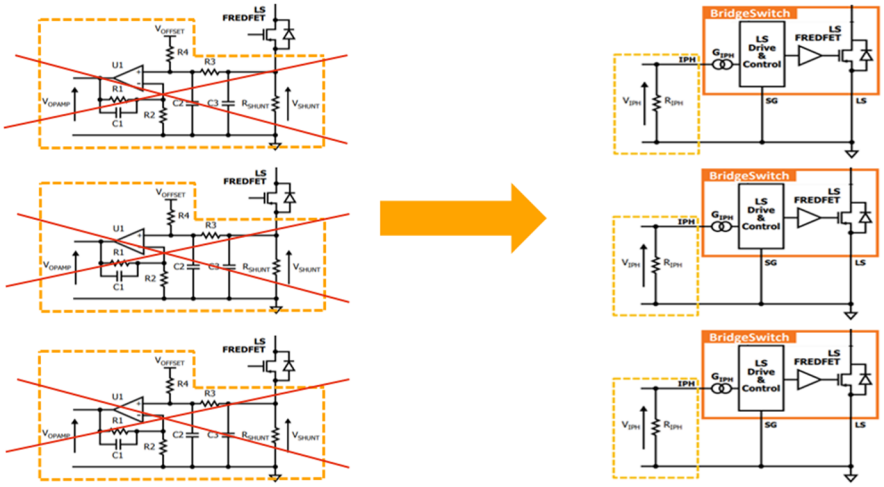


Figure 88 – Traditional Current Feedback vs. BridgeSwitch IPH.

9 Revision History

Date	Author	Rev.	Description & Changes	Approval
10-Jun-22	EA	1.0	Initial Release.	Apps & Mktg
20-Oct-22	EA	2.0	Updated with dynamic loading and additional abnormal operating condition	Apps & Mktg

For the latest updates, visit our website: www.power.com

Reference Designs are technical proposals concerning how to use Power Integrations' gate drivers in particular applications and/or with certain power modules. These proposals are "as is" and are not subject to any qualification process. The suitability, implementation and qualification are the sole responsibility of the end user. The statements, technical information and recommendations contained herein are believed to be accurate as of the date hereof. All parameters, numbers, values and other technical data included in the technical information were calculated and determined to our best knowledge in accordance with the relevant technical norms (if any). They may base on assumptions or operational conditions that do not necessarily apply in general. We exclude any representation or warranty, express or implied, in relation to the accuracy or completeness of the statements, technical information and recommendations contained herein. No responsibility is accepted for the accuracy or sufficiency of any of the statements, technical information, recommendations or opinions communicated and any liability for any direct, indirect or consequential loss or damage suffered by any person arising therefrom is expressly disclaimed.

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