DESCRIPTION

The PT2470 device is a brushed-DC motor driver for printers, appliances, industrial equipment, and other small machines. Two logic inputs control the H bridge driver, which consists of four N-channel MOSFETs that can control motors bi-directionally with up to 3.6-A peak current. The inputs can be pulse-width modulated (PWM) to control motor speed, using a choice of current-decay modes. Setting both inputs low enters a low-power sleep mode.

The PT2470 device features integrated current regulation, based on the analog input VREF and the voltage on the ISEN pin, which is proportional to motor current through an external sense resistor. The ability to limit current to a known level can significantly reduce the system power requirements and bulk capacitance needed to maintain stable voltage, especially for motor startup and stall conditions.

The device is fully protected from faults and short circuits, including under voltage (UVLO), overcurrent (OCP), and over temperature (TSD). When the fault condition is removed, the device automatically resumes normal operation.

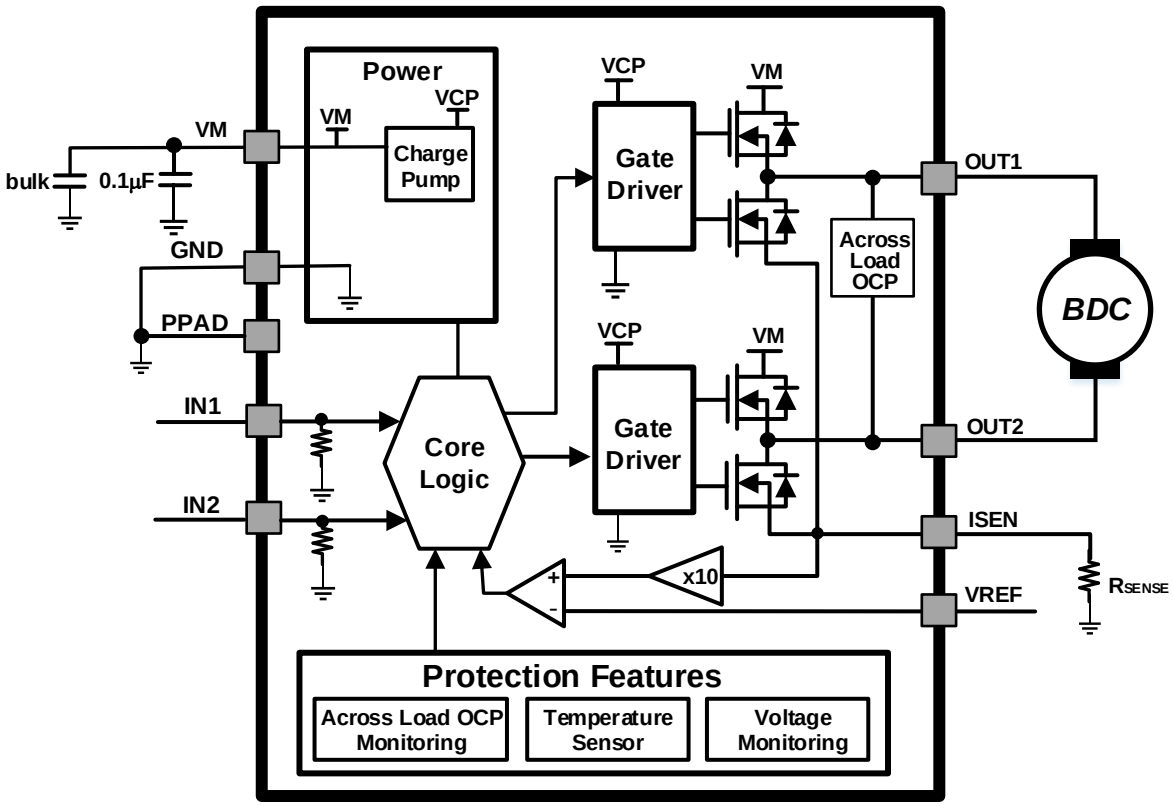
FEATURES

- H-Bridge Motor Driver
  – Drives One DC Motor, One Winding of a Stepper Motor, or Other Loads
- Wide 9-V to 36-V Operating Voltage
- 500-mΩ Typical $R_{DS(on)}$ (HS + LS)
- 3.6-A Peak Current Drive
- PWM Control Interface
- Integrated Current Regulation
- Low-Power Sleep Mode
- Small Package and Footprint
  – 8-Pin HSOP With ThermalPAD
- **Integrated Protection Features**
  – VM Under voltage Lockout (UVLO)
  – Across the Load Overcurrent Protection (OCP)
  – Thermal Shutdown (TSD)
  – Automatic Fault Recovery

APPLICATIONS

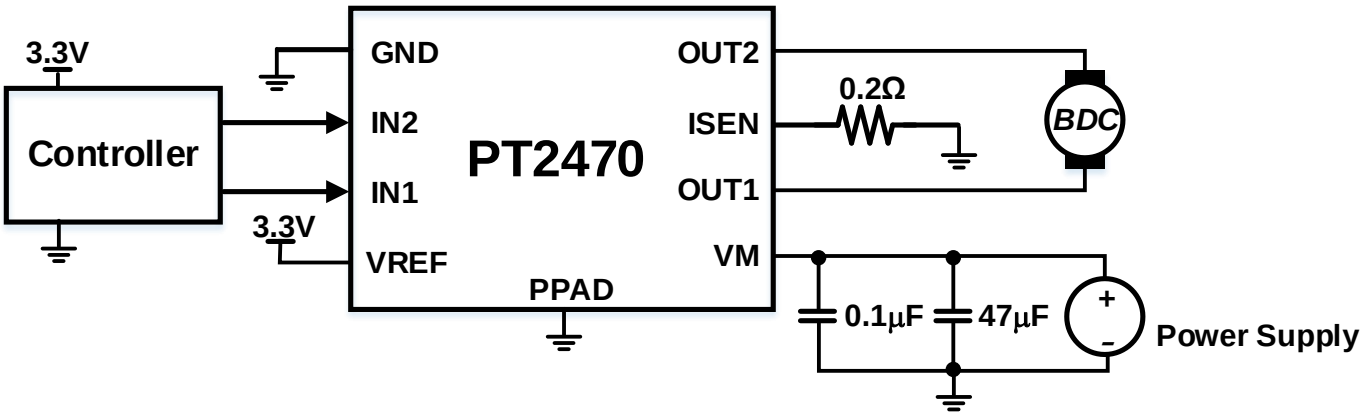
- Printers
- Appliances
- Industrial Equipment
- Other Mechatronic Applications

BLOCK DIAGRAM



APPLICATION CIRCUIT

The PT2470 device is typically used to drive one brushed DC motor.

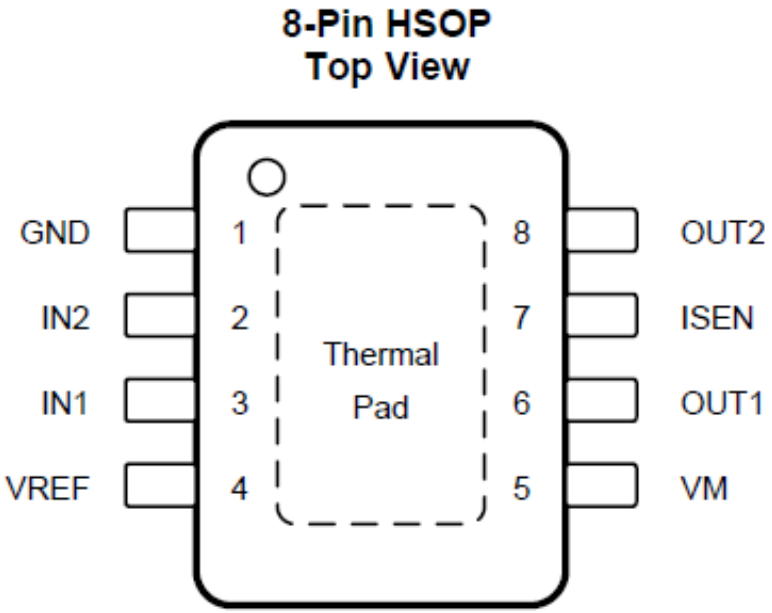


Typical Connections

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2470-HS	8 Pins, HSOP	PT2470-HS

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	Type	Description	Pin No.
GND	PWR	Logic ground. Connect to board ground.	1
IN2	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns.	2
IN1	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns.	3
VREF	I	Analog input. Apply a voltage between 0.3 to 5 V.	4
OUT1	O	H-bridge output. Connect directly to the motor or other inductive load.	6
ISEN	PWR	High-current ground path. If using current regulation, connect ISEN to a resistor (low-value, high-power-rating) to ground. If not using current regulation, connect ISEN directly to ground.	7
OUT2	O	H-bridge output. Connect directly to the motor or other inductive load.	8
PAD	-	Thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.	-

FUNCTION DESCRIPTION

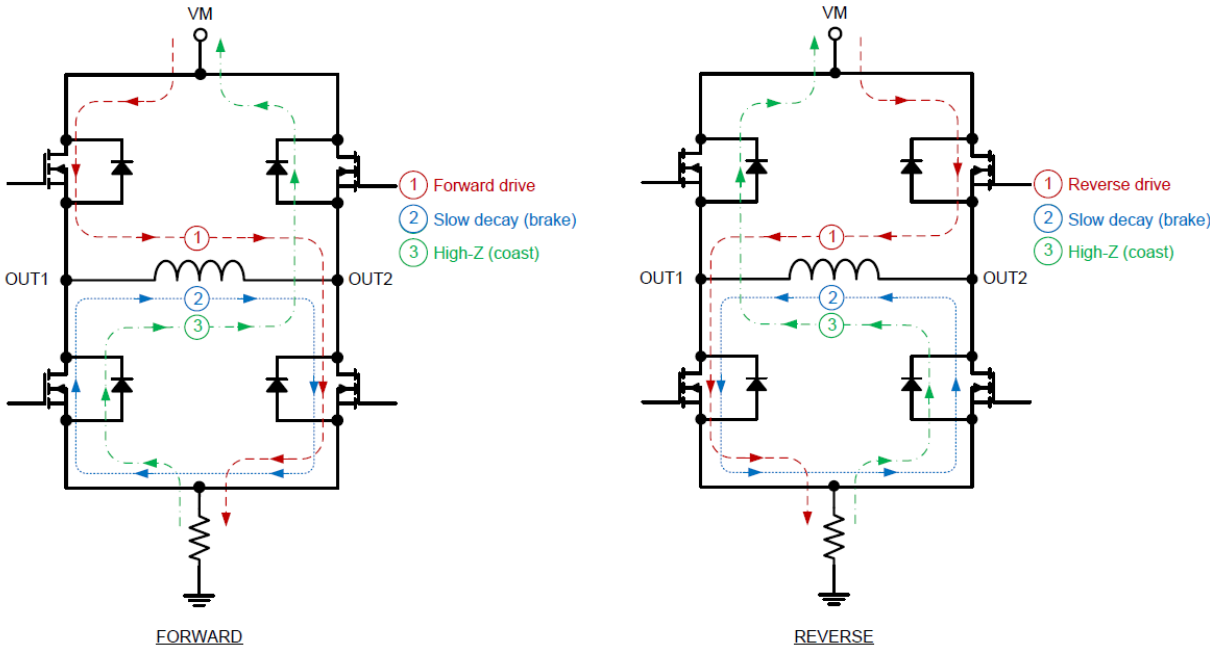
H-BRIDGE CONTROL

The PT2470 output consists of four N-channel MOSFETs that are designed to drive high current. These outputs are controlled by the two logic inputs IN1 and IN2 as listed in Table 1.

Table 1. H-Bridge Control

IN1	IN2	OUT1	OUT2	DESCRIPTION
0	0	High-Z	High-Z	Coast; H-bridge disabled to High-Z (sleep entered after1 ms)
0	1	L	H	Reverse (Current OUT2→Out1)
1	0	H	L	Forward (Current OUT1→Out2)
1	1	L	L	Brake; low side slow decay

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving and braking typically works best. For example, to drive a motor forward with 50% of the maximum RPM, IN1 = 1 and IN2 = 0 during the driving period,and IN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for *fast currentdecay* is also available. The input pins can be powered before VM is applied.



H-Bridge Current Paths

SLEEP MODE

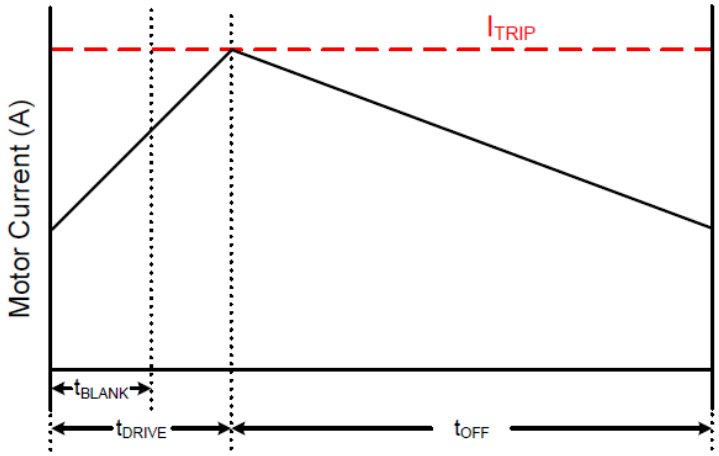
When the IN1 and IN2 pins are both low for time t_{SLEEP} (typically 1 ms), the PT2470 device enters a low-power sleep mode, where the outputs remain High-Z and the device uses $I_{VMSLEEP}$ (μA) of current. If the device is powered up while both inputs are low, it immediately enters sleep mode. After the IN1 or IN2 pins are high for at least 5 μs, the device is operational 50 μs (t_{ON}) later

CURRENT REGULATION

The PT2470 device limits the output current based on the analog input, VREF, and the resistance of an external sense resistor on the ISEN pin according to Equation 1:

$$I_{TRIP}\ (A) = \frac{VREF\ (V)}{A_v \times R_{ISEN}\ (\Omega)} = \frac{VREF\ (V)}{10 \times R_{ISEN}\ (\Omega)} \quad (1)$$

For example, if VREF = 3.3 V and a R_{ISEN} = 0.2 Ω, the PT2470 device limits motor current to 1.65 A no matter how much load torque is applied. When I_{TRIP} is reached, the device enforces slow current decay by enabling both low-side FETs, and it does this for a time of t_{OFF} (typically 25 µs).

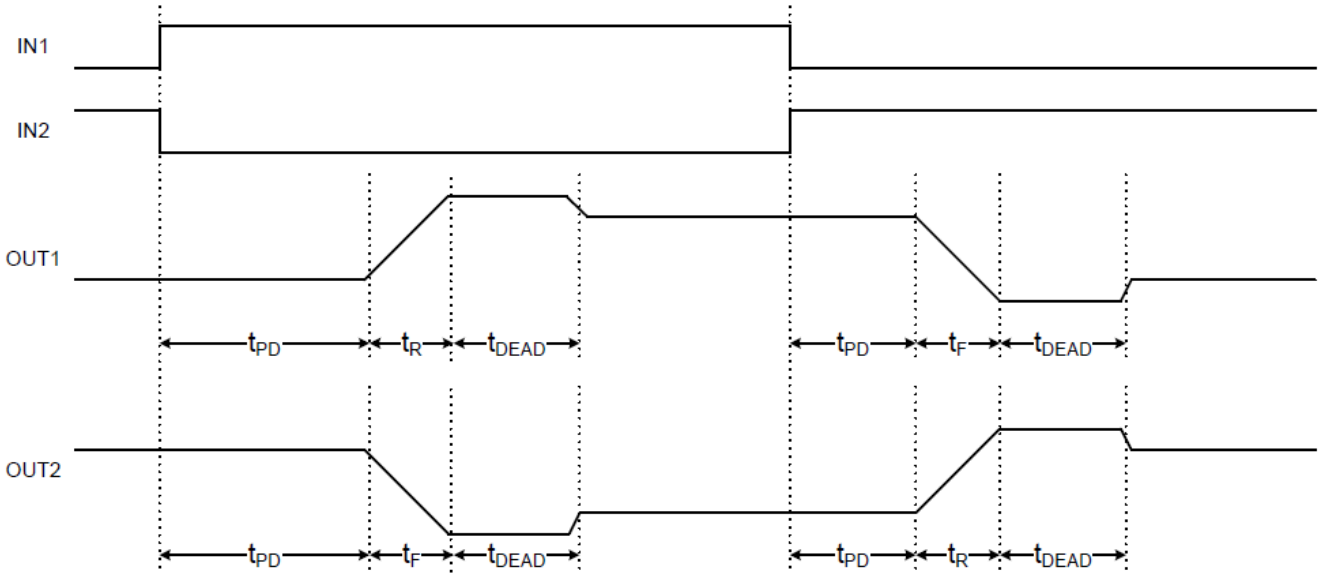


Current-Regulation Time Periods

After t_{OFF} elapses, the output is re-enabled according to the two inputs, INx. The drive time (t_{DRIVE}) until reaching another I_{TRIP} event heavily depends on the VM voltage, the back-EMF of the motor, and the inductance of the motor.

DEAD TIME

When an output changes from driving high to driving low, or driving low to driving high, dead time is automatically inserted to prevent shoot-through. The t_{DEAD} time is the time in the middle when the output is High-Z. If the output pin is measured during t_{DEAD}, the voltage depends on the direction of current. If the current is leaving the pin, the voltage is a diode drop below ground. If the current is entering the pin, the voltage is a diode drop above VM. This diode is the body diode of the high-side or low-side FET.



Propagation Delay Time

VM UNDERVOLTAGE LOCKOUT (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage-lockout threshold voltage, all FETs in the Hbridge will be disabled. Operation resumes when VM rises above the UVLO threshold.

OVERCURRENT PROTECTION (OCP)

If the output current exceeds the OCP threshold, I_{OCP}, for longer than t_{OCP}, all FETs in the H-bridge are disabled for a duration of t_{RETRY}. After that, the H-bridge is re-enabled according to the state of the INx pins. If the overcurrent fault is still present, the cycle repeats; otherwise normal device operation resumes.

THERMAL SHUTDOWN (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

POWER SUPPLY RECOMMENDATIONS

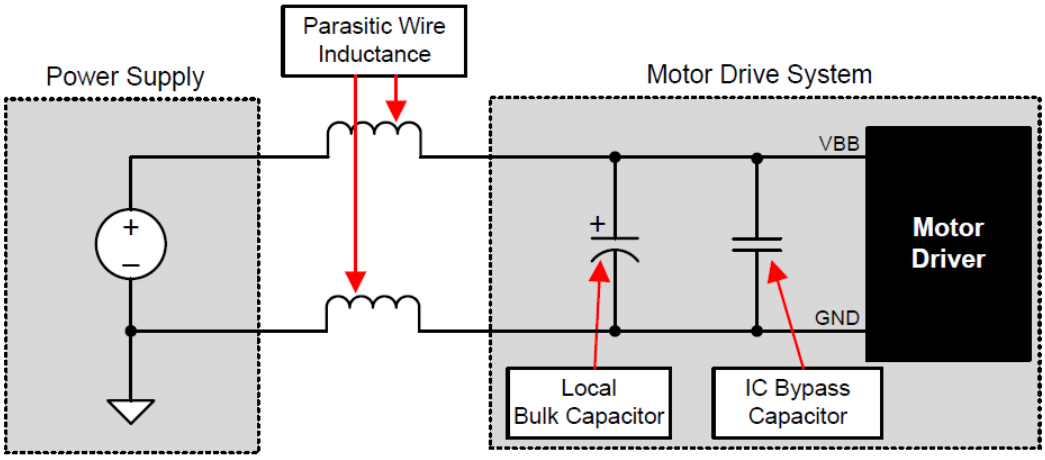
Having appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance of the power supply and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits how the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.



Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

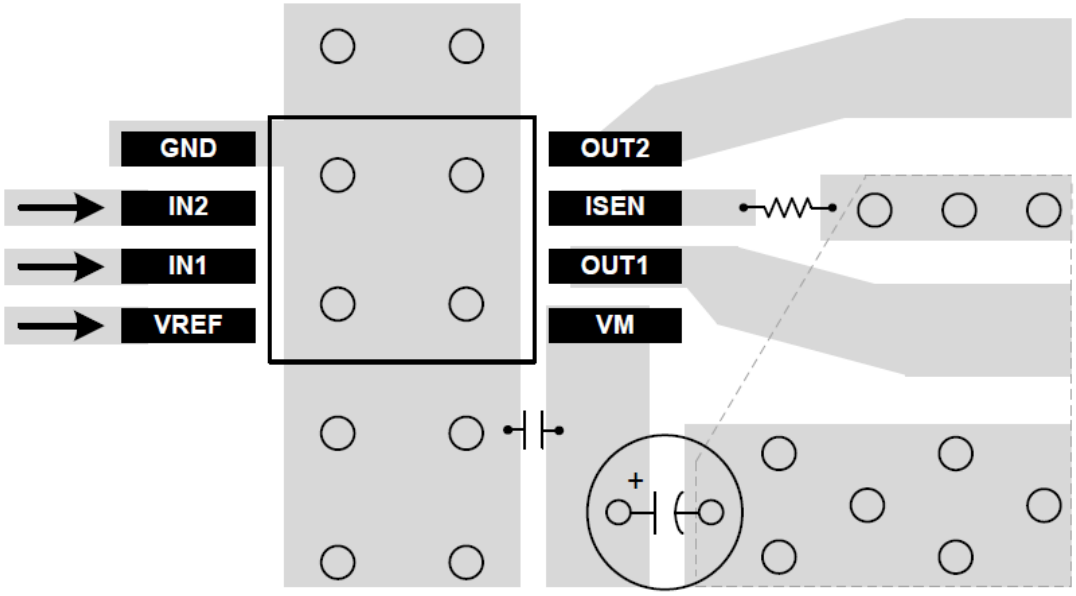
LAYOUT GUIDELINES

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.



Layout Recommendation

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

Parameter	MIN	MAX	UNIT
Power supply voltage (VM)	-0.3	40	V
Logic input voltage (IN1, IN2)	-0.3	5.5	V
Reference input pin voltage (VREF)	-0.3	5.5	V
Continuous phase node pin voltage (OUT1, OUT2)	-0.7	VM+0.7	V
Current sense input pin voltage (ISEN)	-0.5	1	V
Output current (100% duty cycle)	0	3.6	A
Operating junction temperature, TJ	-40	150	°C
Storage temperature, Tstg	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

Parameter	Symbol	MIN	MAX	UNIT
Power supply voltage	VM	9	36	V
VREF input voltage	VREF	0.3(1)	5	V
Logic input voltage (IN1, IN2)	V_I	0	5.5	V
Logic input PWM frequency (IN1, IN2)	f_{PWM}	0	200(2)	KHz
Peak output current(3)	I_{peak}	0	3.6	A
Operating ambient temperature(3)	T_A	-40	125	°C

(1) Operational at VREF = 0 to 0.3 V, but accuracy is degraded.

(2) The voltages applied to the inputs should have at least 800 ns of pulse width to ensure detection. Typical devices require at least 400ns. If the PWM frequency is 200 kHz, the usable duty cycle range is 16% to 84%.

(3) Power dissipation and thermal limits must be observed.

ELECTRICAL CHARACTERISTICS

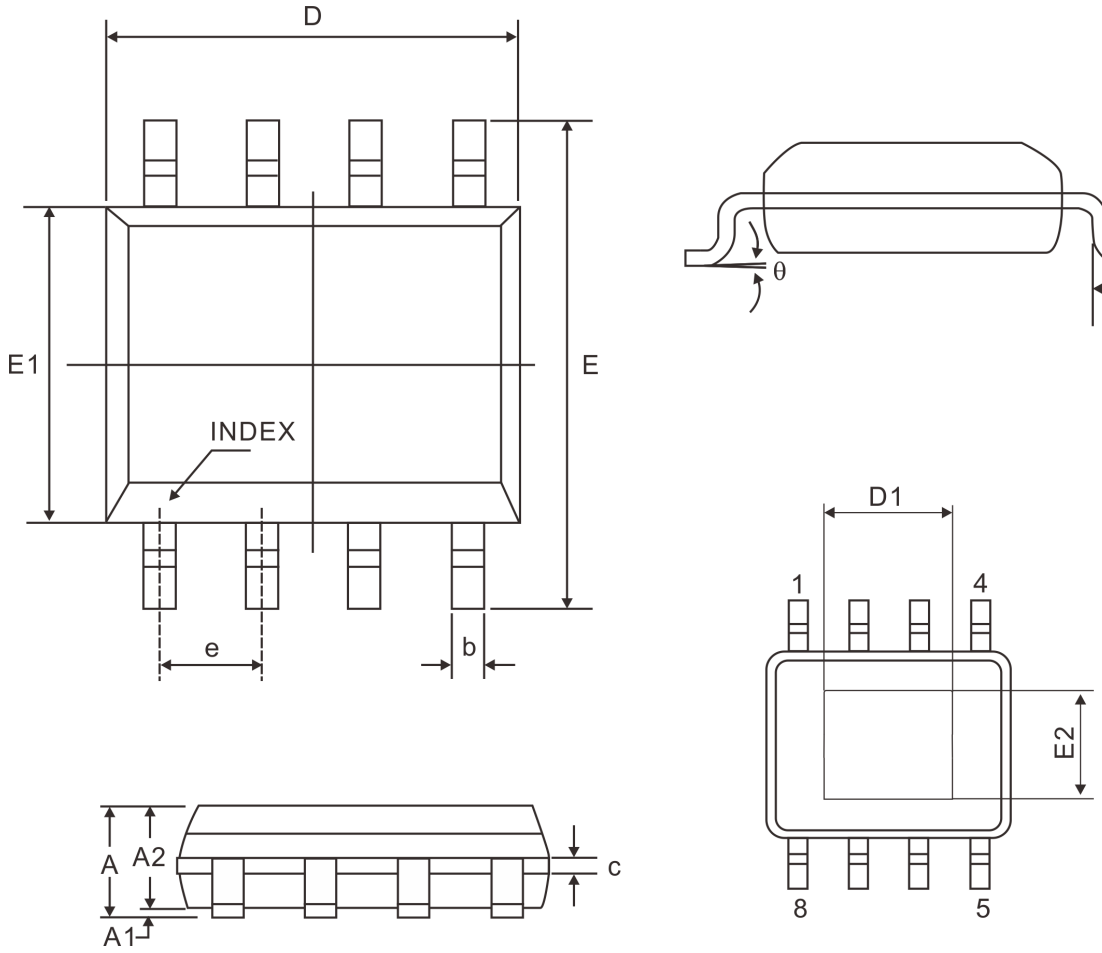
TA = 25°C, over recommended operating conditions (unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
POWER SUPPLY (VM)						
VM operating voltage	VM		9		36	V
VM operating supply current	I_{VM}	VM = 12 V		4	10	mA
VM sleep current	$I_{VMSLEEP}$	VM = 12 V			15	uA
Turn-on time	t_{ON}(1)	VM > VUVLO with IN1 or IN2 high		40	50	uS
LOGIC-LEVEL INPUTS (IN1, IN2)						
Input logic low voltage	V_{IL}				0.5	V
Input logic high voltage	V_{IH}		1.5			V
Input logic hysteresis	V_{HYS}			0.5		V
Input logic low current	I_{IL}	V_{IN} = 0 V	-1		1	uA
Input logic high current	I_{IH}	V_{IN} = 3.3 V		33	100	uA
Pulldown resistance	R_{PD}	to GND		100		kΩ
Propagation delay	t_{PD}	INx to OUTx change		0.6	1	uS
Time to sleep	t_{sleep}	Inputs low to sleep		1	1.5	mS
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
High-side FET on resistance	$R_{DS(ON)}$	VM = 24 V, I = 1 A, f_{PWM} = 25 kHz		250	300	mΩ
Low-side FET on resistance	$R_{DS(ON)}$	VM = 24 V, I = 1 A, f_{PWM} = 25 kHz		250	300	mΩ
Output dead time	t_{DEAD}			200		nS
Body diode forward voltage	V_d	IOUT = 1 A		0.8	1	V
CURRENT REGULATION						
ISEN gain	A_V	VREF = 2.5 V	9.4	10	10.4	V/V
PWM off-time	t_{OFF}			25		uS
PWM blanking time	t_{BLANK}			2		uS
PROTECTION CIRCUITS						
VM undervoltage lockout	V_{UVLO}	VM falls until UVLO triggers		6.1	6.4	V
		VM rises until operation recovers		6.3	6.5	V
VM undervoltage hysteresis	$V_{UV,HYS}$	Rising to falling threshold	100	180		mV
Overcurrent protection trip level	I_{OCP}	Across the Load	3.7	4.5	6.4	A
Overcurrent deglitch time	t_{OCP}			1.5		uS
Overcurrent retry time	t_{RETRY}			3		mS
Thermal shutdown temperature	T_{SD}		150	175		°C
Thermal shutdown hysteresis	T_{HYS}			40		°C

(1) tON applies when the device initially powers up, and when it exits sleep mode.

PACKAGE INFORMATION

8 PINS, HSOP



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	1.70
A1	0.00	-	0.15
A2	1.25	-	-
b	0.31	-	0.51
c	0.10	-	0.25
e	1.27 BSC		
D	4.90 BSC		
D1	2.81	-	3.30
E	6.00 BSC		
E1	3.90 BSC		
E2	2.05	-	2.41
L	0.40	0.60	1.27
θ	0°	-	8°

Notes: Refer to JEDEC MS-012 BA

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