DESCRIPTION

The PT4308 is a compact, fully integrated OOK / ASK receiver with ±4 KV ESD（HBM）protection for 433.92 MHz frequency band and requires few external components. The PT4308 consists of a low-noise amplifier （LNA）, an image-rejection mixer（IRM）, a built-in channel-select filter （CSF）, an OOK / ASK demodulator, a data filter, and a data slicing comparator. The local oscillator （LO） sub-system incorporates a monolithic VCO, a ÷32 feedback divider, a loop filter and a fast start-up reference oscillator to form a complete phase-locked loop-based frequency synthesizer for single channel applications.

The PT4308 is available in an 8-pin SOP package and is specified over the temperature range from –40 to +85 °C.

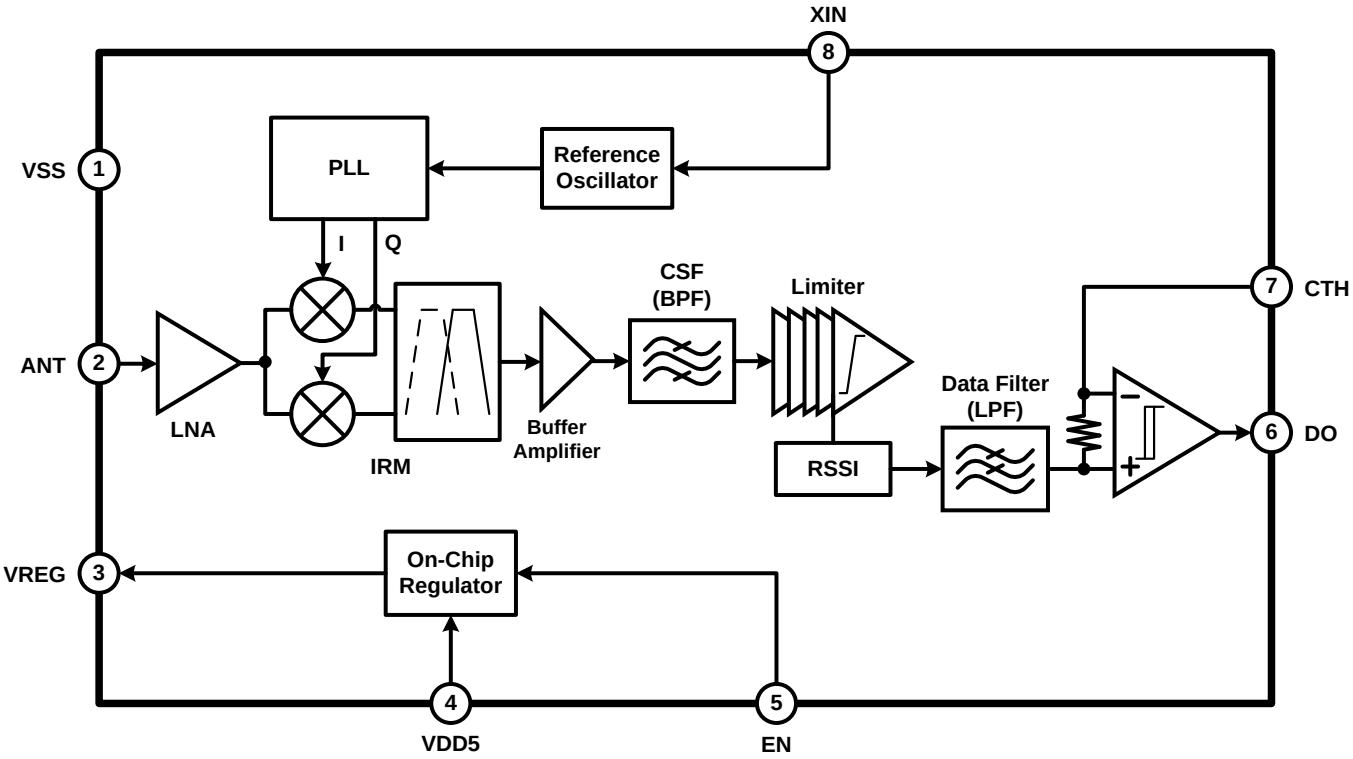
FEATURES

- Normal operating of 4.3 mA at 433.92 MHz
- Requires few external components
- Achieves sensitivity of –114 dBm （peak ASK signal level）
- Supply voltage range: 2.1 to 5.5 V
- Supports data rates up to 10 Kb / s
- Wide input dynamic range with automatic gain control handling
- Image-rejection ratio of 25 dB
- ESD protection level up to ±4 KV for HBM, ±400 V for MM and ±1 KV for CDM

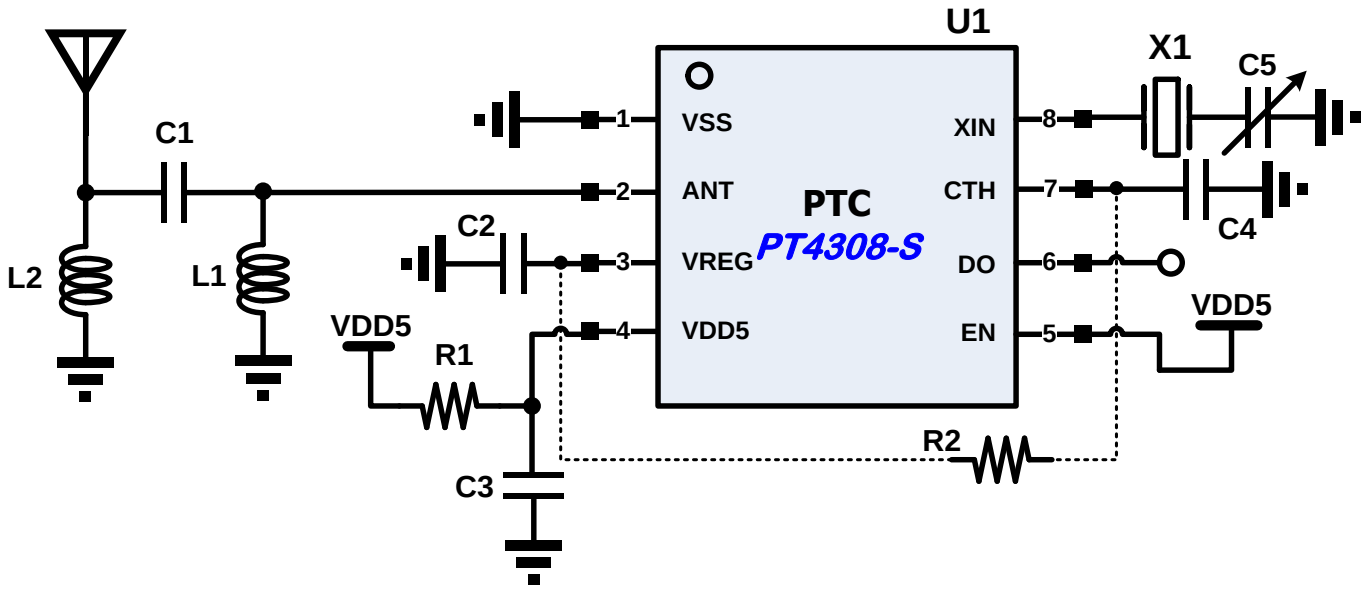
APPLICATIONS

- Automotive Remote Keyless Entry （RKE）
- Remote control
- Garage door and gate openers
- Suitable for applications that must adhere to either the European ETSI-300-220 or the North American FCC （Part 15）regulatory standards

BLOCK DIAGRAM



EVALUATION BOARD SCHEMATIC



BILL OF MATERIALS

Part	Value	Unit	Description
L1	39 n	H	Antenna input matching, coil inductor
L2	56 n	H	Antenna ESD protection, coil inductor（*optional*）
C1	1.5 p	F	Antenna input matching
C2 / C3	100 n	F	Power supply de-coupling capacitor
C4	470 n	F	C_{TH}, affects coding type and start-up time
C5	220 p	F	Dependent upon crystal oscillator vendor; for frequency fine-tuning （*optional*）
R1	10	Ω	Power supply de-coupling resistor （*optional*）
R2	5.1 M	Ω	For reducing data output noise （*optional*）
X1	13.598	MHz	Crystal with C_{Load} = *220 pF*, for reference oscillator
U1	PT4308 IC	U1	Receiver chip

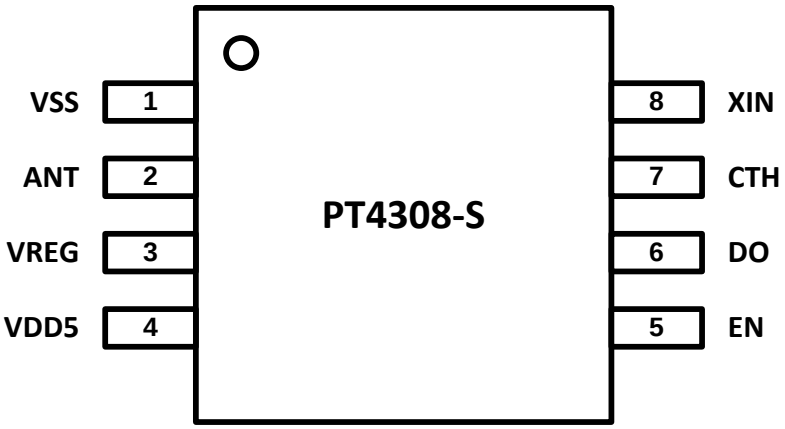
Notes:

1. L1 and C1 are the components for input matching network. They may need to be adjusted for different PCB layout and antenna requirements.
2. *The value of C4 depends upon the data rate and coding pattern.*
3. The *optional* components may be used depending upon specific application requirements.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT4308-S	8 Pins, SOP, 150 mil	PT4308-S

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	I / O	Description
1	VSS	G	Ground
2	ANT	I	RF input connected to antenna via a matching network
3	VREG	P	Regulated core voltage
4	VDD5	P	5 V regulator input
5	EN	I	Chip enable（tie HIGH to enable the chip）
6	DO	O	Data output
7	CTH	I / O	Connection for data slicing threshold capacitor
8	XIN	I	Reference oscillator input

FUNCTION DESCRIPTION

POWER SUPPLY

The PT4308 provides a regulated core voltage, VREG （pin 3）, to the core blocks by an on-chip voltage regulator. A bypass capacitor, C2, has to be connected with the VREG pin, and it should be placed as close as possible to the VREG pin in the PCB layout. The VDD5 pin （pin 4） should connect to the external supply voltage and should incorporate series-R, shunt-C filtering. The PT4308 chip can operate in the supply voltage range from 2.1 V to 5.5 V.

RF FRONT-END

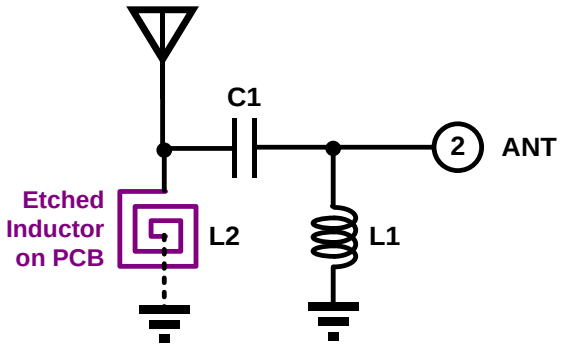
The RF front-end of the receiver employs a super-heterodyne configuration that down-converts the input radio frequency （RF） signal to an intermediate frequency （IF） signal. According to the block diagram, the RF front-end consists of an LNA and an image rejection down-conversion mixer, and the in-phase（I）and quadrature（Q）local oscillator（LO） signals for the mixer are generated from the PLL frequency synthesizer.

A special feature of the PT4308 is its integrated double-balanced image-rejection mixer （IRM）, which eliminates the need for a costly front-end SAW filter for many applications. The advantages of not using a SAW filter include simplified antenna matching, less board space, and lower BOM cost. The mixer cell consists of a pair of double-balanced mixers that perform an I-Q down-conversion of the RF input to the IF band with high-side injection （i.e. $f_{RF} = f_{LO} - f_{IF}$）. The image-rejection circuit then combines these signals to achieve an image-rejection ratio typically over 25 dB. High-side injection is mandatory （e.g. low-side injection may not be selected） due to the nature of the on-chip image rejection implementation. The IF output of IRM is connected to a buffer amplifier to drive the succeeding IF-band, channel-select filter （CSF）.

The ANT pin can be matched to 50 Ohm with an L-type circuit. Inductor L1 and capacitor C1 values may be different from table depending on PCB material, PCB thickness, ground configuration, and the length of traces used in the layout.

ANTENNA PIN ESD PROTECTION

The PT4308 IC provides the ESD protection levels better than 4 KV for HBM （Human Body Mode）, 400 V for MM （Machine Mode） and 1 KV for CDM （Charge Device Mode）. However, higher ESD protection level at the ANT pin may still be required at the system level for some applications. Achieving an enhanced ESD protection level may need to rely on the external components. Changing L1 from SMD type to coil type could enhance ESD protection level up to 1 KV, and adding a shunt coil inductor L2 of 56 nH （can either use an etched inductor on PCB） in front of C1 could help to further improve the ESD protection.



REFERENCE OSCILLATOR

All timing and tuning operations on the PT4306 are derived from the internal one-pin one-pin Colpitts reference oscillator. When a crystal is used, the minimum oscillation voltage swing is 300 mV_{PP}.

As with any super-heterodyne receiver, the mixing product between the internal LO（local oscillator）frequency, f_{LO}, and the incoming transmit frequency, f_{TX}, must ideally equal the IF center frequency, f_{IF}. The following equations may be used to compute the appropriate f_{LO} for a given f_{TX}:

$f_{LO} = f_{TX} \times$（352 / 351） for 433.92 MHz band. Hence, $f_{IF} = f_{TX} \div 351$.

Using the above equations, frequencies f_{TX} and f_{LO} are computed in MHz. High-side LO injection results in an image frequency above the frequency of interest. For a given value of f_{LO}, the equation below may be used to compute the reference oscillator frequency, f_{REFOSC}:

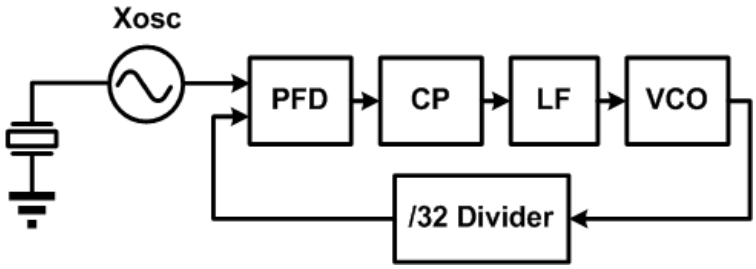
$f_{REFOSC} = f_{LO} \div 32$.

So that the f_{REFOSC} is 13.598 MHz for the PT4308 chip （high-side LO mixing）.

PHASE-LOCKED LOOP（PLL）

The PT4308 utilizes an integer-N PLL to generate the receiver LO. The PLL consists of a voltage-controlled oscillator（VCO）, a reference crystal oscillator, an asynchronous ÷32 fixed-modulus divider, a charge pump, a loop filter and a phase-frequency detector（PFD）. All components are integrated on-chip. The PFD compares two signals and produces an error signal that is proportional to the difference between the input signal phases. The error signal passes through a loop filter that provides a loop bandwidth of approximately 200 KHz, and is used to control the VCO. The VCO output frequency is fed back through the fixed-modulus frequency divider to one input of the PFD. The other input to the PFD comes directly from the reference crystal oscillator. Thus, the VCO output frequency, which is used as the LO frequency, is phase-locked to the reference frequency and $f_{REFOSC} =$（$f_{TX} + f_{IF}$）$\div 32 = f_{LO} \div 32$.

The block diagram below illustrates the basic elements of the PLL.



CHANNEL-SELECT FILTER

PT4308 embeds a channel-select filter （CSF） with a bandwidth of approximately 380 KHz. The CSF utilizes a sixth-order active filter for the low-IF architecture. An automatic frequency tuning circuit is also included on-chip and its absolute reference clock is derived from the reference crystal oscillator. The automatic frequency tuning circuit centers the pass-band of the CSF at the IF frequency （f_{IF}）.

ASK DEMODULATOR

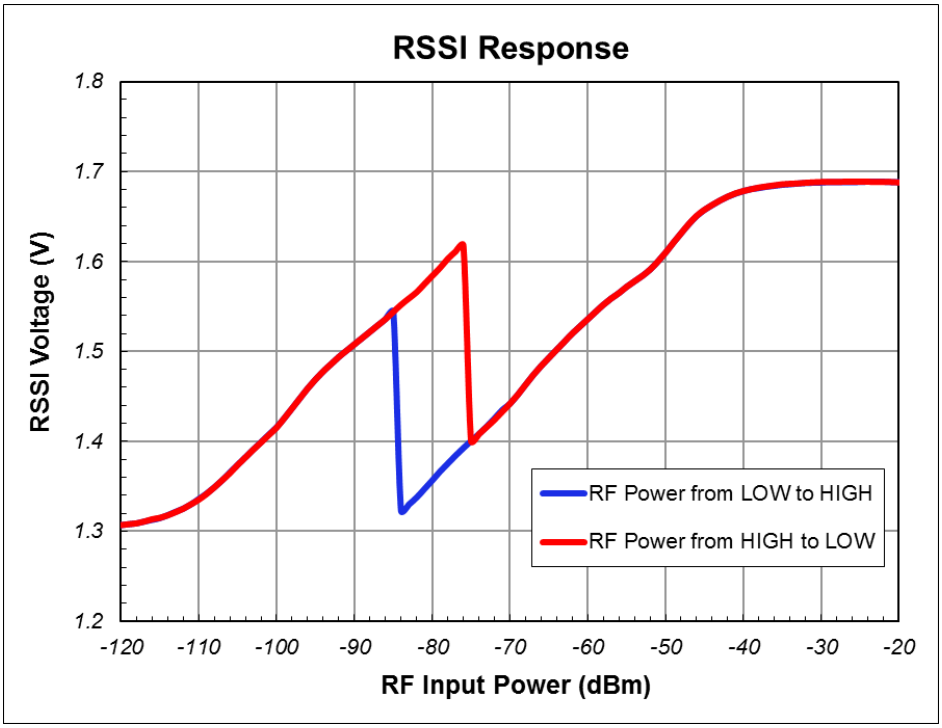
The OOK / ASK demodulation is done by comparing the received signal strength indicator （RSSI） signal level. The RSSI signal is decimated and filtered in the data filter and the data decision is then completed by the slicing comparator.

The RSSI is implemented as a successive compression log amplifier following by the internal CSF. The log amplifier achieves ±3 dB log linearity; the RSSI output level has the dynamic range of over 80 dB with AGC circuitry. The RSSI slope is approximately 7 mV / dB.

AUTOMATIC GAIN CONTROL （AGC）

The AGC circuitry monitors the RSSI voltage levels. When the RSSI voltage reaches a first value corresponding to an RF input level of approximately –85 dBm, the AGC reduces the gain of receiver chain by 28 dB, thereby reducing the RSSI output by approximately 210 mV. When the RSSI voltage drops below a level corresponding to an RF input of approximately –75 dBm, the AGC sets the receiver chain back to high-gain mode.

The following figure shows the change of RSSI voltage versus RF input power. When the RSSI level increases and then exceeds 1.61 V （RF input power rising）, the AGC switches the receiver chain from high-gain mode to low-gain mode. As RSSI level decreases back to 1.32 V （RF input power falling）, the AGC switches the receiver chain from low-gain mode back to high-gain mode. The AGC has an additional protection mechanism （delay timer of $2^{21}\times T_{ref}$ *seconds*） when the receiver chain is reset back to the high-gain state.



Parameter	Condition	f_{RF} = 433.92 MHz
AGC Decay Time	RF input power changes from High to Low	$2^{21}\times T_{ref}$ ~ 154 ms

DATA FILTER

The data filter（post-demodulator filter）is utilized to remove additional unwanted spurious signals after the OOK / ASK demodulator. The data filter is implemented as a 2nd-order low-pass Sallen-Key filter. The data filter bandwidth（BW_{DF}）has be fixed to 5 KHz. According to the application requirement, the shortest pulse-width of the data pattern should be set according to the following equation

0.65 / Shortest pulse-width ≤ 5 KHz （BW_{DF}）

DATA SLICER

The purpose of the data slicer is to take the analog output of the data filter and convert it to a digital signal. Extraction of the DC value of the demodulated signal for purposes of logic-level data slicing is accomplished using the external threshold capacitor C_{TH} and the on-chip resistor R_{TH}, shown in the block diagram. Slicing level time constant values vary somewhat with decoder type, data pattern, and data rate, but typical values range from 2 ms to 20 ms. Optimization of the value of C_{TH} is required to maximize range.

The first step in the process is selection of a data-slicing-level time constant. This selection is strongly dependent on system issues including system decode response time and data code structure. The effective resistance of R_{TH} is 32.5 KΩ and a τ of 3x the period of longest “LOW” or “HIGH” bit stream is recommended. Assuming that a slicing level time constant τ has been established, capacitor C_{TH} may be computed using equation

$C_{TH} = \tau / R_{TH}$

A standard ±20 % X7R ceramic capacitor is generally sufficient.

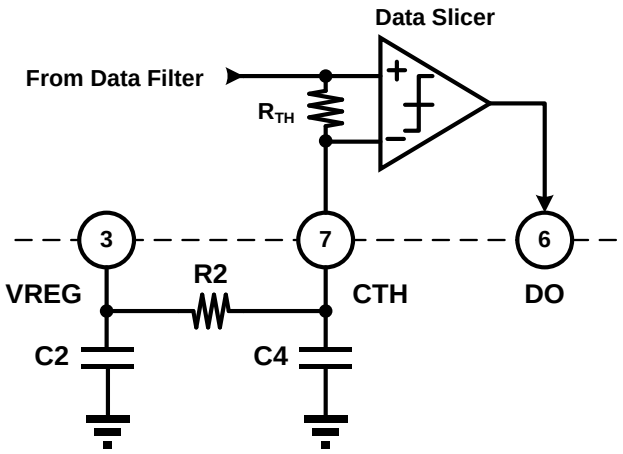
DATA SQUELCHING

During quiet periods（no signal）, the data output（DO pin）varies randomly with noise. Most decoders can discriminate between this random noise and actual data, but for some systems, the random toggling does present a problem. There are two possible approaches to reduce this output noise:

1. Implement analog squelch by raising the demodulator threshold.
2. Add an output filter in order to filter the （high frequency） noise glitches on the data output pin.

The simplest solution is add analog squelch by introducing a small offset, or squelch voltage, on the CTH pin so that noise does not trigger the internal slicer. Usually 20 mV to 30 mV is sufficient and may be achieved by connecting a several mega-Ohm resistor from the CTH pin to the internal supply voltage. The squelch-offset requirement does not change as the local noise strength changes from installation to installation. Introducing squelch will reduce both sensitivity and the receiving dynamic range. Only an amount of offset sufficient to quiet the output should be introduced. Typical squelch resistor is around 5.1 MΩ.

The circuit drawn below shows an application example of analog squelch, where R2 is the squelch resistor. The demodulated data then enters into a quasi-mute state as the RF input signal becomes very small （when there is no RF signal received or the RF signal is too small） and the DO output remains mostly at a logic “LOW” level. If the environment is very noisy, the value of R2 may be reduced to achieve better immunity against noise, but at the cost of loss of sensitivity.



SENSITIVITY AND SELECTIVITY

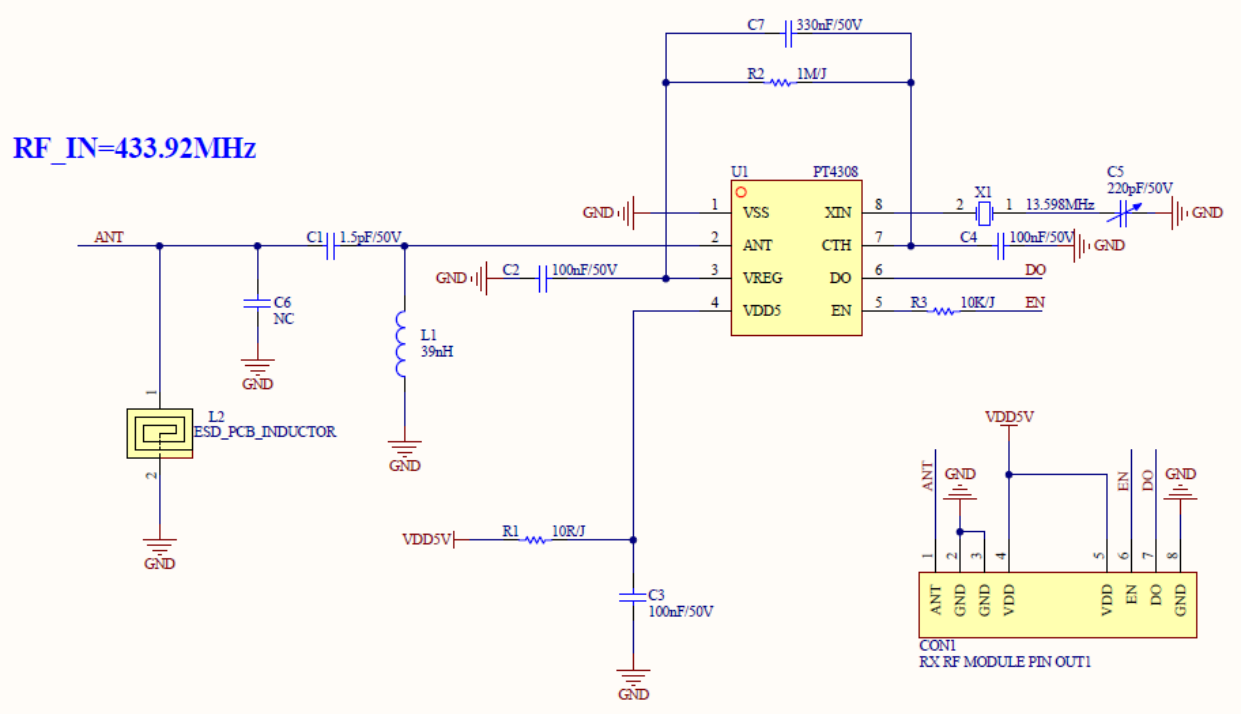
In digital radio systems, sensitivity is often defined as the lowest signal level at the receiver input that will achieve a specified bit error ratio（BER）at the output. The sensitivity of the PT4308 receiver is typically –114 dBm（ASK modulated with 2 Kb / s, 50% duty cycle square wave）to achieve a 0.1% BER（with input was matched to a 50 Ω signal source）.

The selectivity is governed by the response of the receiver front-end circuitry, the CSF（on-chip active IF filter）, and the data filter. Note that the CSF provides not only channel selectivity, but also the interference rejection. Within the pass band of the receiver, no rejection for interfering signals is provided.

POWER-DOWN CONTROL

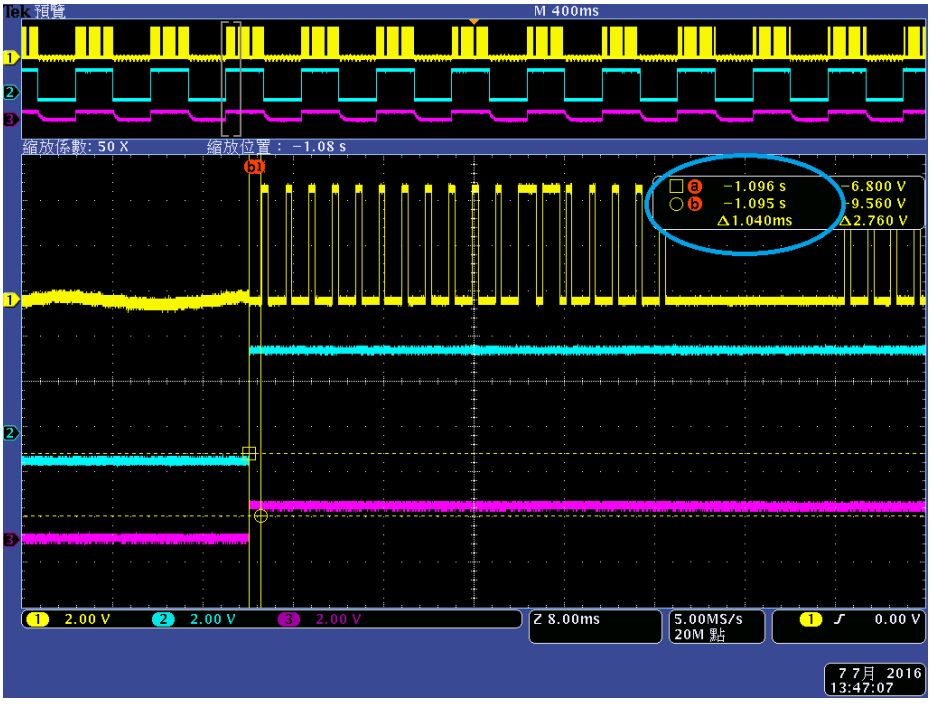
The chip enable （EN） pin controls the power on / off behavior of the PT4308. Connecting EN to “HIGH” sets the PT4308 to its normal operation mode; connecting EN to “LOW” sets the PT4308 to standby mode. The chip consumption current will be lower than 1 μA in standby mode. Once enabled, the PT4308 relies on an internal fast start-up circuit to achieve a start-up time < 2 ms to recover received data at 3-dB above the minimum received RF input level.

The application schematic for the fast start-up system is shown below. The threshold capacitor CTH and squelch resistor R2 have been adjusted for this application. An additional capacitor C7 has been added in parallel with R2 to accelerate the system start-up time. The chosen values for CTH, C7 and R2 depend on the encoding pattern that is used.



Schematic for Fast Start-Up System

The following figure exhibits the system start-up time in the conditions of Temp=27ºC, f_{RF} = 433.92 MHz, P_{RF} = –105 dBm （OOK）, C7 = 330 nF, C_{TH} = 100 nF and D_{RATE} = 2 Kb / s. The EN pin is triggered every 500 mS.



Measured System Start-Up Time （f_{RF} = 433.92 MHz, P_{RF} = –105 dBm （OOK））

ANTENNA DESIGN

For a λ / 4 dipole antenna and operating frequency, f （in MHz）, the required antenna length, L （in cm）, may be calculated by using the formula

$$L = \frac{7132}{f}$$

For example, if the frequency is 433.92 MHz, then the length of a λ / 4 antenna is 16.4 cm. If the calculated antenna length is too long for the application, then it may be reduced to λ / 8, λ / 16, etc. without degrading the input return loss. However, the RF input matching circuit may need to be re-optimized. Note that in general, the shorter the antenna, the worse the receiver sensitivity and the shorter the detection distance. Usually, when designing a λ / 4 dipole antenna, it is better to use a single conductive wire （diameter about 0.8 mm to 1.6 mm） rather than a multiple core wire.

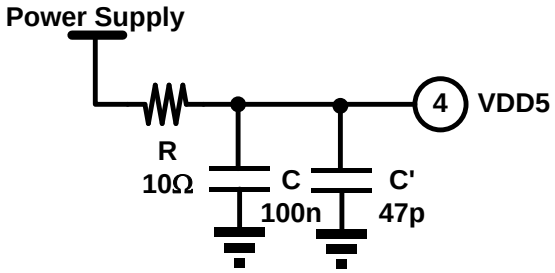
If the antenna is printed on the PCB, ensure there is neither any component nor ground plane underneath the antenna on the backside of PCB. For an FR4 PCB （ε_r = 4.7） and a strip-width of 30 mil, the length of the antenna, L （in cm）, is calculated by

$$L = \frac{c}{4 \times f \times \sqrt{\varepsilon_r}}$$ where "c" is the speed of light （3 x10^{10} cm / s）.

PCB LAYOUT CONSIDERATION

Proper PCB layout is extremely critical in achieving good RF performance. At the very least, using a two-layer PCB is strongly recommended, so that one layer may incorporate a continuous ground plane. A large number of via holes should connect the ground plane areas between the top and bottom layers. Note that if the PCB design incorporates a printed loop antenna, there should be no ground plane beneath the antenna.

Careful consideration must also be paid to the supply power and ground at the board level. The larger ground area plane should be placed as close as possible to all the VSS pins. To reduce supply bus noise coupling, the power supply trace should be incorporate series-R, shunt-C filtering as shown below.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage Range	V_{DD5}	–0.3	6	V
Analog I / O Voltage	—	–0.3	3	V
Digital I / O Voltage	—	–0.3	6	V
Operating Temperature Range	T_A	–40	+85	°C
Storage Temperature Range	T_{STG}	–40	+125	°C
ESD Rating （HBM）	V_{ESD} （HBM）	±4000	—	V
ESD Rating （MM）	V_{ESD} （MM）	±400	—	V
ESD Rating （CDM）	V_{ESD} （CDM）	±1000	—	V

PACKAGE THERMAL CHARACTERISTIC

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
From Chip Conjunction Dissipation to External Environment	Rja	T_A = 27 °C	—	37.15	—	°C / W
From Chip Conjunction Dissipation to Package Surface	Rjc		—	1	1.8	

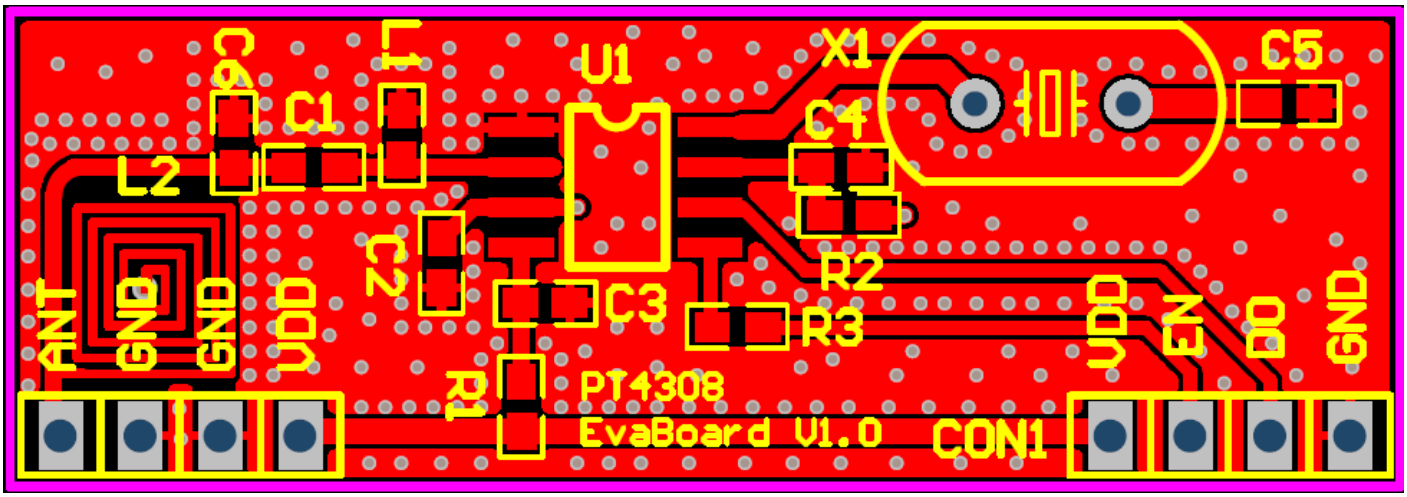
ELECTRICAL CHARACTERISTICS

Nominal conditions: V_{DD5} = 5.0 V, V_{SS} = 0 V, f_{RF} = 433.92 MHz, CE = HIGH, T_A = +27°C.

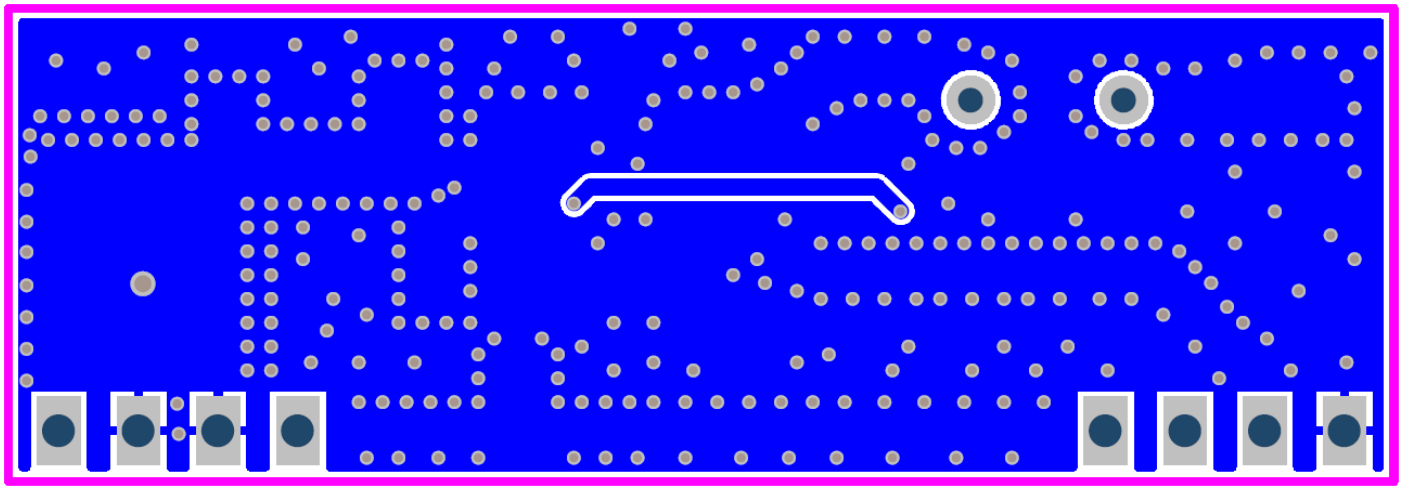
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General Characteristics						
Supply Voltage	V_{DD5}	Supply voltage applied to VDD5 pin only	2.1	5.0	5.5	V
Current Consumption	I_{DD5}		—	4.3	—	mA
Standby Current	I_{STBY}	CE = LOW	—	—	1	μA
Operating Frequency Range	f_{RF}		390	433.92	480	MHz
Maximum Receiver Input Level	$P_{RF,MAX}$		–20	–15	—	dBm
Sensitivity[1]	S_{IN}	ASK[2], D_{RATE} = 2 Kb / s, Peak power level	—	–114	—	dBm
		OOK, D_{RATE} = 2 Kb / s, Peak power level	—	–108	—	
Data Rate	D_{RATE}		—	2	10	Kb / s
System Start-Up Time[3]	T_{STUP}	With fast start-up circuit	—	2	3	ms
RF Front-End						
Image Rejection Ratio	IRR		—	25	—	dB
LO Leakage	L_{LO}	Measured at antenna input	—	—	–80	dBm
IF Section						
IF Center Frequency	f_{IF}		—	1.236	—	MHz
IF Bandwidth	BW_{IF}		—	380	—	KHz
RSSI Slope	SL_{RSSI}		—	8	—	mV / dB
Receive Modulation Duty Cycle	DUTY		20	—	80	%
Demodulator						
Post-Demodulator Filter Bandwidth	BW_{DF}		—	5.0	—	KHz
CTH Leakage Current	I_{ZCTH}	T_A = +85 °C	—	±100	—	nA
Phase-Locked Loop						
Reference Frequency	f_{REFOSC}		—	13.598	—	MHz
Reference Signal Voltage Swing[4]	V_{REF}	Peak-to-peak voltage （V_{PP}）	0.3	—	2	V
VCO Frequency Range	f_{VCO}		370	—	500	MHz
Divider Ratio	DIV		—	32	—	—
Digital / Control Interface						
Input-High Voltage	V_{IH}	For CE pin	0.8 × V_{DD5}	—	—	V
Input-Low Voltage	V_{IL}	For AGCDIS, CE, FDIV, SELA and SELB pins	—	—	0.2 × V_{DD5}	V
Output Current	I_{OUT}	Source current at 0.8 × V_{DD5}	—	480	—	μA
		Sink current at 0.2 × V_{DD5}	—	600	—	
Output-High Voltage	V_{OH}	DO pin, I_{OUT} = –1 μA	0.9 × V_{DD5}	—	—	V
Output-Low Voltage	V_{OL}	DO pin, I_{OUT} = +1 μA	—	—	0.1 × V_{DD5}	V
Output Rise / Fall Times	t_R / t_F	DO pin, C_{LOAD} = 15 pF	—	2	—	μs

Notes:
1. Packet Error Rate （PER） < 1e-2 with one byte packet of $A5_{hex}$.
2. AM 99% with square-wave modulation
3. Depends on the coding pattern and values of peripheral components
4. Depends on the ESR of crystal

EVALUATION BOARD LAYOUT



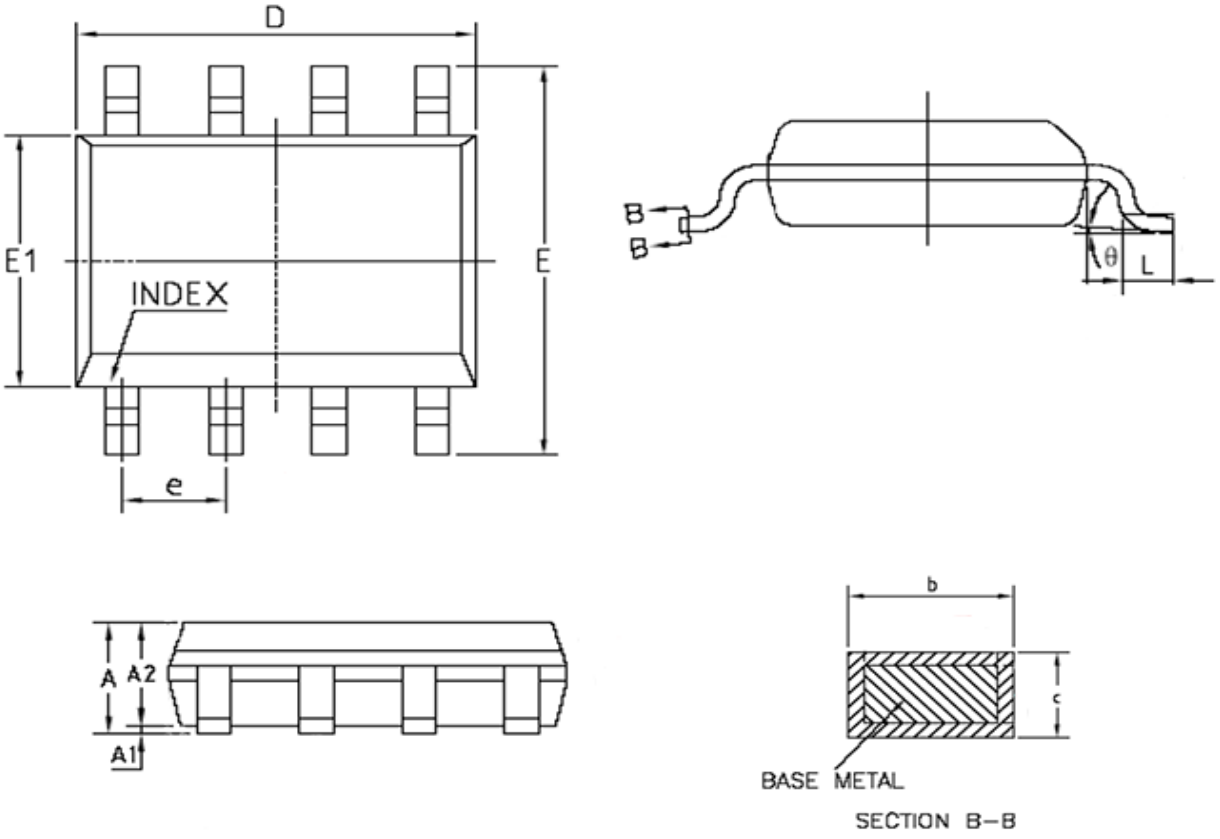
<Top Side>



<Bottom Side>

PACKAGE INFORMATION

8 Pins, SOP（Small Outline Package with 3.9 mm × 4.9 mm Body Size, 1.27 mm Pitch Size and 1.5 mm Thick Body）



Symbol	Dimensions（mm）		
	Min.	Nom.	Max.
A	1.40	1.50	1.60
A1	0.00	—	0.10
A2	—	1.45	—
B	0.33	—	0.51
C	0.19	—	0.25
D	4.80	—	5.00
E1	3.80	3.90	4.00
e	—	1.27	—
E	5.80	6.00	6.20
L	0.40	—	1.27
θ	0º	—	8º

Notes:

1. Refer to JEDEC MS-012 AA
2. Unit: mm

IMPORTANT NOTICE

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