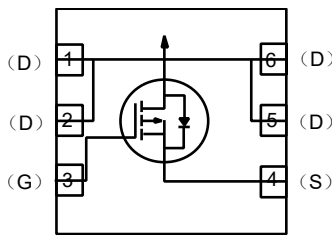


Description

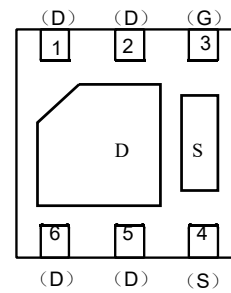
The enhancement mode MOS is extremely high density cell and low on-resistance.

MOSFET Product Summary		
V _{DS} (V)	R _{DS(on)} (mΩ)	I _D (A)
-30	21 @ V _{GS} =-4.5V	-9

Internal structure



Bottom View



Absolute maximum rating@25°C

Rating	Symbol	Value	Units	
Drain-Source Voltage	V _{DS}	-30	V	
Gate-Source Voltage	V _{GS}	±12	V	
Drain Current	Continuous T _A =25°C	I _D	-9	A
	Pulsed T _A =70°C	I _D	-36	A
Total Power Dissipation	T _A =25°C	P _D	2.4	W
	T _A =125°C	P _D	0.9	W
Operating and Storage Junction Temperature Range	T _J , T _{STG}	-55 to +150	°C	

Thermal Characteristics

Parameter	Symbol	Max.	Units
Thermal Resistance, Junction to Ambient (Note 1)	R _{θJA}	52	°C/W
Thermal Resistance, Junction to Ambient (Note 2)	R _{θJA}	145	
Thermal Resistance, Junction to Case	R _{θJC}	6.9	

Electrical characteristics per line@25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = -250\mu A, V_{GS} = 0V$	-30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30V, V_{GS} = 0V$	-	-	-1.0	μA
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS} = \pm 12V$	-	-	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.6	-1.0	-1.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -5.5A$	-	21	28	m Ω
		$V_{GS} = -2.5V, I_D = -5A,$	-	28	40	m Ω
Maximum Body-Diode Continuous Current	I_s	-	-	-	2	A
Forward Trans conductance	g_{FS}	$V_{DS} = -5V, I_D = -9A$	21	-	-	S
Total Gate Charge	Q_g	$I_D = -9A, V_{DD} = -6V,$ $V_{GS} = -4.5V$	-	13.8	-	nC
Gate-to-Source Charge	Q_{gs}		-	2.5		
Gate-to-Drain(Miller) Charge	Q_{gd}		-	3.3		
Input Capacitance	C_{ISS}	$V_{GS} = 0V, V_{DS} = -15V,$ $f = 1MHz$	-	780		pF
Output Capacitance	C_{DSS}		-	150		pF
Reverse Transfer Capacitance	C_{RSS}		-	98		pF
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6.0V, I_D = -9A,$ $V_{GS} = -4.5V, R_{GEN} = 6\Omega,$	-	11	-	ns
Rise Time	t_r		-	8	-	
Turn-Off Delay Time	$t_{d(off)}$		-	28.5	-	
Fall Time	t_f		-	10.5	-	
Source to Drain Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_s = -2A$		-0.6	-1.2	V

Note1: Surface mounted on FR4 Board using 1 square inch pad size, 1oz copper

Note2: Surface mounted on FR4 board using minimum pad size, 1oz copper

Note3: Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

Note4: Guaranteed by design, not subject to production

Typical Characteristics

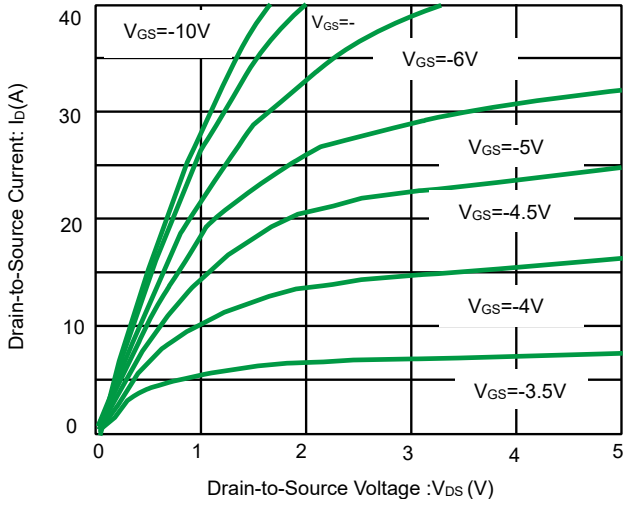


Fig 1. Output Characteristics

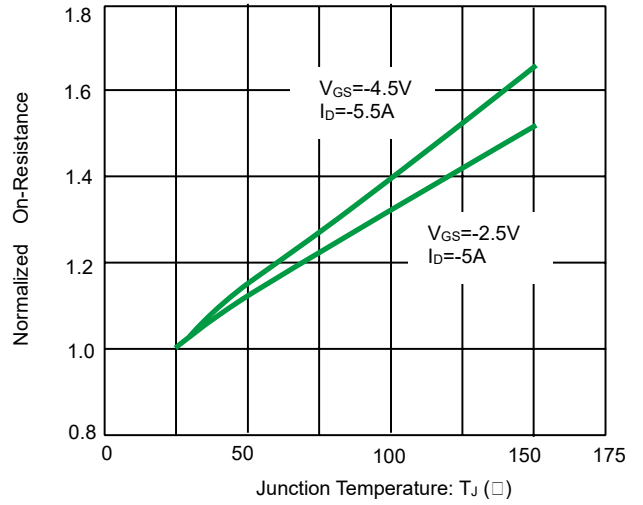


Fig 2. Normalized On-Resistance vs. Junction Temperature

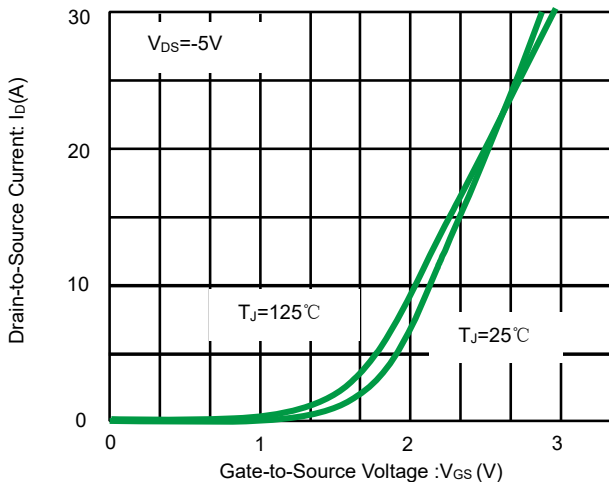


Fig 3. Transfer Characteristics

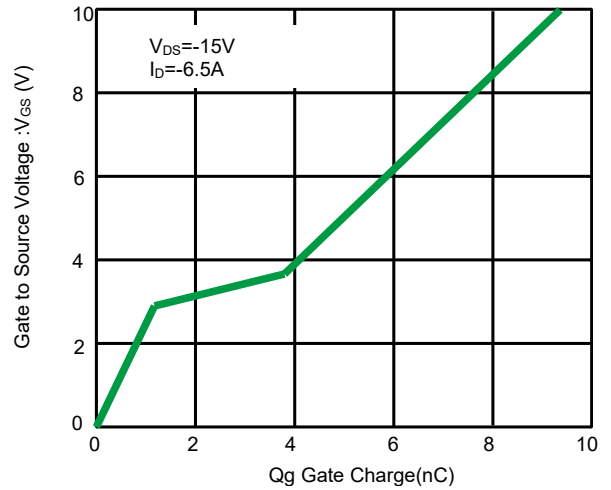


Fig 4. Gate Charge

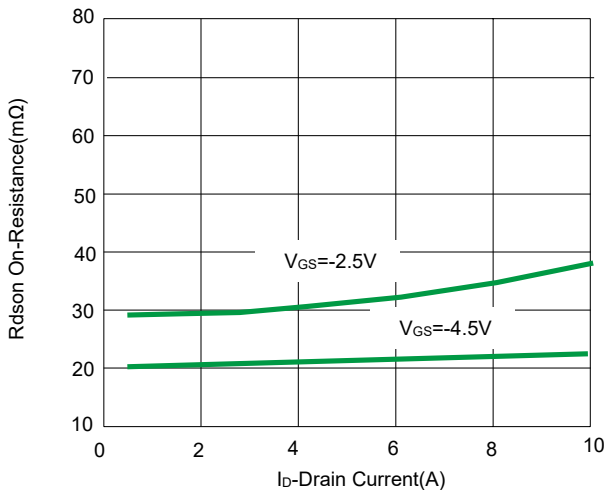


Fig 5. Rdson-Drain Current

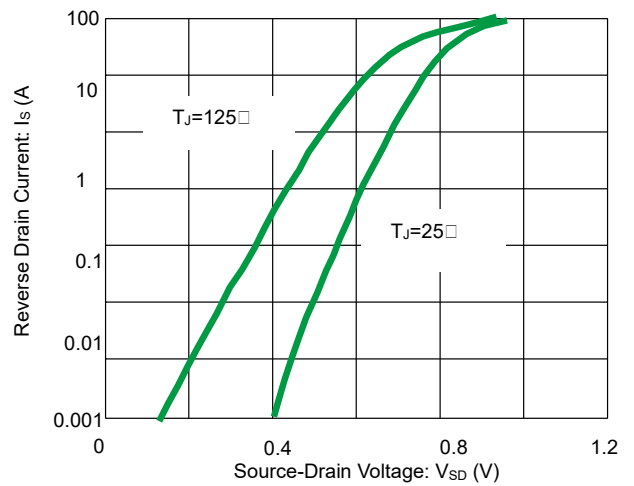


Fig 6. Source to Drain Diode Forward Voltage vs. Source Current

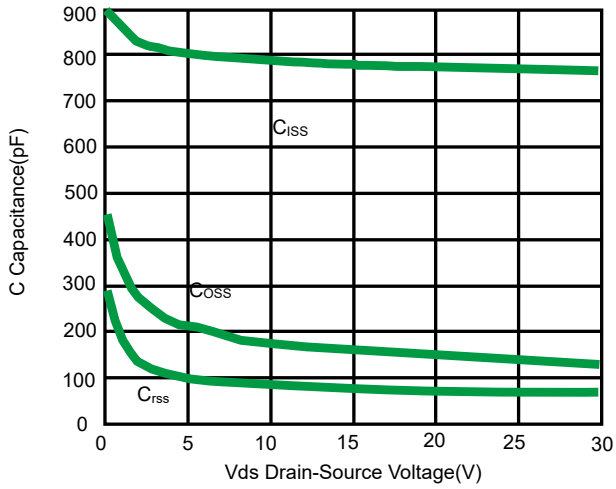


Fig 7. Capacitance vs Vds

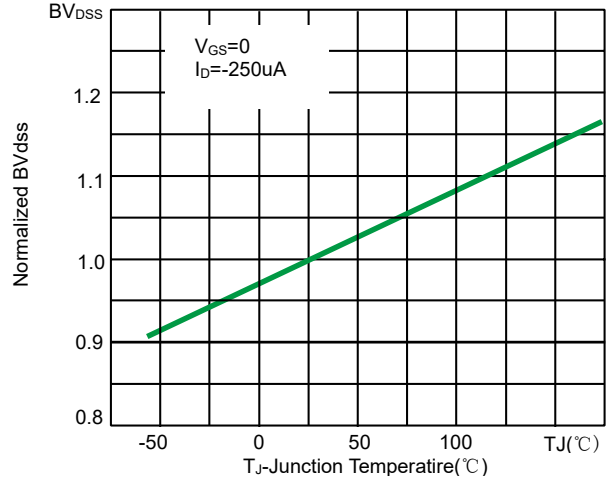


Fig 8. BV_{DSS} vs Junction Temperature

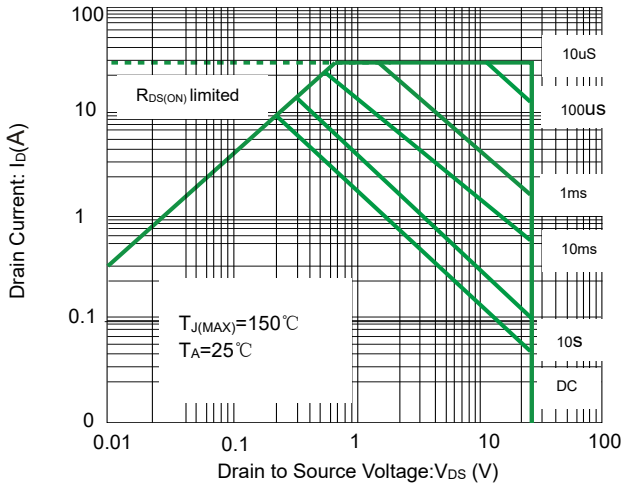


Fig 9. Forward Bias Safe Operating Area

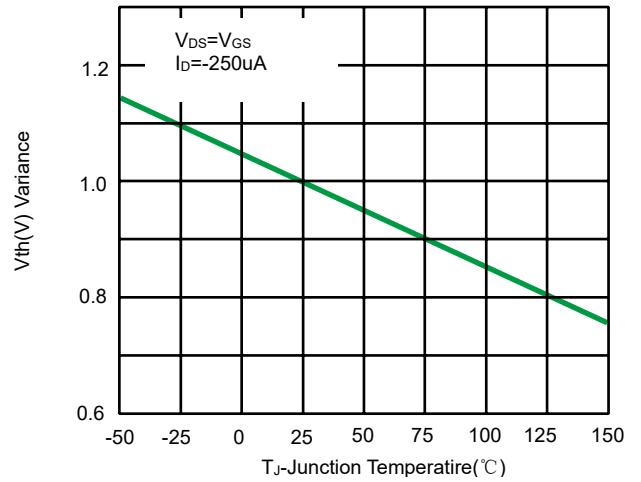


Fig 10. V_{GS(th)} vs Junction Temperature

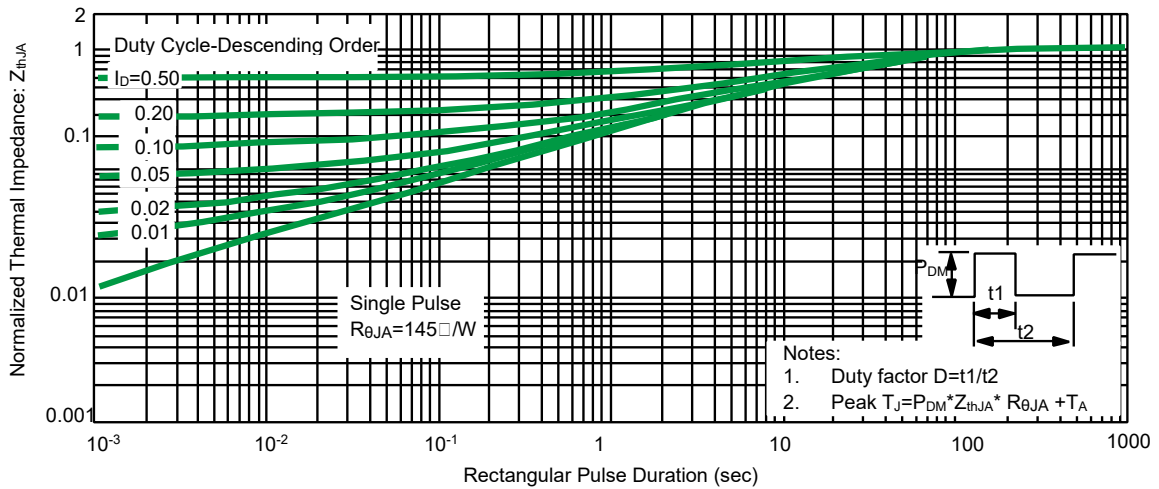
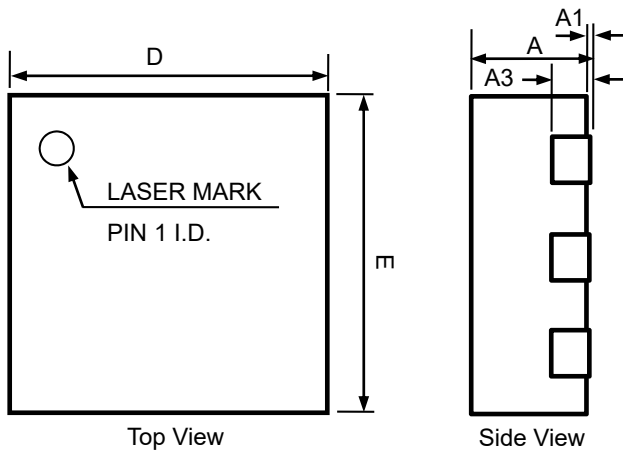
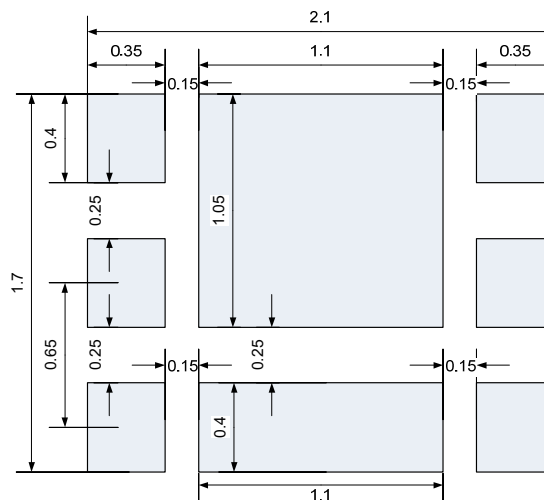
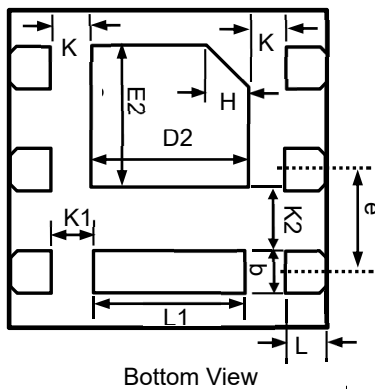


Fig 11. Transient Thermal Response Curve, Junction-to-Ambient

Product dimension (DFN2*2-6L)



Dim	Millimeters		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 Ref.		
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
e	0.55	0.65	0.75
H	0.25 Ref.		
K	0.15	--	--
K1	0.20	--	--
K2	0.25	--	--
L	0.20	0.25	0.30
L1	0.65	0.75	0.85




Suggested PCB Layout

Ordering information

Device	Package	Reel	Shipping
PPM6N30V9	DFN2*2-6L (Pb-Free)	7"	3000 / Tape & Reel


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