Peregrine Semiconductor

Product Specification

PE42520

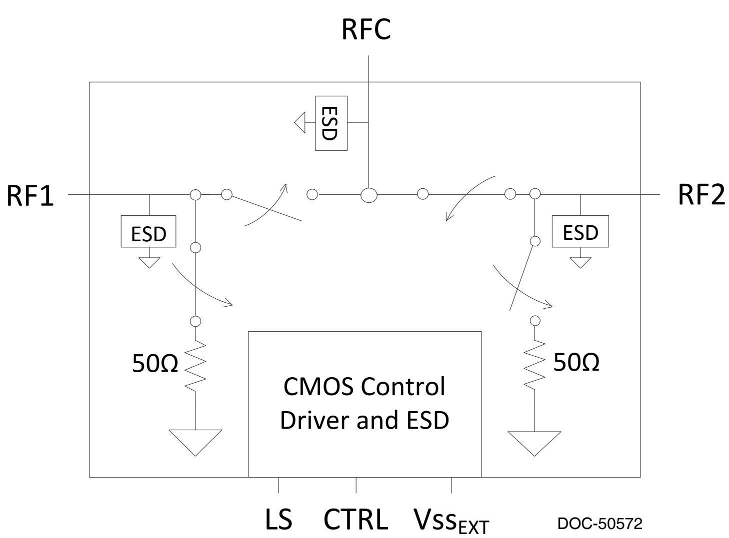
UltraCMOS® SPDT RF Switch 9 kHz–13 GHz

Product Description

The PE42520 SPDT absorptive RF switch is designed for use in Test/ATE and other high performance wireless applications. This broadband general purpose switch maintains excellent RF performance and linearity from 9 kHz through 13 GHz. This switch is a pin-compatible upgraded version of PE42552 with higher power handling of 36 dBm continuous wave (CW) and 38 dBm instantaneous power in 50Ω @ 8 GHz. The PE42520 exhibits high isolation, fast settling time, and is offered in a 3 × 3 mm QFN package.

The PE42520 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration

Figure 1. Functional Diagram



Features

- HaRP™ technology enhanced
  - Fast settling time
  - No gate and phase lag
  - No drift in insertion loss and phase
- High power handling @ 8 GHz in 50Ω
  - 36 dBm CW
  - 38 dBm instantaneous power
  - 26 dBm terminated port
- High linearity
  - 66 dBm IIP3
- Low insertion loss
  - 0.8 dB @ 3 GHz
  - 0.9 dB @ 10 GHz
  - 2.0 dB @ 13 GHz
- High isolation
  - 45 dB @ 3 GHz
  - 31 dB @ 10 GHz
  - 18 dB @ 13 GHz
- ESD performance
  - 4 kV HBM on RF pins to GND
  - 2.5 kV HBM on all pins
  - 1 kV CDM on all pins

Figure 2. Package Type
16-lead 3 × 3 mm QFN

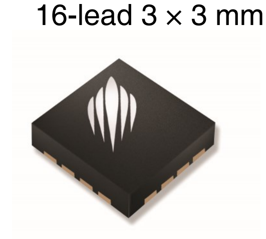


Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3.3V, V_{SS_EXT} = 0V or V_{DD} = 3.4V, V_{SS_EXT} = –3.4V, ($Z_S = Z_L = 50\Omega$), unless otherwise noted

Parameter	Path	Condition	Min	Typ	Max	Unit
Operation frequency			9 kHz		13 GHz	As shown
Insertion loss	RFC–RFX	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz		0.60 0.80 0.85 0.90 1.20 2.00	0.80 1.00 1.05 1.10 1.65 2.70	dB dB dB dB dB dB
Isolation	RFX–RFX	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	70 46 35 24 16 13	90 54 38 27 19 17		dB dB dB dB dB dB
Isolation	RFC–RFX	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz	80 42 41 26 16 13	90 45 44 31 20 18		dB dB dB dB dB dB
Return loss (active port)	RFC–RFX	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz		23 17 15 18 20 10		dB dB dB dB dB dB
Return loss (common port)	RFC–RFX	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz		23 17 15 18 18 10		dB dB dB dB dB dB
Return loss (terminated port)	RFX	9 kHz–10 MHz 10 MHz–3 GHz 3 GHz–7.5 GHz 7.5 GHz–10 GHz 10 GHz–12 GHz 12 GHz–13 GHz		32 24 21 13 8 5		dB dB dB dB dB dB
Input 0.1dB compression point[1]	RFC–RFX	10 MHz–13 GHz		*Fig. 5*		dBm
Input IP2	RFC–RFX	834 MHz, 1950 MHz		120		dBm
Input IP3	RFC–RFX	834 MHz, 1950 MHz, and 2700 MHz		66		dBm
Settling time		50% CTRL to 0.05 dB final value		15	20	µs
Switching time		50% CTRL to 90% or 10% of final value		5.5	9.5	µs

Note 1: The input 0.1dB compression point is a linearity figure of merit. Refer to *Table 3* for the RF input power P_{IN} (50Ω).

Figure 3. Pin Configuration (Top View)

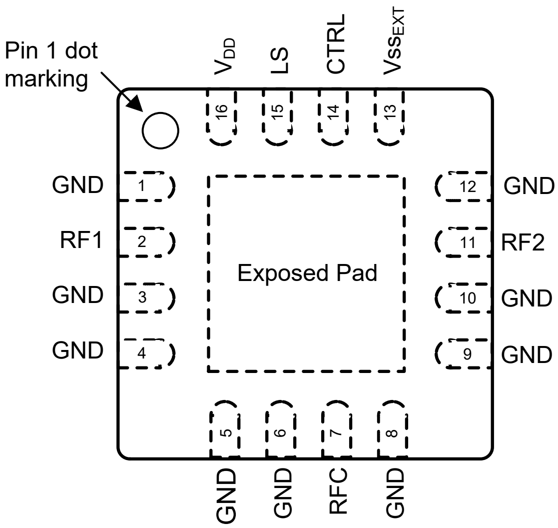


Table 2. Pin Descriptions

Pin #	Pin Name	Description
2	RF1[1]	RF port 1
1, 3, 4, 5, 6, 8, 9, 10, 12	GND	Ground
7	RFC[1]	RF common
11	RF2[1]	RF port 2
13	V_{SS_EXT}[2]	External V_{SS} negative voltage control
14	CTRL	Digital control logic input
15	LS	Logic Select – used to determine the definition for the CTRL pin (see *Table 5*)
16	V_{DD}	Supply voltage
Pad	GND	Exposed pad: ground for proper operation

Notes: 1. RF pins 2, 7 and 11 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Use V_{SS_EXT} (pin 13) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 13) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.

Table 3. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage (normal mode, V_{SS_EXT} = 0V)[1]	V_{DD}	2.3		5.5	V
Supply voltage (bypass mode, V_{SS_EXT} = –3.4V, V_{DD} ≥ 3.4V for full spec. compliance)[2]	V_{DD}	2.7	3.4	5.5	V
Negative supply voltage (bypass mode)[2]	V_{SS_EXT}	–3.6		–3.2	V
Supply current (normal mode, V_{SS_EXT} = 0V)[1]	I_{DD}		120	200	µA
Supply current (bypass mode, V_{SS_EXT} = –3.4V)[2]	I_{DD}		50	80	µA
Negative supply current (bypass mode, V_{SS_EXT} = –3.4V)[2]	I_{SS}	–40	–16		µA
Digital input high (CTRL)	V_{IH}	1.17		3.6	V
Digital input low (CTRL)	V_{IL}	–0.3		0.6	V
Digital input current	I_{CTRL}			10	µA
RF input power, CW (RFC–RFX)[3] 9 kHz ≤ 10 MHz 10 MHz ≤ 8 GHz 8 GHz ≤ 13 GHz	P_{IN_CW}			 *Fig. 4* 36 *Fig. 5*	 dBm dBm dBm
RF input power, pulsed (RFC–RFX)[4] 9 kHz ≤ 10 MHz 10 MHz ≤ 13 GHz	P_{IN_PULSED}			 *Fig. 4* *Fig. 5*	 dBm dBm
RF input power, hot switch, CW[3] 9 kHz ≤ 300 kHz 300 kHz ≤ 13 GHz	P_{IN_HOT}			 *Fig. 4* 20	 dBm dBm
RF input power into terminated ports, CW (RFX)[3] 9 kHz ≤ 600 kHz 600 kHz ≤ 13 GHz	P_{IN_TERM}			 *Fig. 4* 26	 dBm dBm
Operating temperature range	T_{OP}	–40	+25	+85	°C

Notes: 1. Normal mode: connect V_{SS_EXT} (pin 13) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2. Bypass mode: use V_{SS_EXT} (pin 13) to bypass and disable internal negative voltage generator.
3. 100% duty cycle, all bands, 50Ω.
4. Pulsed, 5% duty cycle of 4620 µs period, 50Ω.

Table 4. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	–0.3	5.5	V
Digital input voltage (CTRL)	V_{CTRL}	–0.3	3.6	V
LS input voltage	V_{LS}	–0.3	3.6	V
RF input power, CW (RFC–RFX)[1] 9 kHz ≤ 10 MHz 10 MHz ≤ 8 GHz 8 GHz ≤ 13 GHz	P_{IN_CW}		*Fig. 4* 36 *Fig. 5*	dBm dBm dBm
RF input power, pulsed (RFC–RFX)[2] 9 kHz ≤ 10 MHz 10 MHz ≤ 13 GHz	P_{IN_PULSED}		*Fig. 4* *Fig. 5*	dBm dBm
RF input power into terminated ports, CW (RFX)[1] 9 kHz ≤ 10 MHz 10 MHz ≤ 13 GHz	P_{IN_TERM}		*Fig. 4* 26	dBm dBm
Maximum junction temperature	T_{J_MAX}		+150	°C
Storage temperature range	T_{ST}	–65	+150	°C
ESD voltage HBM[3] RF pins to GND All pins	V_{ESD_HBM}		4000 2500	V V
ESD voltage MM[4], all pins	V_{ESD_MM}		200	V
ESD voltage CDM[5], all pins	V_{ESD_CDM}		1000	V

Notes: 1. 100% duty cycle, all bands, 50Ω.
2. Pulsed, 5% duty cycle of 4620 μs period, 50Ω.
3. Human Body Model (MIL-STD 883 Method 3015).
4. Machine Model (JEDEC JESD22-A115).
5. Charged Device Model (JEDEC JESD22-C101).

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified.

Latch-up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Switching Frequency

The PE42520 has a maximum 25 kHz switching rate when the internal negative voltage generator is used (pin 13 = GND). The rate at which the PE42520 can be switched is only limited to the switching time (*Table 1*) if an external negative supply is provided (pin 13 = V_{SS_EXT}).

Switching frequency describes the time duration between switching events. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its

Optional External Vss Control (V_{SS_EXT})

For proper operation, the V_{SS_EXT} control pin must be grounded or tied to the V_{SS} voltage specified in *Table 3*. When the V_{SS_EXT} control pin is grounded, FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spur performance, V_{SS_EXT} can be applied externally to bypass the

Spurious Performance

The typical spurious performance of the PE42520 is –152 dBm when V_{SS_EXT} = 0V (pin 13 = GND). If further improvement is desired, the internal negative voltage generator can be disabled by setting V_{SS_EXT} = –3.4V.

Table 5. Control Logic Truth Table

LS	CTRL	RFC–RF1	RFC–RF2
0	0	off	on
0	1	on	off
1	0	on	off
1	1	off	on

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE42520 in the 16-lead 3 × 3 mm QFN package is MSL3.

Logic Select (LS)

The Logic Select feature is used to determine the definition for the CTRL pin.

Thermal Data

Psi-JT (Ψ_{JT}), junction top-of-package, is a thermal metric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51-2).

$\Psi_{JT} = (T_J - T_T)/P$

where

Ψ_{JT} = junction-to-top of package characterization parameter, °C/W

T_J = die junction temperature, °C

T_T = package temperature (top surface, in the center), °C

P = power dissipated by device, Watts

Table 6. Thermal Data for PE42520

Parameter	Typ	Unit
Ψ_{JT}	51	°C/W
Θ_{JA}, junction-to-ambient thermal resistance	79	°C/W

Figure 4. Power De-rating Curve for 9 kHz–10 MHz (50Ω)

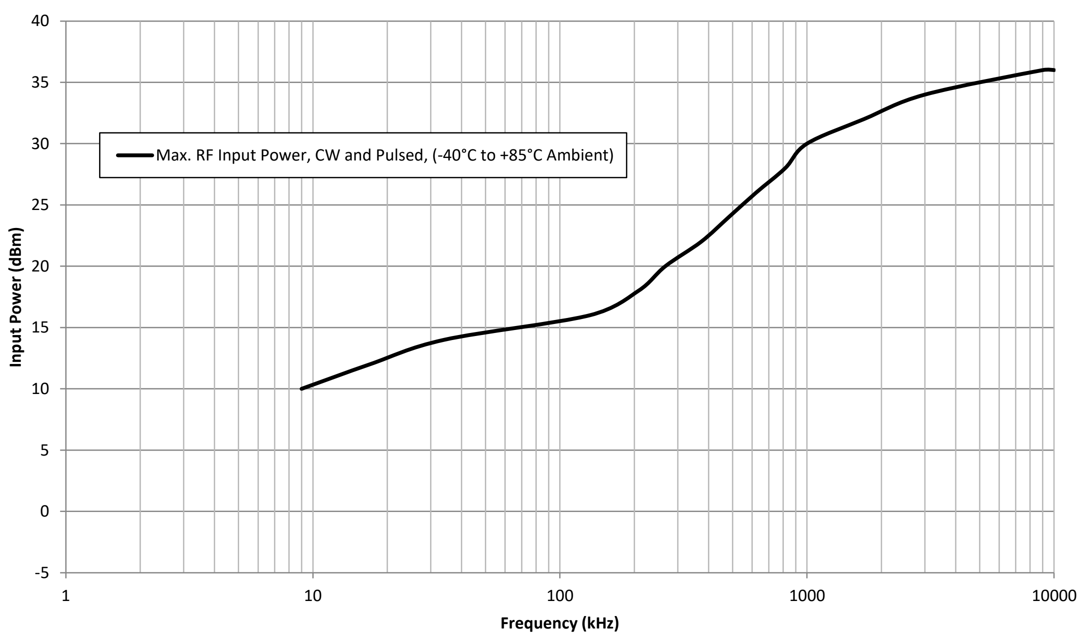


Figure 5a. Power De-rating Curve for 10 MHz–13 GHz @ +25 °C Ambient (50Ω)

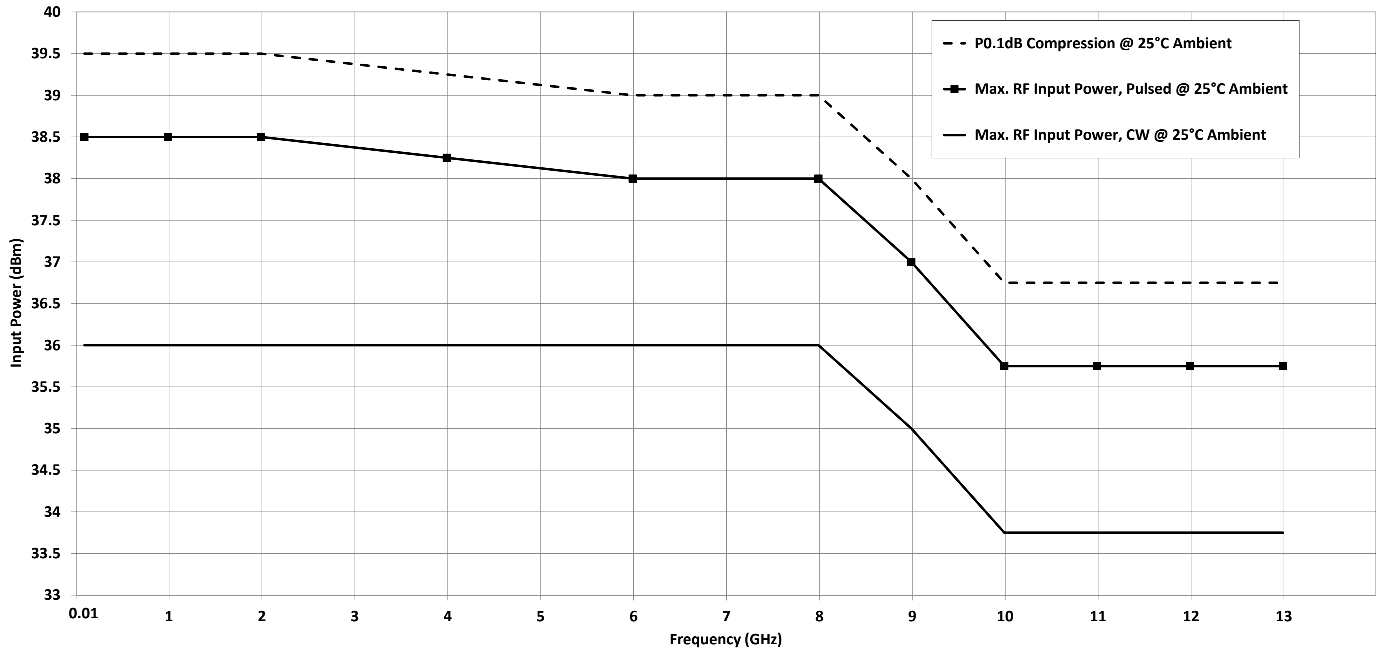
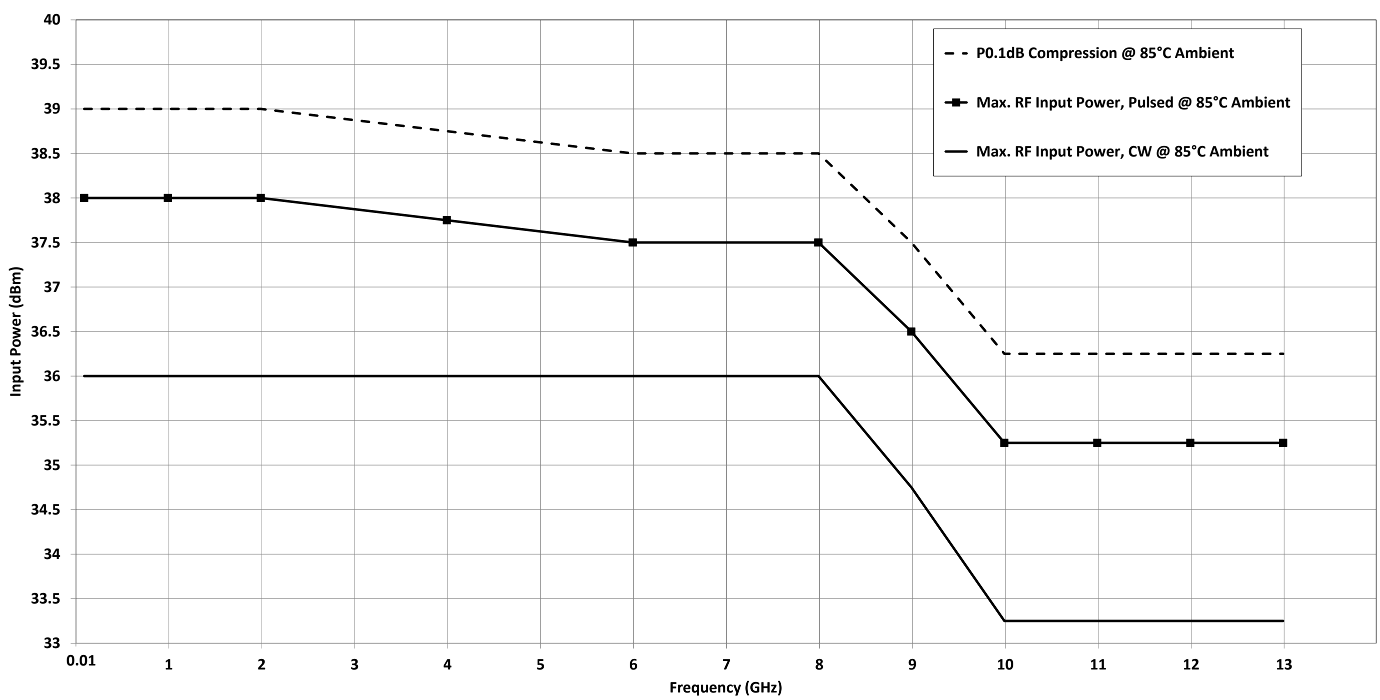


Figure 5b. Power De-rating Curve for 10 MHz–13 GHz @ +85 °C Ambient (50Ω)



Typical Performance Data @ +25 °C and V_{DD} = 3.4V, unless otherwise specified

Figure 6. Insertion Loss vs. Temp (RFC–RF1)

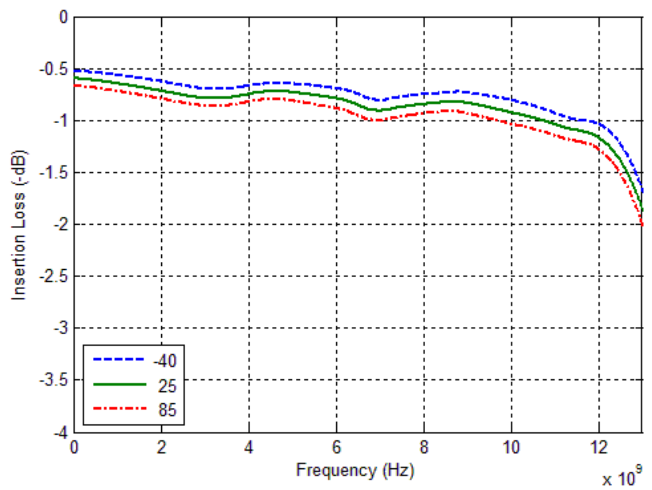


Figure 7. Insertion Loss vs. V_{DD} (RFC–RF1)

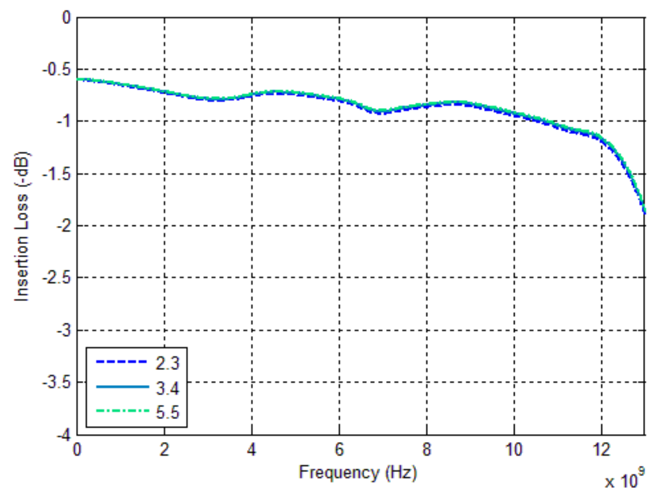


Figure 8. Insertion Loss vs. Temp (RFC–RF2)

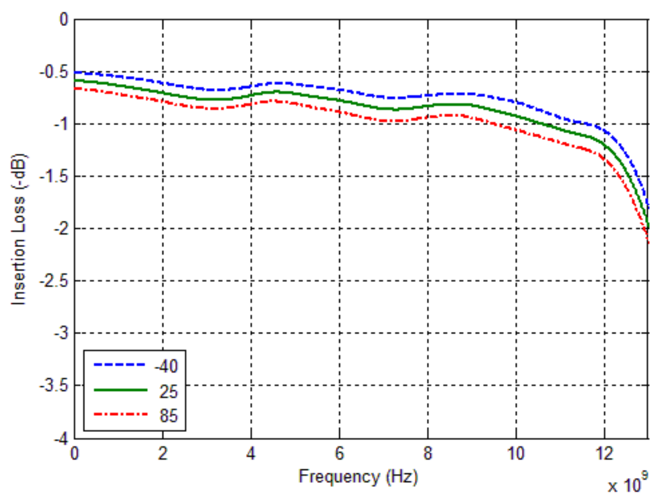
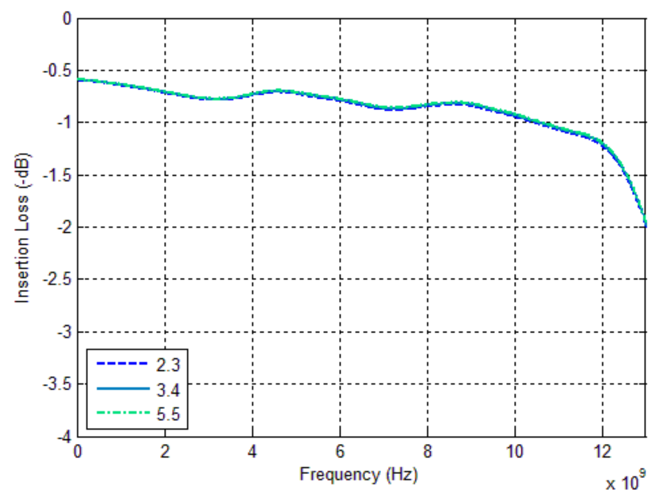


Figure 9. Insertion Loss vs. V_{DD} (RFC–RF2)



Typical Performance Data @ +25 °C and V_{DD} = 3.4V, unless otherwise specified (Cont.)

Figure 10. RFC Port Return Loss vs. Temp (RF1 Active)

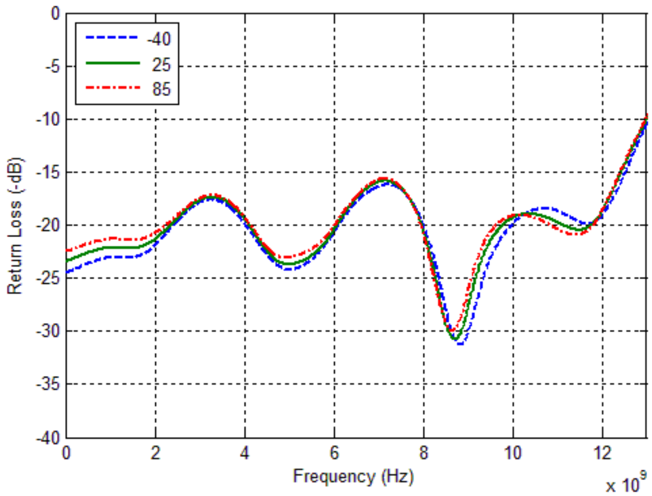


Figure 11. RFC Port Return Loss vs. V_{DD} (RF1 Active)

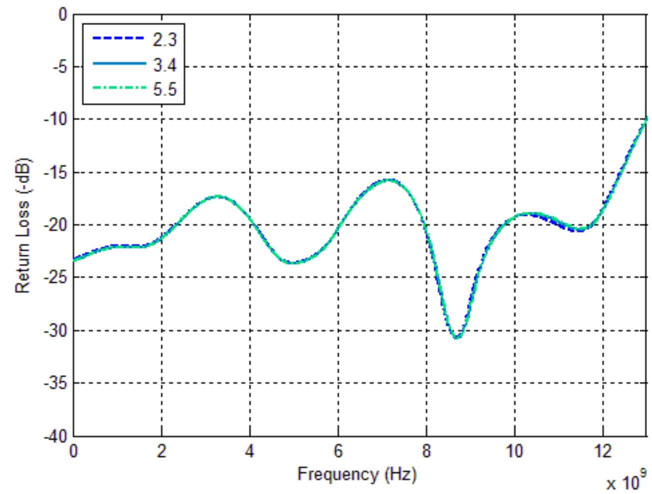


Figure 12. RFC Port Return Loss vs. Temp (RF2 Active)

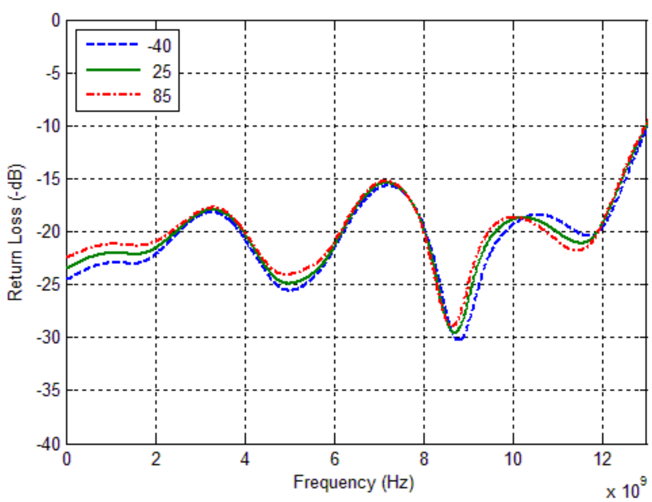
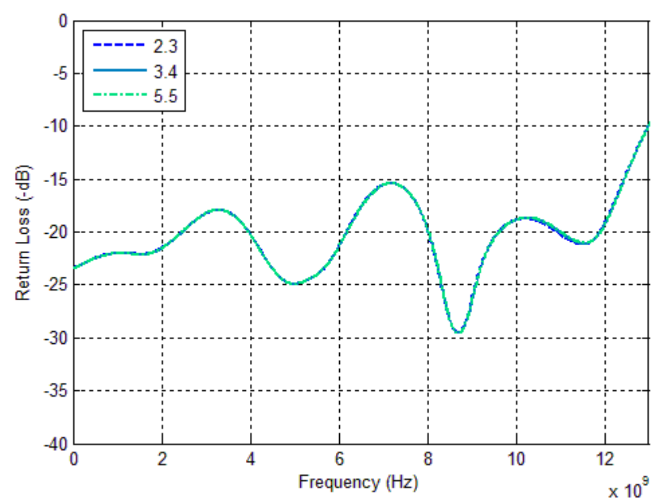


Figure 13. RFC Port Return Loss vs. V_{DD} (RF2 Active)



Typical Performance Data @ +25 °C and V_{DD} = 3.4V, unless otherwise specified (Cont.)

Figure 14. Active Port Return Loss vs. Temp (RF1 Active)

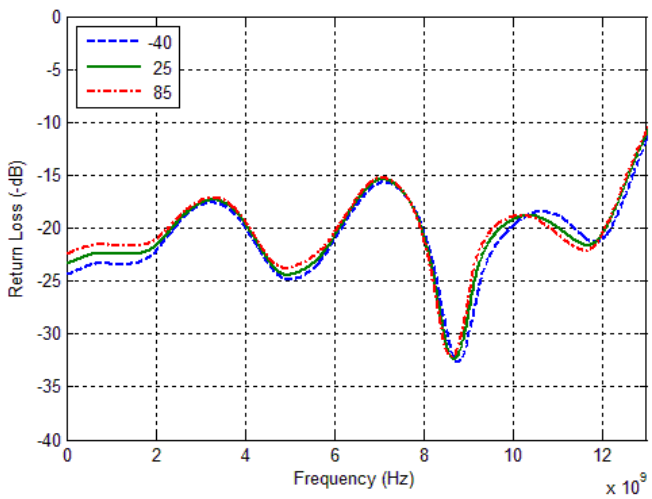


Figure 15. Active Port Return Loss vs. V_{DD} (RF1 Active)

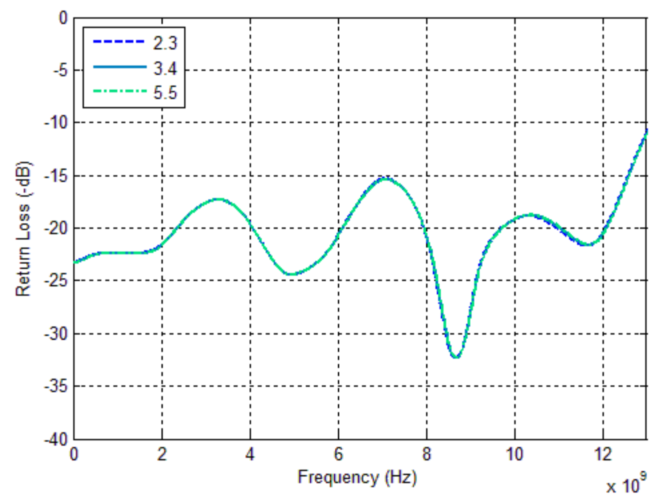


Figure 16. Active Port Return Loss vs. Temp (RF2 Active)

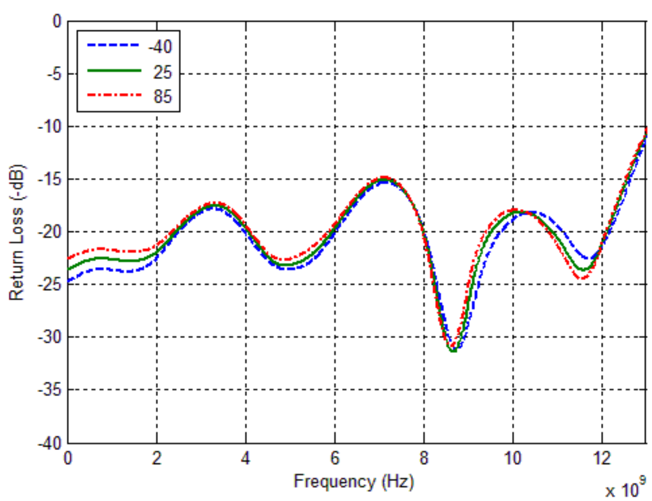
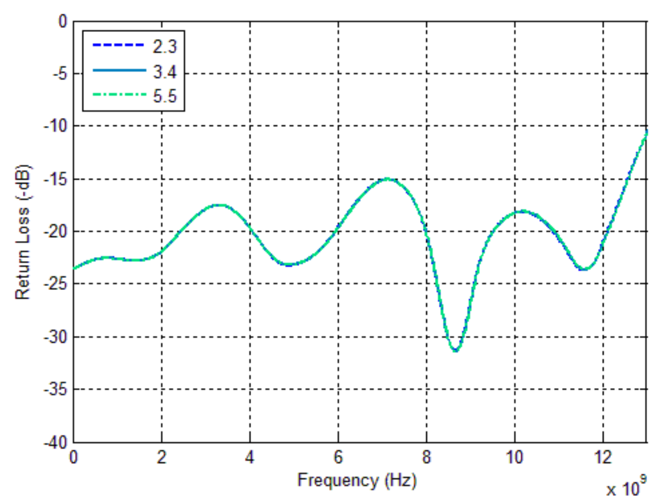


Figure 17. Active Port Return Loss vs. V_{DD} (RF2 Active)



Typical Performance Data @ +25 °C and V_{DD} = 3.4V, unless otherwise specified (Cont.)

Figure 18. Terminated Port Return Loss vs. Temp (RF1 Active)

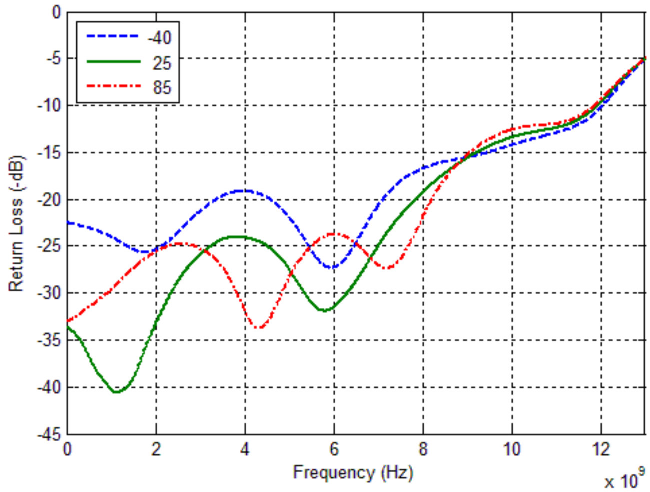


Figure 19. Terminated Port Return Loss vs. V_{DD} (RF1 Active)

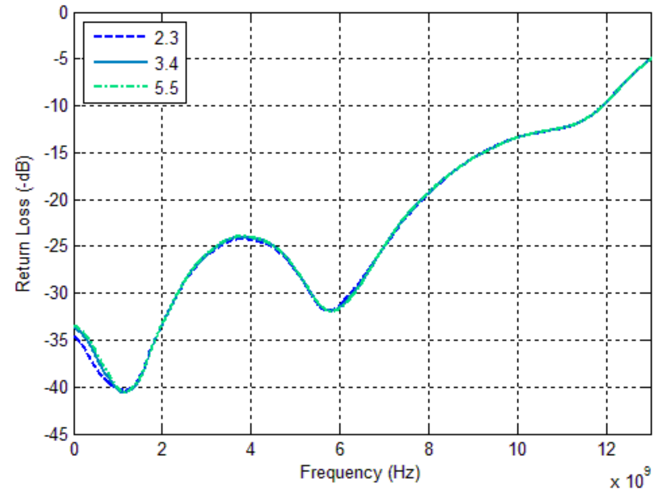


Figure 20. Terminated Port Return Loss vs. Temp (RF2 Active)

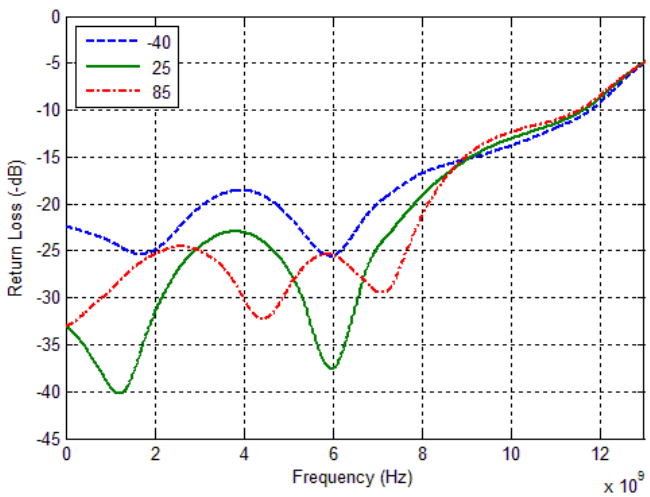
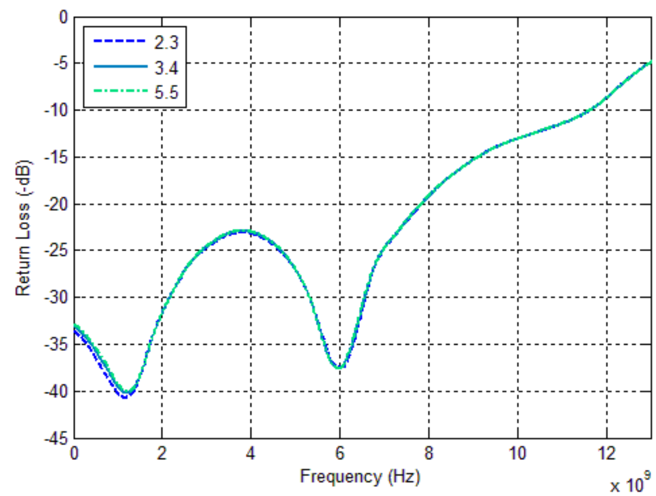


Figure 21. Terminated Port Return Loss vs. V_{DD} (RF2 Active)



Typical Performance Data @ +25 °C and V_{DD} = 3.4V, unless otherwise specified (Cont.)

Figure 22. Isolation vs. Temp (RF1–RF2, RF1 Active)

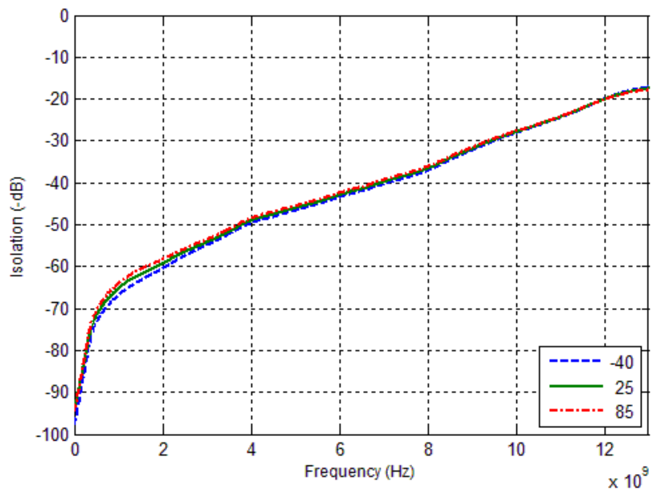


Figure 23. Isolation vs. V_{DD} (RF1–RF2, RF1 Active)

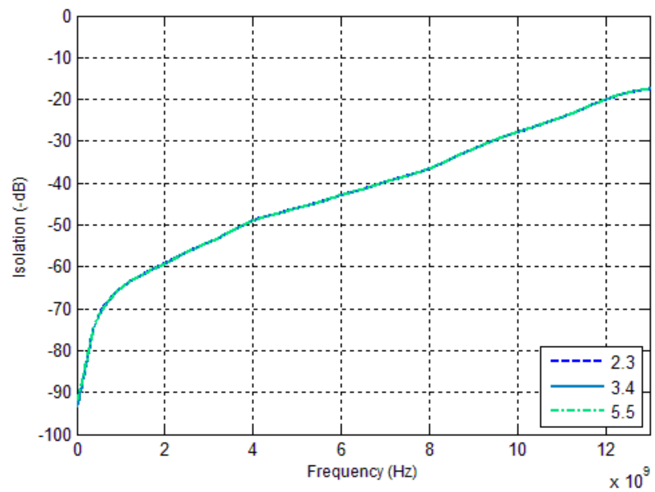


Figure 24. Isolation vs. Temp (RF2–RF1, RF2 Active)

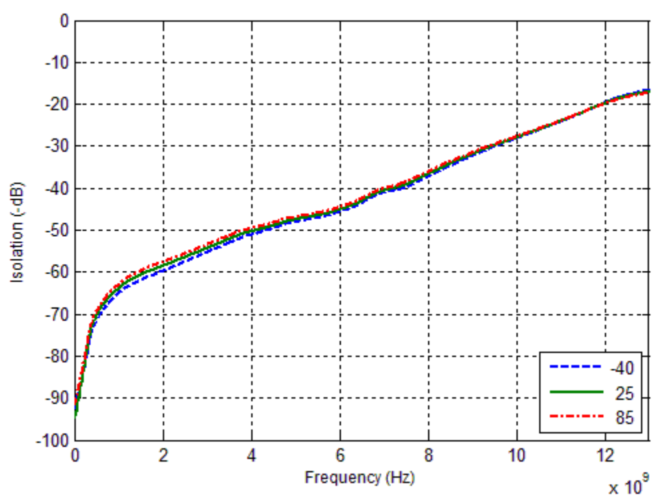
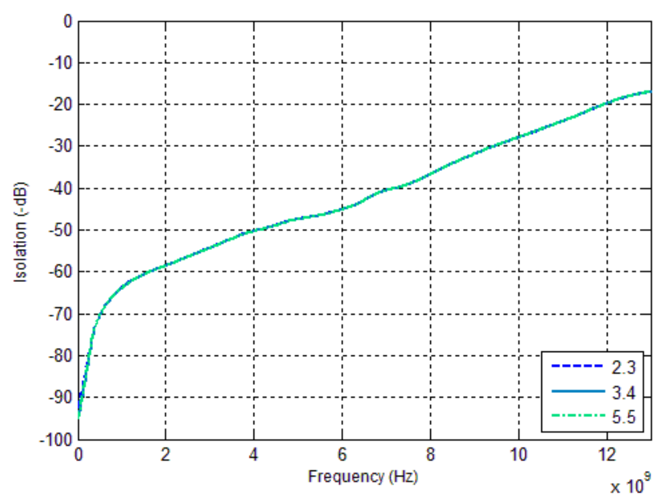


Figure 25. Isolation vs. V_{DD} (RF2–RF1, RF2 Active)



Typical Performance Data @ +25 °C and V_{DD} = 3.4V, unless otherwise specified (Cont.)

Figure 26. Isolation vs. Temp (RFC–RF2, RF1 Active)

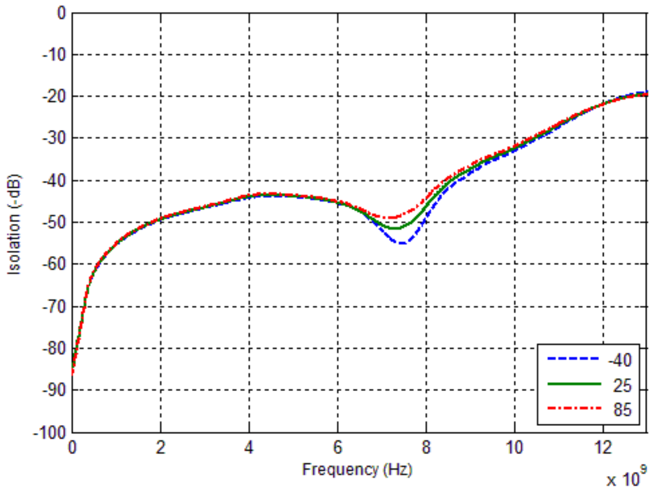


Figure 27. Isolation vs. V_{DD} (RFC–RF2, RF1 Active)

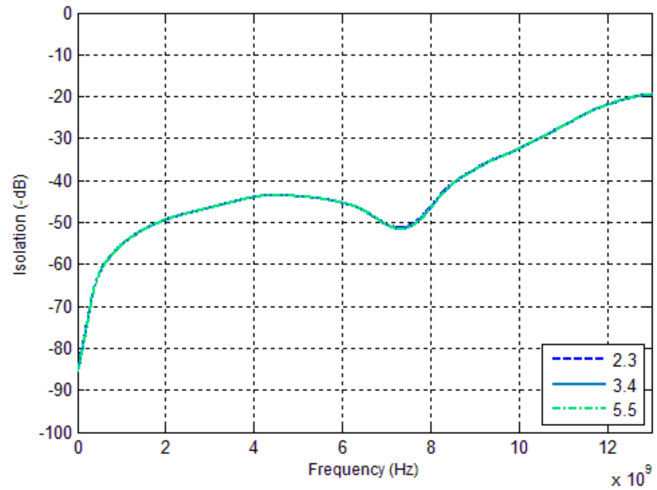


Figure 28. Isolation vs. Temp (RFC–RF1, RF2 Active)

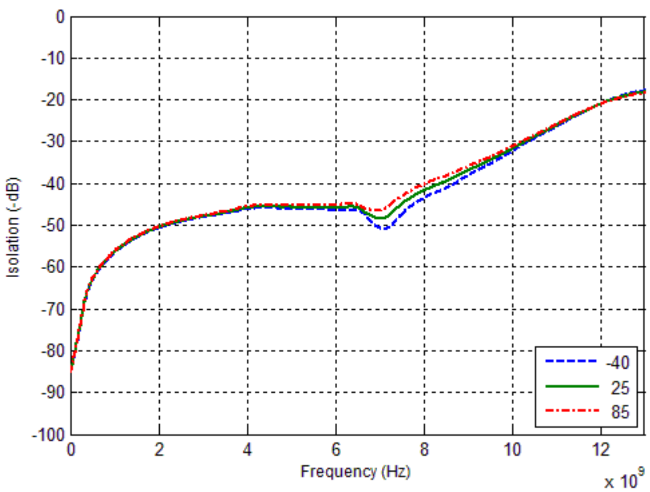
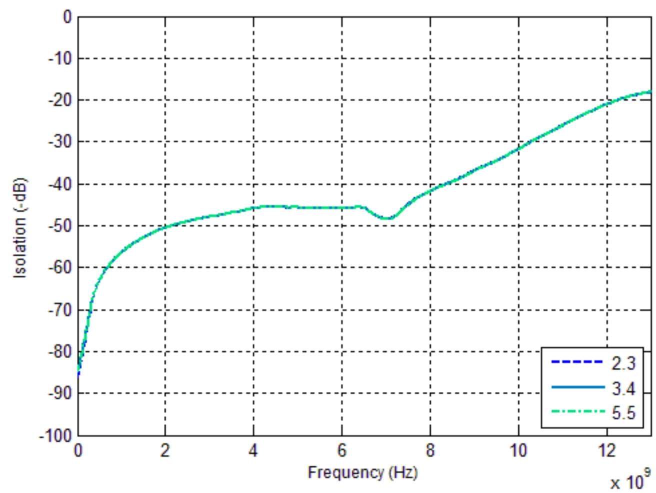


Figure 29. Isolation vs. V_{DD} (RFC–RF1, RF2 Active)

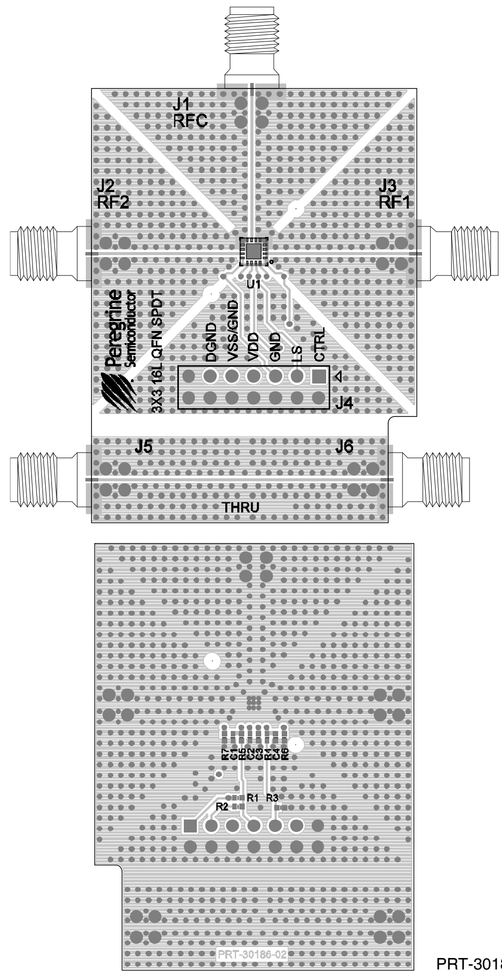


Evaluation Kit

The SPDT switch evaluation board was designed to ease customer evaluation of pSemi's PE42520. The RF common port is connected through a 50Ω transmission line via the SMA connector, J1. RF1 and RF2 ports are connected through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A 50Ω through transmission line is available via SMA connectors J5 and J6, which can be used to de-embed the loss of the PCB. J4 provides DC and digital inputs to the device.

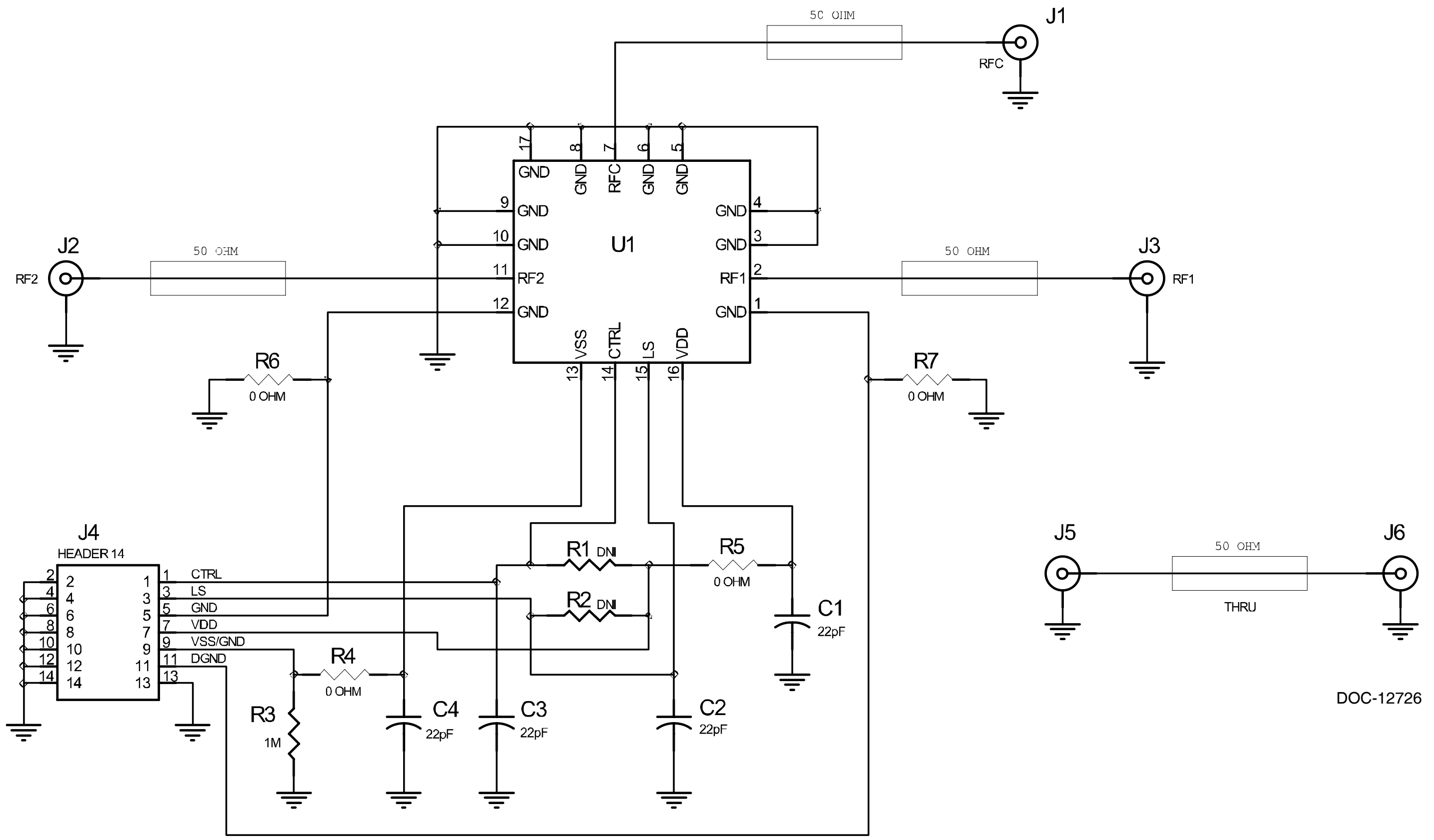
For the true performance of the PE42520 to be realized, the PCB should be designed in such a way that RF transmission lines and sensitive DC I/O traces are heavily isolated from one another.

Figure 30. Evaluation Kit Layout



PRT-30186

Figure 31. Evaluation Board Schematic



Notes: 1. Use PRT-30186-02 PCB.
2. CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).

Figure 32. Package Drawing

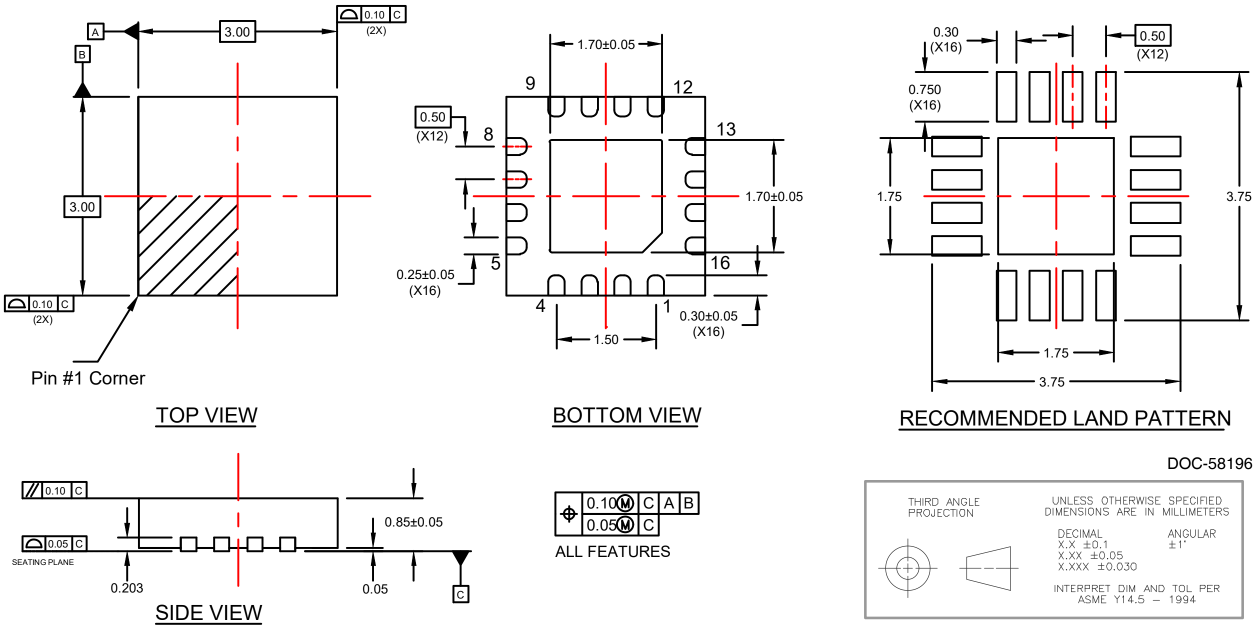
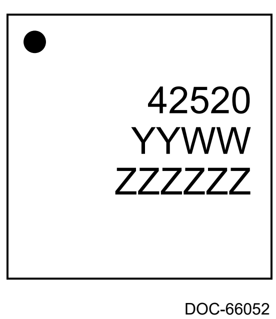
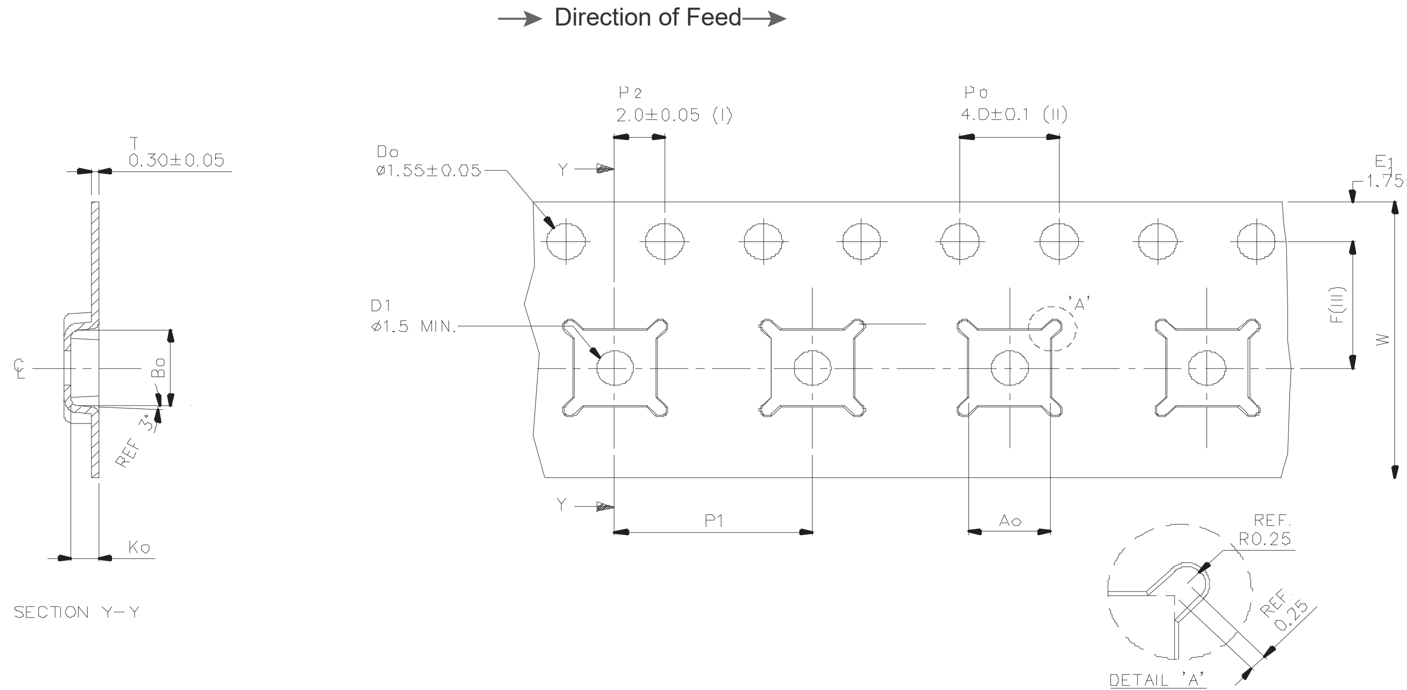


Figure 33. Top Marking Specifications



● = Pin 1 designator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZ = Assembly lot code (maximum six characters)

Figure 34. Tape and Reel Specifications

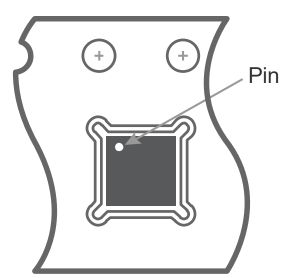


Ao	3.30 ± 0.1
Bo	3.30 ± 0.1
Ko	1.10 ± 0.1
F	5.50 ± 0.05
P1	8.00 ± 0.1
W	12.00 ± 0.3

Notes:

1. Measured from centerline of sprocket hole to centerline of pocket.
2. Cumulative tolerance of 10 sprocket holes ± 0.20.
3. Measured from centerline of sprocket hole to centerline of sprocket.

Dimensions are in millimeters unless otherwise specified.



Device Orientation in Tape

Table 7. Ordering Information

Order Code	Description	Package	Shipping Method
PE42520C-Z	PE42520 SPDT RF switch	Green 16-lead 3 × 3 mm QFN	3000 units / T&R
EK42520-03	PE42520 Evaluation kit	Evaluation kit	1 / Box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.