PE4152

Document Category: Product Specification

UltraCMOS® Quad MOSFET Mixer

Peregrine Semiconductor

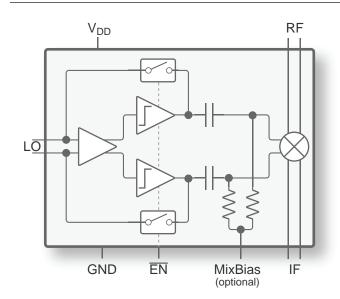
Features

- Quad MOSFET array with integrated LO enable and bypass mode
- · Ultra high linearity in both LO modes
 - LO enable: 25 dBm IIP3, 52 dBm IIP2
 - LO bypass: 24 dBm IIP3, 46 dBm IIP2
- · High isolation in both LO modes
 - LO enable: 30/30 dB LO-RF/IF
 - LO bypass: 60/58 dB LO–RF/IF
- · Low conversion loss in both LO modes
- Packaging 20-lead 4 x 4 x 0.85 mm QFN

Applications

- Land-mobile-radio (LMR)
 - Portable radio
 - Mobile radio
- · Cellular infrastructure
- Set-top box (STB)/CATV systems

Figure 1 • PE4152 Functional Diagram



Product Description

The PE4152 is a high linearity quad metal-oxide-semiconductor field-effect transistor (MOSFET) mixer with an integrated local oscillator (LO) amplifier. The LO amplifier allows for LO input drive levels of less than 0 dBm to produce third-order intercept point (IIP3) values similar to a quad MOSFET array driven with a 15 dBm LO drive. The PE4152 operates with differential signals at the radio frequency (RF) and intermediate frequency (IF) ports and the integrated LO buffer amplifier drives the mixer core. It can be used as an upconverter or a downconverter.

The PE4152 also offers an integrated LO amplifier bypass option providing additional flexibility for low power or increased linearity operation. The bypassed LO amplifier allows superior LO to RF and LO to IF isolation levels relative to the enabled mode.

The PE4152 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.



Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • Absolute Maximum Ratings for PE4152

Parameter/Condition	Min	Max	Unit	
Supply voltage, V _{DD}		4.0	V	
Maximum DC plus peak AC across drain-source		±3.3	V	
Maximum DC current across drain-source		6	mA	
Maximum AC current across drain-source		36	mA _{P-P}	
Storage temperature range	-65	+150	°C	
Operating junction temperature		+125	°C	
ESD voltage HBM, all pins ^(*)		1000	V	
Note: * Human body model (MIL-STD 883 Method 3015).				

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for the PE4152. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • Recommended Operating Conditions for PE4152

Parameter	Min	Тур	Max	Unit
Supply voltage, V _{DD}	2.9		3.1	V
Operating temperature range	-40		+85	°C
LO input power (LO enable)	-10		-6	dBm
LO input power (LO bypass)			23	dBm
RF input power (LO enable)			2	dBm
RF input power (LO bypass)			2	dBm



Electrical Specifications

Table 3 and **Table 4** provide the PE4152 key electrical specifications @ +25 °C, V_{DD} = 3.0V, unless otherwise specified.

Table 3 • PE4152 Electrical Specifications—LO Enable Mode

Parameter	Condition	Min	Тур	Max	Unit	
LO enable mode						
Current drain	A function of frequency		9.5	16	mA	
Off state leakage current				20	μΑ	
RF input frequency	VHF band UHF1 band UHF2 band 700 MHz 800 MHz 900 MHz	136 380 450 764 851 935		174 470 520 776 870 941	MHz MHz MHz MHz MHz MHz	
LO frequency	VHF band UHF1 band UHF2 band 700 MHz 800 MHz 900 MHz	245.65 270.35 340.35 873.65 741.35 825.35		283.65 360.35 410.35 885.65 760.35 831.35	MHz MHz MHz MHz MHz MHz	
IF output frequency			109.65		MHz	
LO input power		-10		-6	dBm	
RF input power				2	dBm	
Conversion loss ⁽¹⁾	VHF, UHF1, UHF2 700, 800 and 900 MHz		6.5 7.3	7.0 8.25	dB dB	
Input IP3 ⁽²⁾		20.5	25		dBm	
Input IP2 ⁽³⁾	VHF, UHF1, UHF2 700, 800 and 900 MHz	45 40	52 50		dBm dBm	
RF to IF isolation ⁽⁴⁾	VHF, UHF1, UHF2 700, 800 and 900 MHz	35 35	45 45		dB dB	
LO to IF isolation		18.5	22		dB	
LO to RF isolation		26	30		dB	

Notes:

- 1) Measured with a 1:1 balun on the RF and IF ports.
- 2) Measured with two tones at 2 dBm, 100 kHz spacing.
- 3) Measured with half-IF method.
- 4) Measured with an input frequency equal with IF.



Table 4 • PE4152 Electrical Specifications—LO Bypass Mode

Parameter	Condition	Min	Тур	Max	Unit
LO bypass mode					
Off state leakage current			20		μA
RF input frequency	VHF band UHF1 band UHF2 band 700 MHz 800 MHz 900 MHz	136 380 450 764 851 935		174 470 520 776 870 941	MHz MHz MHz MHz MHz MHz
LO frequency	VHF band UHF1 band UHF2 band 700 MHz 800 MHz 900 MHz	245.65 270.35 340.35 873.65 741.35 825.35		283.65 360.35 410.35 885.65 760.35 831.35	MHz MHz MHz MHz MHz MHz
IF output frequency			109.65		MHz
LO input power				23	dBm
RF input power				2	dBm
Conversion loss ⁽¹⁾	VHF, UHF1, UHF2 700, 800 and 900 MHz		6.5 7.5	8.0 8.7	dB dB
Input IP3 ⁽²⁾	VHF, UHF1, UHF2 700, 800 and 900 MHz	24 19	26 24		dBm dBm
Input IP2 ⁽³⁾	VHF, UHF1, UHF2 700, 800 and 900 MHz		46 46		dBm dBm
RF to IF isolation ⁽⁴⁾	VHF, UHF1, UHF2 700, 800 and 900 MHz		38 38		dB dB
LO to IF isolation		30	58		dB
LO to RF isolation		35	60		dB
Notes					

Notes:

- 1) Measured with a 1:1 balun on the RF and IF ports.
- 2) Measured with two tones at 2 dBm, 100 kHz spacing.
- 3) Measured with half-IF method.
- 4) Measured with an input frequency equal with IF.



Typical Performance Data

Figure 2-Figure 23 show the typical performance data @ +25 °C, V_{DD} = 3.0V, unless otherwise specified.

Figure 2 • Conversion Loss vs LO Power (LO Enable)

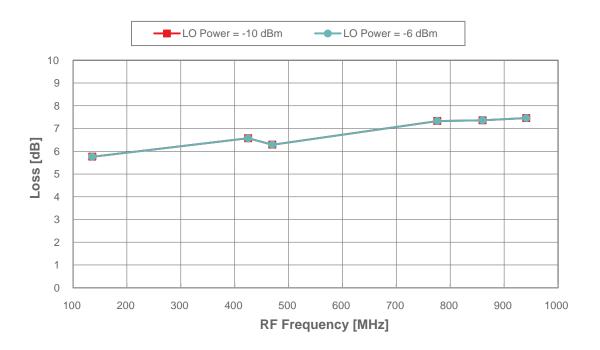


Figure 3 • Conversion Loss vs V_{DD} (LO Enable)

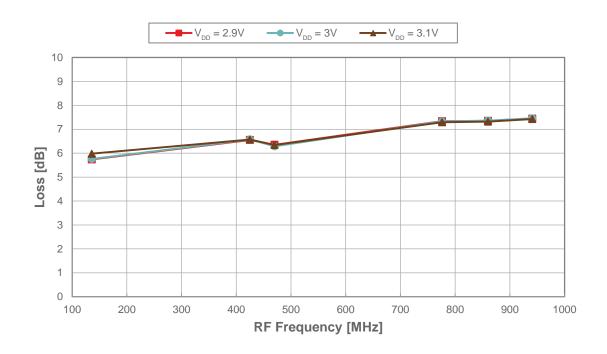




Figure 4 • Conversion Loss vs Temperature (LO Enable)

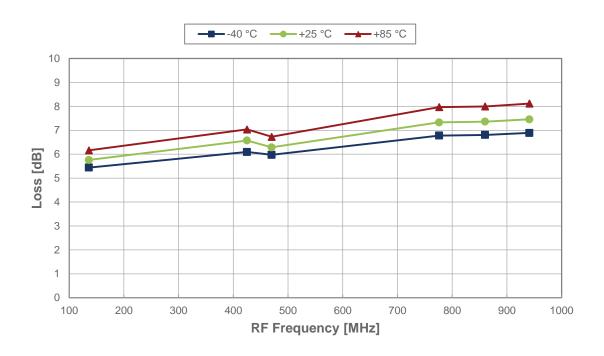


Figure 5 • Conversion Loss vs LO Power (LO Bypass Enable)

Page 6

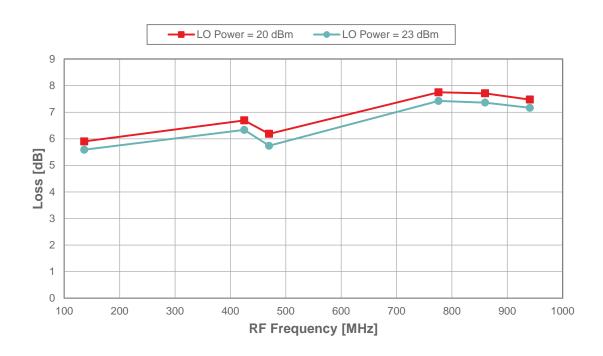




Figure 6 • Conversion Loss vs V_{DD} (LO Bypass Enable)

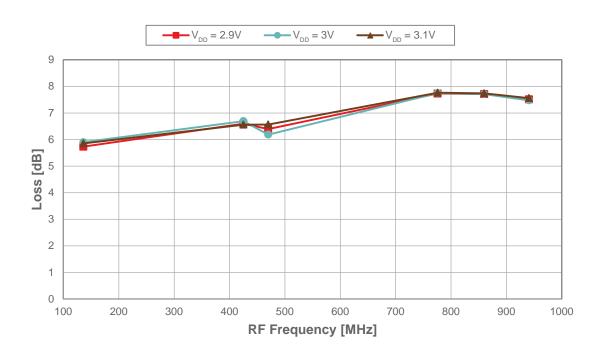


Figure 7 • Conversion Loss vs Temperature (LO Bypass Enable)

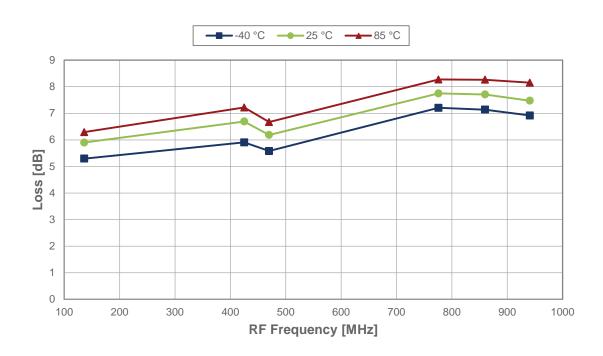




Figure 8 • IIP2 / IIP3 vs LO Power (LO Bypass)

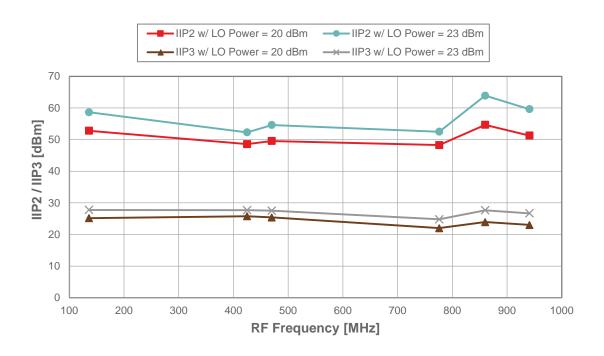


Figure 9 • IIP2 / IIP3 vs Temperature (LO Bypass)

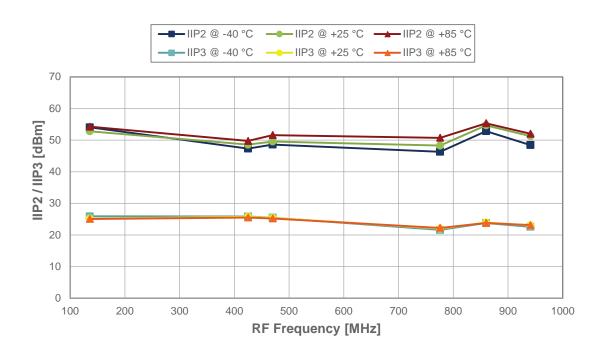




Figure 10 • IIP2 / IIP3 vs LO Power (LO Enable)

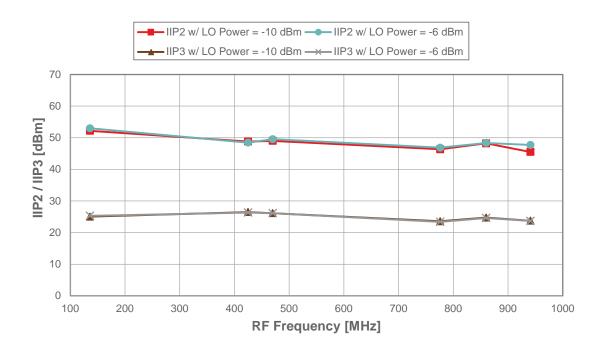


Figure 11 • IIP2 / IIP3 vs Temperature (LO Enable)

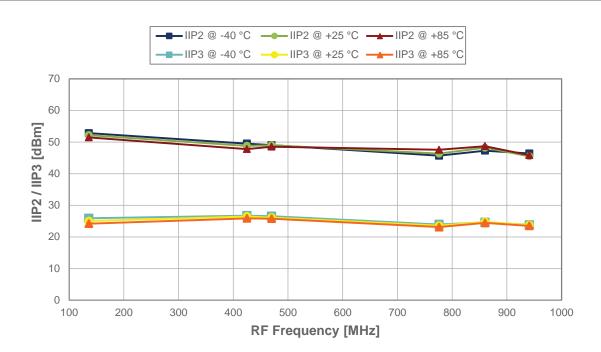




Figure 12 • LO-IF Isolation vs LO Power (LO Bypass)

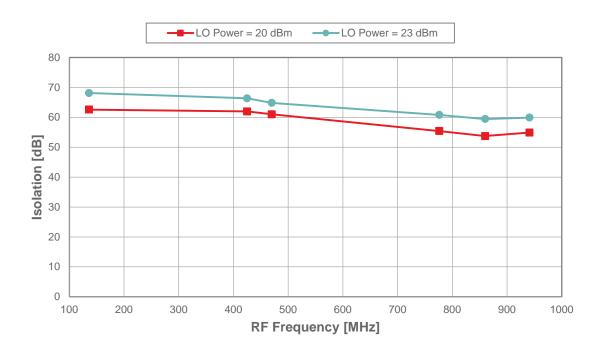


Figure 13 • LO-IF Isolation vs Temperature (LO Bypass)

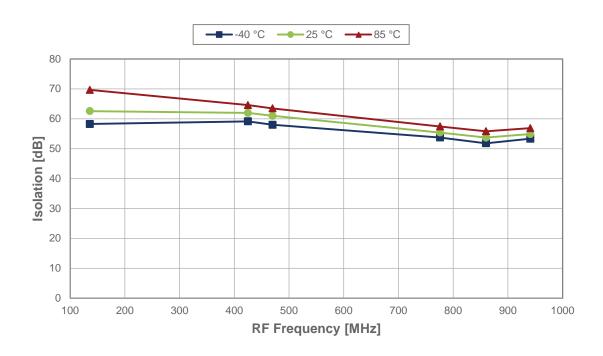




Figure 14 • LO-IF Isolation vs LO Power (LO Enable)

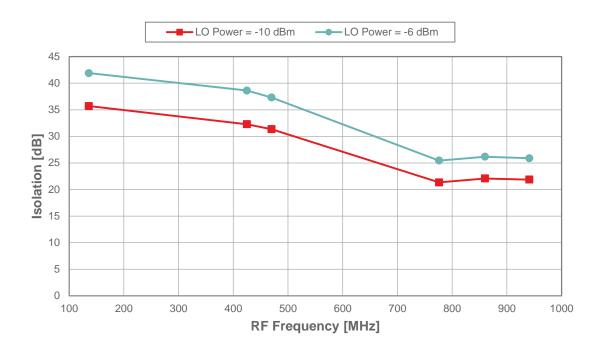


Figure 15 • LO-IF Isolation vs Temperature (LO Enable)

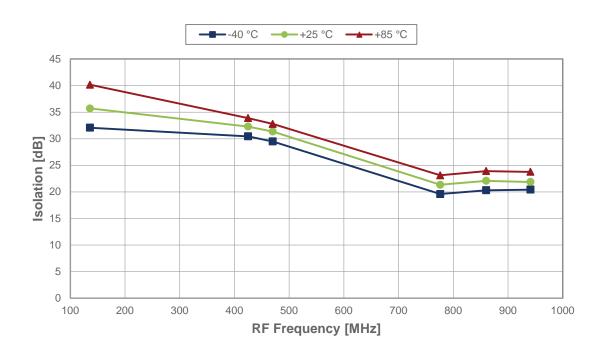




Figure 16 • LO-RF Isolation vs LO Power (LO Bypass)

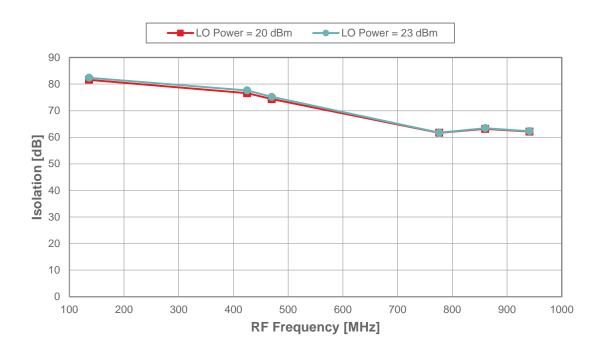


Figure 17 • LO-RF Isolation vs Temperature (LO Bypass)

Page 12

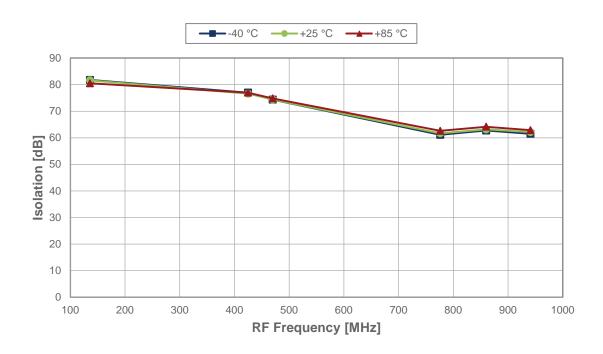




Figure 18 • LO-RF Isolation vs LO Power (LO Enable)

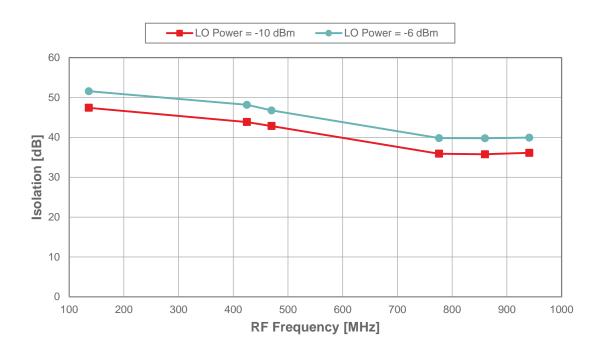


Figure 19 • LO-RF Isolation vs Temperature (LO Enable)

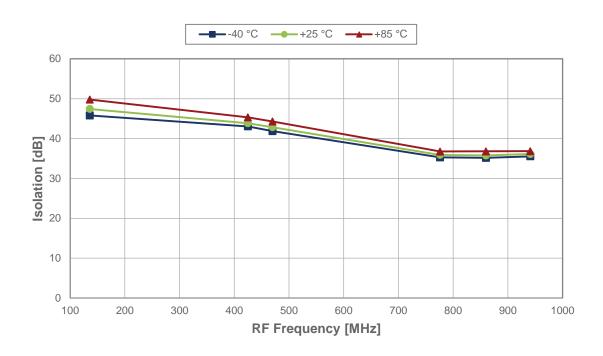




Figure 20 • RF-IF Isolation vs LO Power (LO Bypass)

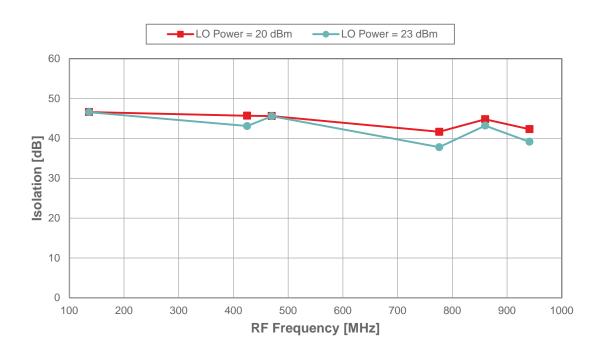


Figure 21 • RF—IF Isolation vs Temperature (LO Bypass)

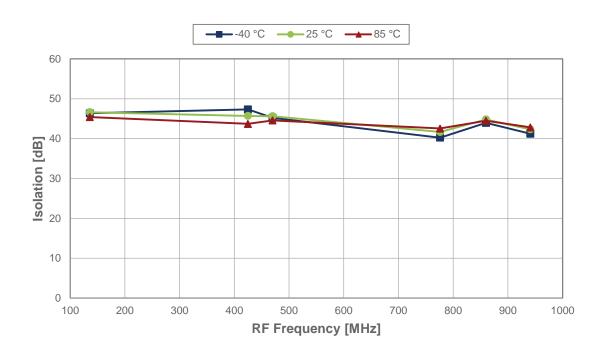




Figure 22 • RF-IF Isolation vs LO Power (LO Enable)

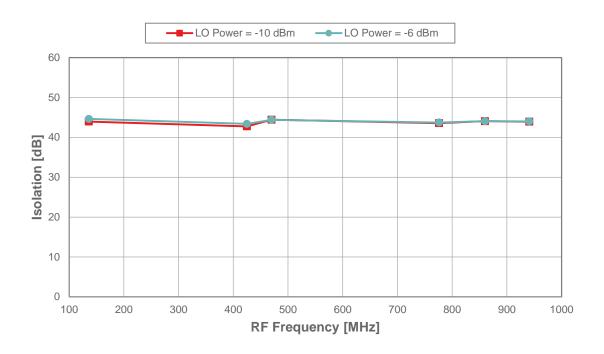
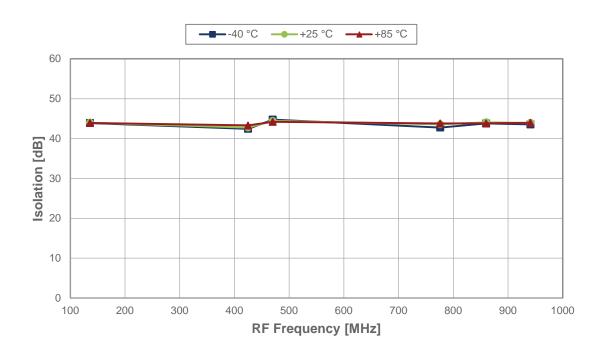


Figure 23 • RF–IF Isolation vs Temperature (LO Enable)





Evaluation Kit

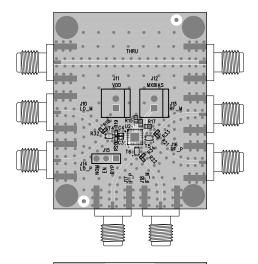
Page 16

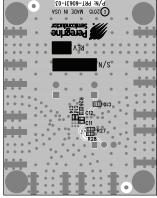
The PE4152 evaluation board (EVB) was designed to ease customer evaluation of the PE4152 mixer. The EVB is assembled with a PE4152 field-effect transistor (FET) mixer, baluns, headers and SubMiniature version A (SMA) connectors.

V_{DD} is applied to the device at J11. The LO bypass mode is selected by applying an active high signal to pin 6 via jumper J15 as show in **Figure 24**. The baluns have been selected to provide uniform amplitude and phase balance across the 100 to 1000 MHz frequency range.

The PCB design should use proper RF layout techniques for best performance. The signal lines should have 50Ω impedence and the package ground (exposed paddle) should be connected directly to the ground plane.

Figure 24 • Evaluation Kit Layout for PE4152







Pin Information

This section provides pinout information for the PE4152. **Figure 25** shows the pin map of this device for the available package. **Table 5** provides a description for each pin.

Figure 25 • Pin Configuration (Top View)

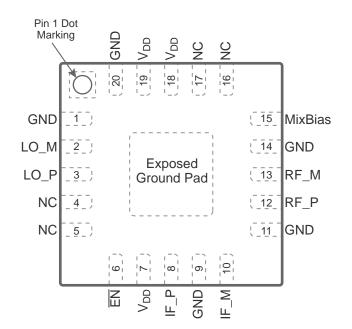


Table 5 • Pin Descriptions for PE4152

Pin No.	Pin Name	Description
1, 9, 11, 14, 20	GND	Ground
2	LO_M	Minus LO output
3	LO_P	Positive LO output
4, 5, 16, 17	NC	No connect
6	EN	LO enable (active low)
7, 18, 19	V _{DD}	Supply voltage
8	IF_P	Positive IF port
10	IF_M	Minus IF port
12	RF_P	Positive RF input
13	RF_M	Minus RF port
15	MixBias ^(*)	External mixer bias
Pad	GND	Exposed pad: ground for proper operation

Note: * For applications where the DC level of the RF and IF ports are not at 0V, the MixBias pin can be set to the equivalent DC bias level. For example, if the RF and IF signals are biased at 1 VDC, a 1V level can be applied to the MixBias pin. This will maintain the RF performance similar to the 0V case. The MixBias pin can be used in both LO states.



Packaging Information

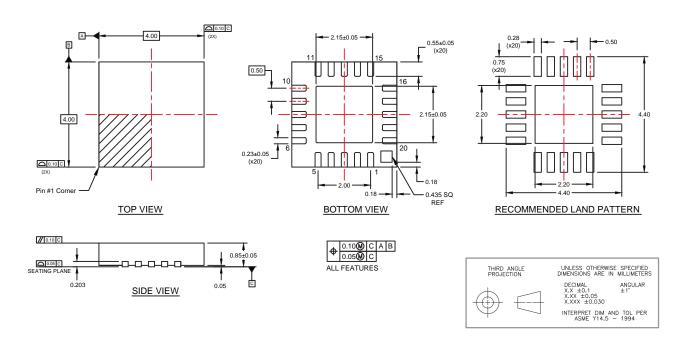
This section provides packaging data including the moisture sensitivity level, package drawing, package marking information and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE4152 in the 20-lead $4 \times 4 \times 0.85$ mm QFN package is MSL1.

Package Drawing

Figure 26 • Package Mechanical Drawing for 20-lead 4 × 4 × 0.85 mm QFN



Top-Marking Specification

Figure 27 • Package Marking Specifications for PE4152



= Pin 1 indicator

YY = Last two digits of assembly year

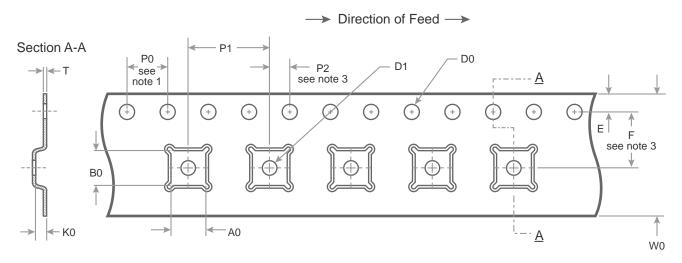
WW = Assembly work week

ZZZZZZ = Assembly lot code (maximum six characters)



Tape and Reel Specification

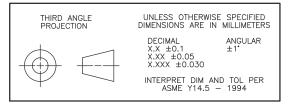
Figure 28 • Tape and Reel Specifications for 20-lead $4 \times 4 \times 0.85$ mm QFN

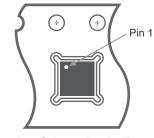


Notes:

A0	3.30
B0	3.30
K0	1.10
D0	1.50 + 0.1/ -0.0
D1	1.5 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
Т	0.30 ± 0.05
W0	12.00 ± 0.3

- 1. 10 Sprocket hole pitch cumulative tolerance ±0.2
- 2. Camber in compliance with EIA 481
- 3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole





Device Orientation in Tape



Ordering Information

Table 6 lists the available ordering codes for the PE4152 as well as available shipping methods.

Table 6 • Order Codes for PE4152

Order Codes	Description	Packaging	Shipping Method
PE4152A-Z	PE4152 mixer with integrated LO	Green 20-lead 4 × 4 mm QFN	3000 units / T&R
EK4152-02	PE4152 Evaluation kit	Evaluation kit	1 / Box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

Peregrine products are protected under one or more of the following U.S. patents: patents: patents: patents.psemi.com

Copyright and Trademark

©2015–2016, Peregrine Semiconductor Corporation. All rights reserved. The Peregrine name, logo, UTSi and UltraCMOS are registered trademarks and HaRP, MultiSwitch and DuNE are trademarks of Peregrine Semiconductor Corp.

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Not Recommended for New Designs (NRND)

This product is in production but is not recommended for new designs.

End of Life (EOL)

This product is currently going through the EOL process. It has a specific last-time buy date.

Obsolete

This product is discontinued. Orders are no longer accepted for this product.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for RF Mixer category:

Click to view products by pSemi manufacturer:

Other Similar products are found below:

 HMC337-SX
 mamx-009646-23dbml
 HMC339-SX
 CHR3664-QEG
 HMC8192-SX
 MIQ24MS-2
 M85C
 M74C
 MD-174-PIN
 HMC554A-SX

 HMC521A-SX
 HMC521A-SX
 HMC521A-SX
 HMC558A
 CMD258C4
 CMD258
 LT5511EFE
 MAMX-011023-SMB
 HMC399MS8TR
 HMC333TR

 HMC214MS8TR
 HMC175MS8TR
 HMC1043LC3TR
 MAMXSS0012TR-3000
 109728-HMC129LC4
 CSM2-13
 CSM1-13

 SA612AD/01.112
 HMC785LP4ETR
 LT5579IUH#PBF
 HMC773ALC3BTR
 HMC329ALC3B
 MY63H
 AD8343ARUZ-REEL7
 AD608AR

 AD608ARZ
 AD831APZ
 AD831APZ-REEL7
 AD8342ACPZ-REEL7
 AD8343ARUZ
 AD8344ACPZ-REEL7
 ADL5350ACPZ-R7

 ADL5363ACPZ-R7
 ADL5365ACPZ-R7
 ADL5802ACPZ-R7
 HMC1056LP4BE
 HMC1057-SX
 HMC1063LP3E
 HMC1081-SX
 HMC1093-SX