PE4314

Document Category: Product Specification

UltraCMOS® RF Digital Step Attenuator, 1 MHz–2.5 GHz

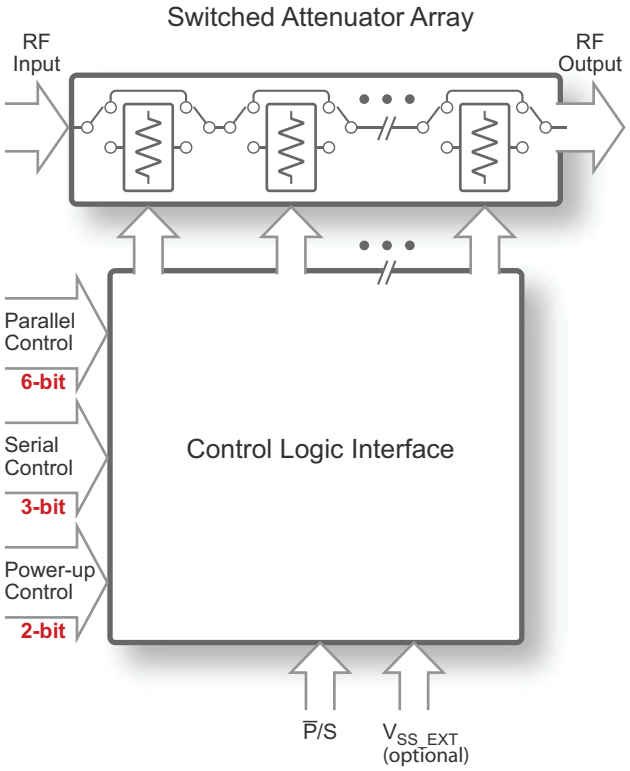
Features

- Attenuation step of 0.5 dB up to 31.5 dB
- Glitch-less attenuation state transitions
- Low distortion for CATV and multi-carrier applications
- Extended +105 °C operating temperature
- Parallel and Serial programming interfaces
- Packaging – 20-lead 4 × 4 × 0.85 mm QFN

Applications

- DOCSIS 3.1/0 customer premises equipment (CPE) and infrastructure
- Satellite CPE and infrastructure
- Fiber CPE and infrastructure

Figure 1 ▪ PE4314 Functional Diagram



Product Description

The PE4314 is a 75Ω HaRP™ technology-enhanced, 6-bit RF digital step attenuator (DSA) that supports a frequency range from 1 MHz to 2.5 GHz. It features glitch-less attenuation state transitions and supports 1.8V control voltage and an extended operating temperature range up to +105 °C, making this device ideal for multiple wired broadband applications.

The PE4314 is a pin-compatible upgraded version of the PE4304, PE4307, PE4308 and PE43404. An integrated digital control interface supports both Serial and Parallel programming of the attenuation, including the capability to program an initial attenuation state at power up.

The PE4314 covers a 31.5 dB attenuation range in a 0.5 dB step. It is capable of maintaining 0.5 dB monotonicity through 2.5 GHz. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE4314 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Optional External V_{SS}

For proper operation, the V_{SS_EXT} pin must be grounded or tied to the V_{SS} voltage specified in **Table 2**. When the V_{SS_EXT} pin is grounded, FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spur performance, V_{SS_EXT} can be applied externally to bypass the internal negative voltage generator.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • Absolute Maximum Ratings for PE4314

Parameter/Condition	Min	Max	Unit
Supply voltage, V_{DD}	–0.3	5.5	V
Digital input voltage	–0.3	3.6	V
RF input power, 75Ω 1–30 MHz ≥30 MHz–2.5 GHz		 See **Fig. 5** +30	 dBm dBm
Storage temperature range	–65	+150	°C
ESD voltage HBM(1), all pins		1500	V
ESD voltage CDM(2), all pins		1000	V

Notes:
1) Human body model (MIL-STD 883 Method 3015).
2) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for the PE4314. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 ▪ Recommended Operating Conditions for PE4314

Parameter	Min	Typ	Max	Unit
Normal mode, V_{SS_EXT} = 0V[1]				
Supply voltage, V_{DD}	2.3	3.3	5.5	V
Supply current, I_{DD}		130	200	µA
Bypass mode, V_{SS_EXT} = –3.4V[2]				
Supply voltage, V_{DD} (Table 3 spec compliance applies for V_{DD} ≥ 3.4V.)	2.7	3.4	5.5	V
Supply current, I_{DD}		50	80	µA
Negative supply voltage, V_{SS_EXT}	–3.6		–3.2	V
Negative supply current, I_{SS}	–40	–16		µA
Normal or bypass mode				
Digital input high	1.17		3.6	V
Digital input low	–0.3		0.6	V
Digital input current[3]			20	µA
RF input power, CW[4] 1–30 MHz ≥30 MHz–2.5 GHz			 Fig. 5 +24	 dBm dBm
RF input power, pulsed[5] 1–30 MHz ≥30 MHz–2.5 GHz			 Fig. 5 +27	 dBm dBm
Operating temperature range	–40	+25	+105	°C

Notes:

1) Normal mode: connect V_{SS_EXT} (pin 12) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2) Bypass mode: use V_{SS_EXT} (pin 12) to bypass and disable internal negative voltage generator.
3) Applies to all pins except pins 1, 5, 7 and 20. Pins 1, 7 and 20 have an internal 1 MΩ pull-down resistor to ground and pin 5 has an internal 2 MΩ pull-up resistor to internal V_{DD}.
4) 100% duty cycle, all bands, 75Ω.
5) Pulsed, 5% duty cycle of 4620 µs period, 75Ω.

Electrical Specifications

Table 3 provides the PE4314 key electrical specifications @ +25 °C, Z_S = Z_L = 75Ω, unless otherwise specified. Normal mode(1) is @ V_{DD} = 3.3V and V_{SS_EXT} = 0V. Bypass mode(2) is @ V_{DD} = 3.4V and V_{SS_EXT} = –3.4V.

Table 3 ▪ PE4314 Electrical Specifications

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operating frequency			1 MHz		2.5 GHz	As shown
Attenuation range	0.5 dB step			0–31.5		dB
Insertion loss	Reference state	1–204 MHz 204–870 MHz 870–1218 MHz 1218–2500 MHz		1.0 1.2 1.3 1.5	1.25 1.50 1.80 1.90	dB dB dB dB
Attenuation error	Any bit or bit combination	1–204 MHz 204–1218 MHz 1218–1794 MHz 1794–2500 MHz		See Fig. 13–Fig. 17	±(0.15 + 2% of attenuation setting) ±(0.15 + 3% of attenuation setting) ±(0.15 + 4% of attenuation setting) ± (0.15 + 8% of attenuation setting)	dB dB dB dB
Return loss	Input and output ports, reference state	1–204 MHz 204–870 MHz 870–1794 MHz 1794–2500 MHz		19 17 16 19		dB dB dB dB
Relative phase	All states	870 MHz 1000 MHz 1218 MHz		9 11 14		deg deg deg
Input 0.1dB compression point(3)		30–2500 MHz		30		dBm
Input IP2	Two tones at +15 dBm 10 kHz spacing 0 dB and 31.5 dB attenuation states	5 MHz 10 MHz 17 MHz 35 MHz 500 MHz 1000 MHz 1900 MHz 2500 MHz		0 dB / 31.5 dB 70 / 100 76 / 101 80 / 104 88 / 105 104 / 110 106 / 113 98 / 102 110 / 99		dBm dBm dBm dBm dBm dBm dBm dBm

Table 3 ▪ PE4314 Electrical Specifications (Cont.)

Parameter	Condition	Frequency	Min	Typ		Max	Unit
				0 dB	31.5 dB		
Input IP3	Two tones at +15 dBm 10 kHz spacing 0 dB and 31.5 dB attenuation states	5 MHz 10 MHz 17 MHz 35 MHz 500 MHz 1000 MHz 1900 MHz 2500 MHz		57 69 63 62 62 59 60 58	62 61 62 61 62 55 55 57		dBm dBm dBm dBm dBm dBm dBm dBm
Video feed-through	DC measurement			7			mV_{PP}
Settling time	50% CTRL to 0.05 dB of final value			1.8			µs
Settling time	50% CTRL to 0.5 dB of final value			0.4			µs
Switching time	50% CTRL to 90% or 10% RF			370		700	ns
Attenuation transient (envelope)		250 MHz		0.5			dB

Notes:

1) Normal mode: connect V_{SS_EXT} (pin 12) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2) Bypass mode: use V_{SS_EXT} (pin 12) to bypass and disable internal negative voltage generator.
3) The input 0.1dB compression point is a linearity figure of merit. Refer to **Table 2** for the operating RF input power (75Ω).

Spur-Free Performance

The typical spurious performance of the PE4314 in normal mode is –158 dBm/Hz (pin 12 tied to ground). The spur fundamental occurs around 2.6 MHz and it has a bandwidth of 100 kHz. This results in a CATV band typical spurious level for frequencies above 5 MHz of –154 dBm. If spur-free performance is desired, the internal negative voltage generator can be disabled by applying a negative voltage to V_{SS_EXT} (pin 12).

Glitch-less Attenuation State Transitions

The PE4314 features a novel architecture to provide the best-in-class glitch-less transition behavior when changing attenuation states. When RF input power is applied, the output power spikes are greatly reduced (0.5 dB) during attenuation state changes when comparing to previous generations of DSAs.

Thermal Data

Psi-JT (Ψ_{JT}), junction top-of-package, is a thermal metric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51-2).

$$\Psi_{JT} = (T_J - T_T)/P$$

where

Ψ_{JT} = junction-to-top of package characterization parameter, °C/W

T_J = die junction temperature, °C

T_T = package temperature (top surface, in the center), °C

P = power dissipated by device, Watts

Table 4 ▪ Thermal Data for PE4314

Parameter	Typ	Unit
Maximum junction temperature, T_{JMAX} (RF input power, CW = 24 dBm, +105 °C ambient)	124	°C
Ψ_{JT}	25	°C/W
θ_{JA}, junction-to-ambient thermal resistance	74	°C/W

Truth Tables

Table 5 and Table 6 provide the truth tables for the PE4314.

Table 5 ▪ Parallel Truth Table for PE4314(*)

$\overline{P}$/S	C16	C8	C4	C2	C1	C0.5	Attenuation Setting RF1–RF2
0	0	0	0	0	0	0	Reference IL
0	0	0	0	0	0	1	0.5 dB
0	0	0	0	0	1	0	1 dB
0	0	0	0	1	0	0	2 dB
0	0	0	1	0	0	0	4 dB
0	0	1	0	0	0	0	8 dB
0	1	0	0	0	0	0	16 dB
0	1	1	1	1	1	1	31.5 dB

Note: * Not all 64 possible combinations of C0.5–C16 are shown.

Table 6 ▪ Parallel Power-up Truth Table for PE4314(*)

$\overline{P}$/S	LE	PUP1	PUP2	Attenuation Setting RF1–RF2
0	0	0	0	Reference IL
0	0	0	1	8 dB
0	0	1	0	16 dB
0	0	1	1	31.5 dB
0	1	X	X	Defined by C0.5–C16

Note: * Power up with LE = 1 provides normal parallel operation with C0.5–C16, and PUP1 and PUP2 are not active.

Programming Options

Parallel/Serial Selection

Either a Parallel or Serial interface can be used to control the PE4314. The $\overline{P}$/S bit provides this selection, with $\overline{P}$/S = LOW selecting the Parallel interface and $\overline{P}$/S = HIGH selecting the Serial interface.

Parallel Mode Interface

The Parallel interface consists of six CMOS-compatible control lines that select the desired attenuation state, as shown in **Table 5**.

The Parallel interface timing requirements are defined by **Figure 3**, **Table 8** and switching time in **Table 3**.

For Latched Parallel programming, the latched enable (LE) should be held LOW while changing attenuation state control values, then pulsed LE HIGH to LOW (per **Figure 3**) to latch new attenuation state into the device.

For Direct Parallel programming, the LE line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches or jumpers).

In Parallel mode, DATA and CLOCK (CLK) pins are "don't care" and may be tied to logic LOW or logic HIGH.

Serial Interface

The Serial interface is a 6-bit Serial-in, Parallel-out shift register buffered by a transparent latch. It is controlled by using three CMOS-compatible signals: DATA, CLK and LE. The DATA and CLK inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input. Serial data is clocked in MSB first.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the Serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. The Serial timing for the operation is defined by **Figure 2** and **Table 7**.

Power-up Control Settings

The PE4314 always assumes a specifiable attenuation setting on power up. This feature exists for both the Serial and Parallel modes of operation, and allows a known attenuation state to be established before an initial Serial or Parallel control word is provided.

When the attenuator powers up in Serial mode ($\overline{P}$/S = 1), the six control bits are set to whatever data is present on the six Parallel data inputs (C0.5–C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

When the attenuator powers up in Parallel mode ($\overline{P}$/S = 0) with LE = 0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up (PUP) control bits, PUP1 and PUP2, as shown in **Table 6**.

Figure 2 ▪ Serial Interface Timing Diagram

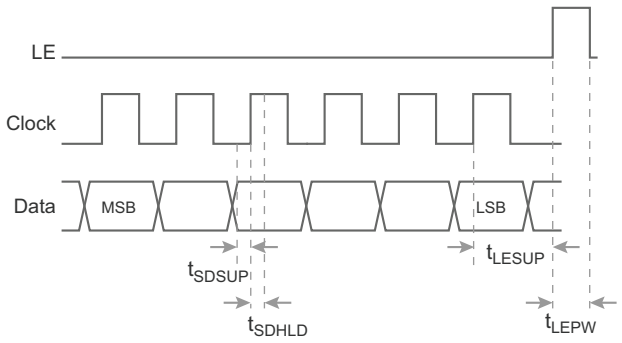
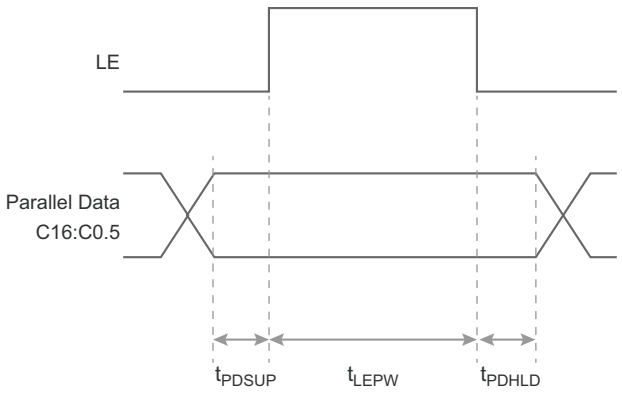


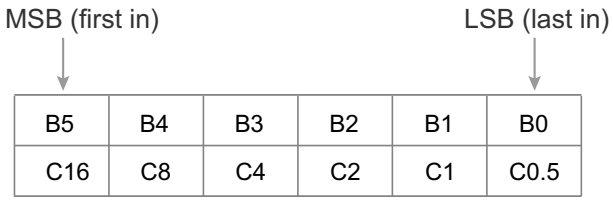
Figure 3 ▪ Parallel Interface Timing Diagram



Serial Register Map

Figure 4 provides the Serial programming register map for the PE4314.

Figure 4 • Serial Register Map(*)



Note: * For backward compatibility, the same programming scheme can be used.

Table 7 • Serial Interface AC Characteristics(1)

Parameter	Min	Max	Unit
Serial data clock frequency, f_{CLK}(2)		10	MHz
Serial clock HIGH time, t_{CLKH}	30		ns
Serial clock LOW time, t_{CLKL}	30		ns
LE set-up time after last clock rising edge, t_{LESUP}	10		ns
LE minimum pulse width, t_{LEPW}	30		ns
Serial data set-up time before clock rising edge, t_{SDSUP}	10		ns
Serial data hold time after clock rising edge, t_{SDHLD}	10		ns

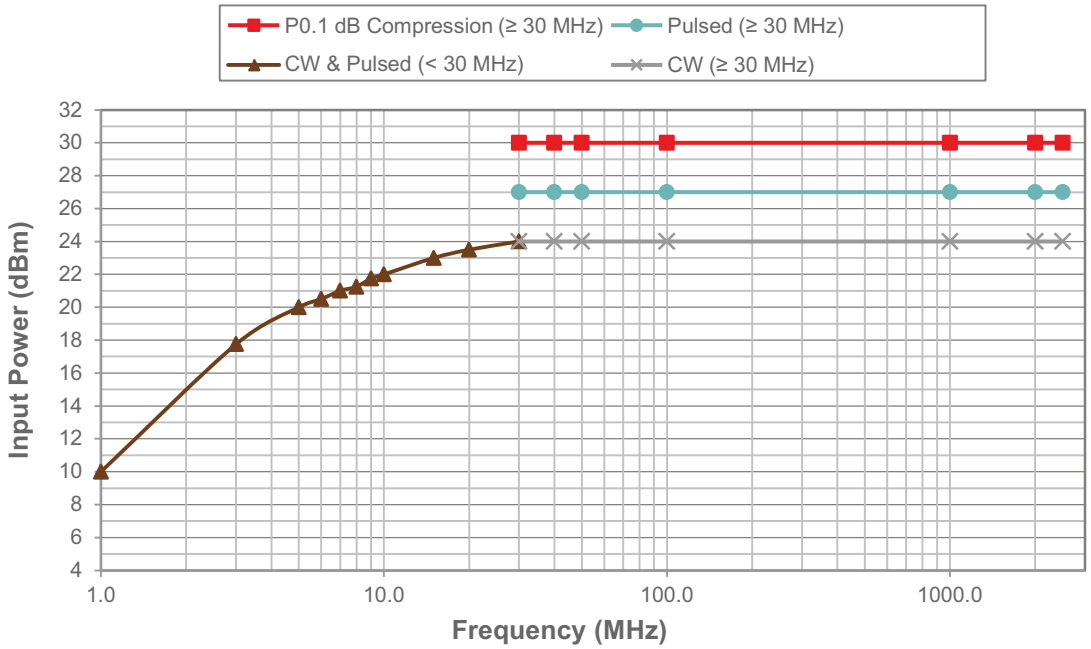
Notes:
1) V_{DD} = 3.3V or 5.0V, –40 °C < T_A < +105 °C, unless otherwise specified.
2) f_{CLK} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{CLK} specification.

Table 8 • Parallel Interface AC Characteristics(*)

Parameter	Min	Max	Unit
LE minimum pulse width, t_{LEPW}	10		ns
Data set-up time before rising edge of LE, t_{PDSUP}	10		ns
Data hold time after falling edge of LE, t_{PDHLD}	10		ns

Note: * V_{DD} = 3.3V or 5.0V, –40 °C < T_A < +105 °C, unless otherwise specified.

Figure 5 ▪ Power De-rating Curve, 1 MHz–2.5 GHz, –40 to +105 °C Ambient, 75?



Typical Performance Data

Figure 6–Figure 27 show the typical performance data at +25 °C, V_{DD} = 3.3V, Z_S = Z_L = 75Ω, unless otherwise specified.

Figure 6 ▪ Insertion Loss vs Temperature

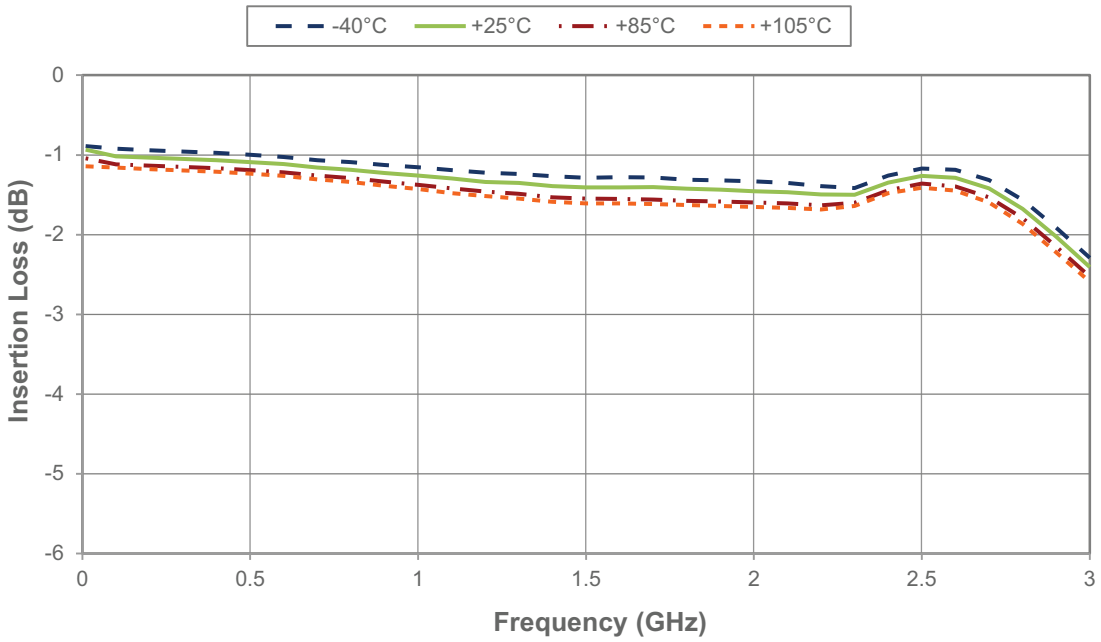


Figure 7 ▪ Input Return Loss vs Attenuation Setting

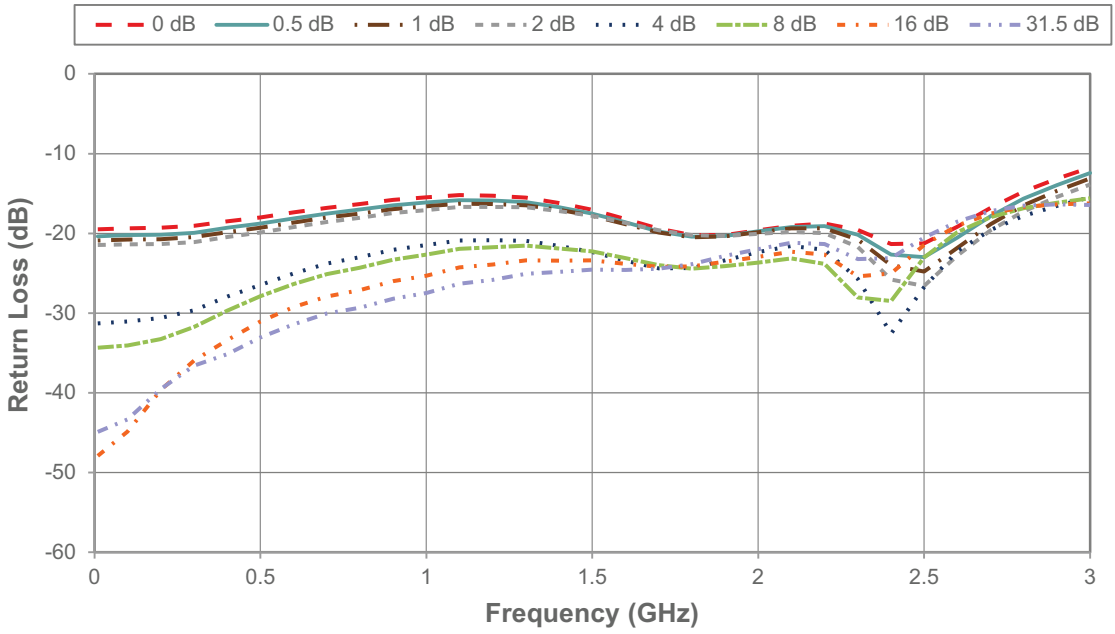


Figure 8 ▪ Output Return Loss vs Attenuation Setting

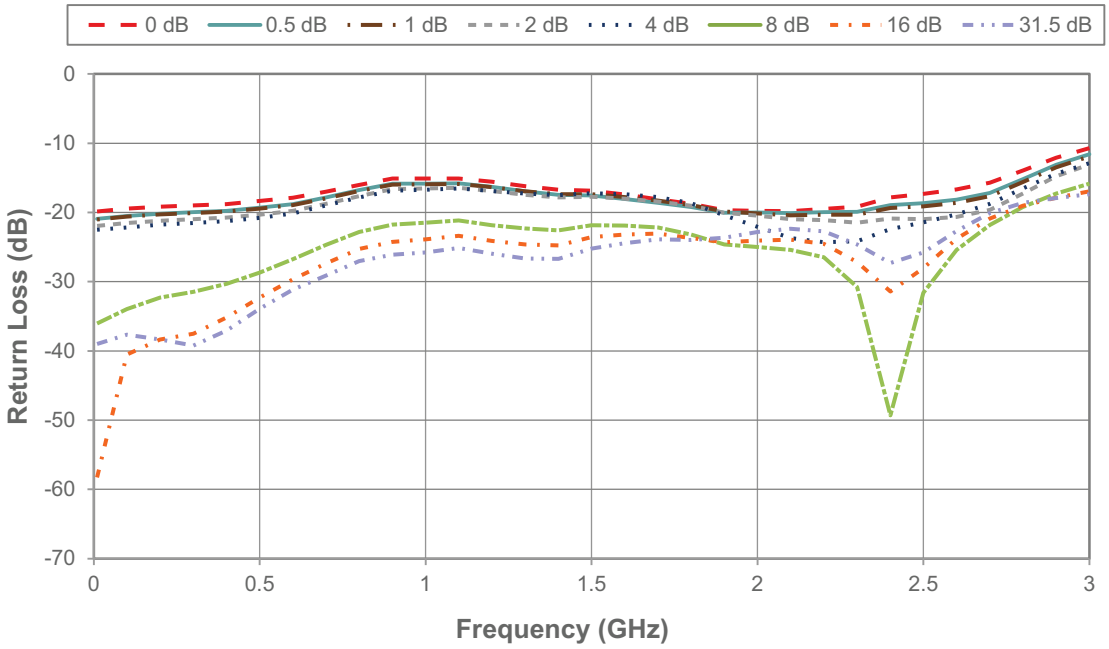


Figure 9 ▪ Input Return Loss for 16 dB Attenuation Setting vs Temperature

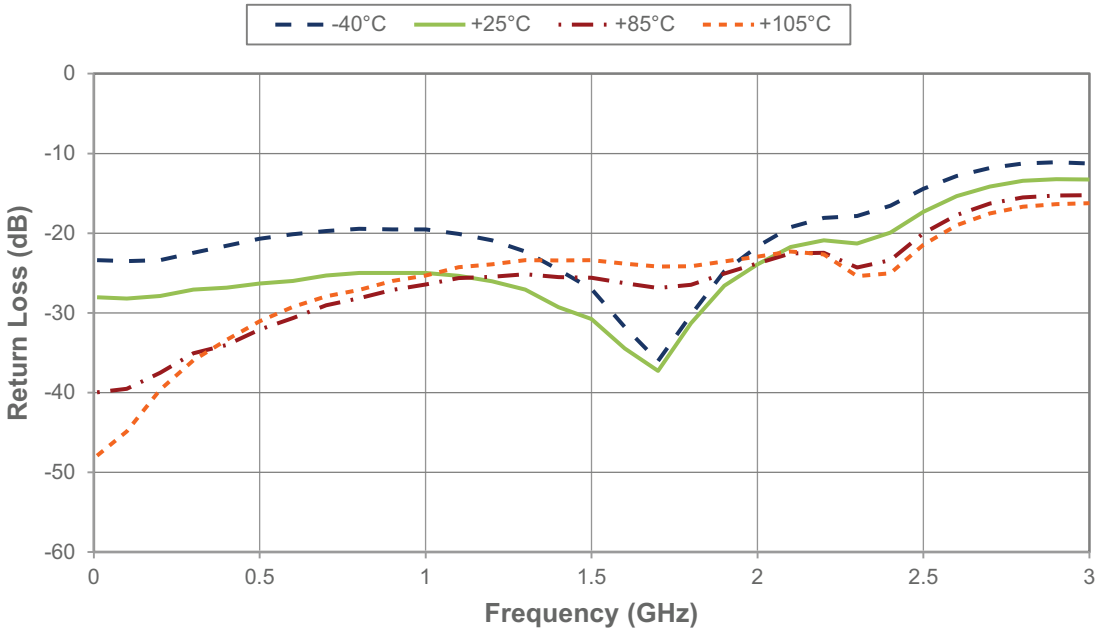


Figure 10 ▪ Output Return Loss for 16 dB Attenuation Setting vs Temperature

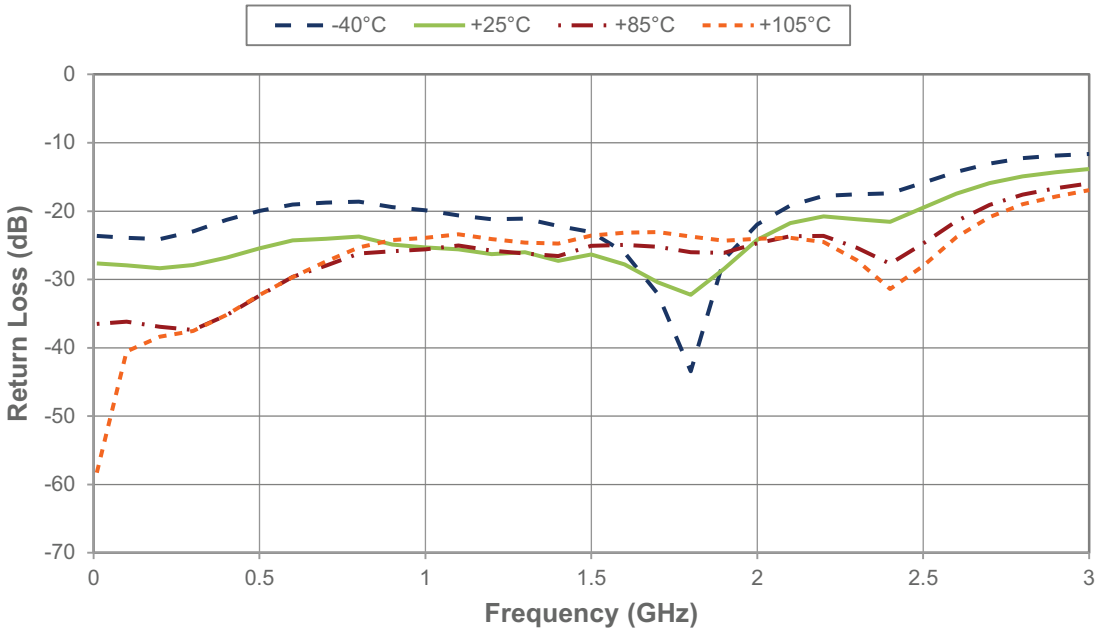


Figure 11 ▪ Relative Phase Error vs Attenuation Setting

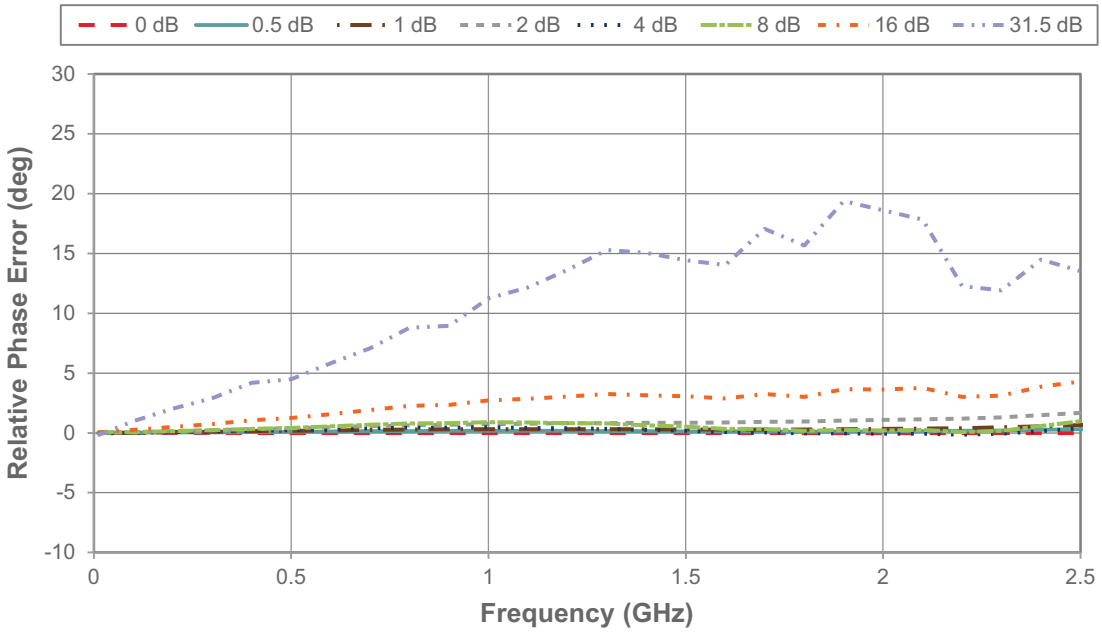


Figure 12 ▪ Relative Phase Error for 31.5 dB Attenuation Setting vs Frequency

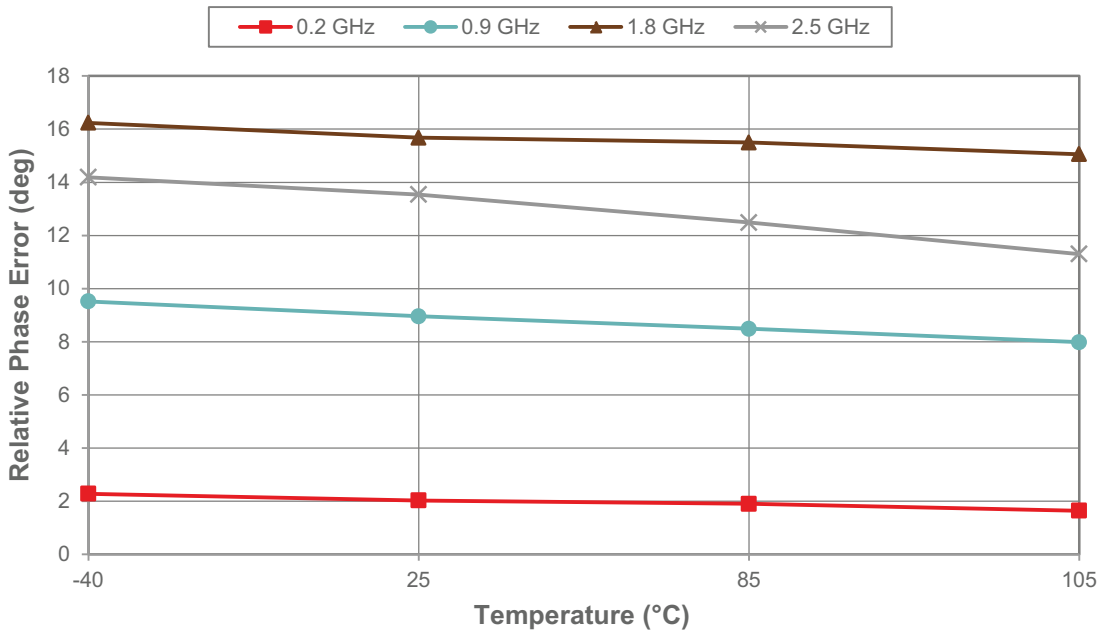
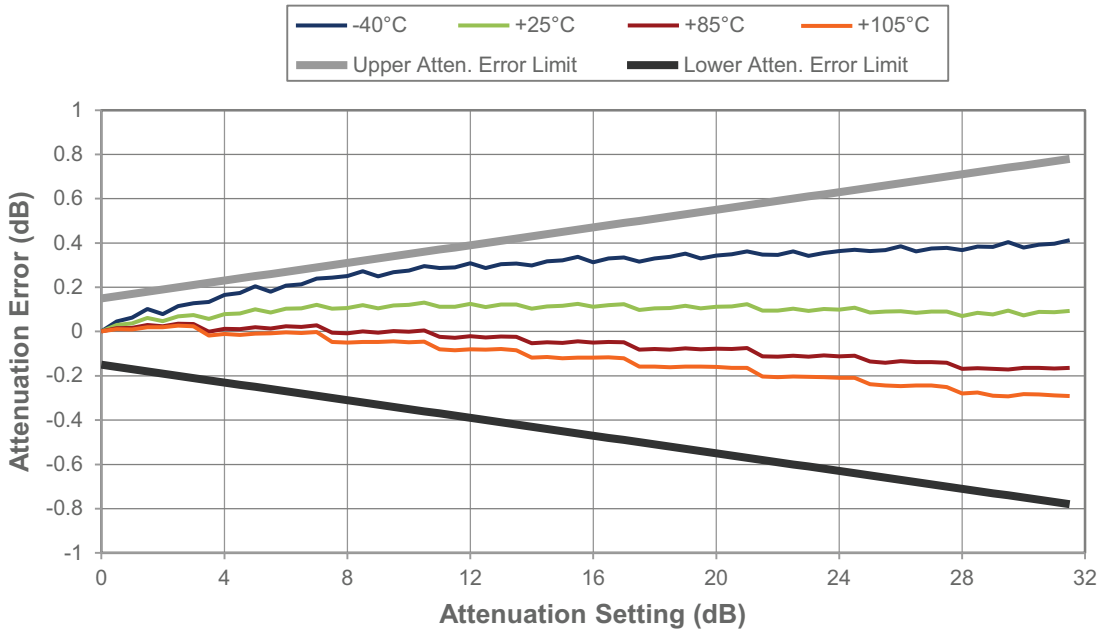
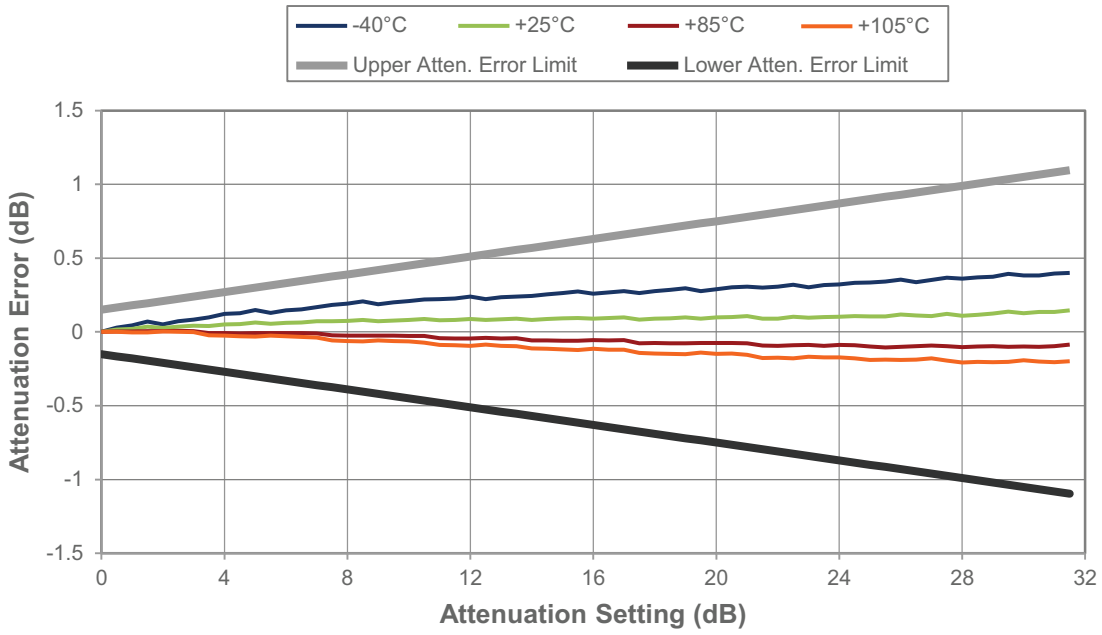


Figure 13 ▪ Attenuation Error @ 200 MHz vs Temperature(*)



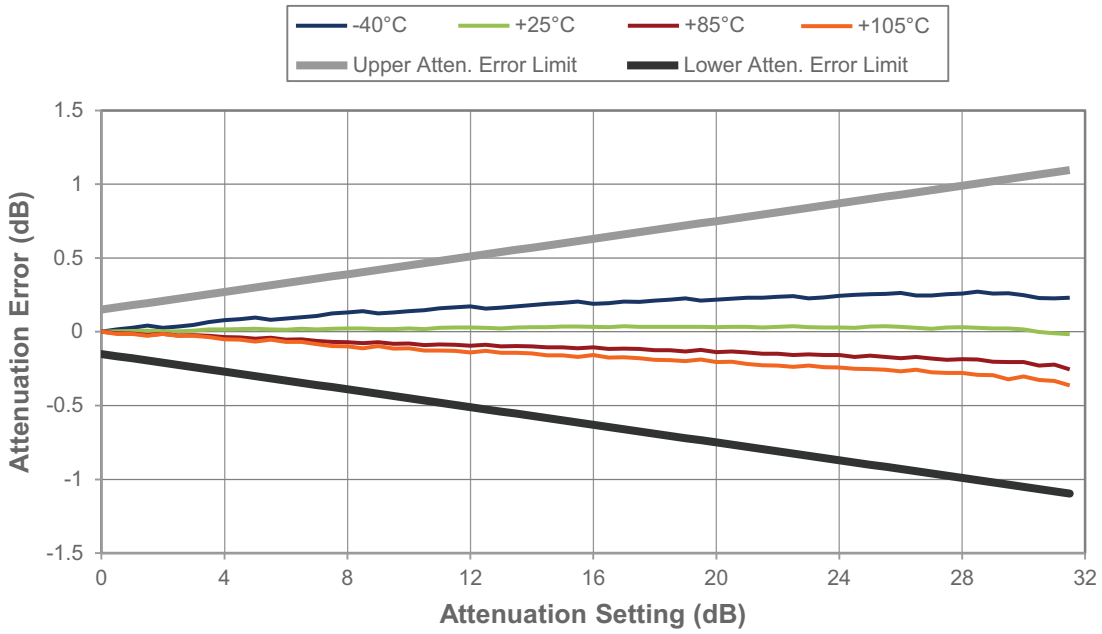
Note: * Attenuation error limit @ ±(0.15 + 2% of attenuation setting).

Figure 14 ▪ Attenuation Error @870 MHz vs Temperature(*)



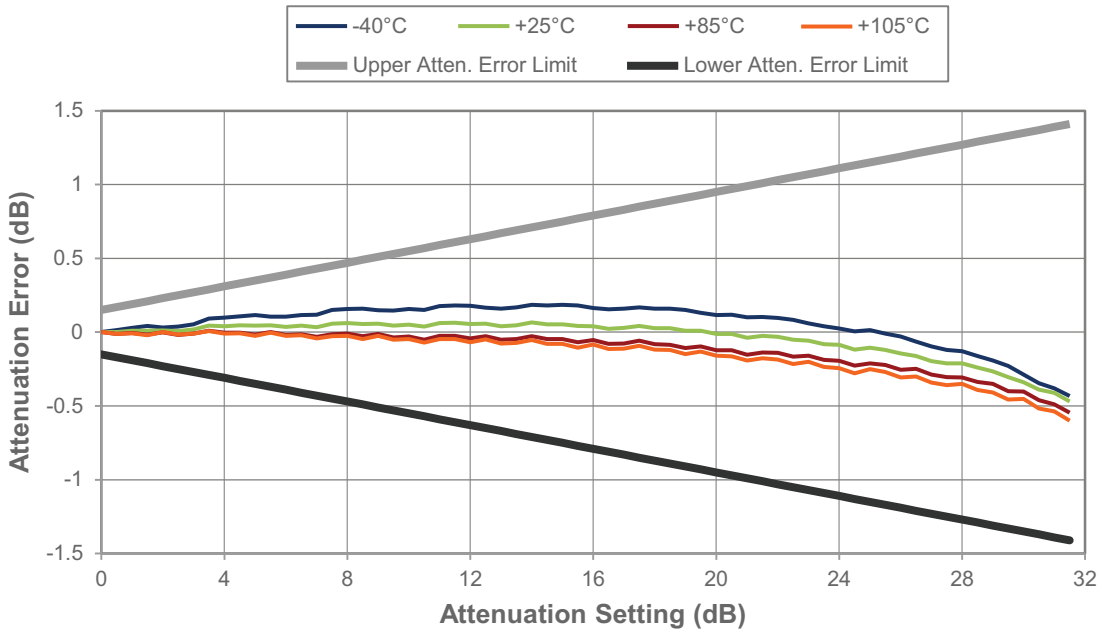
Note: * Attenuation error limit @ ±(0.15 + 3% of attenuation setting).

Figure 15 ▪ Attenuation Error @ 1218 MHz vs Temperature(*)



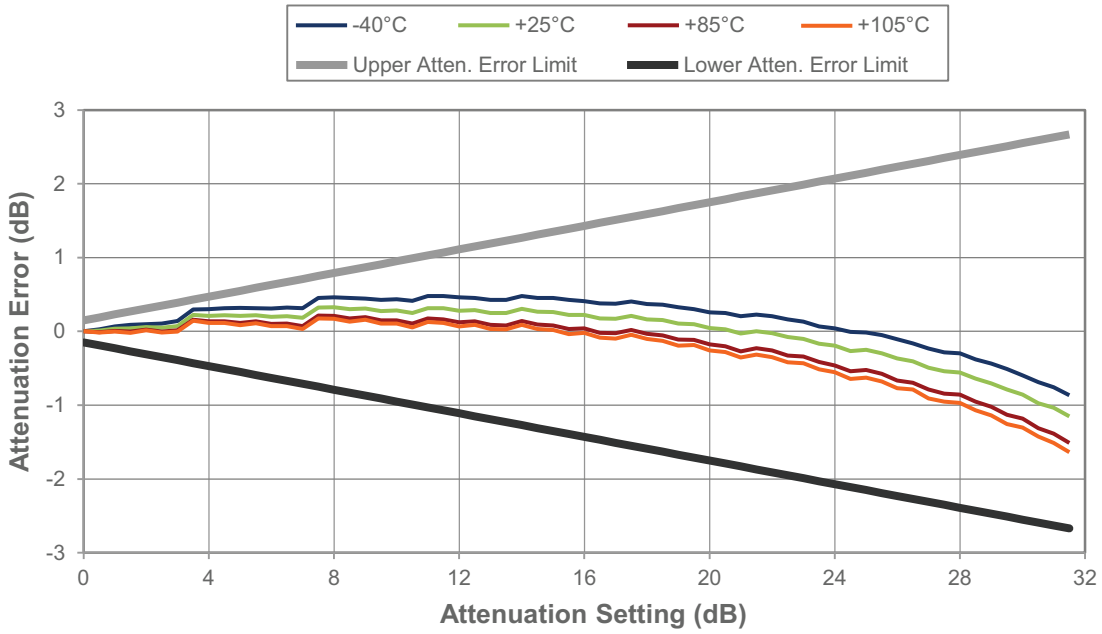
Note: * Attenuation error limit @ ±(0.15 + 3% of attenuation setting).

Figure 16 ▪ Attenuation Error @ 1790 MHz vs Temperature (*)



Note: * Attenuation error limit @ ±(0.15 + 4% of attenuation setting).

Figure 17 ▪ Attenuation Error @ 2500 MHz vs Temperature (*)



Note: * Attenuation error limit @ ±(0.15 + 8% of attenuation setting).

Figure 18 ▪ IIP3 vs Attenuation Setting (Low Frequencies)

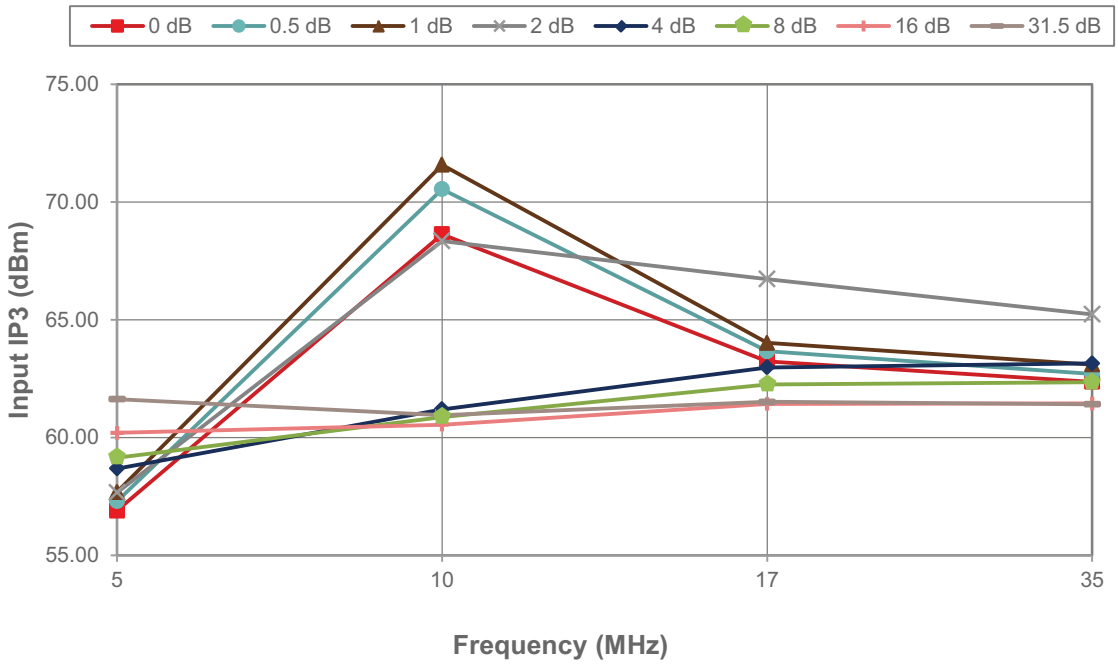


Figure 19 ▪ IIP3 vs Attenuation Setting (High Frequencies)

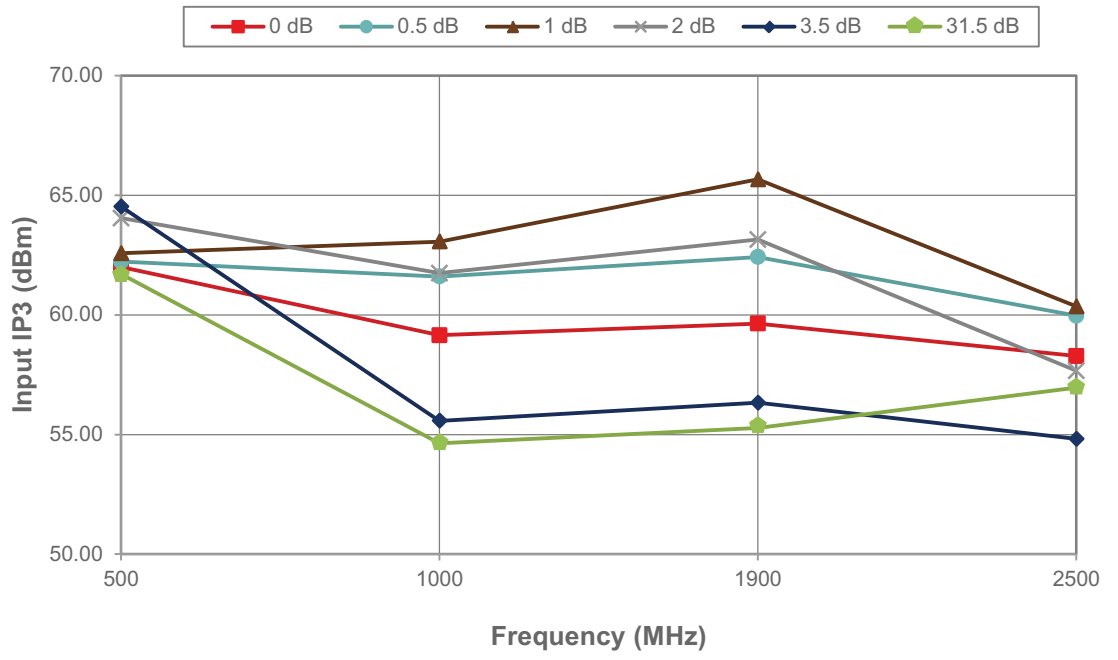


Figure 20 ▪ IIP2 vs Attenuation Setting (Low Frequencies)

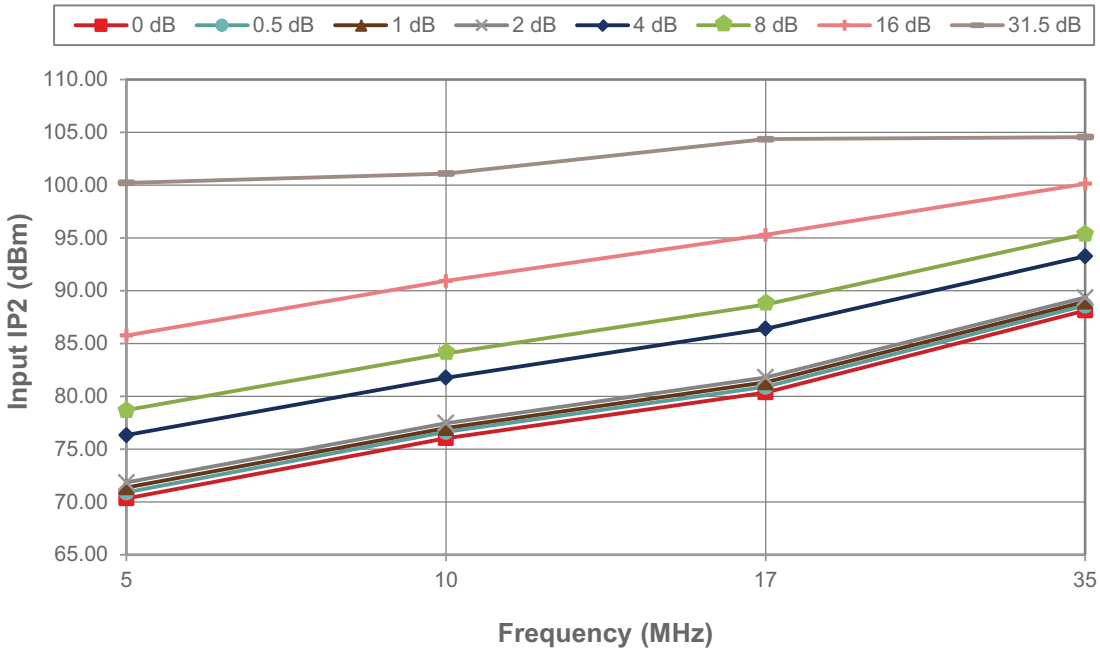


Figure 21 ▪ IIP2 vs Attenuation Setting (High Frequencies)

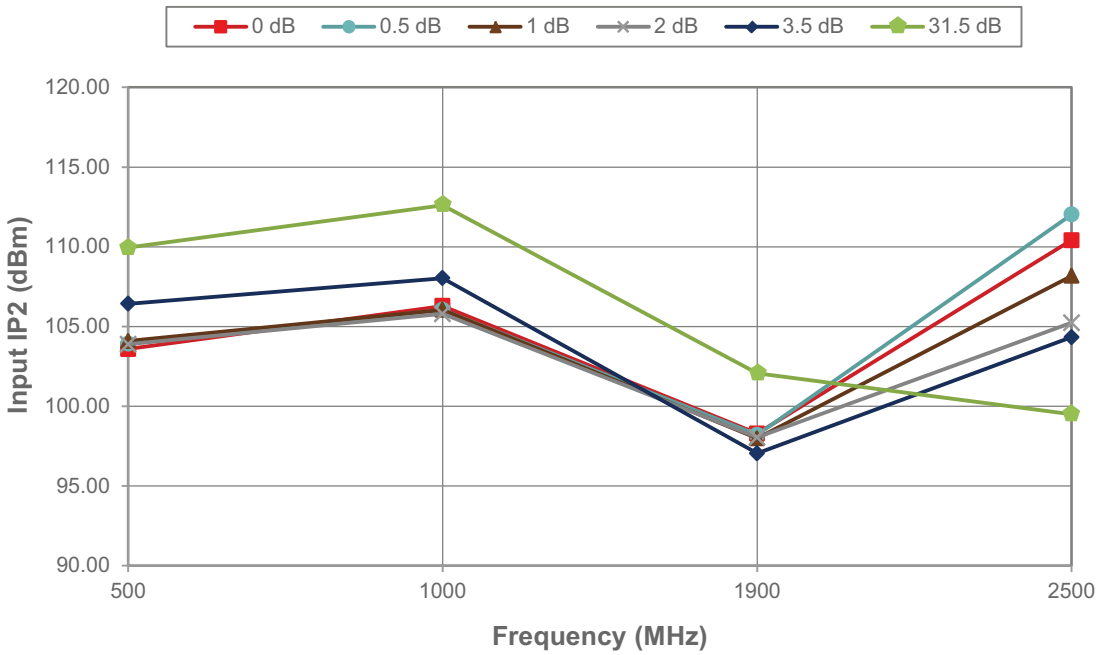
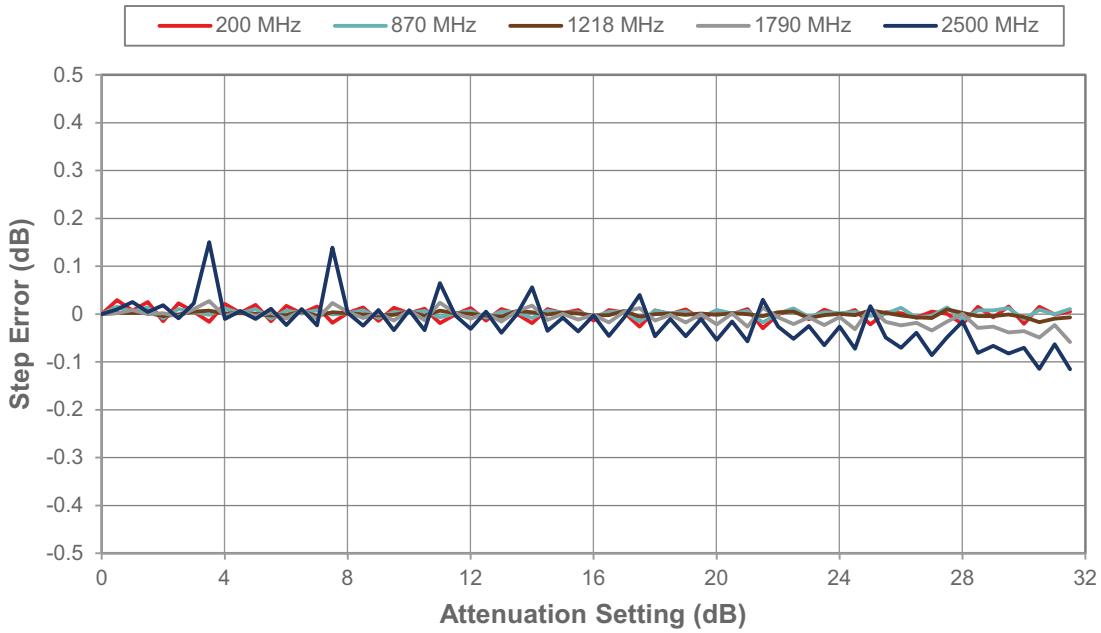


Figure 22 ▪ 0.5 dB Step Error vs Frequency(*)



Note: * Monotonicity is held so long as step error does not cross below –0.5 dB.

Figure 23 ▪ 0.5 dB Step, Actual vs Frequency

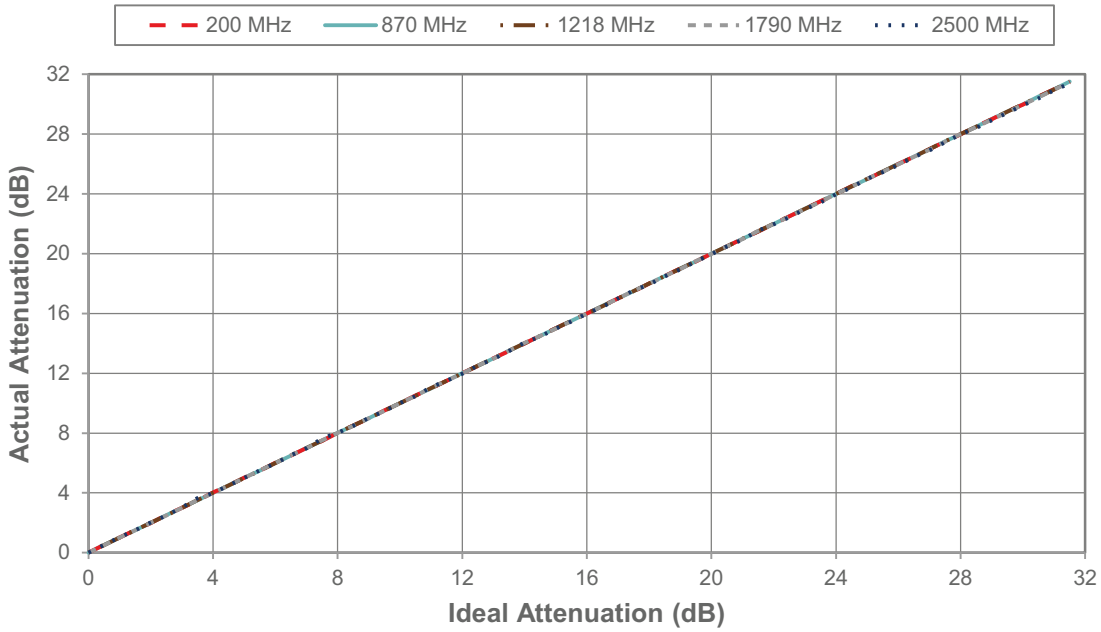


Figure 24 ▪ 0.5 dB Major State Bit Error vs Attenuation Setting

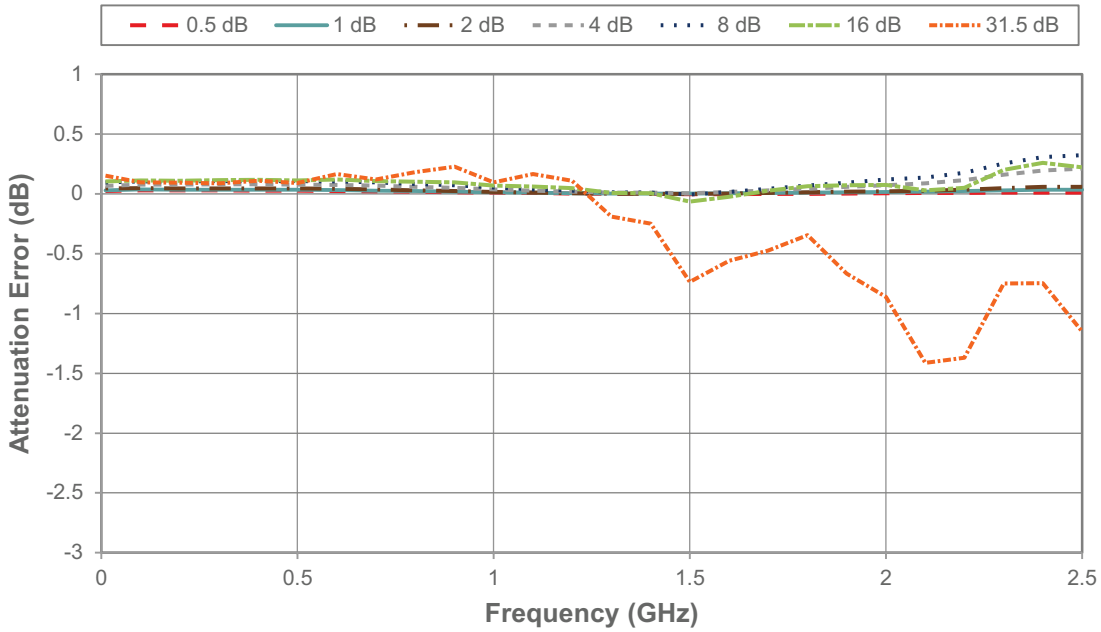


Figure 25 ▪ 0.5 dB Attenuation Error vs Frequency

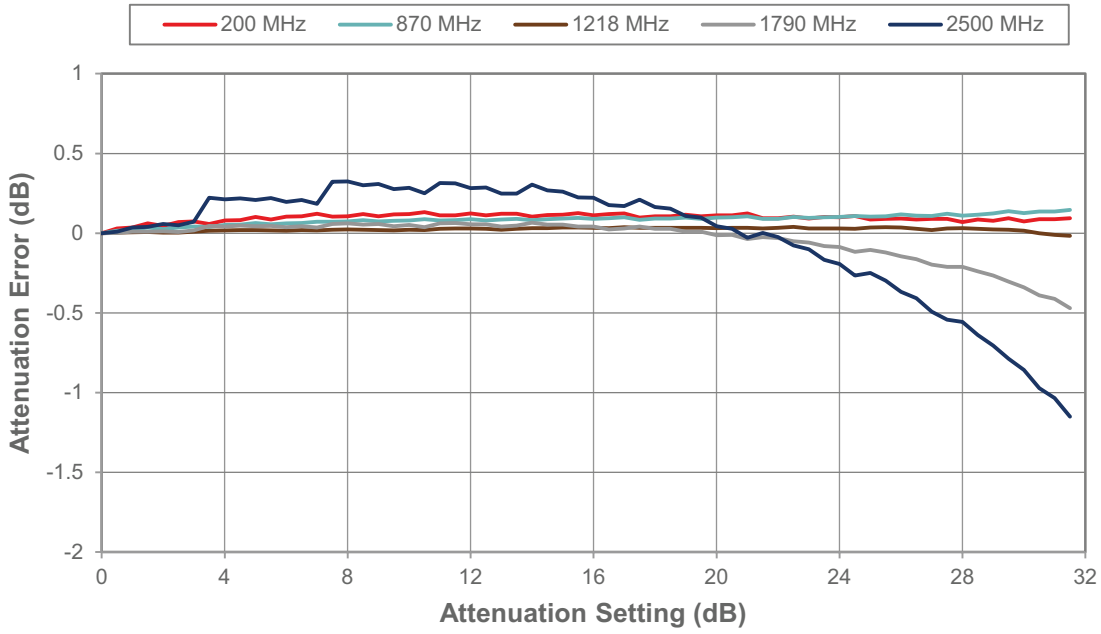


Figure 26 ▪ Attenuation Transient (15.5–16 dB), Typical Switching Time = 370 ns

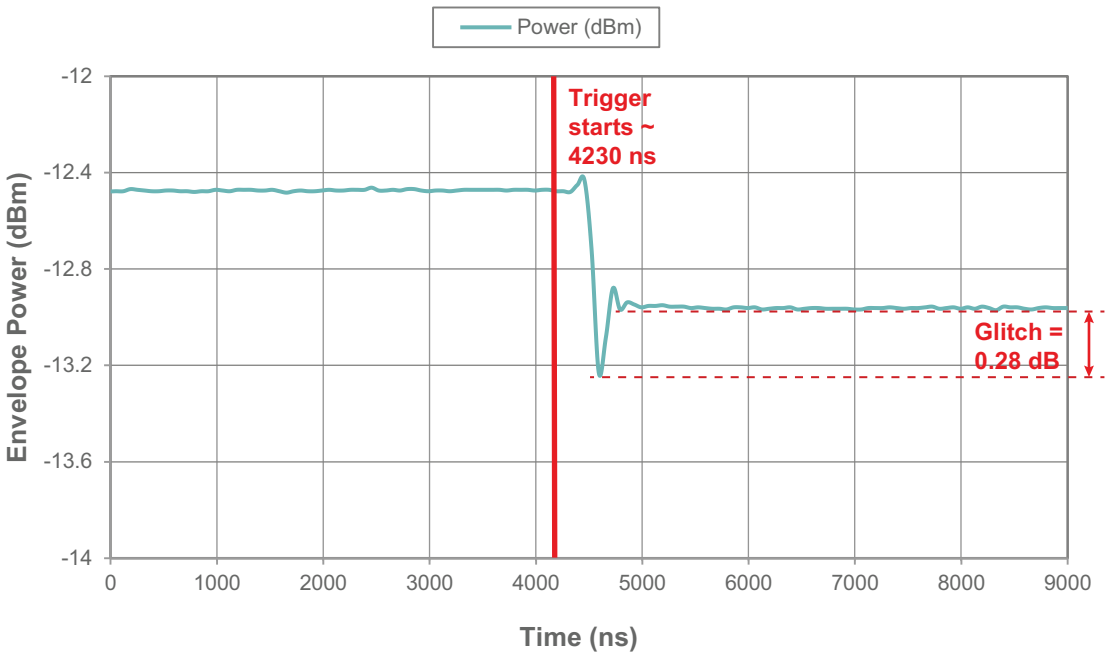
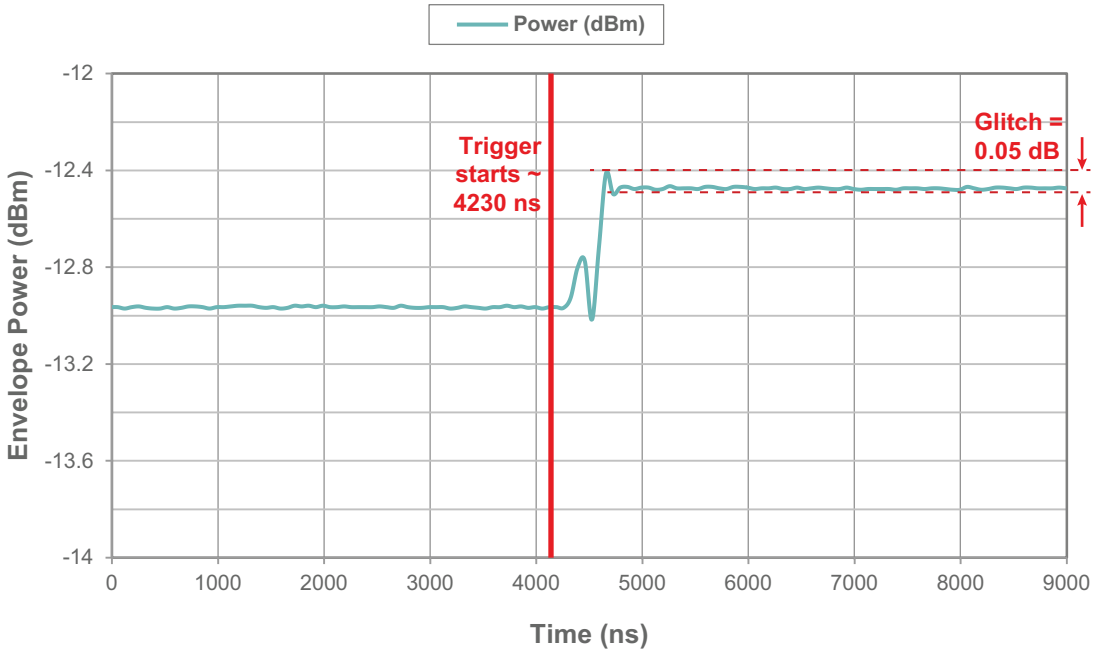


Figure 27 ▪ Attenuation Transient (16–15.5 dB), Typical Switching Time = 370 ns



Evaluation Kit

The digital step attenuator evaluation board (EVB) was designed to ease customer evaluation of the

PE4314 digital step attenuator. The PE4314 EVB supports Direct Parallel, Latched Parallel and Serial modes.

Evaluation Kit Setup

Connect the EVB with the USB dongle board and USB cable as shown in **Figure 28**.

Direct Parallel Programming Procedure

Direct Parallel programming is suitable for manual operation without software programming. For manual Direct Parallel programming, position the Parallel/Serial ($\overline{P}$/S) select switch to the Parallel position. The LE switch must be switched to HIGH position. Switches D1–D6 are SP3T switches that enable the user to manually program the parallel bits. When D1–D6 are toggled to the HIGH position, logic high is presented to the parallel input. When toggled to the LOW position, logic low is presented to the parallel input. Setting LE and D1–D6 to the EXTERNAL position presents as OPEN, which is set for software programming of Latched Parallel and Serial modes. **Table 5** depicts the Parallel truth table.

Latched Parallel Programming Procedure

For automated Latched Parallel programming, connect the USB dongle board and cable that is provided with the evaluation kit (EVK) from the USB port of the PC to the J1 header of the PE4314 EVB, and set the LE and D1–D6 SP3T switches to the EXTERNAL position. Position the Parallel/Serial ($\overline{P}$/S) select switch to the Parallel position. The evaluation software is written to operate the DSA in Parallel mode. Ensure that the software GUI is set to Latched Parallel mode. Use the software GUI to enable the desired attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

Serial Programming Procedure

For automated Serial programming, connect the USB dongle board and cable that is provided with the EVK from the USB port of the PC to the J1 header of the PE4314 EVB, and set the LE and D1–D6 SP3T switches to the EXTERNAL position. Position the Parallel/Serial ($\overline{P}$/S) select switch to the Serial position. The software GUI is written to operate the DSA in Serial mode. Use the software GUI to enable each setting to the desired attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

Figure 28 • Evaluation Kit for PE4314

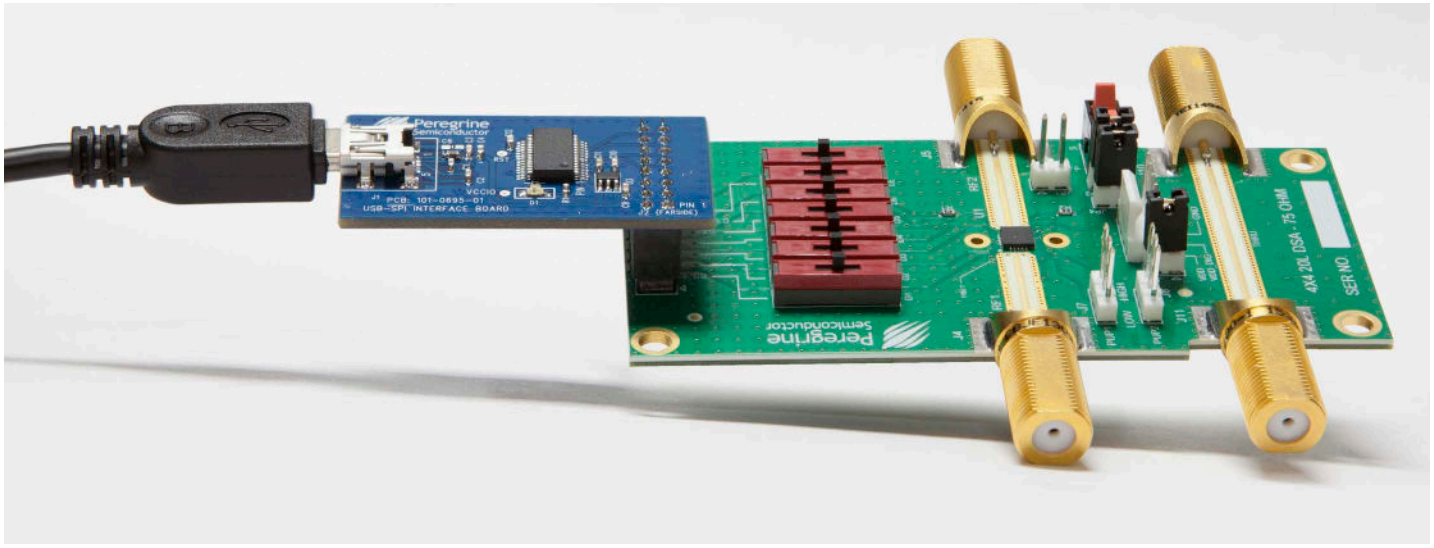
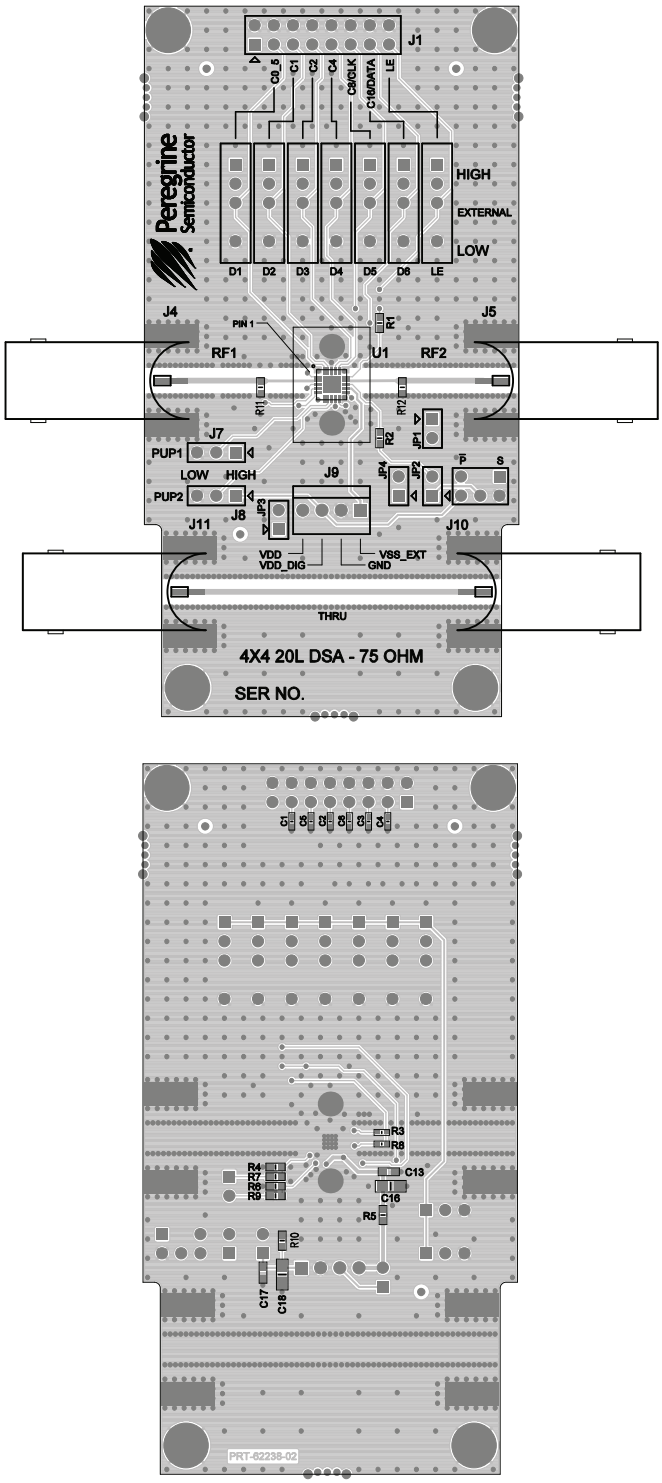


Figure 29 ▪ Evaluation Kit Layout for PE4314



Pin Information

This section provides pinout information for the PE4314. **Figure 30** shows the pin map of this device for the available package. **Table 9** provides a description for each pin.

Figure 30 • Pin Configuration (Top View)

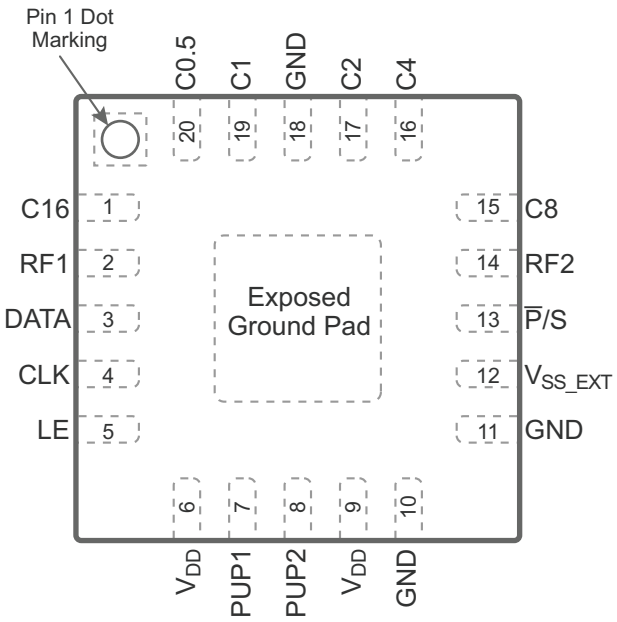


Table 9 • Pin Descriptions for PE4314

Pin No.	Pin Name	Description
1	C16[1][2]	Parallel control bit, 16 dB
2	RF1[3]	RF1 port
3	DATA	Serial interface data input
4	CLK	Serial interface clock input
5	LE[4]	Serial interface latch enable input
6, 9	V_{DD}	Supply voltage
7	PUP1[1][2]	Power-up control bit, MSB
8	PUP2[1]	Power-up control bit, LSB
10, 11, 18	GND	Ground
12	V_{SS_EXT}[5]	External V_{SS} negative control voltage
13	$\overline{P}$/S	Parallel/Serial mode select
14	RF2[3]	RF2 port
15	C8[1]	Parallel control bit, 8 dB
16	C4[1]	Parallel control bit, 4 dB
17	C2[1]	Parallel control bit, 2 dB
19	C1[1]	Parallel control bit, 1 dB
20	C0.5[1][2]	Parallel control bit, 0.5 dB
Pad	GND	Exposed pad: ground for proper operation

Notes:

1) Ground PUP1, PUP2, C0.5, C1, C2, C4, C8 and C16 if not in use.
2) C0.5, C16 and PUP1 have an internal 1 MΩ pull-down resistor to ground.
3) RF pins 2 and 14 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
4) LE (pin 5) has an internal 2 MΩ pull-up resistor to internal V_{DD}.
5) Use V_{SS_EXT} (pin 12) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 12) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.

Packaging Information

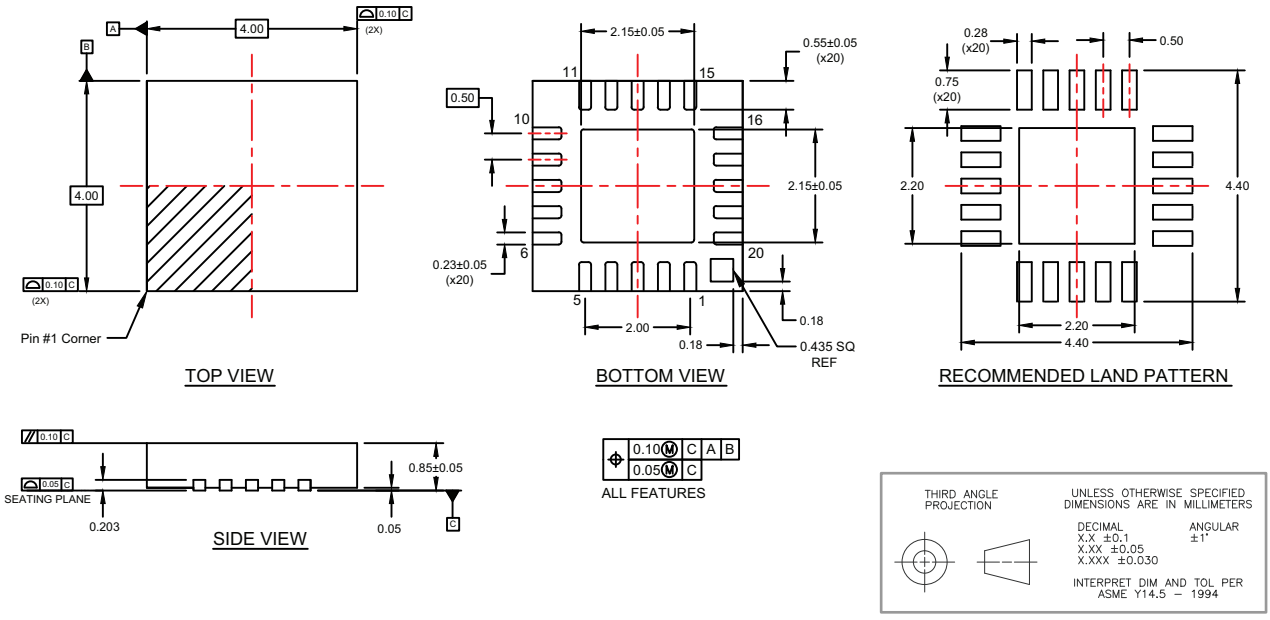
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE4314 in the 20-lead 4 × 4 × 0.85 mm QFN package is MSL1.

Package Drawing

Figure 31 ▪ Package Mechanical Drawing for 20-lead 4 × 4 × 0.85 mm QFN



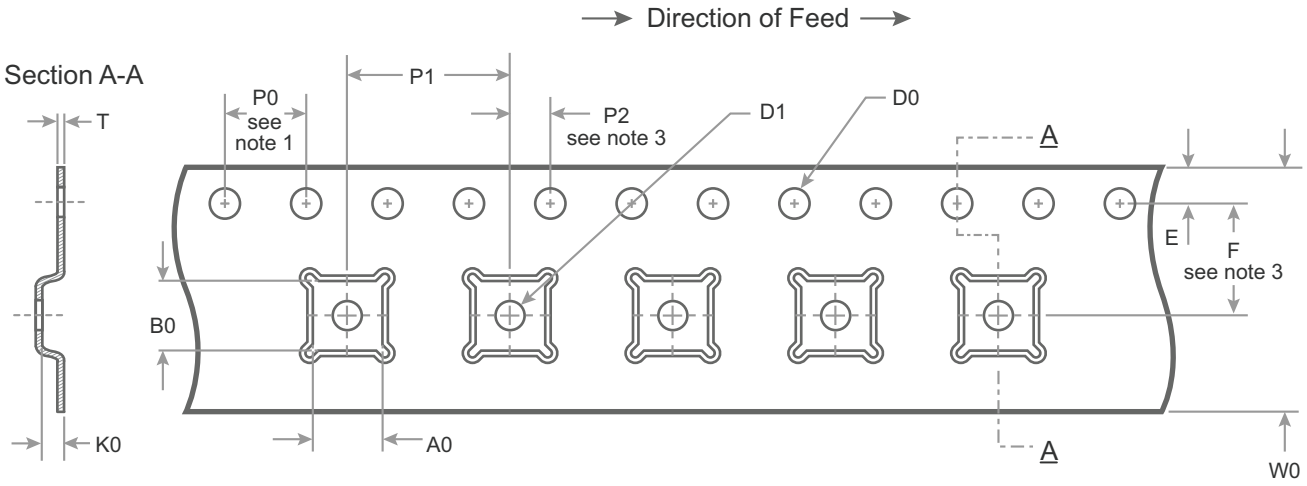
Top-Marking Specification

Figure 32 ▪ Package Marking Specifications for PE4314

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Assembly lot code (maximum six characters)

Tape and Reel Specification

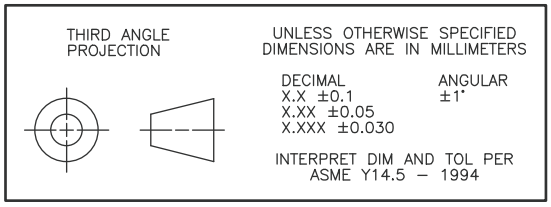
Figure 33 ▪ Tape and Reel Specifications for 20-lead 4 × 4 × 0.85 mm QFN

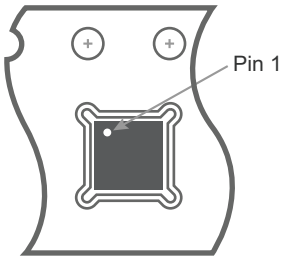


Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

A0	4.35
B0	4.35
K0	1.10
D0	1.50 + 0.10/ -0.00
D1	1.50 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.30





Device Orientation in Tape

Ordering Information

Table 10 lists the available ordering codes for the PE4314 as well as available shipping methods.

Table 10 • Order Codes for PE4314

Order Codes	Description	Packaging	Shipping Method
PE4314B–Z	PE4314 digital step attenuator	Green 20-lead 4 × 4 mm QFN	3000 Units/T&R
EK4314–02	PE4314 evaluation kit	Evaluation kit	1/Box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

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Product Brief

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