

## -20V P-Channel Enhancement Mode MOSFET

**VDS= -20V**

**RDS(ON), Vgs@-4.5V, Ids@-2.3A < 130mΩ**

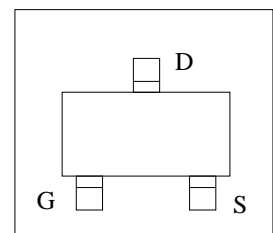
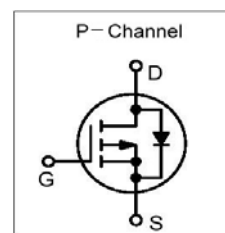
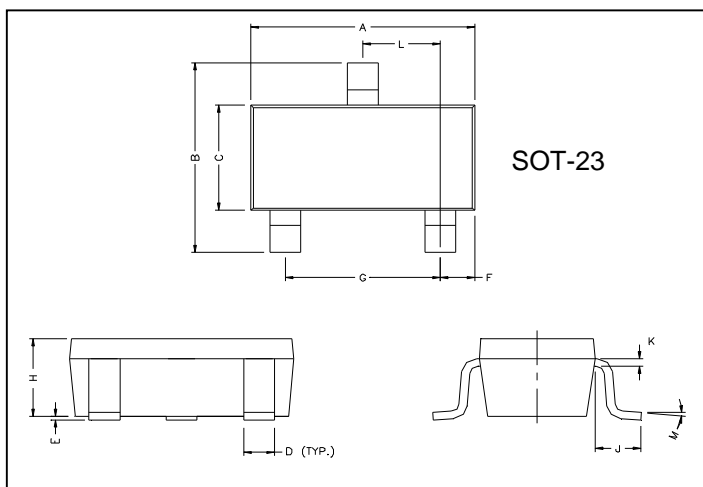
**RDS(ON), Vgs@-2.5V, Ids@-2.0A < 190mΩ**

### Features

Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

### Package Dimensions



REF.	Millimeter		REF.	Millimete	
	Min.	Max.		Min.	Max.
A	2.80	3.00	G	1.80	2.00
B	2.30	2.50	H	0.90	1.1
C	1.20	1.40	K	0.10	0.20
D	0.30	0.50	J	0.35	0.70
E	0	0.10	L	0.92	0.98
F	0.45	0.55	M	0°	10°

### Maximum Ratings and Thermal Characteristics (TA = 25oC unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	-20	V	
Gate-Source Voltage	V <sub>GS</sub>	±8		
Continuous Drain Current	I <sub>D</sub>	-2.3	A	
Pulsed Drain Current <sup>1)</sup>	I <sub>DM</sub>	-8		
Maximum Power Dissipation <sup>2)</sup>	P <sub>D</sub>	TA = 25°	1.25	W
		TA = 75°C	0.8	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C	
Junction-to-Ambient Thermal Resistance (PCB mounted) <sup>2)</sup>	R <sub>thJA</sub>	100	°C/W	
Junction-to-Ambient Thermal Resistance (PCB mounted) <sup>3)</sup>		166		

#### Notes

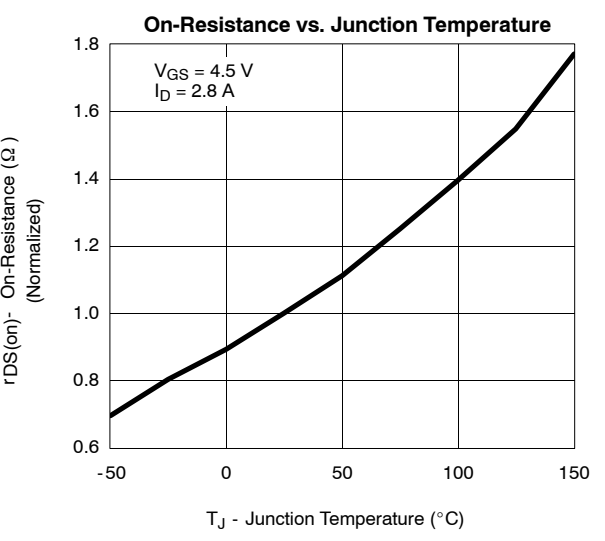
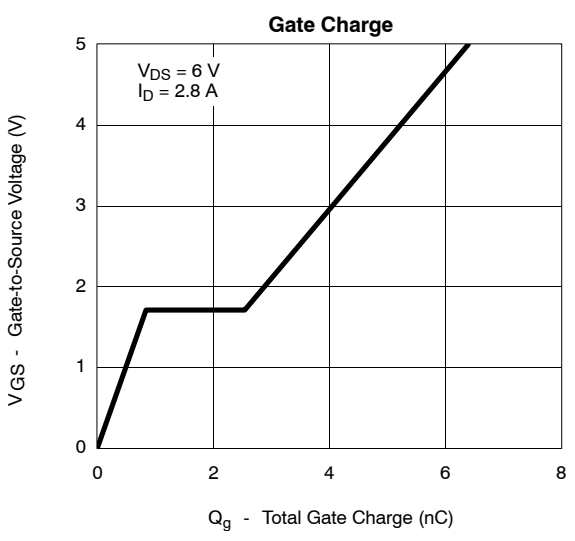
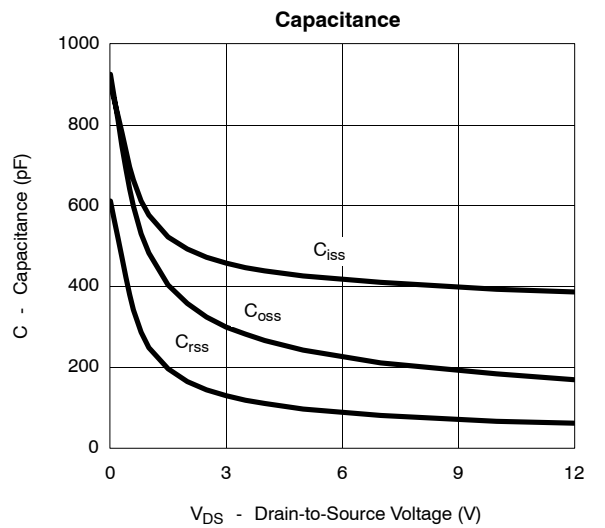
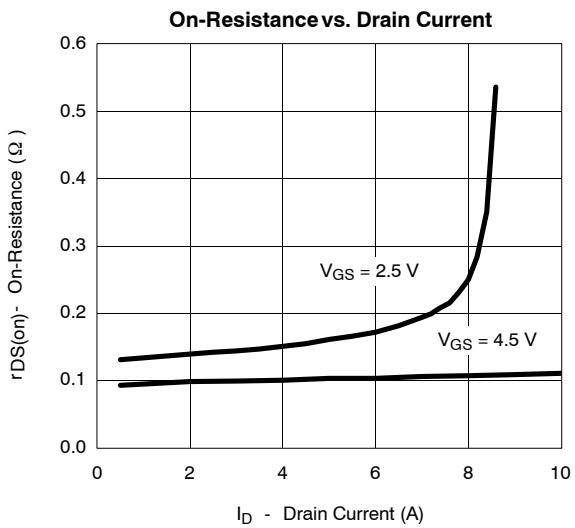
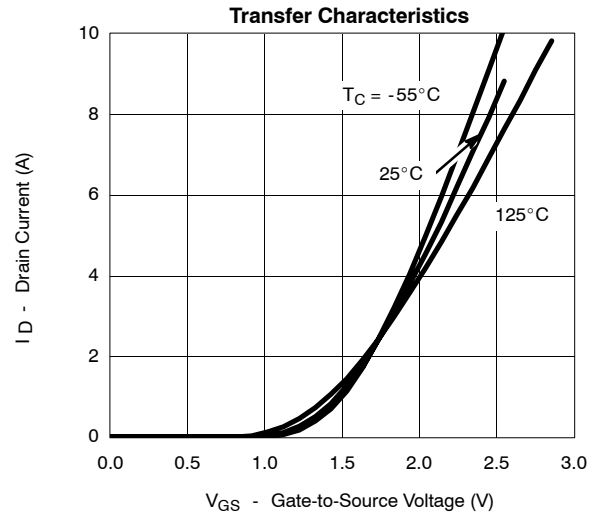
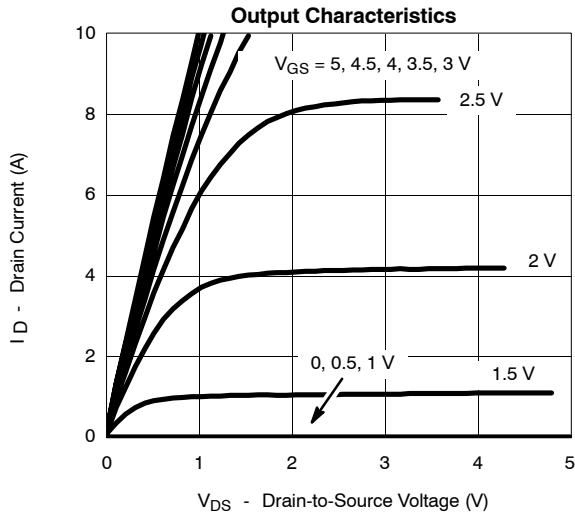
- 1) Pulse width limited by maximum junction temperature.
- 2) Surface Mounted on FR4 Board, t ≤ 5 sec.
- 3) Surface Mounted on FR4 Board.

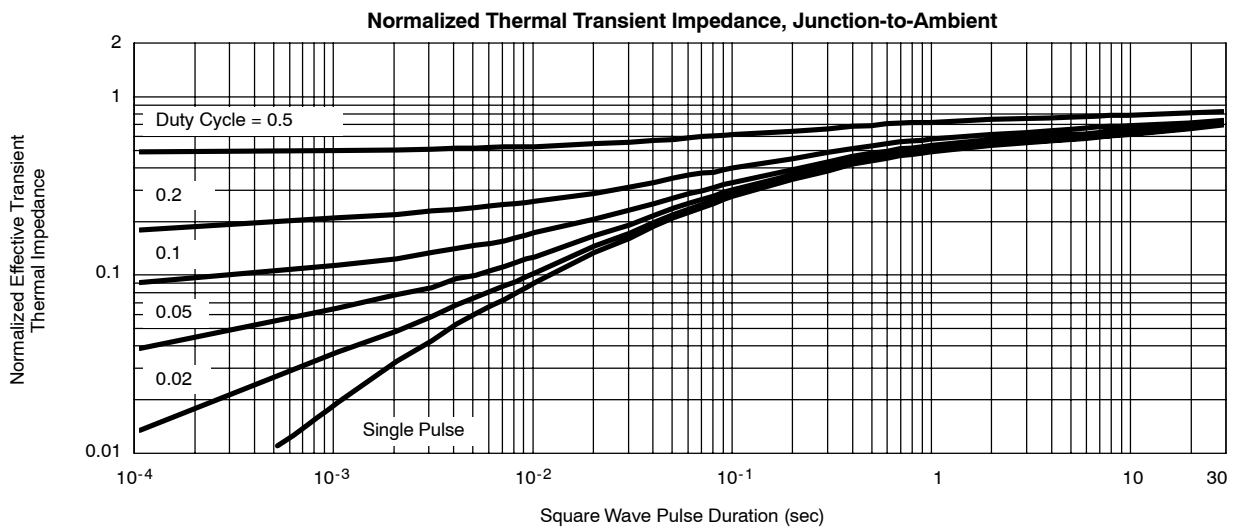
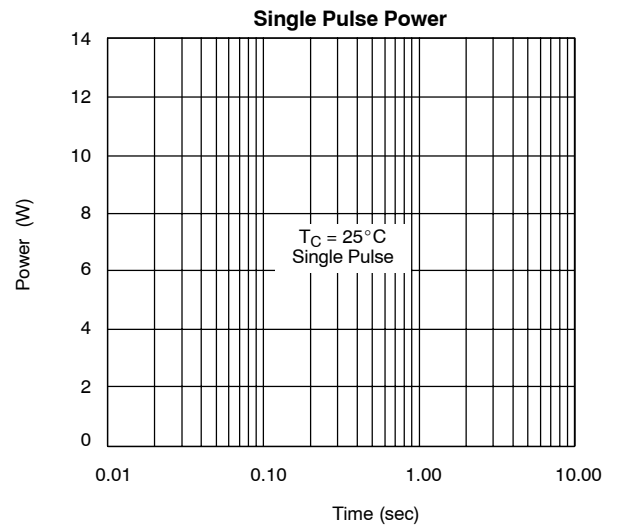
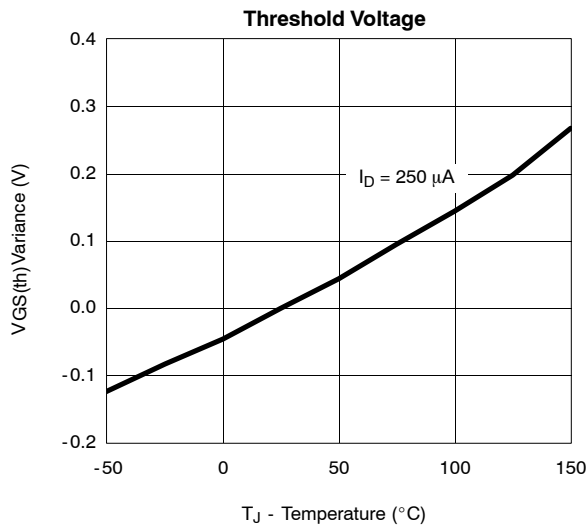
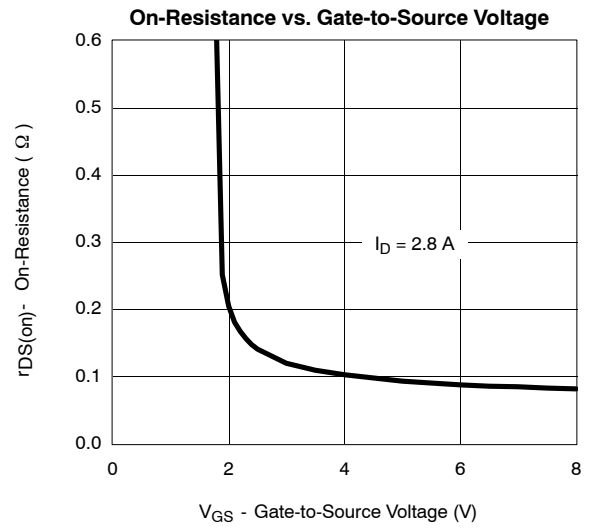
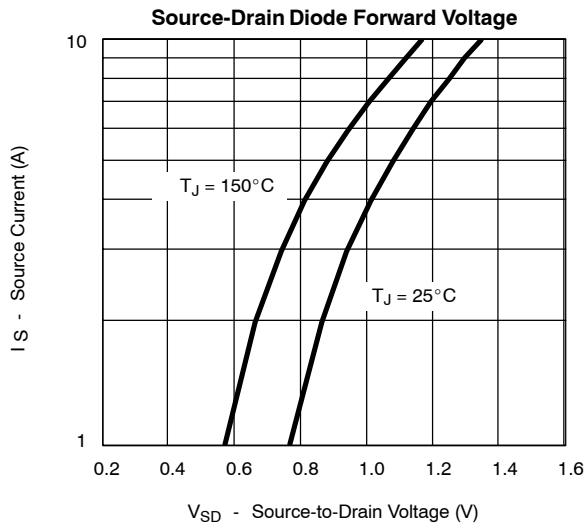
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## ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Drain-Source On-State Resistance <sup>1)</sup>	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -2.3A$		105	130	m $\Omega$
		$V_{GS} = -2.5V, I_D = -2.0A$		145	190	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.45			V
Zero Gate Voltage Drain Current $I_{D0}$	$I_{DSS}$	$V_{DS} = -16V, V_{GS} = 0V$			-1	uA
		$V_{DS} = -16V, V_{GS} = 0V, T_J = 55^\circ C$			-10	
Gate Body Leakage	$I_{GSS}$	$V_{GS} = \pm 8V, V_{DS} = 0V$			$\pm 100$	nA
Forward Transconductance <sup>1)</sup>	$g_{fs}$	$V_{DS} = -5V, I_D = -2.3A$		6.5	—	S
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS} = -6V, I_D \cong -2.3A$ $V_{GS} = -4.5V$		5.8		nC
Gate-Source Charge	$Q_{gs}$			0.85		
Gate-Drain Charge	$Q_{gd}$			1.7		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6V, R_L = 6\Omega$ $I_D \cong -1.0A, V_{GEN} = -4.5V$ $R_G = 6\Omega$		13		ns
Turn-On Rise Time	$t_r$			36		
Turn-Off Delay Time	$t_{d(off)}$			42		
Turn-Off Fall Time	$t_f$			34		
Input Capacitance	$C_{iss}$	$V_{DS} = -6V, V_{GS} = 0V$ $f = 1.0 MHz$		415		pF
Output Capacitance	$C_{oss}$			223		
Reverse Transfer Capacitance	$C_{rss}$			87		
<b>Source-Drain Diode</b>						
Max. Diode Forward Current	$I_S$				-1.6	A
Diode Forward Voltage	$V_{SD}$	$I_S = -1.0A, V_{GS} = 0V$		-0.8	-1.2	V

<sup>1)</sup> Pulse test: pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$





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