

PTD3004
30V/50A N-Channel Advanced Power MOSFET

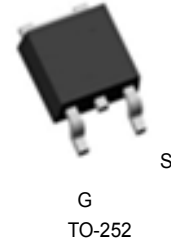
Features

- Low $R_{DS(on)}$ @ 5V Logic.
- 5V Logic Level Control
- TO-252 SMD Package
- Pb-Free, RoHS Compliant

BVDSS	30	V
ID	50	A
$R_{DS(on)}@V_{GS}=10V$	10	mΩ
$R_{DS(on)}@V_{GS}=5V$	13	mΩ

Applications

- High Side Load Switch
- Battery Switch
- Optimized for Power Management Applications for Portable Products, such as Aeromodelling, Power bank, Brushless motor, Main board , and Others



Absolute Maximum Ratings

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Symbol	Parameter	Rating	Unit	
Common Ratings (T_c=25°C Unless Otherwise Noted)				
V _{GS}	Gate-Source Voltage	±20	V	
V _{(BR)DSS}	Drain-Source Breakdown Voltage	30	V	
T _J	Maximum Junction Temperature	175	°C	
T _{STG}	Storage Temperature Range	-55 to 175	°C	
I _S	Diode Continuous Forward Current	T _c = 25°C	50	A
Mounted on Large Heat Sink				
I _{DM}	Pulse Drain Current Tested (Silicon Limit)	T _c = 25°C	140	A
I _D	Continuous Drain current @V _{GS} =10V (Note 2)	T _c = 25°C	50	A
P _D	Maximum Power Dissipation	T _c = 25°C	32	W
EAS	Avalanche Energy, Single Pulsed (Note 3)		220	mJ
R _{θJA}	Thermal Resistance <i>Junction-to-Ambient</i> – Steady State (Note 1)		62	°C/W
	Thermal Resistance <i>Junction-to-Ambient</i> – t ≤ 5 s (Note 1)		3.3	°C/W

Note :

1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [2 oz] including traces).
2. Pulse Test: pulse width ≤ 300 us, duty cycle ≤ 2%
3. Limited by Tjmax, starting T_J = 25°C, L = 0.1mH, R_G = 25Ω, I_{AS} = 35A, V_{GS} = 10V. Part not recommended for use above this value

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Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	30	--	--	V
I _{DSS}	Zero Gate Voltage Drain current(Tc=25°C)	VDS=24V,VGS=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tc=125°C)	VDS=24V,VGS=0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
V _{GS(TH)}	Gate Threshold Voltage	VDS=VGS,ID=-250μA	1.2	1.8	2.5	V
R _{DS(ON)}	Drain-Source On-State Resistance note A	VGS=10V, ID=30A		7.5	10	mΩ
R _{DS(ON)}	Drain-Source On-State Resistance note A	VGS=5V, ID=20A	--	9	13	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated) note B						
C _{iss}	Input Capacitance	VDS=15V,VGS=0V, f=1MHz	--	1500	--	pF
C _{oss}	Output Capacitance		--	300	--	pF
C _{rss}	Reverse Transfer Capacitance		--	135	--	pF
Q _g	Total Gate Charge	VGS=10V	--	11	--	nC
		VGS=4.5V		9		nC
Q _{gs}	Gate-Source Charge	VDS=15V,ID=10A, VGS=10V	--	25	--	nC
Q _{gd}	Gate-Drain Charge		--	5	--	nC
Switching Characteristics note B						
t _{d(on)}	Turn-on Delay Time	VDD=15V, ID=10A, RG=4.7Ω, VGS=10V	--	22	--	nS
t _r	Turn-on Rise Time		--	8	--	nS
t _{d(off)}	Turn-Off Delay Time		--	9	--	nS
t _f	Turn-Off Fall Time		--	6	--	nS
Source- Drain Diode Characteristics@ T_J = 25°C (unless otherwise stated)						
I _{SD}	Source-drain current(Body Diode)	Tc=25°C	--	--	50	A
V _{SD}	Forward on voltage	IS=20A,VGS=0V	--	0.82	1.2	V
t _{rr}	Reverse Recovery Time	Tj=25°C,ISD=20A, VGS=0V	--	22	--	nS
Q _{rr}	Reverse Recovery Charge		di/dt=100A/μs	--	15	--

Note:

A: Pulse Test: pulse width ≤ 300 us, duty cycle ≤ 2%

B: Guaranteed by design, not subject to production testing.

Typical Characteristics

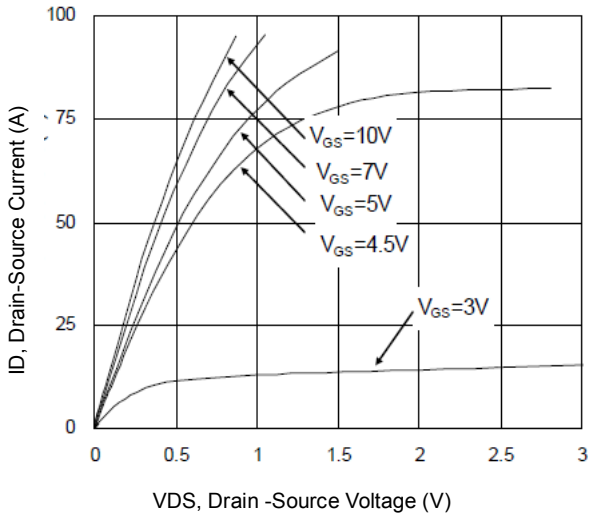


Fig1. Typical Output Characteristics

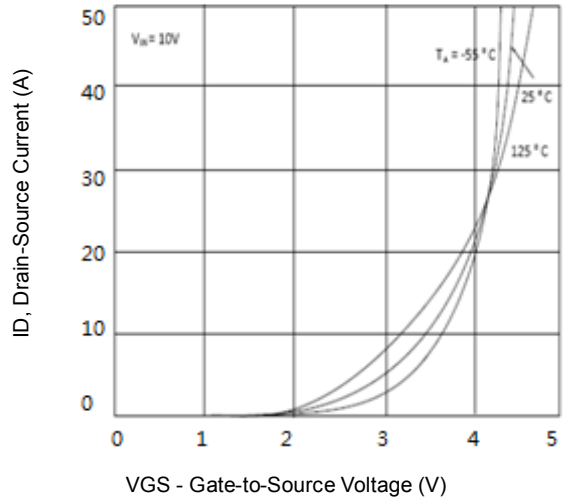


Fig2. Transfer Characteristics

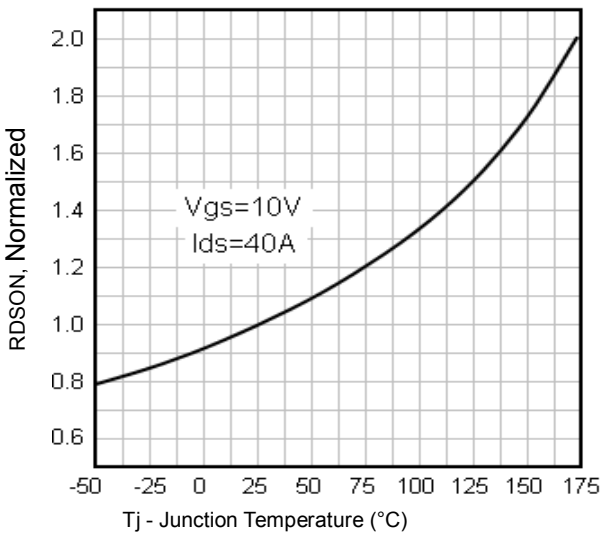


Fig3. Normalized On-Resistance Vs. Temperature

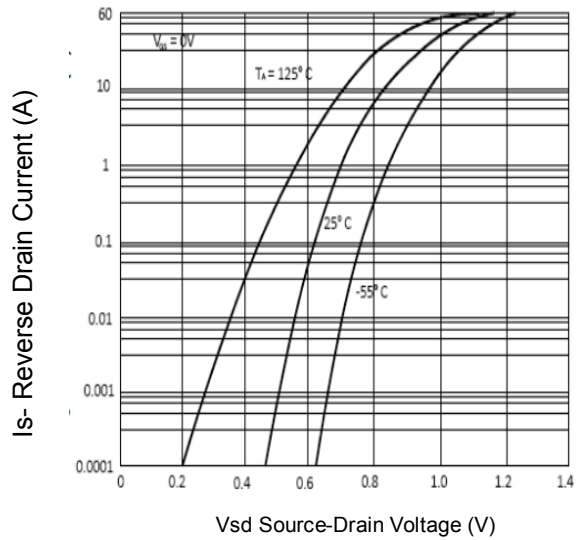


Figure4. Source-Drain Diode Forward

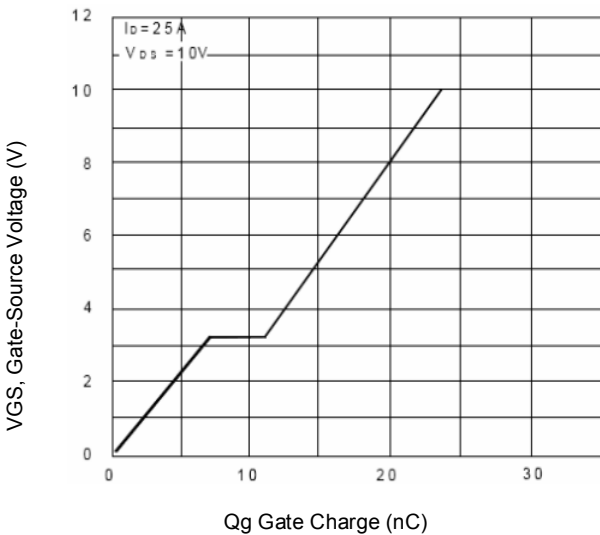


Figure 5. Gate Charge Vs. Gate-Source Voltage

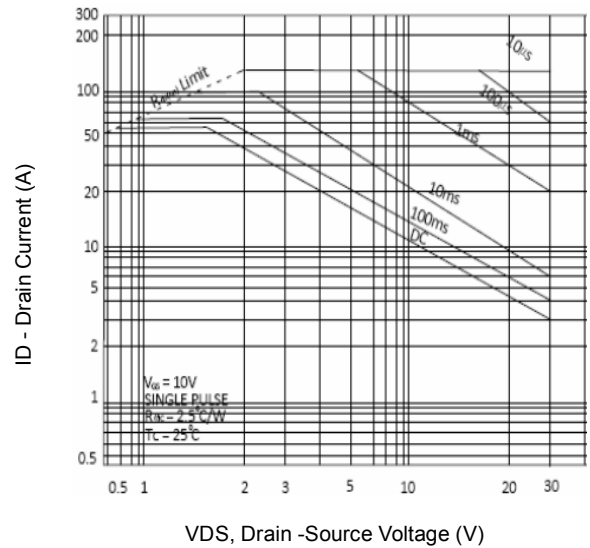


Fig6. Maximum Safe Operating Area

Typical Characteristics

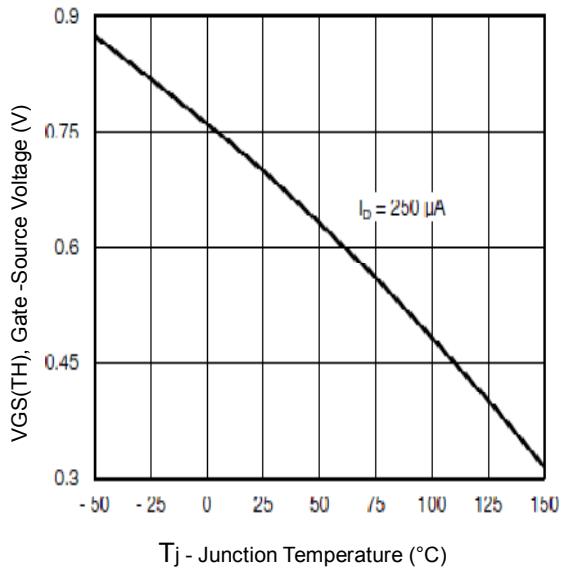


Fig7. Threshold Voltage Vs. Temperature

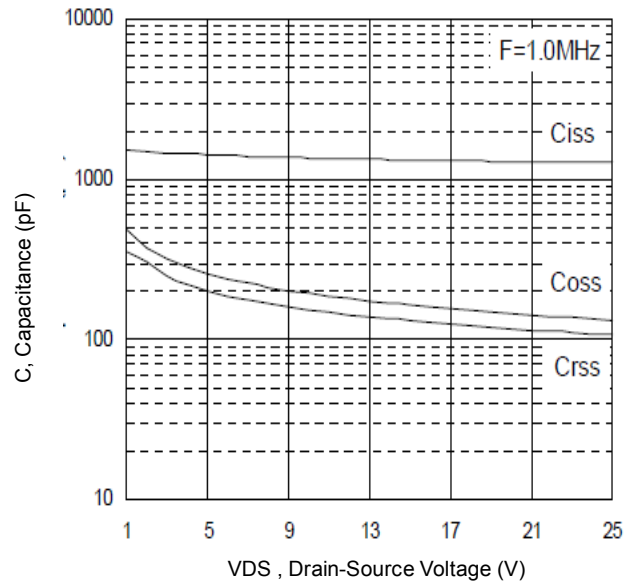


Fig8. Typical Capacitance Vs. Drain-Source Voltage

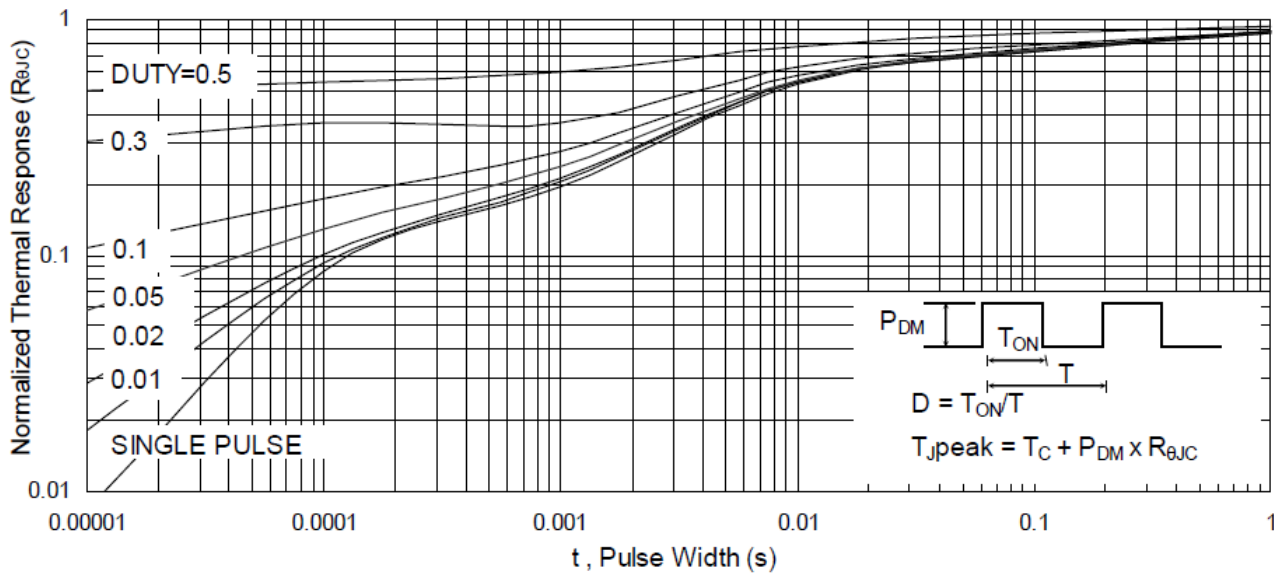


Fig9. Normalized Maximum Transient Thermal Impedance

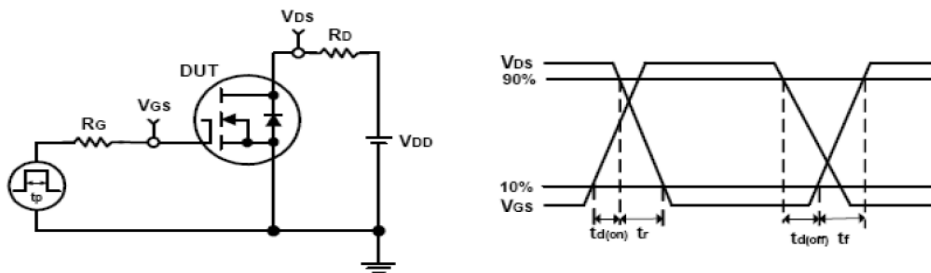


Fig10. Switching Time Test Circuit and waveforms

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