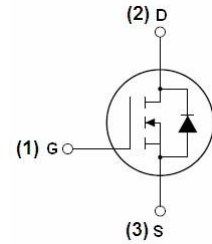


PTD60N02

20V N-Channel Enhancement Mode MOSFET

Description

The PTD60N02 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = 20V$ $I_D = 60A$

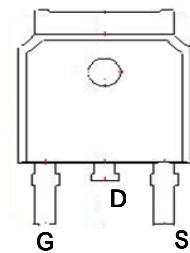
$R_{DS(ON)} < 6m\Omega @ V_{GS}=4.5V$

Application

Battery protection

Load switch

Uninterruptible power supply



TO-252

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	60	A
Drain Current-Continuous($T_c=100^\circ C$)	$I_D(100^\circ C)$	42	A
Pulsed Drain Current	I_{DM}	210	A
Maximum Power Dissipation	P_D	60	W
Single pulse avalanche energy (Note 5)	E_{AS}	64	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	2.1	$^\circ C/W$

20V N-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_c=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	20	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±12V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.5	0.75	1.0	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =20 A	-	4.8	6	mΩ
		V _{GS} =2.5V, I _D =15A		6.2	9	mΩ
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =20A	15	-	-	S
Input Capacitance	C _{ISS}	V _{DS} =10V, V _{GS} =0V, F=1.0MHz	-	2000	-	PF
Output Capacitance	C _{OSS}		-	500	-	PF
Reverse Transfer Capacitance	C _{RSS}		-	200	-	PF
Turn-on Delay Time	t _{d(on)}	V _{DD} =10V, I _D =2A, R _L =1Ω V _{GS} =4.5V, R _G =3Ω	-	6.4	-	nS
Turn-on Rise Time	t _r		-	17.2	-	nS
Turn-Off Delay Time	t _{d(off)}		-	29.6	-	nS
Turn-Off Fall Time	t _f		-	16.8	-	nS
Total Gate Charge	Q _g	V _{DS} =10V, I _D =20A, V _{GS} =10V	-	27		nC
Gate-Source Charge	Q _{gs}		-	6.5		nC
Gate-Drain Charge	Q _{gd}		-	6.4		nC
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =10A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	60	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 20A di/dt = 100A/μs ^(Note3)	-	25	-	nS
Reverse Recovery Charge	Q _{rr}		-	24	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition : T_J=25°C, V_{DD}=10V, V_G=10V, L=0.5mH, I_{AS}=16A

20V N-Channel Enhancement Mode MOSFET

Typical Electrical and Thermal Characteristics (Curves)

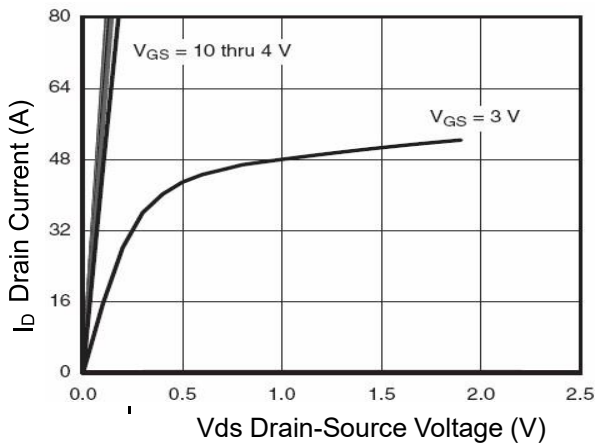


Figure 1 Output Characteristics

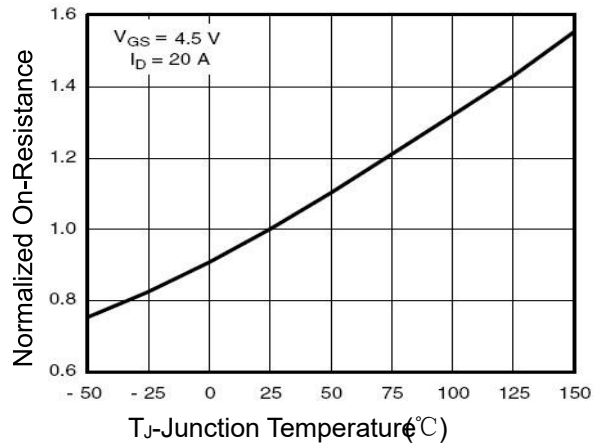


Figure 4 Rdson-Junction Temperature

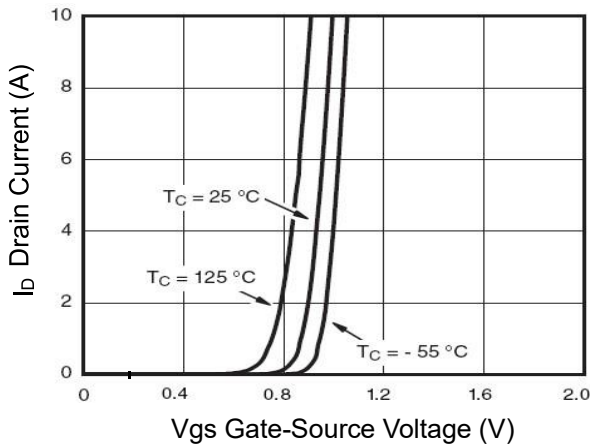


Figure 2 Transfer Characteristics

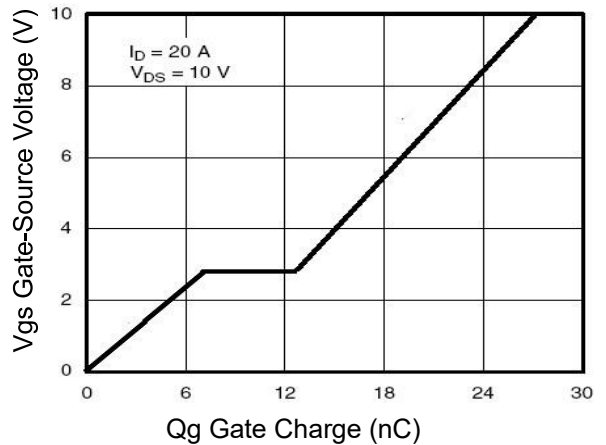


Figure 5 Gate Charge

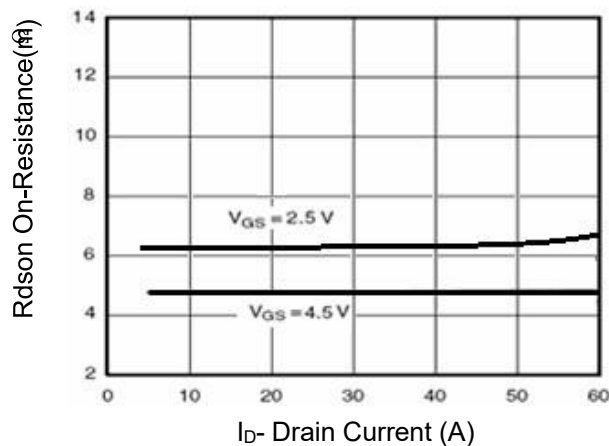


Figure 3 Rdson- Drain Current

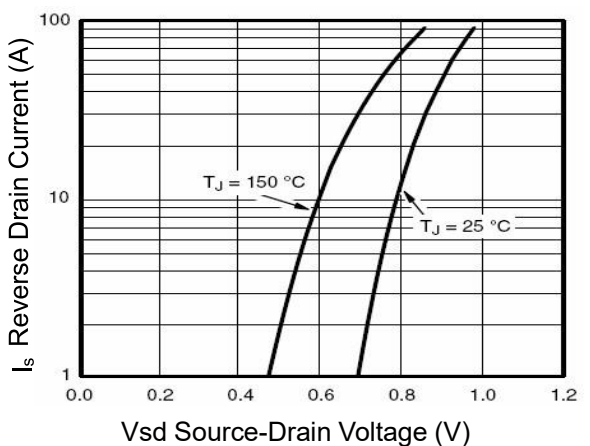
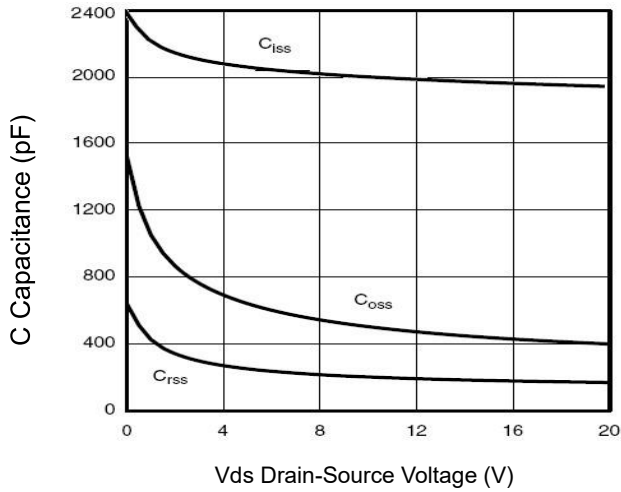
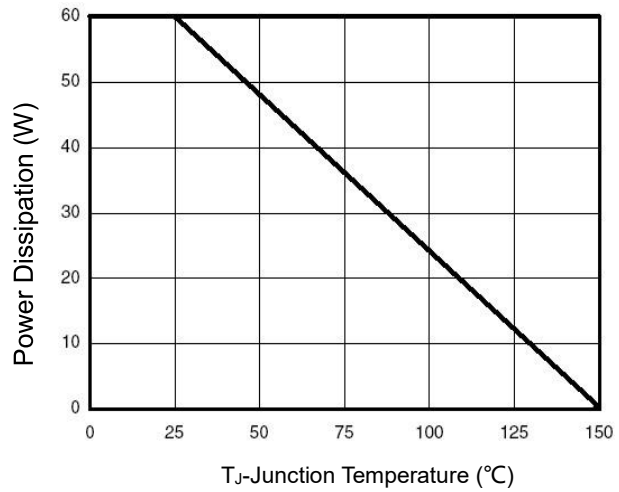


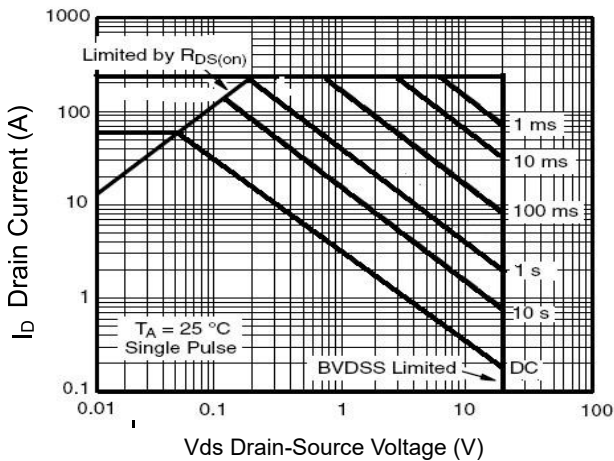
Figure 6 Source- Drain Diode Forward



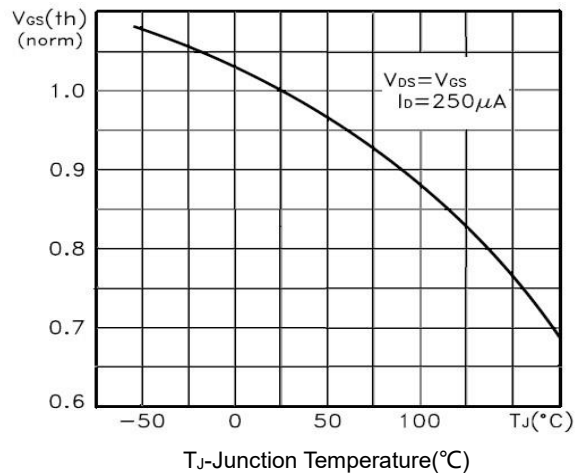
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



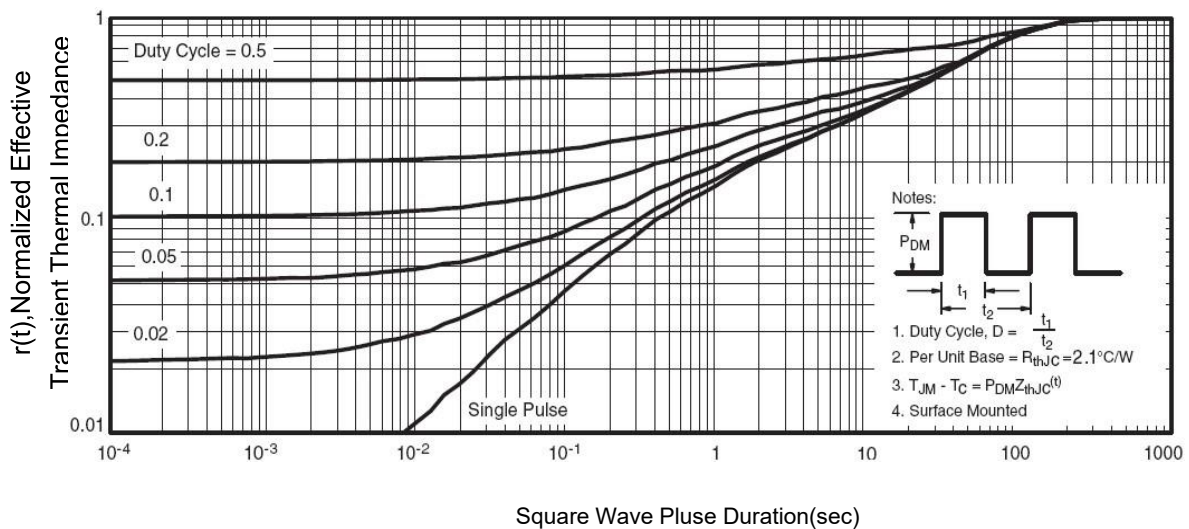
T_J-Junction Temperature (°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_J-Junction Temperature(°C)
Figure 10 V_{GS(th)} vs Junction Temperature



Square Wave Pulse Duration(sec)
Figure 11 Normalized Maximum Transient Thermal Impedance

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