PTN3006

PUOLOP 迪浦

30V/80A N-Channel Advanced Power MOSFET

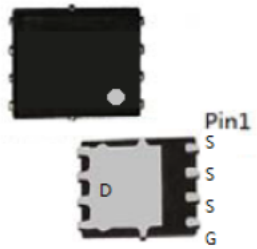
BVDSS	30	V
ID	80	A
R_{DSON}@V_{GS}=10V	4.5	mΩ
R_{DSON}@V_{GS}=5V	6.2	mΩ

Features

- *Low $R_{DS(on)}$ @ 5V Logic.*
- *5V Logic Level Control*
- *PDFN5X6 SMD Package*
- *Pb−Free, RoHS Compliant*

Applications

- *High Side Load Switch*
- *Battery Switch*
- *Optimized for Power Management Applications for Portable Products, such as Aeromodelling, Power bank, Brushless motor, Main board , and Others*



PDFN5x6

Absolute Maximum Ratings

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Symbol	Parameter		Rating	Unit
Common Ratings (T_C=25°C Unless Otherwise Noted)				
V_{GS}	Gate-Source Voltage		±20	V
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage		30	V
T_J	Maximum Junction Temperature		175	°C
T_{STG}	Storage Temperature Range		-55 to 175	°C
I_S	Diode Continuous Forward Current	T_C=25°C	60	A
Mounted on Large Heat Sink				
I_{DM}	Pulse Drain Current Tested (Sillicon Limit)	T_C=25°C	240	A
I_D	Continuous Drain current @V_{GS}=10V (Note 2)	T_C=25°C	80	A
P_D	Maximum Power Dissipation	T_C=25°C	41	W
EAS	Avalanche Energy, Single Pulsed (Note 3)		85	mJ
$R_{\theta JA}$	Thermal Resistance *Junction−to−*Ambient – Steady State (Note 1)		62	°C/W
	Thermal Resistance *Junction−to−*Ambient –t ≤ 5 s (Note 1)		2.2	°C/W

Note :

1. Surface−mounted on FR4 board using 1 in sq. pad size (Cu area = 1.127 in sq. [2 oz] including traces).
2. Pulse Test: pulse width ≤ 300 us, duty cycle ≤ 2%
3. Limited by Tjmax, starting TJ = 25°C, L = 0.1mH,R_G = 25Ω, I_{AS} = 40A, V_{GS} =10V. Part not recommended for use above this value

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V ID=250μA	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain current(Tc=25℃)	VDS=24V,VGS=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tc=125℃)	VDS=24V,VGS=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	VDS=VGS,ID=-250μA	1.2	1.8	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance note A	VGS=10V, ID=30A		4.5	6.5	mΩ
$R_{DS(ON)}$	Drain-Source On-State Resistance note A	VGS=5V, ID=20A	--	7.0	8.5	mΩ
Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise stated) note B						
C_{iss}	Input Capacitance	VDS=15V,VGS=0V, f=1MHz	--	1900	--	pF
C_{oss}	Output Capacitance		--	190	--	pF
C_{rss}	Reverse Transfer Capacitance		--	65	--	pF
Q_g	Total Gate Charge VGS=10V	VDS=15V,ID=20A, VGS=10V	--	15	--	nC
	Total Gate Charge VGS=4.5V			13		nC
Q_{gs}	Gate-Source Charge		--	30	--	nC
Q_{gd}	Gate-Drain Charge		--	8	--	nC
Switching Characteristics note B						
$t_{d(on)}$	Turn-on Delay Time	VDD=15V, ID=20A, RG=4.7Ω, VGS=10V	--	29	--	nS
t_r	Turn-on Rise Time		--	11	--	nS
$t_{d(off)}$	Turn-Off Delay Time		--	12	--	nS
t_f	Turn-Off Fall Time		--	9	--	nS
Source- Drain Diode Characteristics@ TJ = 25°C (unless otherwise stated)						
I_{SD}	Source-drain current(Body Diode)	Tc=25℃	--	--	60	A
V_{SD}	Forward on voltage	IS=40A,VGS=0V	--	0.80	1.2	V
t_{rr}	Reverse Recovery Time	Tj=25℃,ISD=20A, VGS=0V di/dt=100A/μs	--	28	--	nS
Q_{rr}	Reverse Recovery Charge		--	18	--	nC

Note:

A: Pulse Test: pulse width ≤ 300 us, duty cycle ≤ 2%

B:Guranteed by design, not subject to production testing.

Typical Characteristics

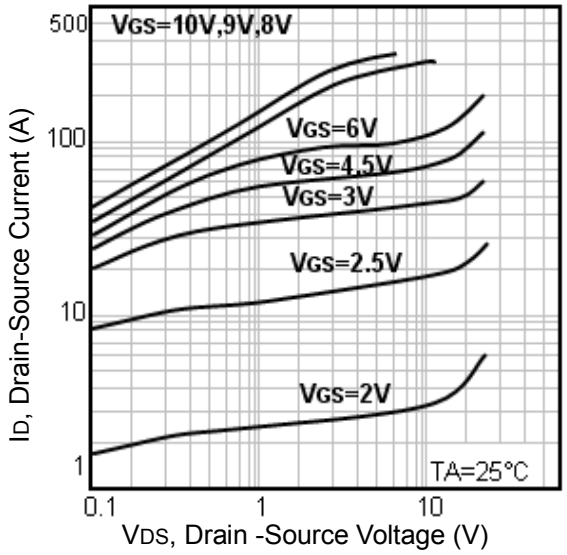


Fig1. Typical Output Characteristics

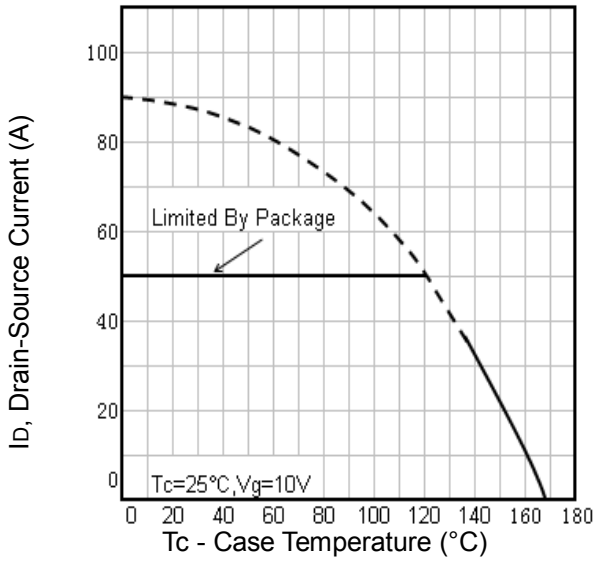


Fig2. Maximum Drain Current Vs.Case Temperature

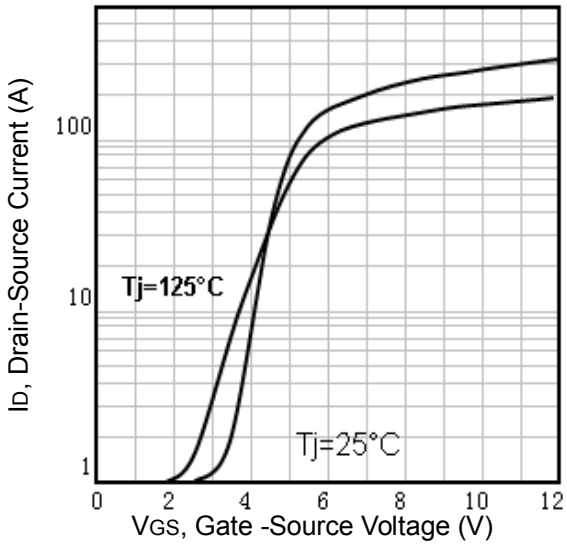


Fig3. Typical Transfer Characteristics

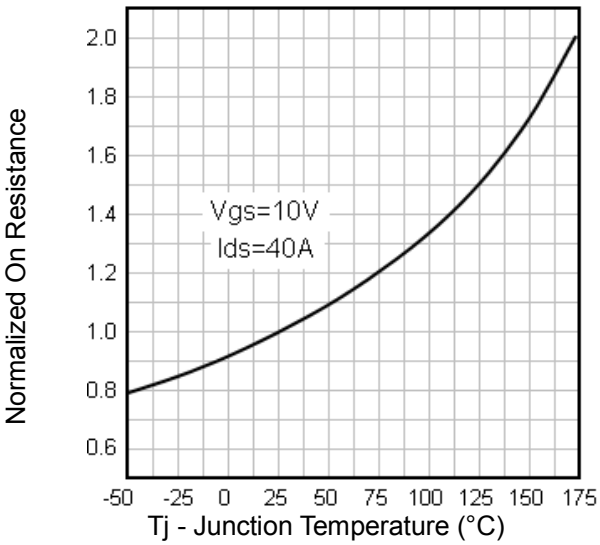


Fig4. Normalized On-Resistance Vs. Temperature

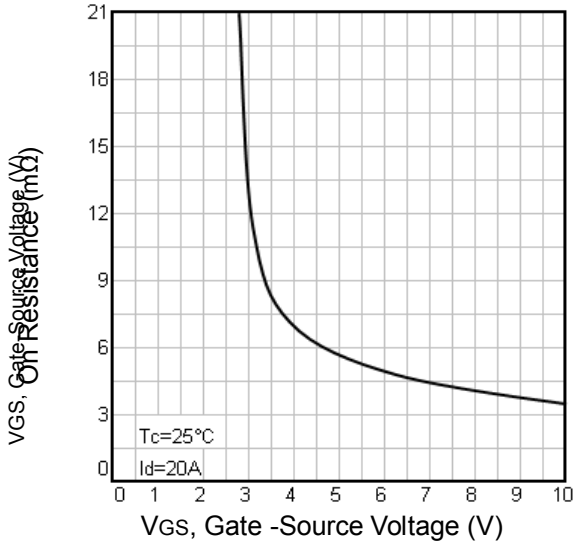


Fig5. On Resistance Vs. Gate -Source Voltage

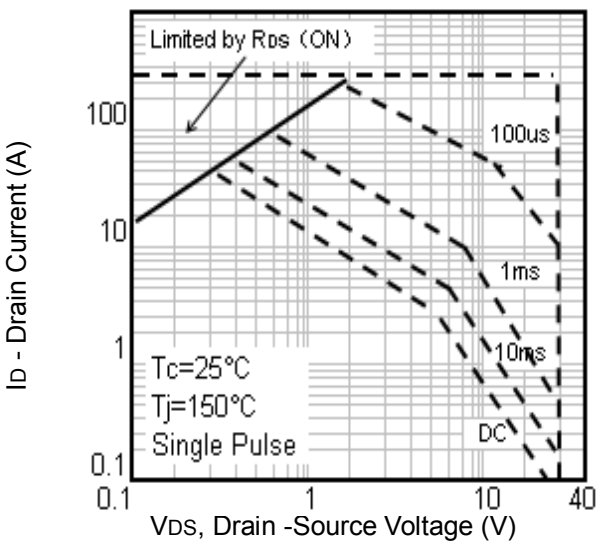


Fig6. Maximum Safe Operating Area

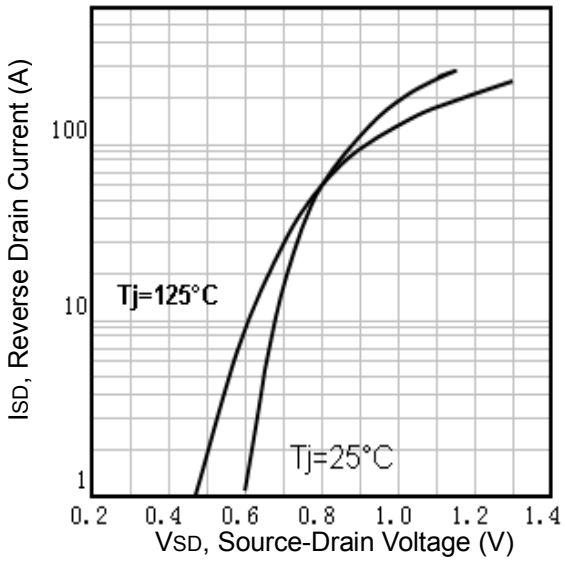


Fig7. Typical Source-Drain Diode Forward Voltage

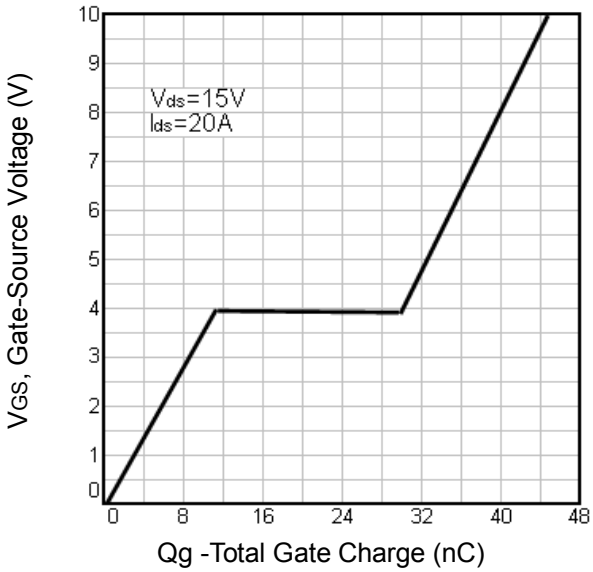


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

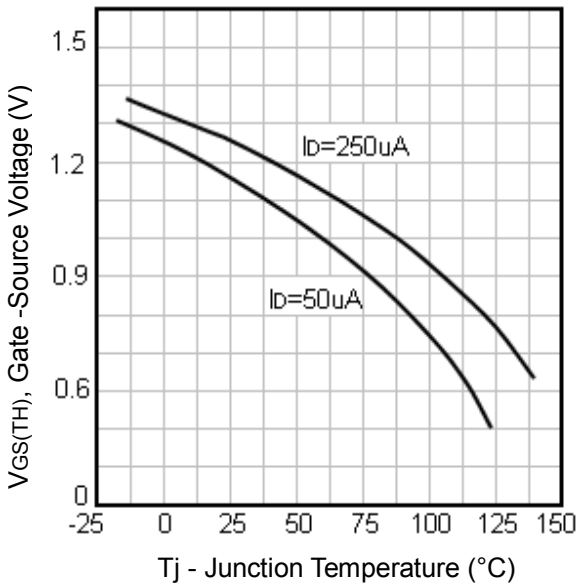


Fig9. Threshold Voltage Vs. Temperature

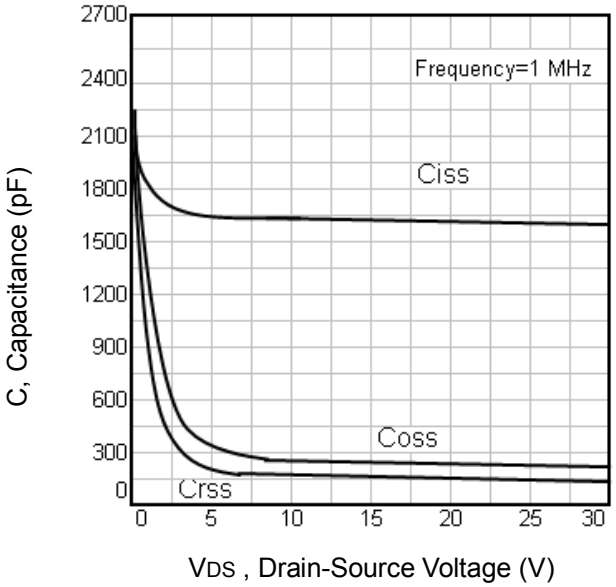


Fig10. Typical Capacitance Vs.Drain-Source Voltage

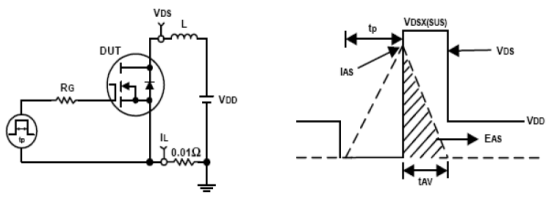


Fig11. Unclamped Inductive Test Circuit and waveforms

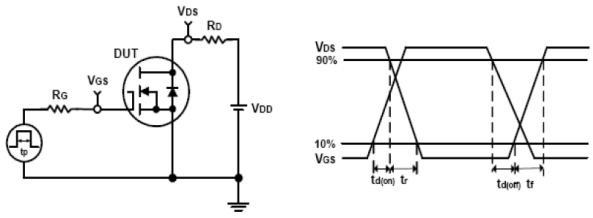


Fig12. Switching Time Test Circuit and waveforms

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