

## 20V N-Channel Enhancement Mode MOSFET

### VDS= 20V

RDS(ON), Vgs@ 4.5V, Ids@ 3.6A <70mΩ

RDS(ON), Vgs@ 2.5V, Ids@ 3.1A <80mΩ

### Features

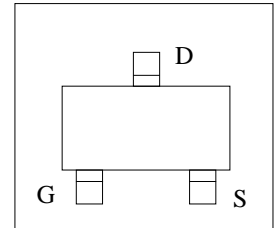
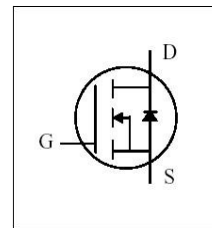
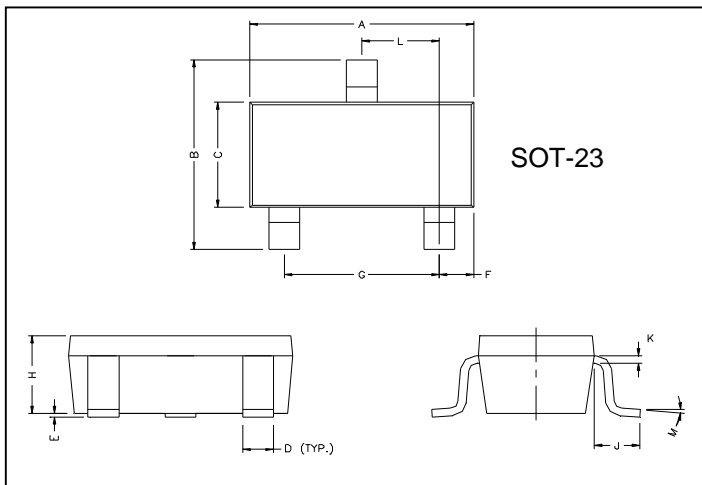
Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

High Power and Current handing capability

Ideal for Li ion battery pack applications

### Package Dimensions



REF.	Millimeter		REF.	Millimete	
	Min.	Max.		Min.	Max.
A	2.80	3.00	G	1.80	2.00
B	2.30	2.50	H	0.90	1.1
C	1.20	1.40	K	0.10	0.20
D	0.30	0.50	J	0.35	0.70
E	0	0.10	L	0.92	0.98
F	0.45	0.55	M	0°	10°

### Maximum Ratings and Thermal Characteristics (TA = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	20	V	
Gate-Source Voltage	V <sub>GS</sub>	± 12		
Continuous Drain Current	I <sub>D</sub>	3.6	A	
Pulsed Drain Current <sup>1)</sup>	I <sub>DM</sub>	8		
Maximum Power Dissipation	P <sub>D</sub>	TA = 25°C	1.25	W
		TA = 75°C	0.8	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C	
Junction-to-Ambient Thermal Resistance (PCB mounted) <sup>2)</sup>	R <sub>θJA</sub>	78	°C/W	

#### Notes

<sup>1)</sup> Pulse width limited by maximum junction temperature.

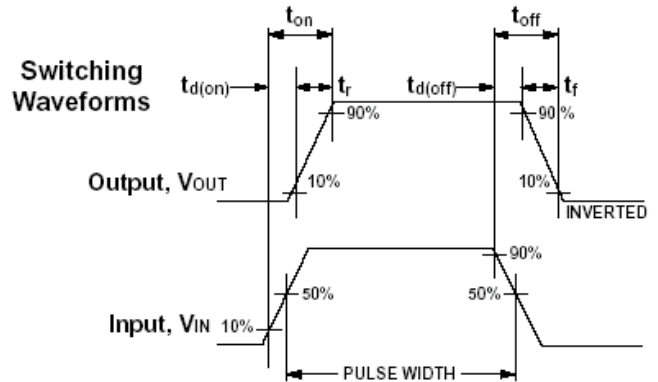
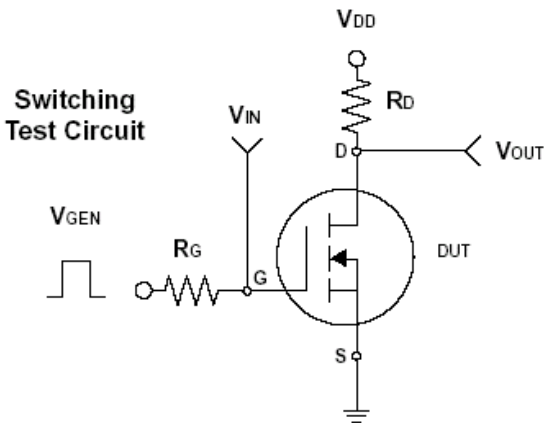
<sup>2)</sup> Surface Mounted on FR4 Board, t ≤ 5 sec.

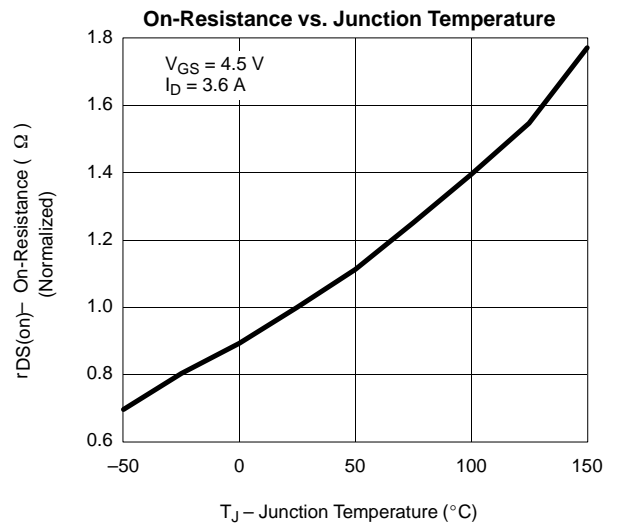
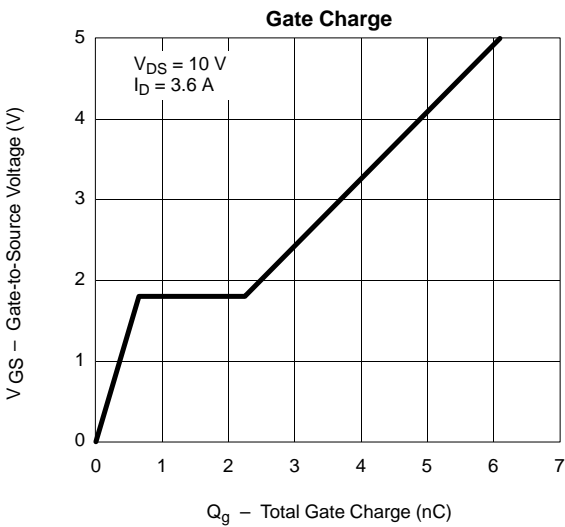
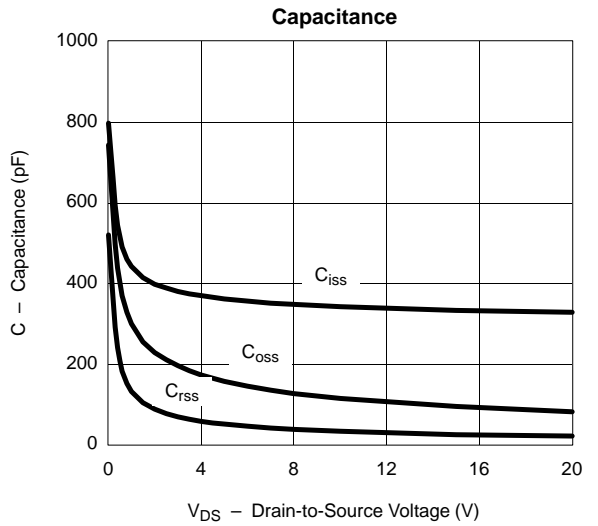
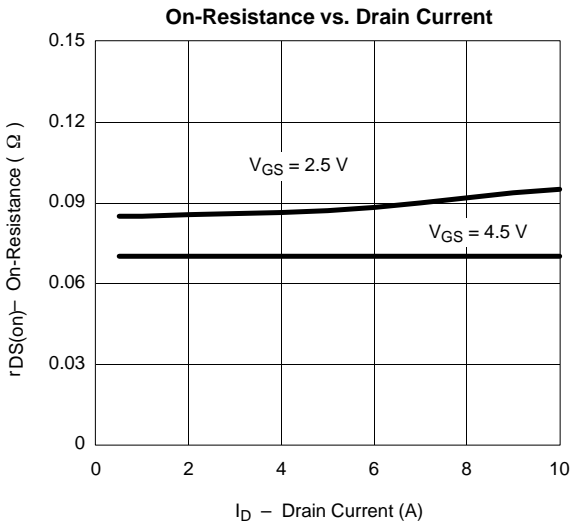
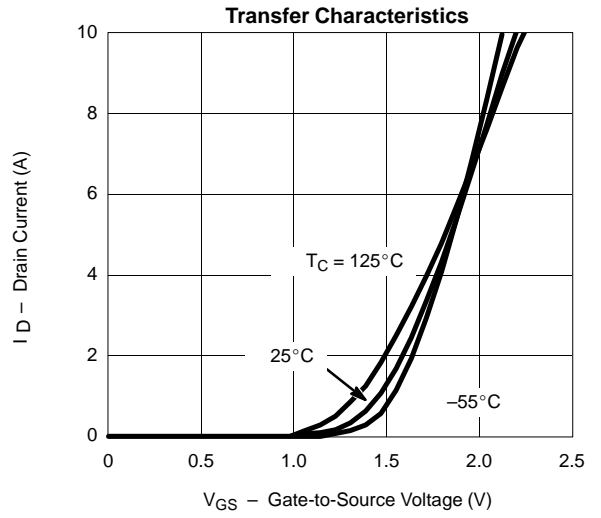
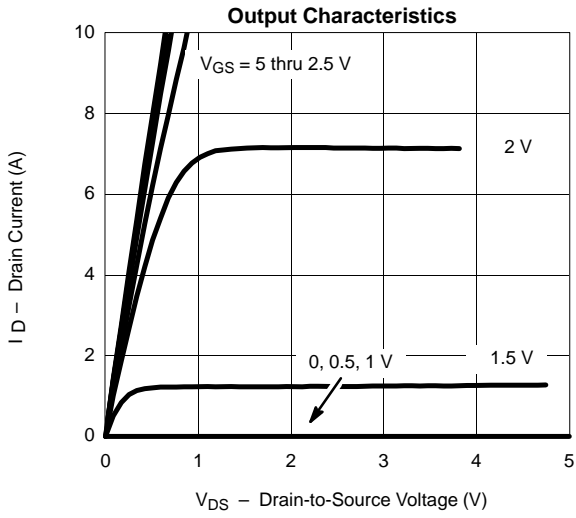
ELECTRICAL CHARACTERISTICS (TA = 25oC unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Static</b> <sup>3)</sup>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	20			V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 2.5V, I_D = 3.1A$		70.0	80.0	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 3.6A$		60.0	70.0	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.5	0.76	1.5	V
Zero Gate Voltage Drain Current 0	$I_{DSS}$	$V_{DS} = 20V, V_{GS} = 0V$			1	uA
Gate Body Leakage	$I_{GSS}$	$V_{GS} = \pm 12V, V_{DS} = 0V$			±100	nA
Forward Transconductance	$g_{fs}$	$V_{DS} = 5V, I_D = 4.2A$		5	—	S
<b>Dynamic</b> <sup>4)</sup>						
Total Gate Charge	$Q_g$	$V_{DS} = 10V, I_D = 3.6A$ $V_{GS} = 4.5V$		5.4		nC
Gate-Source Charge	$Q_{gs}$			0.65		
Gate-Drain Charge	$Q_{gd}$			1.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10V, R_G = 6\Omega$ $I_D = 1A, V_{GS} = 4.5V$ $R_L = 5.5\Omega$		12		ns
Turn-On Rise Time	$t_r$			36		
Turn-Off Delay Time	$t_{d(off)}$			34		
Turn-Off Fall Time	$t_f$			10		
Input Capacitance	$C_{iss}$	$V_{DS} = 10V, V_{GS} = 0V$ $f = 1.0\text{ MHz}$		340		pF
Output Capacitance	$C_{oss}$			115		
Reverse Transfer Capacitance	$C_{rss}$			33		
<b>Source-Drain Diode</b>						
Max. Diode Forward Current	$I_S$				1.6	A
Diode Forward Voltage	$V_{SD}$	$I_S = 1.0A, V_{GS} = 0V$			1.0	V

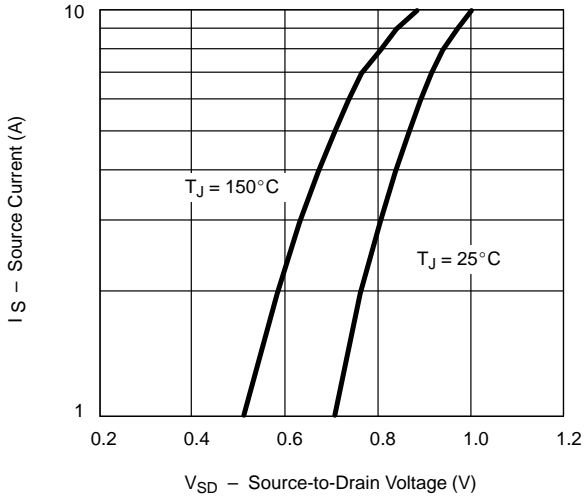
Notes

- 3) Short duration test pulse used to minimize self-heating effect.
- 4) Pulse test pulse width ≤ 300us, duty cycle ≤ 2%.

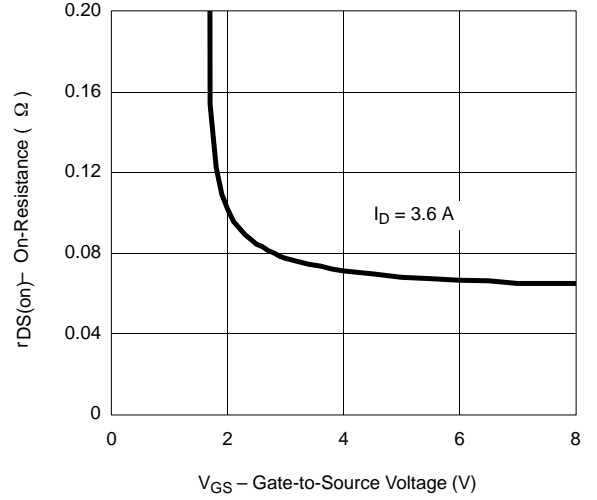




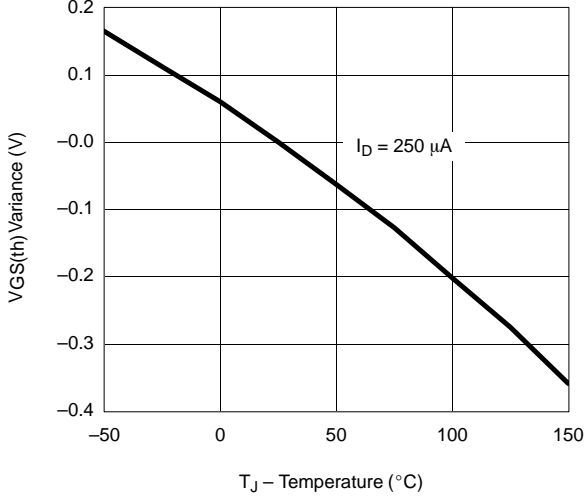
Source-Drain Diode Forward Voltage



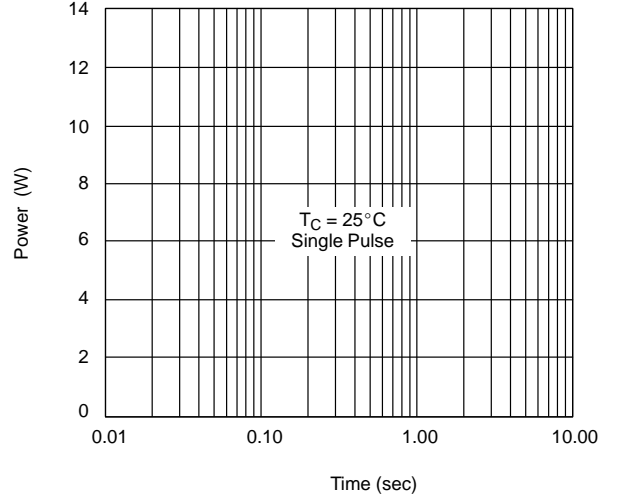
On-Resistance vs. Gate-to-Source Voltage



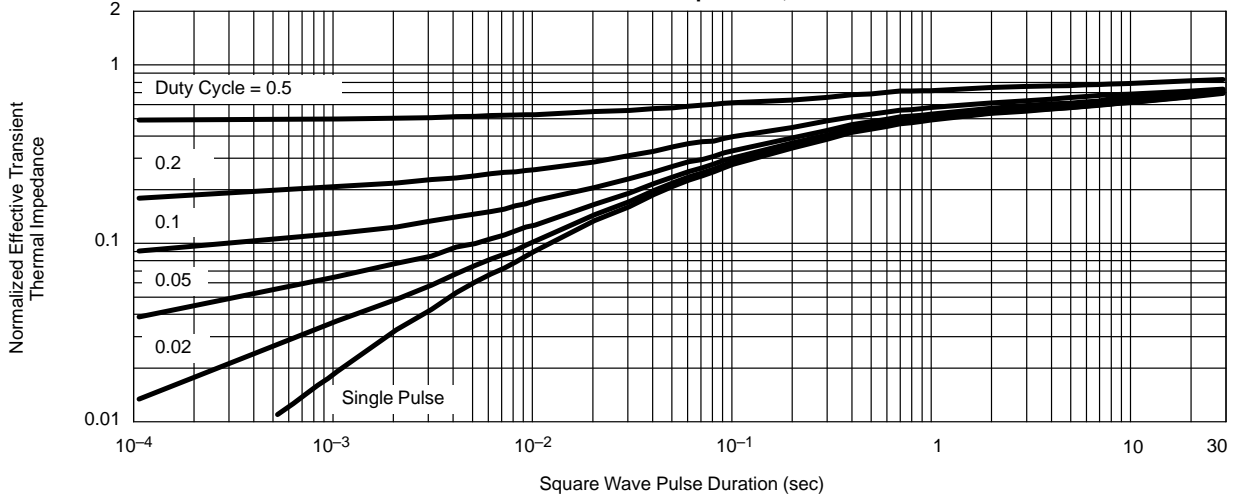
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



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