
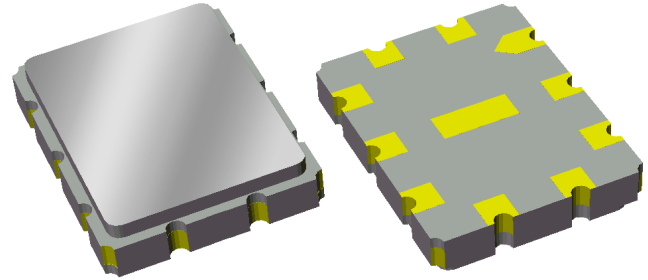


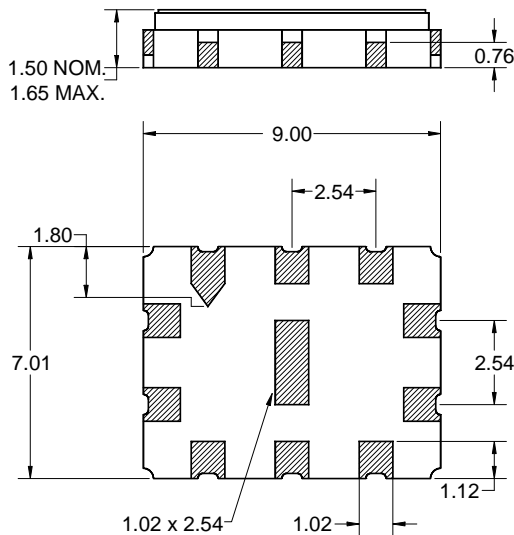
Features

- For broadband applications
- Typical 3dB bandwidth of 33.2 MHz
- High attenuation
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Replaces Sawtek P/N 851937 (BW 3dB=32 MHz)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



Package

Surface Mount 9.00 x 7.01 x 1.50 mm
SMP-35B

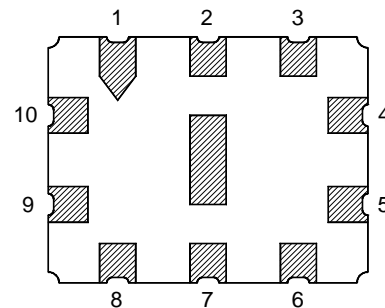


Dimensions shown are nominal in millimeters
All tolerances are ± 0.15 mm except overall
length and width $+0.10$ mm/ -0.15 mm

Body: Al_2O_3 ceramic
Lid: Kovar, Ni plated
Terminations: Au plating 0.5 - 1.0 μ m,
over a 2 - 6 μ m Ni plating

Pin Configuration

Bottom View



Single-ended Configuration

Pin No.	Description
4	Output
5	Output return
9	Input
10	Input return
1,2,3,6,7,8	Case ground

Electrical Specifications ⁽¹⁾

Operating Temperature Range: ⁽²⁾ 0 to +70 °C

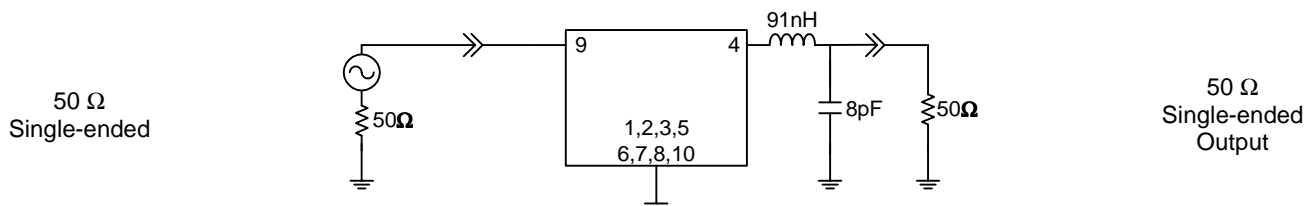
Parameter ⁽³⁾	Minimum	Typical ⁽⁴⁾	Maximum	Unit
Center Frequency	-	140	-	MHz
Minimum Insertion Loss	-	21.7	22.5	dB
Lower 1 dB Bandedge ⁽⁵⁾	-	124.29	125.15	MHz
Upper 1 dB Bandedge	154.85	155.88	-	
Lower 3 dB Bandedge ⁽⁵⁾	-	123.42	124.2	MHz
Upper 3 dB Bandedge	155.8	156.64	-	
Lower 40 dB Bandedge ⁽⁵⁾	119.65	120.31	-	MHz
Upper 40 dB Bandedge	-	159.58	160.35	
Amplitude Variation 125.15 - 154.85 MHz	-	0.46	1.10	dB p-p
Phase Linearity 125.15 - 154.85 MHz	-	2.75	6.0	deg p-p
Group Delay Variation 125.15 - 154.85 MHz	-	15.46	30	ns p-p
Absolute Delay	-	0.905	-	µsec
Relative Attenuation ⁽⁵⁾				
15 - 60 MHz	45	56	-	dB
60 - 115 MHz	43	54	-	dB
165 - 200 MHz	42	52	-	dB
200 - 300 MHz	47	58	-	dB
Terminating Source Impedance: ⁽⁶⁾	-	50	-	Ω
Terminating Load Impedance: ⁽⁶⁾	-	50	-	Ω
Substrate Material	-	128 LiNbO ₃	-	-
Temperature Coefficient of Frequency	-	-74	-	ppm/°C

Notes:

1. All specifications are based on the TriQuint test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Typical values are based on average measurements at room temperature
5. Relative to minimum insertion loss
6. This is the optimum impedance in order to achieve the performance shown

Test Circuit:

Actual matching values may vary due to PCB layout and parasitics



Electrical Specifications ⁽¹⁾

Operating Temperature Range: ⁽²⁾ -40 to +85 °C

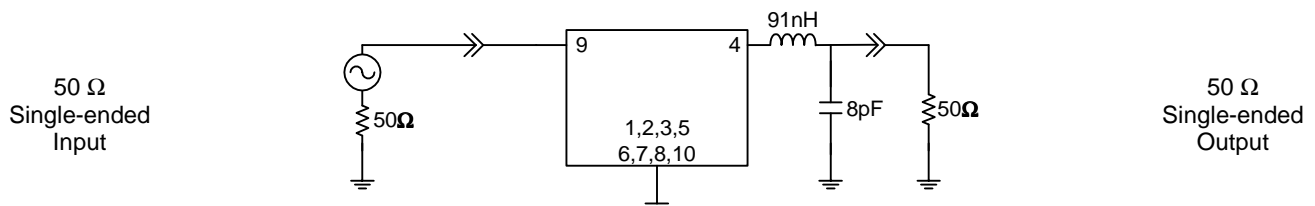
Parameter ⁽³⁾	Minimum	Typical ⁽⁴⁾	Maximum	Unit
Center Frequency	-	140	-	MHz
Minimum Insertion Loss	-	21.7	22.5	dB
Lower 1 dB Bandedge ⁽⁵⁾	-	124.29	125.25	MHz
Upper 1 dB Bandedge	154.75	155.88	-	
Lower 3 dB Bandedge ⁽⁵⁾	-	123.42	124.3	MHz
Upper 3 dB Bandedge	155.7	156.64	-	
Lower 40 dB Bandedge ⁽⁵⁾	119.50	120.31	-	MHz
Upper 40 dB Bandedge	-	159.58	160.55	
Amplitude Variation 125.15 - 154.85 MHz	-	0.46	1.30	dB p-p
Phase Linearity 125.15 - 154.85 MHz	-	2.75	6.5	deg p-p
Group Delay Variation 125.15 - 154.85 MHz	-	15.46	37	ns p-p
Absolute Delay	-	0.905	-	µsec
Relative Attenuation ⁽⁵⁾				
15 - 60 MHz	44	56	-	dB
60 - 115 MHz	43	54	-	dB
165 - 200 MHz	42	52	-	dB
200 - 300 MHz	46	58	-	dB
Terminating Source Impedance: ⁽⁶⁾	-	50	-	Ω
Terminating Load Impedance: ⁽⁶⁾	-	50	-	Ω
Substrate Material	-	128 LiNbO ₃	-	-
Temperature Coefficient of Frequency	-	-74	-	ppm/°C

Notes:

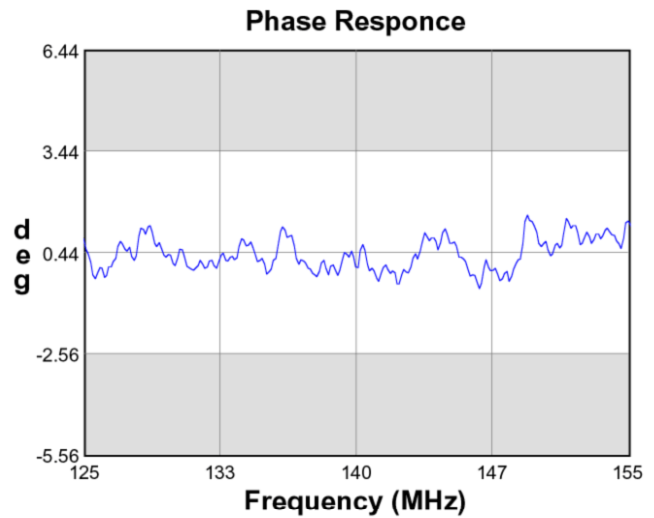
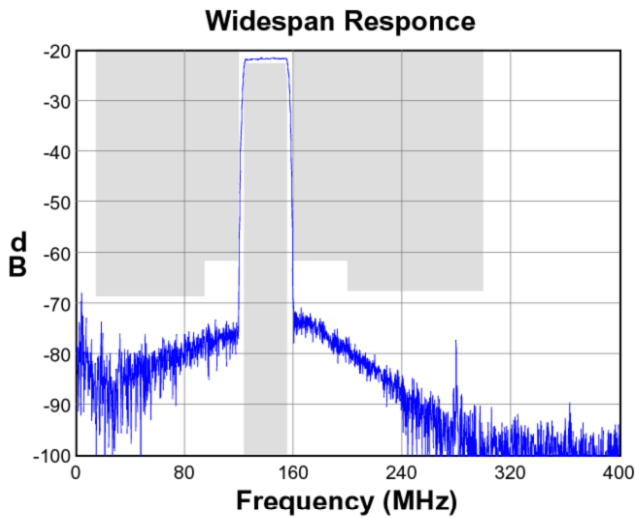
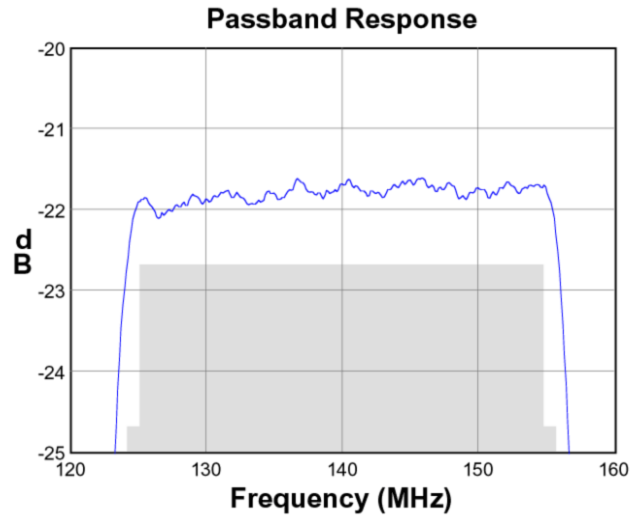
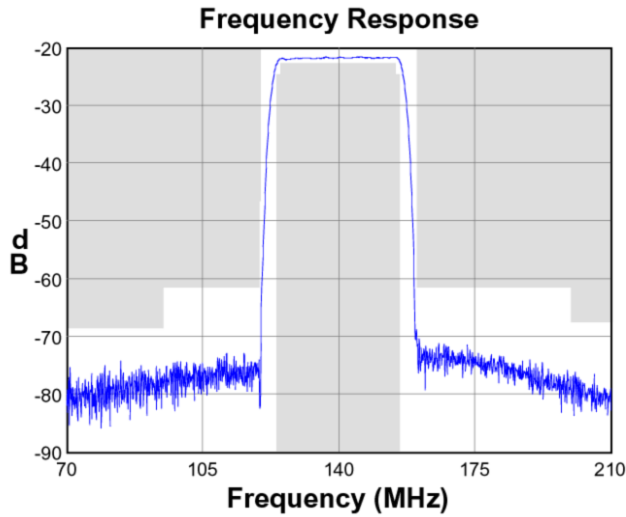
1. All specifications are based on the TriQuint test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
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4. Typical values are based on average measurements at room temperature
5. Relative to minimum insertion loss
6. This is the optimum impedance in order to achieve the performance shown

Test Circuit:

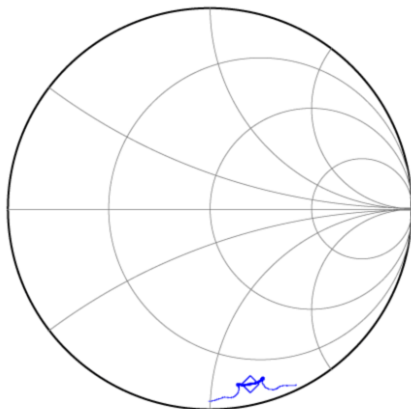
Actual matching values may vary due to PCB layout and parasitics



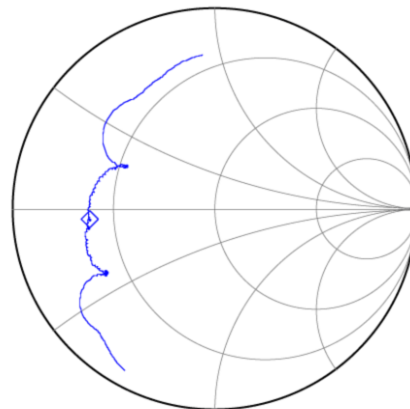
Typical Performance (at room temperature)



Input Smith Chart

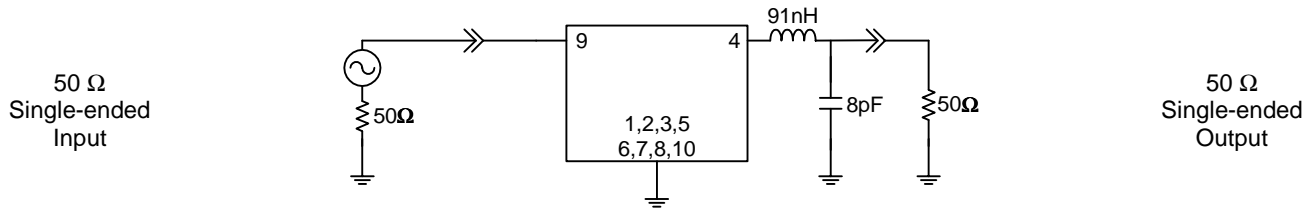


Output Smith Chart



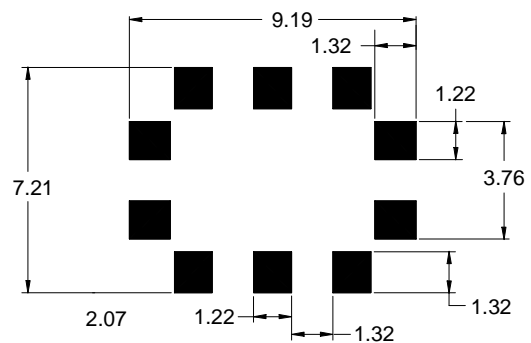
Matching Schematics

Actual matching values may vary due to PCB layout and parasitics



Marking

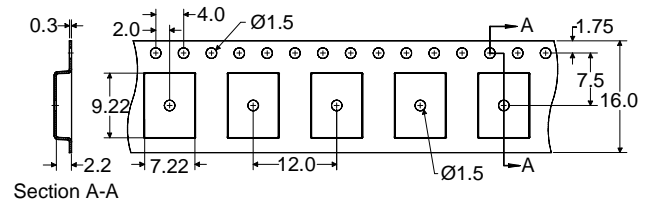
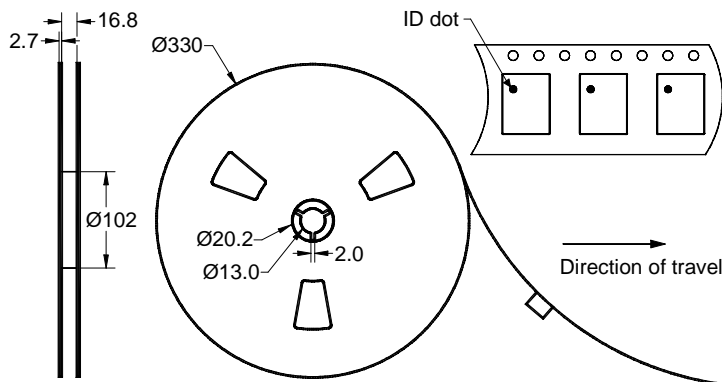
PCB Footprint



The date code consists of: day of the current year (Julian, 3 digits), last digit of the year (1 digit) and hour (2 digits)

This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel




Dimensions shown are nominal in millimeters
Packaging quantity: 2000 units/reel

Maximum Ratings


Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	-40	+85	°C
Storage Temperature Range	T _{stg}	-40	+85	°C

Important Notes

Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

Solderability

- Compatible with JESD22-B102, Pb-free process, 260C peak reflow temperature ([see soldering profile](#))

Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS Information](#)

[Other Technical Information](#)

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