ACT4533C

Wide Input Sensorless CC/CV Step-Down DC/DC Converter

FEATURES

- 40 V Input Voltage Surge
- 36 V Steady State Operation
- Up to 3.5 A output current
- Output Voltage up to 18 V
- 125 kHz Switching Frequency Eases EMI Design
- 91% Efficiency (V_{OUT} = 5 V@2.4 A at V_{IN} = 12 V)
- Stable with Low-ESR Ceramic Capacitors to Allow Low-Profile Designs
- Integrated Over Voltage Protection
- Excellent EMI Performance
- Patented ActiveCC Sensorless Constant Current Control Improves Efficiency and Lowers Cost.
- Resistor Programmable
  - Current Limit from 1.5 A to 4.0 A
  - Patented Cable Compensation from 0 to 0.25 Ω
- ±7.5% CC Accuracy
  - Compensation of Input /Output Voltage Change
  - Temperature Compensation
  - Independent of inductance and Inductor DCR
- 2% Feedback Voltage Accuracy
- Advanced Feature Set
  - Integrated Soft Start
  - Thermal Shutdown
  - Secondary Cycle-by-Cycle Current Limit
  - Protection Against Shorted I_{SET} Pin
- SOP-8EP Package

APPLICATIONS

- Car Charger/ Adaptor
- Rechargeable Portable Device
- CV/CC regulation DC/DC converter

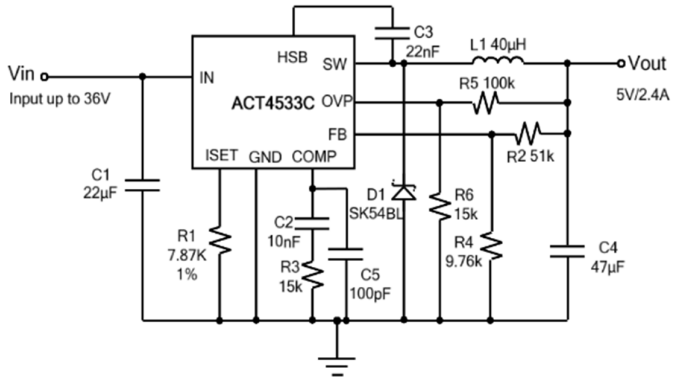
GENERAL DESCRIPTION

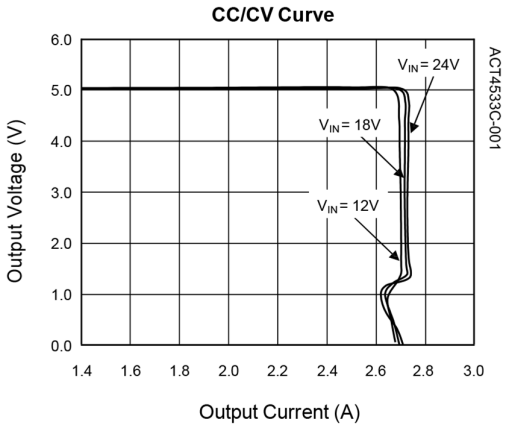
ACT4533C is a wide input voltage, high efficiency ActiveCC step-down DC/DC converter that operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode. ACT4533C provides up to 3.5 A output current at 125 kHz switching frequency.

ActiveCC is a patented control scheme to achieve high-accuracy sensorless constant current control. ActiveCC eliminates the expensive, high accuracy current sense resistor, making it ideal for CLA applications.

ACT4533C integrates adaptive gate drive to achieve excellent EMI performance passing EN55022 Class B EMC standard without adding additional EMI components while maintaining high conversion efficiency.

Protection features include cycle-by-cycle current limit, thermal shutdown, and frequency foldback at short circuit. The devices are available in a SOP-8EP package and require very few external devices for operation.

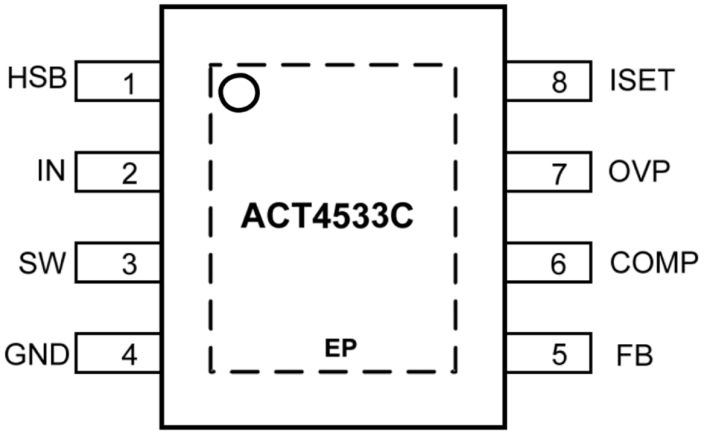




ORDERING INFORMATION

PART NUMBER	OPERATION AMBIENT TEMPERATURE RANGE	OVP/EN PIN	PACKAGE	PINS	PACKING
ACT4533CYH-T	-40 °C to 85 °C	OVP	SOP-8EP	8	TAPE & REEL

PIN CONFIGURATION



SOP-8EP

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	HSB	High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 22 nF capacitor from HSB pin to SW pin.
2	IN	Power Supply Input. Bypass this pin with a 10 µF ceramic capacitor to GND, placed as close to the IC as possible.
3	SW	Power Switching Output to External Inductor.
4	GND	Ground. Connect this pin to a large PCB copper area for best heat dissipation. Return FB, COMP, and ISET to this GND, and connect this GND to power GND at a single point for best noise immunity.
5	FB	Feedback Input. The voltage at this pin is regulated to 0.808 V. Connect to the resistor divider between output and GND to set the output voltage.
6	COMP	Error Amplifier Output. This pin is used to compensate the converter.
7	OVP	OVP input. If the voltage at this pin exceeds 0.8 V, the IC shuts down high - side switch.
8	ISET	Output Current Setting Pin. Connect a resistor from ISET to GND to program the output current.
	Exposed Pad	Heat Dissipation Pad. Connect this exposed pad to large ground copper area with copper and vias.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
IN to GND	-0.3 to 40	V
SW to GND	-1 to V_{IN} +1	V
HSB to GND	V_{SW} - 0.3 to V_{SW} +7	V
FB, I_{SET}, COMP, OVP to GND	-0.3 to +6	V
Junction to Ambient Thermal Resistance	46	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Junction Temperature	-55 to 150	°C
Lead Temperature (Soldering 10 sec.)	300	°C

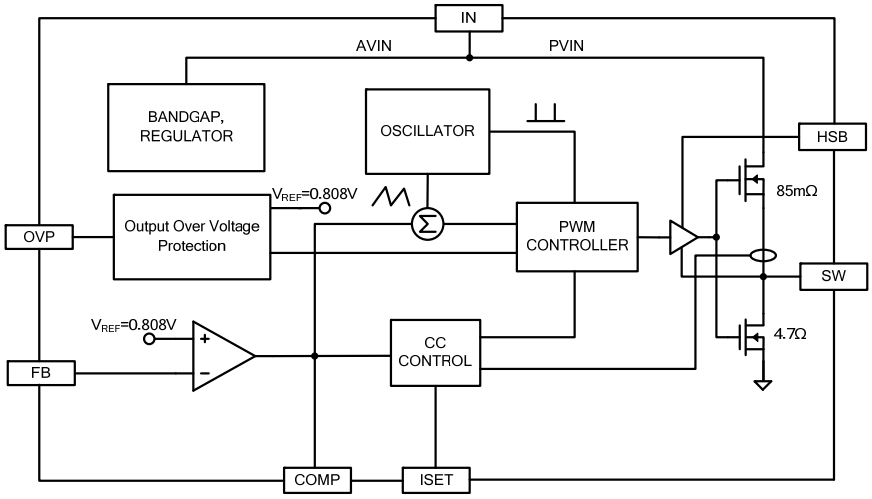
①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, T_A = 25 °C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage		10		38	V
Input Voltage Surge				40	V
V_{IN} UVLO Turn - On Voltage	Input Voltage Rising	9.0	9.4	9.7	V
V_{IN} UVLO Hysteresis	Input Voltage Falling		1.1		V
Standby Supply Current	V_{FB} = 1 V		0.9	1.4	mA
Feedback Voltage		792	808	824	mV
Internal Soft-Start Time			400		µs
Error Amplifier Transconductance	V_{FB} = V_{COMP} = 0.808 V, ΔI_{COMP} = ± 10 µA		650		µA/V
Error Amplifier DC Gain			4000		V/V
Switching Frequency	V_{FB} = 0.808 V		125		kHz
Foldback Switching Frequency	V_{FB} = 0 V		18		kHz
Maximum Duty Cycle			86		%
Minimum On - Time			290		ns
COMP to Current Limit Transconductance	V_{COMP} = 1.2 V		5.1		A/V
Secondary Cycle-by-Cycle Current Limit	Duty = 0.5		6.8		A
Slope Compensation	Duty = D_{MAX}		3.2		A
I_{SET} Voltage			1.0		V
I_{SET} to I_{OUT} DC Room Temp Current Gain	I_{OUT}/I_{SET}, R_{ISET} = 7.87 kΩ		20000		A/A
CC Controller DC Accuracy	R_{ISET} = 7.87 kΩ, V_{OUT} = 4.0 V		2650		mA
OVP Pin Voltage	OVP Pin Voltage Rising		0.8		V
OVP Pin Voltage	OVP Pin Voltage Falling		0.57		V
High - Side Switch ON - Resistance			85		mΩ
Thermal Shutdown Temperature	Temperature Rising		155		°C
Thermal Shutdown Temperature Hysteresis	Temperature Falling		25		°C

FUNCTIONAL BLOCK DIAGRAM FOR ACT4533C



FUNCTIONAL DESCRIPTION

CV/CC Loop Regulation

As seen in Functional Block Diagram, the ACT4533C is a peak current mode pulse width modulation (PWM) converter with CC and CV control. The converter operates as follows:

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off.

At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again. The High-Side Power Switch is driven by logic using HSB as the positive rail. This pin is charged to V_{SW} + 5 V when the Low-Side Power Switch turns on. The COMP voltage is the integration of the error between FB input and the internal 0.808 V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Output current will increase until it reaches the CC limit set by the I_{SET} resistor. At this point, the device will transition from regulating output voltage to regulating output current, and the output voltage will drop with increasing load.

The Oscillator normally switches at 125 kHz. However, if FB voltage is less than 0.6 V, then the switching frequency decreases until it reaches a typical value of 18 kHz at V_{FB} = 0.15 V.

Over Voltage Protection

The ACT4533C has an OVP pin. If the voltage at this pin exceeds 0.8 V, the IC shuts down high-side switch.

Thermal Shutdown

The ACT4533C disables switching when its junction temperature exceeds 155 °C and resumes when the temperature has dropped by 25 °C.

APPLICATIONS INFORMATION

Output Voltage Setting

Figure 1:

Output Voltage Setting

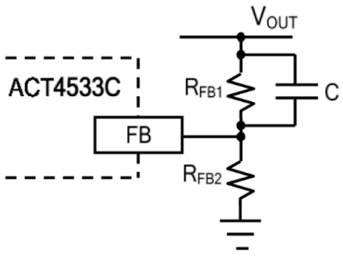


Figure 1 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors R_{FB1} and R_{FB2} based on the output voltage. Adding a capacitor in parallel with R_{FB1} helps the system stability. Typically, use $R_{FB2} \approx 10$ kΩ and determine R_{FB1} from the following equation:

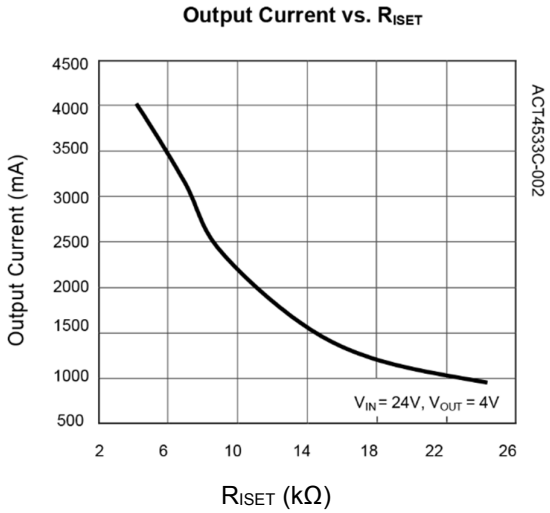
$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT}}{0.808V} - 1\right) \quad (1)$$

CC Current Setting

ACT4533C constant current value is set by a resistor connected between the I_{SET} pin and GND. The CC output current is linearly proportional to the current flowing out of the I_{SET} pin. The voltage at I_{SET} is roughly 1.1 V and the current gain from I_{SET} to output is roughly 21000 (21 mA/1 μA). To determine the proper resistor for a desired current, please refer to Figure 2 as below.

Figure 2:

Curve for Programming Output CC Current

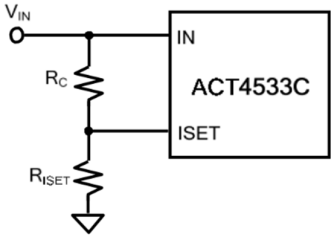


CC Current Line Compensation

When operating at constant current mode, the current limit increase slightly with input voltage. For wide input voltage applications, a resistor RC may be added to compensate line change and keep output high CC accuracy, as shown in Figure 3.

Figure 3:

Input Line Compensation



Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value:

Higher inductance reduces the peak-to-peak ripple current. The trade-off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}\, f_{SW}\, I_{LOADMAX}\, K_{RIPPLE}} \quad (2)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum load current.

With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK-PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}} \quad (3)$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK-PK} \quad (4)$$

The selected inductor should not saturate at I_{LPK}.

The maximum output current is calculated as:

$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK-PK} \quad (5)$$

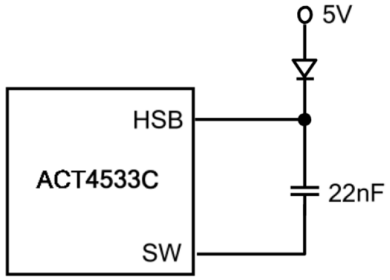
L_{LIM} is the internal current limit, which is typically 4.5 A, as shown in Electrical Characteristics Table.

External High Voltage Bias Diode

It is recommended that an external High Voltage Bias diode be added when the system has a 5 V fixed input or the power supply generates a 5 V output. This helps improve the efficiency of the regulator. The High Voltage Bias diode can be a low cost one such as IN4148 or BAT54.

Figure 4:

External High Voltage Bias Diode



This diode is also recommended for high duty cycle operation and high output voltage applications.

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10 µF. The best choice is the ceramic type, however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1 µF ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{LPK-PK} \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (6)$$

Where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

For ceramic output capacitor, typically choose a capacitance of about 22 µF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50 mΩ ESR.

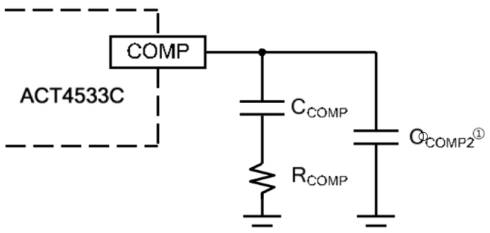
Rectifier Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage.

STABILITY COMPENSATION

Figure 5:

Stability Compensation



①: C_{COMP2} is needed only for high ESR output capacitor

The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in Figure 5. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.808V}{I_{OUT}} A_{VEA} G_{COMP} \quad (7)$$

The dominant pole P1 is due to C_{COMP}:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP}} \quad (8)$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}} \quad (9)$$

The first zero Z1 is due to R_{COMP} and C_{COMP}:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP}} \quad (10)$$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}} \quad (11)$$

The following steps should be used to compensate the IC:

STEP 1. Set the cross over frequency at 1/10 of the switching frequency via R_{COMP}:

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} \times 0.808V} = 5.12 \, x \, 10^7 V_{OUT} C_{OUT} \quad (\Omega) \quad (12)$$

STEP 2. Set the zero f_{Z1} at 1/4 of the cross over frequency. If R_{COMP} is less than 15 kΩ, the equation for C_{COMP} is:

$$C_{COMP} = \frac{2.83 \times 10^{-5}}{R_{COMP}} \quad (F) \quad (13)$$

If R_{COMP} is limited to 15 kΩ, then the actual cross over frequency is 6.58 / ($V_{OUT}C_{OUT}$). Therefore:

$$C_{COMP} = 6.45 \times 10^{-6} V_{OUT} C_{OUT} \quad (F) \quad (14)$$

STEP 3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the cross over frequency, an additional compensation capacitor C_{COMP2} is required. The condition for using C_{COMP2} is:

$$R_{ESRCOUT} \geq Min\left(\frac{1.77 \times 10^{-6}}{C_{OUT}}, 0.006 \times V_{OUT}\right) (\Omega) \quad (15)$$

And the proper value for C_{COMP2} is:

$$C_{COMP2} = \frac{C_{OUT} R_{ESRCOUT}}{R_{COMP}} \quad (16)$$

Though C_{COMP2} is unnecessary when the output capacitor has sufficiently low ESR, a small value C_{COMP2} such as 100 pF may improve stability against PCB layout parasitic effects.

Table 1 shows some calculated results based on the compensation method above.

Table 1:

Typical Compensation for Different Output Voltages and Output Capacitors

V_{OUT}	C_{OUT}	R_{COMP}	V_{COMP}	C_{COMP2}①
2.5 V	47 µF Ceramic CAP	5.6 kΩ	10 nF	None
3.3 V	47 µF Ceramic CAP	8.2 kΩ	10 nF	None
5 V	47 µF Ceramic CAP	15 kΩ	10 nF	None
2.5 V	220 µF/10 V/30 mΩ	15 kΩ	2.2 nF	47 pF
3.3 V	220 µF/10 V/30 mΩ	15 kΩ	2.2 nF	47 pF
5 V	220 µF/10 V/30 mΩ	15 kΩ	2.2 nF	47 pF

①: C_{COMP2} is needed for high ESR output capacitor. CCOMP2 ≤ 47 pF is recommended.

CC Loop Stability

The constant-current control loop is internally compensated over the 1500 mA - 3500 mA output range. No additional external compensation is required to stabilize the CC current.

Output Cable Resistance Compensation

To compensate for resistive voltage drop across the charger's output cable, the ACT4533C integrates a simple, user-programmable cable voltage drop compensation using the impedance at the FB pin.

Use the curve in Figure 6 to choose the proper feedback resistance values for cable compensation. R_{FB1} is the high side resistor of voltage divider.

In the case of high R_{FB1} used, the frequency compensation needs to be adjusted correspondingly. As show in Figure 7, adding a capacitor in paralleled with R_{FB1} or increasing the compensation capacitance at COMP pin helps the system stability

Figure 6:

Cable Compensation at Various Resistor Divider Values

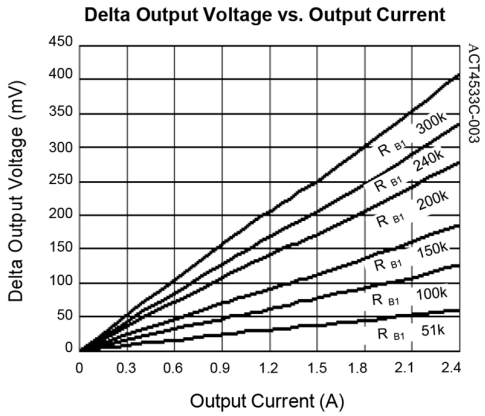
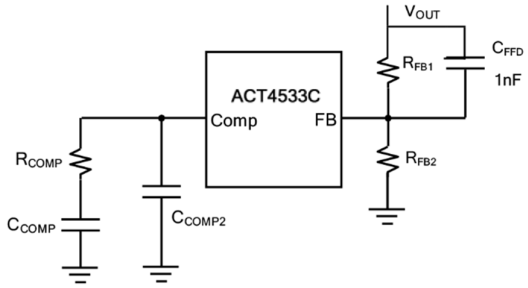


Figure 7:

Frequency Compensation for High R_{FB1}



PC Board Layout Guidance

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

1. Arrange the power components to reduce the AC loop size consisting of C_{IN}, IN pin, SW pin and the Schottky diode.
2. Place input decoupling ceramic capacitor C_{IN} as close to IN pin as possible. C_{IN} is connected power GND with vias or short and wide path.
3. Return FB, COMP and ISET to signal GND pin, and connect the signal GND to power GND at a single point for best noise immunity. Connect exposed pad to power ground copper area with copper and vias.
4. Use copper plane for power GND for best heat dissipation and noise immunity.
5. Place feedback resistor close to FB pin.
6. Use short trace connecting HSB-C_{HSB}-SW loop.

Figure 8 shows an example of PCB layout.

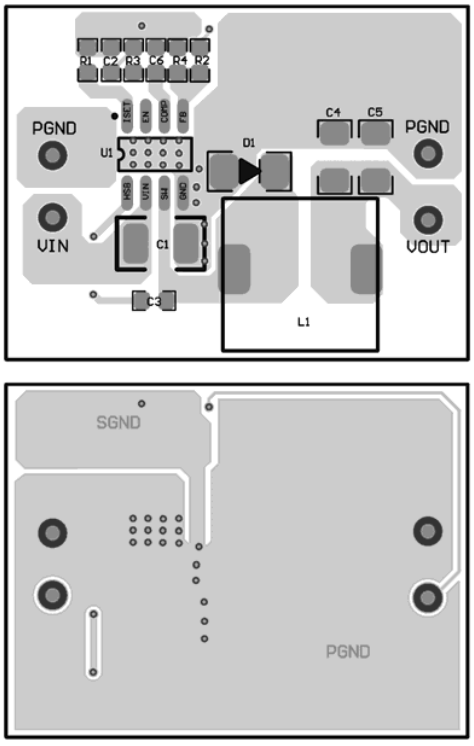


Figure 8: PCB Layout

Figure 9 gives one typical car charger application schematic and associated BOM list.

Figure 9:

Typical Application Circuit for 5 V/2.4 A Car Charger with OVP Circuit

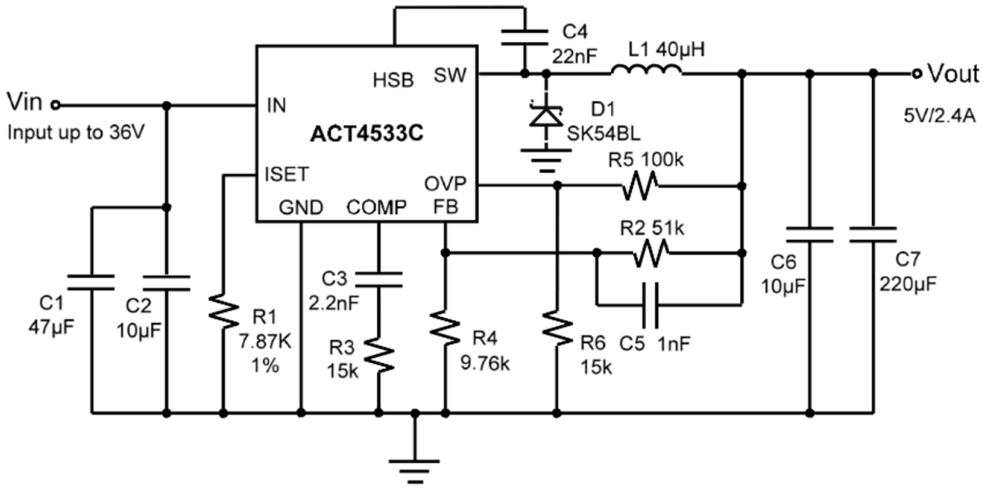


Table 2:

BOM List for 5 V/2.4 A Car Charger

ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1	IC, ACT4533CYH, SOP-8EP	Active-Semi	1
2	C1	Capacitor, Electrolytic, 47 μF/50 V, 6.3 x 7 mm	Murata, TDK	1
3	C2	Capacitor, Ceramic, 10 μF/50 V, 1206, SMD	Murata, TDK	1
4	C3	Capacitor, Ceramic, 2.2 nF/25 V, 0603, SMD	Murata, TDK	1
5	C4	Capacitor, Ceramic, 22 nF/50 V, 1206, SMD	Murata, TDK	1
6	C5	Capacitor, Ceramic, 1 nF/25 V, 0603, SMD	Murata, TDK	1
7	C6	Capacitor, Ceramic, 10 μF/10 V, 0603, SMD	Murata, TDK	1
8	C7	Capacitor, Electrolytic, 220 uF/10 V, 6.3 x 7 mm	Murata, TDK	1
9	L1	Inductor, 40 μH, 3.5 A, 20%, DIP	Sunlord	1
10	D1	Diode, Schottky, 40 V/5 A, SK54BL	Diodes	1
11	R1	Chip Resistor, 7.87 kΩ, 0603, 1%	Murata, TDK	1
12	R2	Chip Resistor, 51 kΩ, 0603, 1%	Murata, TDK	1
13	R3	Chip Resistor, 15 kΩ, 0603, 5%	Murata, TDK	1
14	R4	Chip Resistor, 9.76 kΩ, 0603, 1%	Murata, TDK	1
15	R5	Chip Resistor, 100 kΩ, 0603, 1%	Murata, TDK	1
16	R6	Chip Resistor, 15 kΩ, 0603, 1%	Murata, TDK	1

Figure 10:

Typical Application Circuit for 5 V/2.4 A Car Charger with OVP and Short Circuit Protection

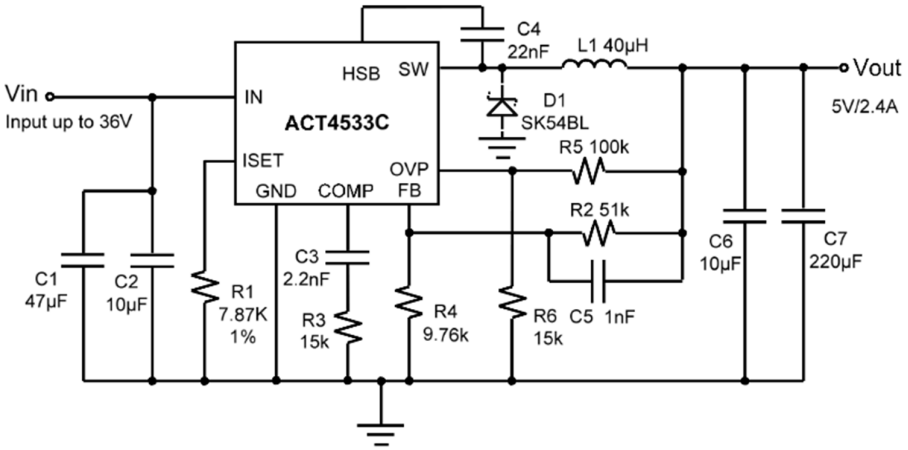


Table 3:

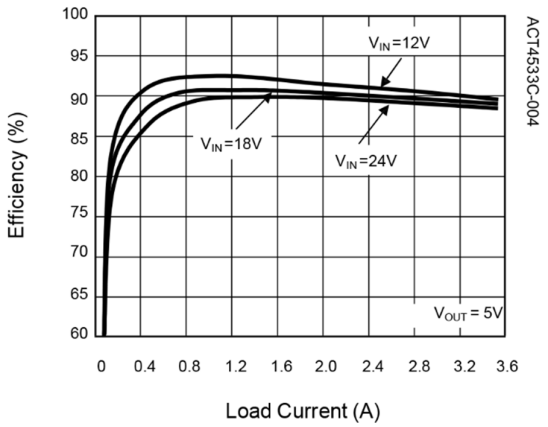
BOM List for 12 V/2.4 A Car Charger

ITEM	REFERENCE	DESCRIPTION	MANUFACTURER	QTY
1	U1	IC, ACT4533CYH, SOP-8EP	Active-Semi	1
2	C1	Capacitor, Electrolytic, 47 μF/50 V, 6.3 x 7 mm	Murata, TDK	1
3	C2	Capacitor, Ceramic, 10 μF/50 V, 1206, SMD	Murata, TDK	1
4	C3	Capacitor, Ceramic, 2.2 nF/25 V, 0603, SMD	Murata, TDK	1
5	C4	Capacitor, Ceramic, 22 nF/50 V, 1206, SMD	Murata, TDK	1
6	C5	Capacitor, Ceramic, 1 nF/25 V, 0603, SMD	Murata, TDK	1
7	C6	Capacitor, Ceramic, 10 μF/16 V, 0603, SMD	Murata, TDK	1
8	C7	Capacitor, Electrolytic, 220 uF/16 V, 6.3 x 7 mm	Murata, TDK	1
9	L1	Inductor, 66 μH, 3.5 A, 20%, DIP	Sunlord	1
10	D1	Diode, Schottky, 40 V/5 A, SK54BL	Diodes	1
11	R1	Chip Resistor, 7.87 kΩ, 0603, 1%	Murata, TDK	1
12	R2	Chip Resistor, 160 kΩ, 0603, 1%	Murata, TDK	1
13	R3	Chip Resistor, 15 kΩ, 0603, 5%	Murata, TDK	1
14	R4, R6	Chip Resistor, 11.5 kΩ, 0603, 1%	Murata, TDK	1
15	R5	Chip Resistor, 200 kΩ, 0603, 1%	Murata, TDK	1

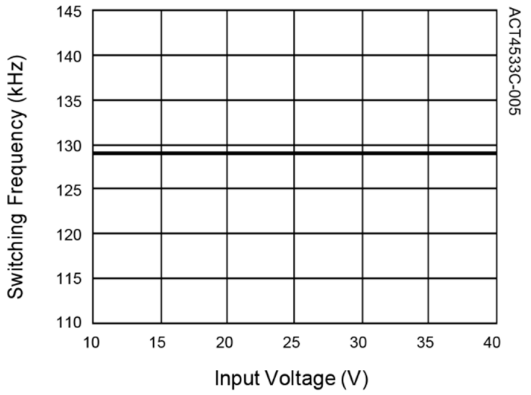
TYPICAL PERFORMANCE CHARACTERISTICS

(Schematic as show in Figure 9, T_a = 25 °C, unless otherwise specified)

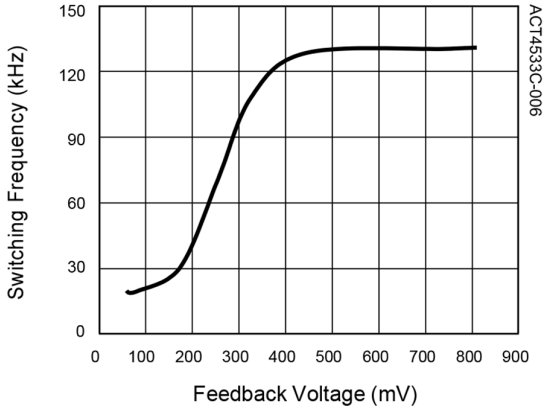
Efficiency vs. Load current



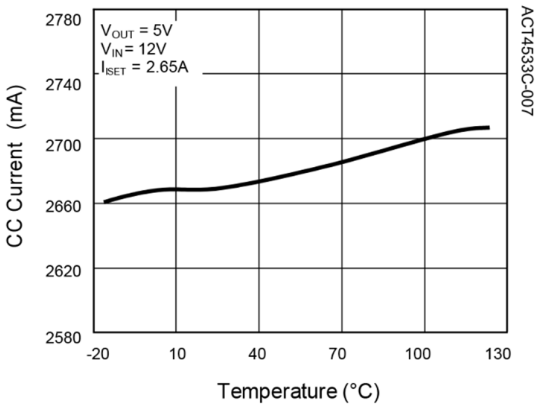
Switching Frequency vs. Input Voltage



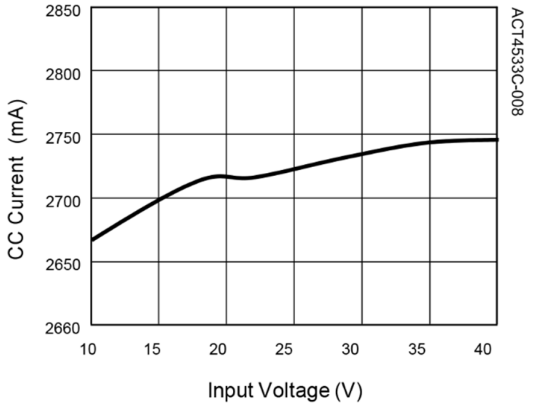
Switching Frequency vs. Feedback Voltage



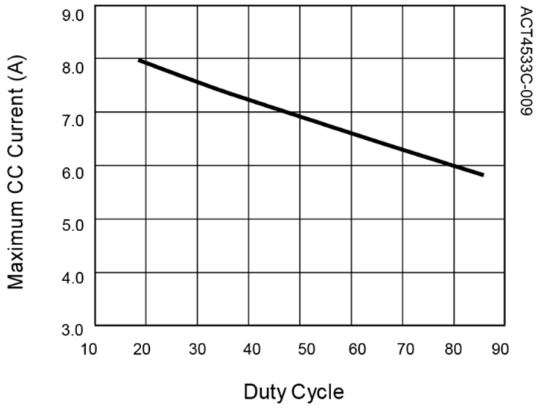
CC Current vs. Temperature



CC Current vs. Input Voltage



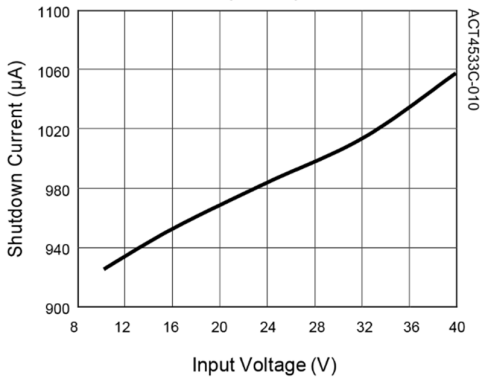
Maximum Peak Current vs. Duty Cycle



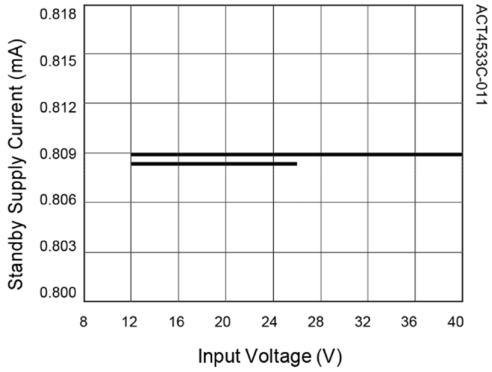
TYPICAL PERFORMANCE CHARACTERISTICS

(Schematic as show in Figure 9, T_a = 25 °C, unless otherwise specified)

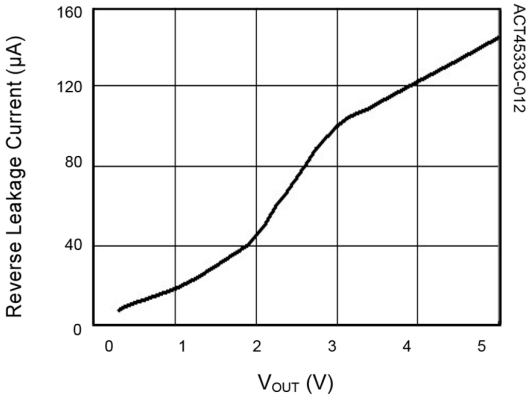
Standby Current vs. Input Voltage (FB=1V)



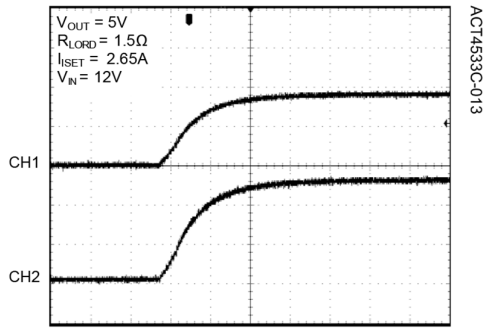
Feedback Voltage vs. Input Voltage



Reverse Leakage Current (V_{IN} Floating)

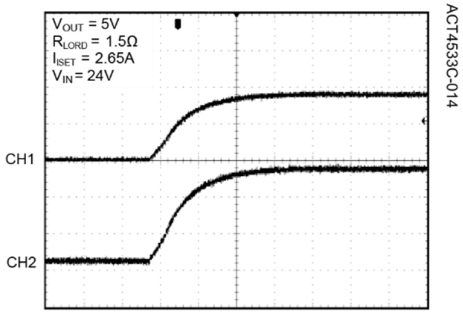


Start up into CC mode



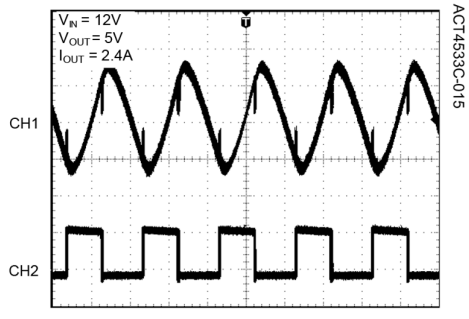
CH1: V_{OUT}, 2V/div
CH2: I_{OUT}, 1A/div
TIME: 400μs/div

Start up into CC mode



CH1: V_{OUT}, 2V/div
CH2: I_{OUT}, 1A/div
TIME: 400μs/div

SW vs. Output Voltage Ripples

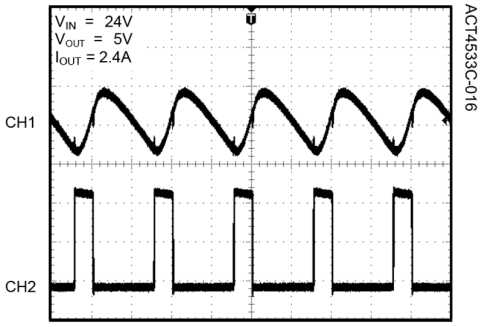


CH1: V_{OUT} Ripple, 20mV/div
CH2: SW, 10V/div
TIME: 4μs/div

TYPICAL PERFORMANCE CHARACTERISTICS

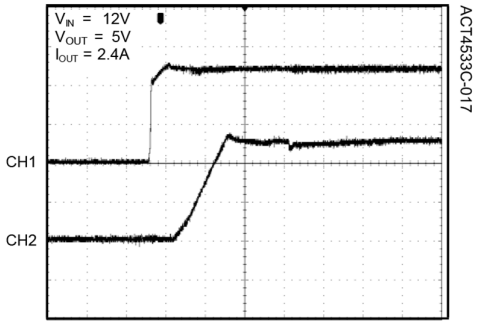
(Schematic as show in Figure 9, T_A = 25 °C, unless otherwise specified)

SW vs. Output Voltage Ripple



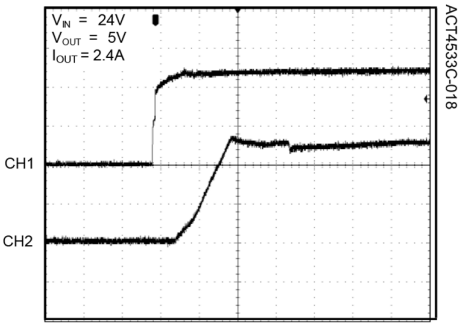
CH1: V_{RIPPLE}, 50mV/div
CH2: SW, 10V/div
TIME: 4μs/div

Start up with VIN



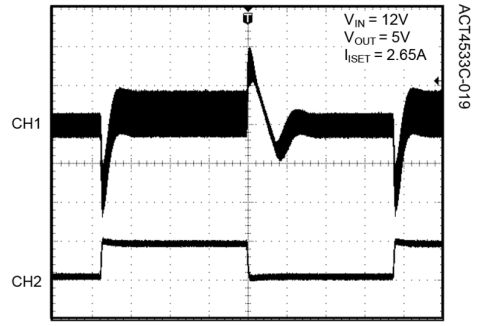
CH1: V_{IN}, 5V/div
CH2: V_{OUT}, 2V/div
TIME: 400μs//div

Start up with VIN



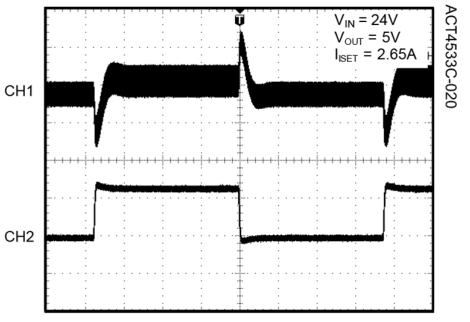
CH1: V_{IN}, 10V/div
CH2: V_{OUT}, 2V/div
TIME: 400μs//div

Load transient (80mA-1A-80mA)



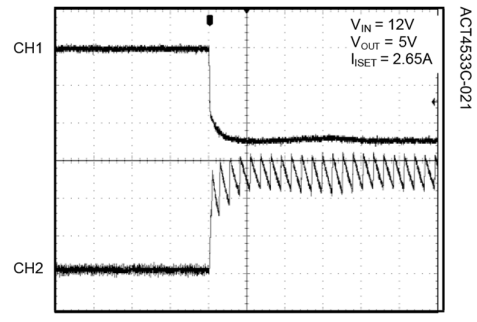
CH1: V_{OUT}, 50mV/div
CH2: I_{OUT}, 1A/div
TIME: 400μs//div

Load transient (1A-2.4A-1A)



CH1: V_{OUT}, 100mV/div
CH2: I_{OUT}, 1A/div
TIME: 400μs//div

Output Short test

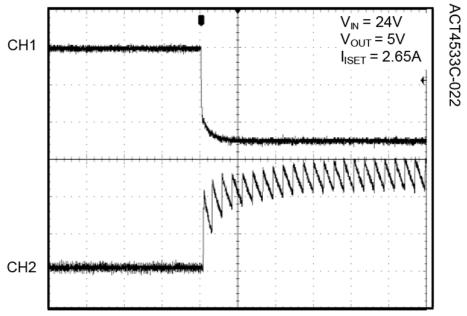


CH1: V_{OUT}, 2V/div
CH2: I_L, 1A/div
TIME: 100μs//div

TYPICAL PERFORMANCE CHARACTERISTICS

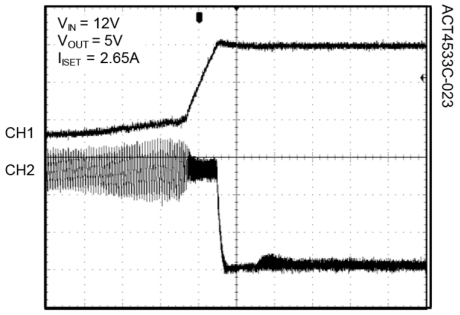
(Schematic as show in Figure 9, T_A = 25 °C, unless otherwise specified)

Output Short test



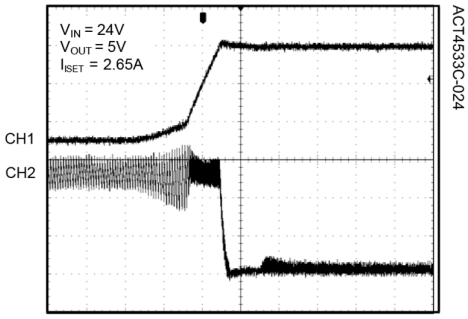
CH1: V_{OUT}, 2V/div
CH2: I_L, 1A/div
TIME: 100μs//div

Output Short Recovery



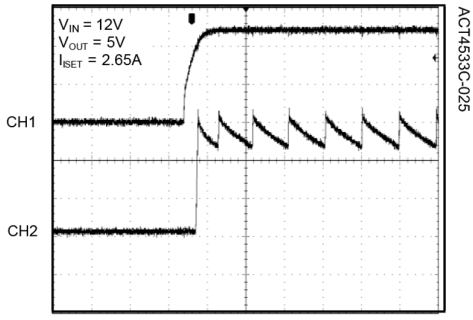
CH1: V_{OUT}, 2V/div
CH2: I_L, 1A/div
TIME: 400μs//div

Output Short Recovery



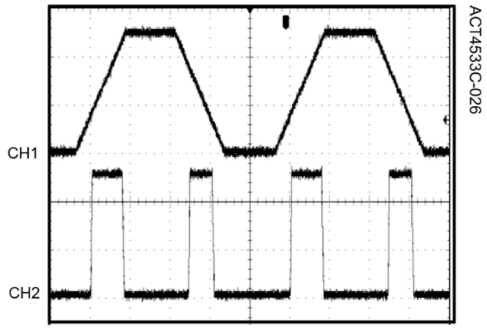
CH1: V_{OUT}, 2V/div
CH2: I_L, 1A/div
TIME: 400μs//div

OVP Test (Start up with FB=0)



CH1: V_{IN}, 5V/div
CH2: V_{OUT}, 2V/div
TIME: 10ms//div

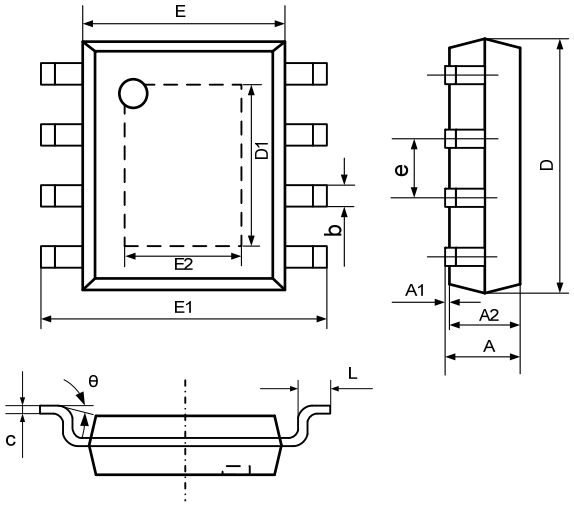
EN/OVP Test



CH1: $V_{EN/OVP}$, 1V/div
CH2: V_{OUT}, 2V/div
TIME: 20ms//div

PACKAGE OUTLINE

SOP-8EP PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.700	0.053	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Notes:

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end.
2. Dimension E does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.

Contact Information

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Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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