

## Applications

- Repeaters
- Mobile Infrastructure
- WiMAX / WiBro
- LTE / WCDMA / EDGE / CDMA

## Product Features

- 60 – 3500 MHz
- +25 dBm P1dB
- +40 dBm Output IP3
- 16.9 dB Gain at 2140 MHz
- 115 mA current draw
- +5V Single Supply
- MTTF > 100 Years
- Lead-free/Green/RoHS-compliant SOT-89 Package

## Product Description

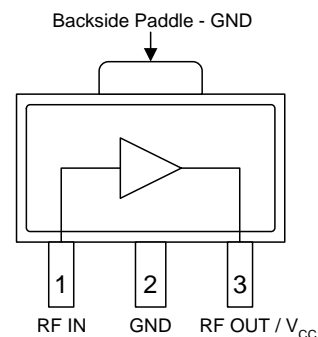
The AH128 is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve high performance across a broad range with +40 dBm OIP3 and +25 dBm of compressed 1dB power while drawing 115 mA current. The AH128 is available in a lead-free/green/RoHS-compliant SOT-89 package. All devices are 100% RF and DC tested.

The AH128 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. Internal biasing allows the AH128 to maintain high linearity over temperature and operate directly off a single +5V supply. This combination makes the device an excellent candidate for transceiver line cards in current and next generation multi-carrier 3G base stations.



3 Pin SOT-89 Package

## Functional Block Diagram



## Pin Configuration

Pin No.	Label
1	RF IN
3	RF OUT / V <sub>CC</sub>
2	GND
Backside Paddle	GND

## Ordering Information

Part No.	Description
AH128-89G	¼ W High Linearity InGaP HBT Amplifier
Standard T/R size = 1000 pieces on a 7" reel	

### Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150°C
RF Input Power, CW, 50Ω, T=25°C	Input P <sub>10</sub> dB
Device Voltage	+6 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

### Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Case Temperature	-40		+85	°C
Device Voltage (V <sub>CC</sub> )	+3.0	+5.0	+5.25	V
T <sub>j</sub> for >10 <sup>6</sup> hours MTTF			+200	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

### Electrical Specifications

Test conditions unless otherwise noted: V<sub>SUPPLY</sub>=+5 V, I<sub>CQ</sub>=115 mA (typ.), Temp= +25°C, tuned application circuit

Parameter	Conditions <sup>(1)</sup>	Min	Typ	Max	Units
Operational Frequency Range		60		3500	MHz
Test Frequency			2140		MHz
Gain		14.5	16.9	18	dB
Input Return Loss			15		dB
Output Return Loss			11		dB
W-CDMA Channel Power <sup>(2)</sup>	-50 dBc ACLR		+15		dBm
Output P1dB			+25		dBm
Output IP3	P <sub>out</sub> =+10 dBm / tone, Δf=1 MHz	+36	+40		dBm
Noise Figure			4.6		dB
Quiescent Collector Current		95	115	130	mA
Thermal Resistance, θ <sub>jc</sub>	Junction to case			116	°C/W

### Typical Performance

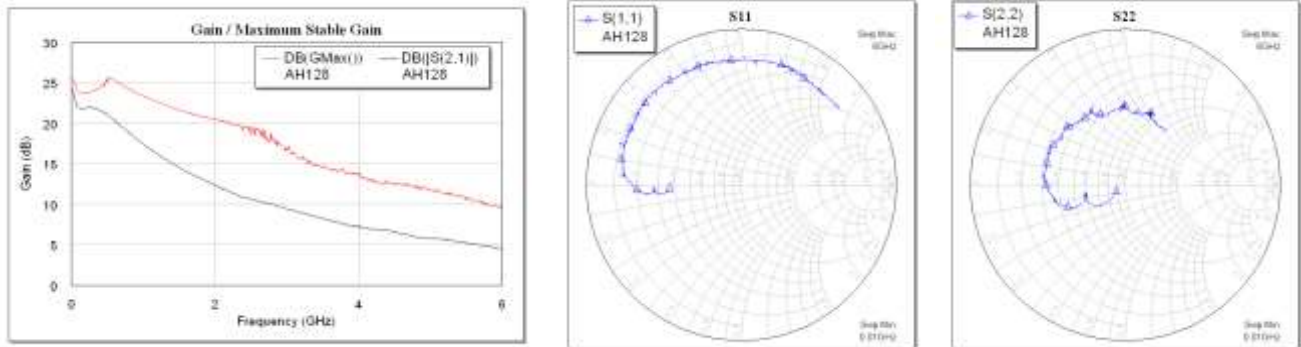
Test conditions unless otherwise noted: V<sub>SUPPLY</sub>=+5 V, I<sub>CQ</sub>=150 mA (typ.), Temp= +25°C, tuned application circuit

Parameter	Conditions <sup>(1)</sup>	Typical			Units
Frequency		920	1960	2140	MHz
Gain		19.7	17.6	16.9	dB
Input Return Loss		12	15	15	dB
Output Return Loss		8.2	11	11	dB
W-CDMA Channel Power	-50 dBc ACLR, Note 2	+15	+15.5	+15	dBm
Output P1dB		+24.7	+25.5	+25	dBm
Output IP3	Δf=1 MHz, Note 3	+40	+40	+40	dBm
Noise Figure		4.6	4.6	4.6	dB

Notes:

1. Test conditions unless otherwise noted: V<sub>CC</sub>=+5 V, Temp=+25 °C, 50 Ω system.
2. W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.3 dB @ 0.01% Probability, 3.84 MHz BW
3. P<sub>OUT</sub> = +13 dBm/tone for 920 MHz, +11 dBm/tone for 1960 MHz and +10 dBm/tone for 2140 MHz.

Device Characterization Data



Note: The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the red line.

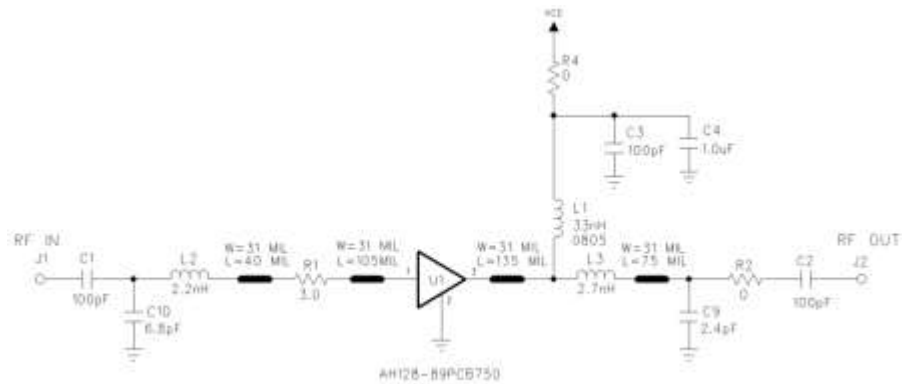
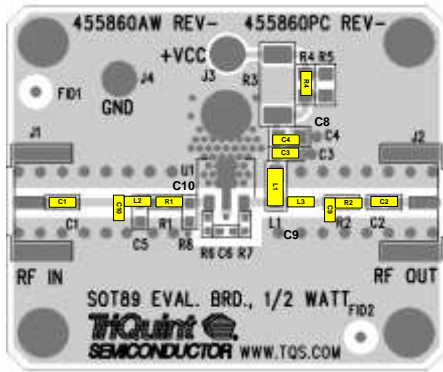
S-Parameters

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-5.38	-173.57	22.87	166.30	-30.49	4.94	-12.66	-146.31
100	-4.89	-176.21	21.96	165.00	-30.37	2.12	-11.24	-162.50
300	-4.91	-175.57	21.84	151.04	-30.66	-0.34	-11.69	-161.87
500	-3.95	-175.05	21.01	130.39	-30.54	1.26	-9.18	-156.72
700	-3.10	-179.25	19.51	114.04	-30.06	-1.57	-7.38	-162.95
900	-2.51	175.19	18.02	102.07	-29.47	-3.23	-6.59	-171.09
1100	-2.25	170.64	16.77	92.59	-29.27	-7.07	-6.09	-178.21
1300	-2.12	165.24	15.56	84.05	-29.04	-9.77	-5.69	175.48
1500	-2.01	160.47	14.47	76.48	-28.75	-12.83	-5.57	170.50
1700	-2.01	156.16	13.46	69.77	-28.78	-16.94	-5.59	165.41
1900	-1.92	150.48	12.74	63.07	-28.52	-20.19	-5.46	159.78
2100	-1.84	145.43	11.87	56.47	-28.43	-24.12	-5.36	154.06
2300	-1.76	141.16	11.08	50.21	-28.64	-26.71	-5.26	150.23
2500	-1.73	137.11	10.51	45.46	-28.47	-29.12	-5.54	146.96
2700	-1.69	131.81	10.11	39.00	-28.22	-33.92	-5.63	140.38
2900	-1.74	127.64	9.60	33.91	-27.96	-37.08	-5.41	135.33
3100	-1.83	121.13	9.17	27.49	-28.09	-40.84	-5.37	131.92
3300	-1.90	115.79	8.52	22.19	-28.02	-43.96	-5.63	129.40
3500	-1.90	112.40	8.12	16.48	-28.00	-46.34	-5.73	121.96

Notes:

1. Test Conditions:  $V_{CC} = +5\text{ V}$ ,  $I_{CQ} = 115\text{ mA}$ ,  $25\text{ }^\circ\text{C}$ , unmatched 50 ohm system, calibrated to device leads

700 – 800 MHz Reference Design



Typical O-FDMA Performance at 25 °C

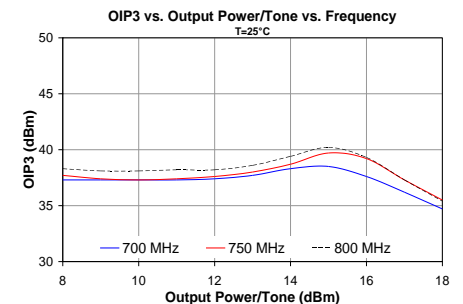
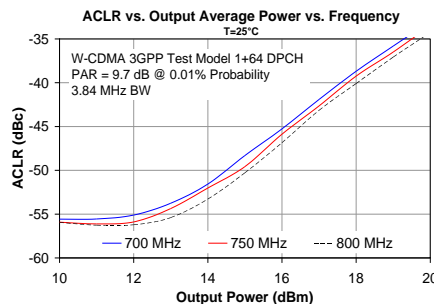
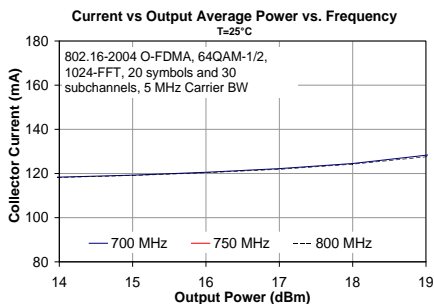
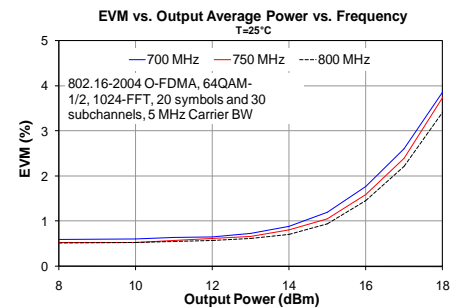
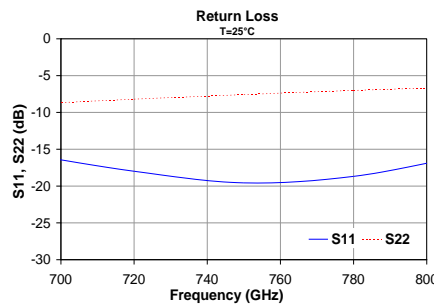
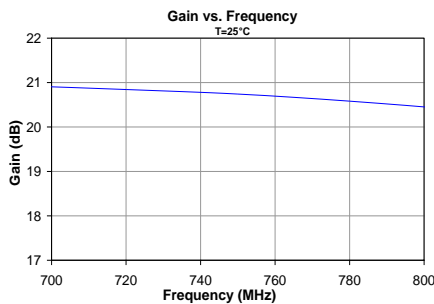
Frequency (MHz)	700	750	800	Units
Gain	20.9	20.7	20.4	dB
Input Return Loss	15.7	19.6	16	dB
Output Return Loss	8.9	7.6	6.6	dB
EVM (Pout=+16 dBm)	1.8	1.6	1.5	%
Output P1dB	+24.3	+24.4	+24.6	dBm
Output IP3 (Pout=+15 dBm/tone, Δf=1MHz)	+38.5	+39.7	+40.2	dBm

Notes:

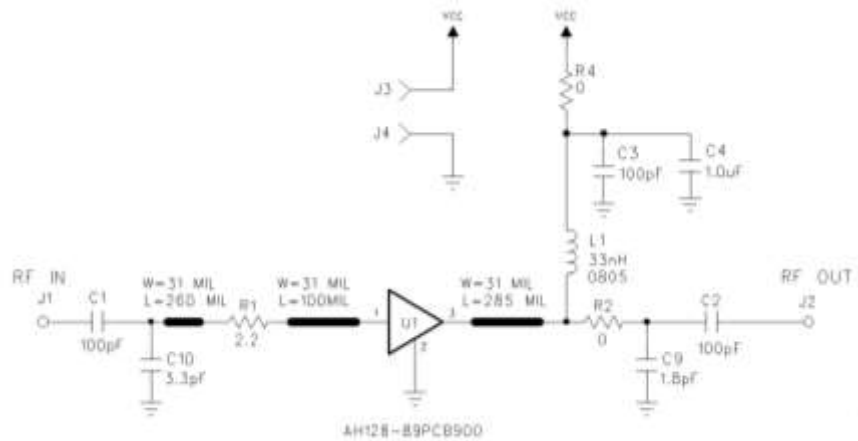
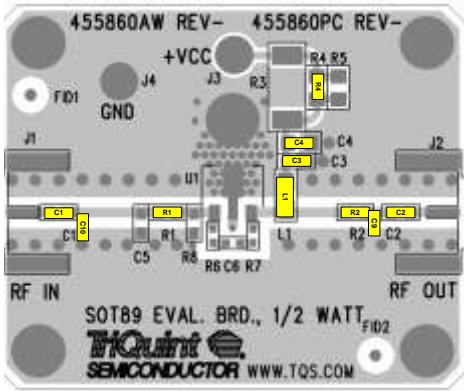
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of R1 is placed 105 mils from the AH128 RFin pin. (4.4° at 750 MHz)
5. The edge of L2 is placed 40 mils from the edge of R1. (1.7° at 750 MHz)
6. The edge of L3 is placed 135 mils from the AH128 RFout pin. (5.6° at 750 MHz)
7. The edge of C9 is placed 75 mils from the edge of L3. (3.1° at 750 MHz)

Performance Plots - 700 – 800 MHz Reference Design

Test conditions unless otherwise noted: V<sub>CC</sub>=+5 V, I<sub>CQ</sub> = 115 mA, Temp=+25 °C, 50 Ω system  
 02.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels, 5 MHz Carrier BW



869 – 960 MHz Reference Design



Typical W-CDMA Performance at 25 °C

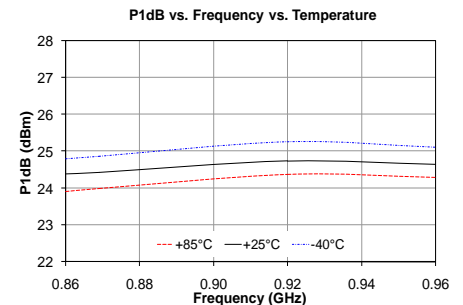
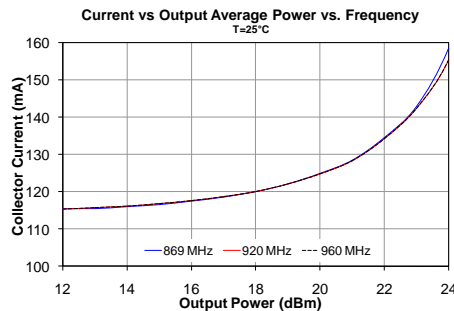
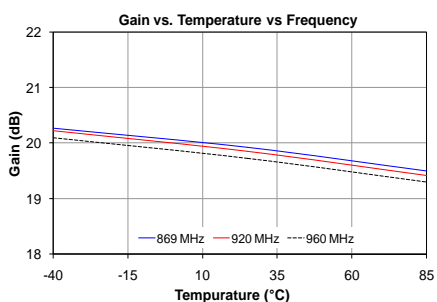
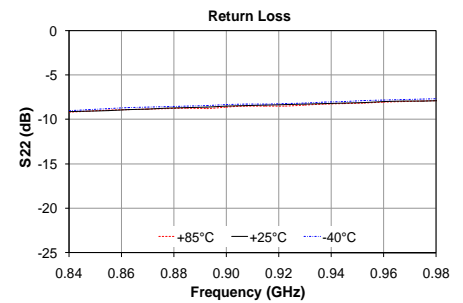
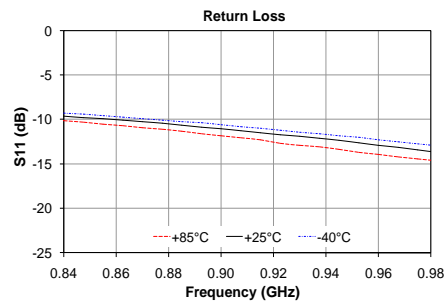
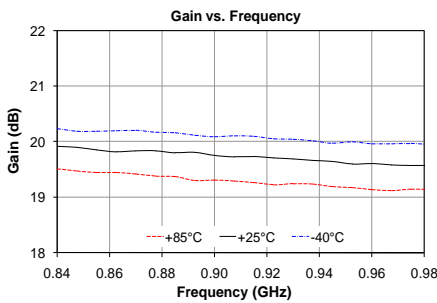
Frequency (MHz)	869	920	960	Units
Gain	19.8	19.7	19.6	dB
Input Return Loss	10	12	13	dB
Output Return Loss	8.8	8.2	7.9	dB
ACLR (Pout=+15 dBm)	-49	-50	-50	%
Output P1dB	+24.4	+24.7	+24.6	dBm
Output IP3 (Pout=+13 dBm/tone, Δf=1MHz)	+39	+40	+41	dBm
Noise Figure	4.7	4.6	4.6	dB

Notes:

1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of R2 is placed at 285 mils from AH128 RFout pin. (14° at 920 MHz)
5. The edge of C9 is placed against the edge of R2.
6. The edge of R1 is placed at 100 mils from AH128 RFin pin. (5° at 920 MHz)
7. The edge of C10 is placed 260 mils from the edge of R1. (13° at 920 MHz)

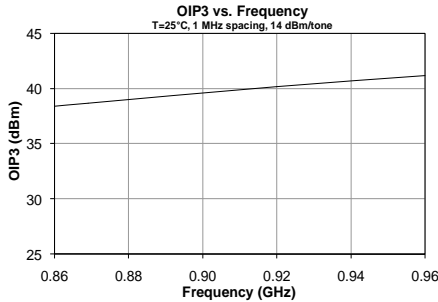
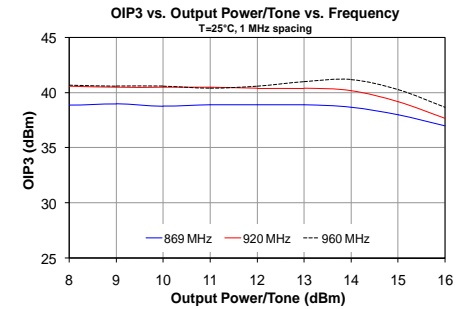
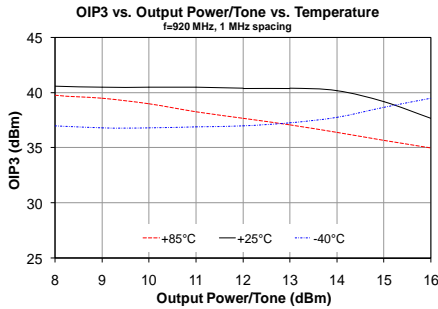
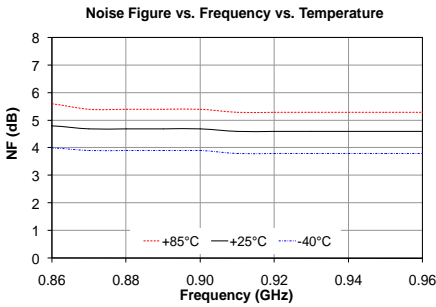
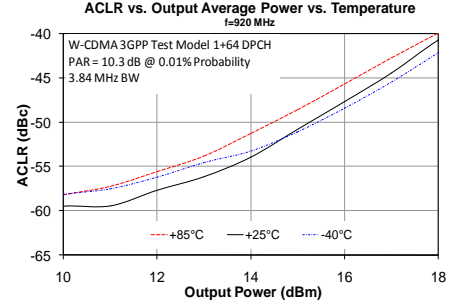
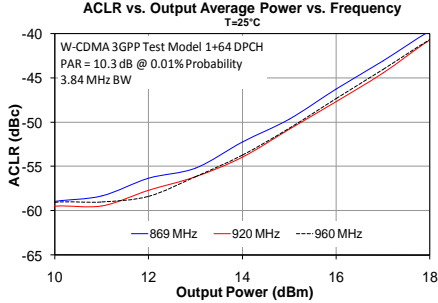
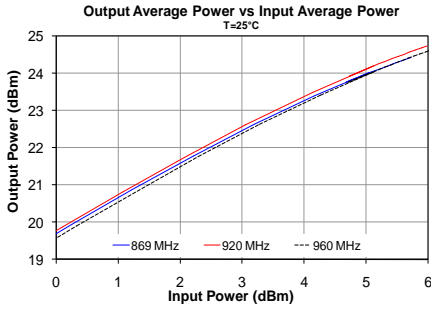
Performance Plots - 869 – 960 MHz Reference Design

Test conditions unless otherwise noted: V<sub>CC</sub>=+5 V, I<sub>CQ</sub> = 115 mA, Temp=+25 °C, 50 Ω system. W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.3 dB @ 0.01% Probability, 3.84 MHz BW

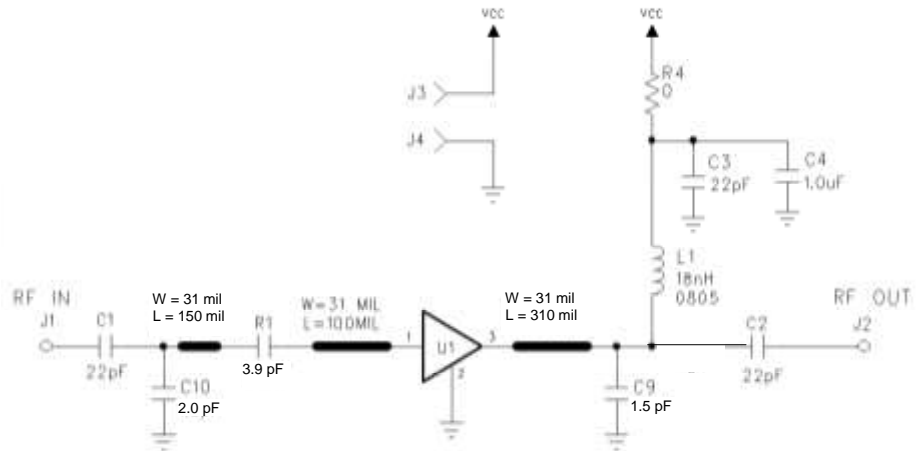
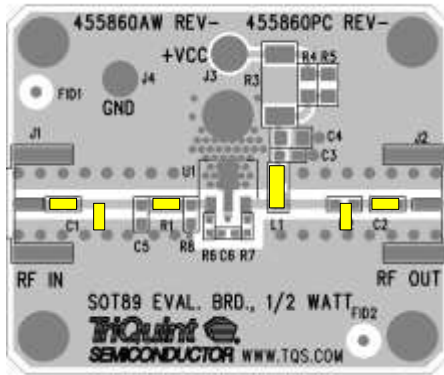


Performance Plots - 869 – 960 MHz Reference Design (cont'd)

Test conditions unless otherwise noted:  $V_{CC}=+5\text{ V}$ ,  $I_{CQ} = 115\text{ mA}$ ,  $Temp=+25\text{ }^{\circ}\text{C}$ ,  $50\ \Omega$  system



1805 – 1880 MHz Reference Design



Typical W-CDMA Performance at 25 °C

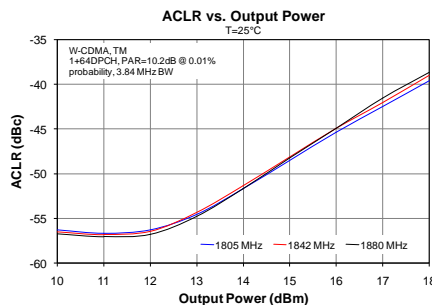
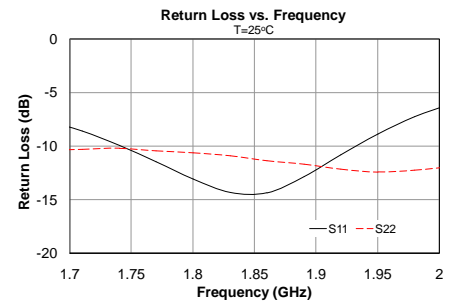
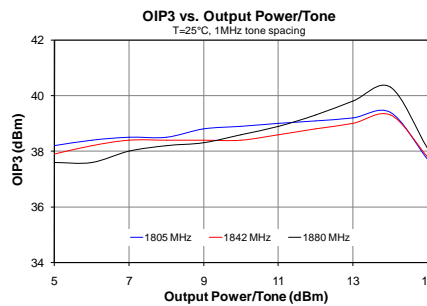
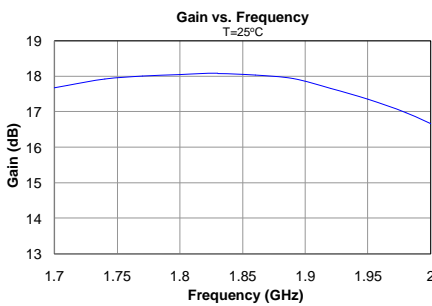
Frequency (MHz)	1805	1842	1880	Units
Gain	18.1	18.1	18.0	dB
Input Return Loss	13.3	14.5	13.5	dB
Output Return Loss	10.6	11.1	11.6	dB
ACLR (Pout=+15 dBm)	-48.5	-48.1	-48.2	%
Output P1dB	+24.7	+24.8	+24.7	dBm
Output IP3 (Pout=+13 dBm/tone, Δf=1MHz)	+39.2	+39.0	+39.8	dBm

Notes:

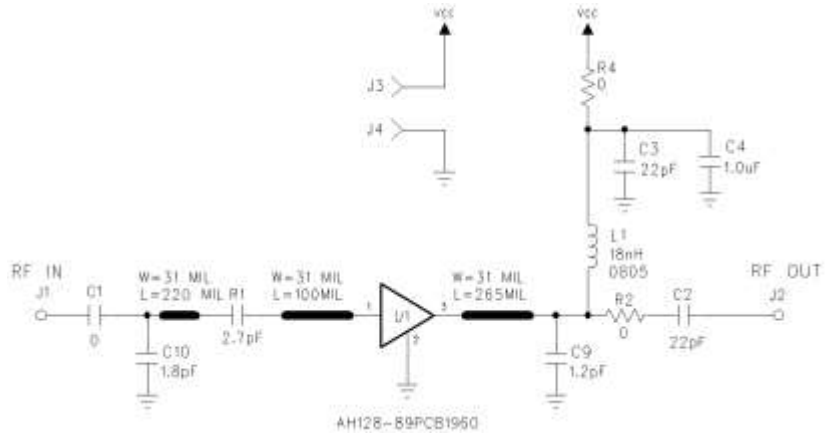
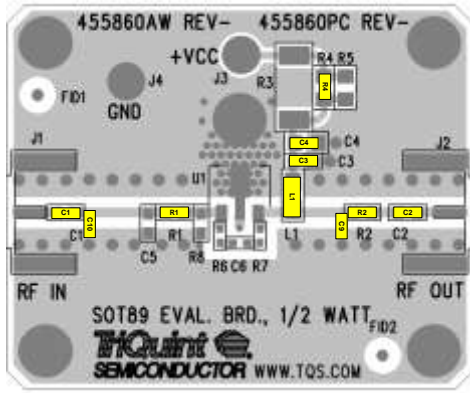
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of C9 is placed at 310 mils from AH128 RFout pin. (48.8° at 1842 MHz)
5. The edge of R1 is placed at 100 mils from AH128 RFIn pin. (15.7° at 1842 MHz)
6. The edge of C10 is placed 150 mils from the edge of R1. (23.6° at 1842 MHz)

Performance Plots - 1805 – 1880 MHz Reference Design

Test conditions unless otherwise noted: V<sub>CC</sub>=+5 V, I<sub>CQ</sub> = 115 mA, Temp=+25 °C, 50 Ω system W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.3 dB @ 0.01% Probability, 3.84 MHz BW



1930 – 1990 MHz Reference Design



Typical W-CDMA Performance at 25 °C

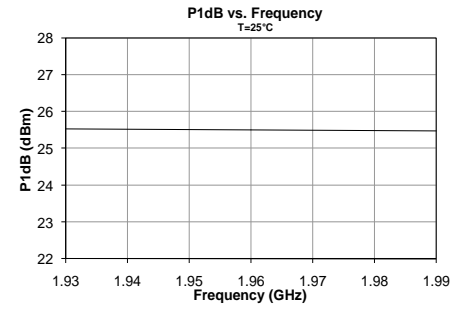
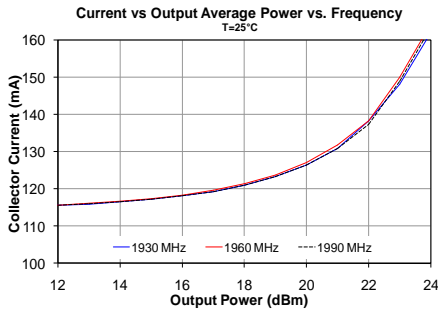
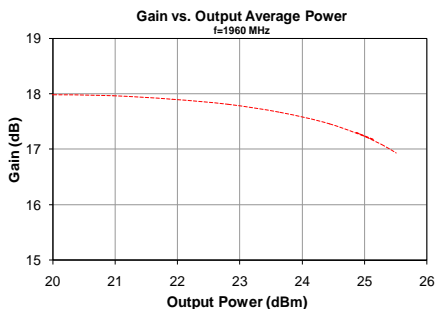
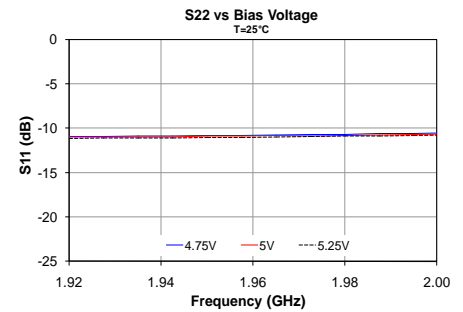
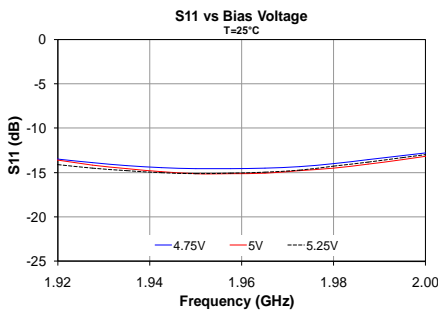
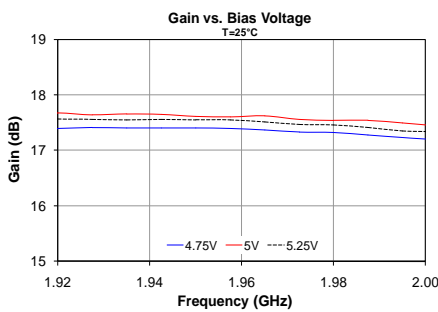
Frequency (MHz)	1930	1960	1990	Units
Gain	17.6	17.6	17.5	dB
Input Return Loss	14	15	14	dB
Output Return Loss	11	11	11	dB
ACLR (Pout=+15 dBm)	-50	-50	-50	%
Output P1dB	+25.5	+25.5	+25.5	dBm
Output IP3 (Pout=+11 dBm/tone, Δf=1MHz)	+39.5	+40	+40	dBm
Noise Figure	4.4	4.6	5.0	dB

Notes:

1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of C9 is placed at 265 mils from AH128 RFout pin. (29° at 1960 MHz)
5. The edge of R2 is placed against the edge of C9.
6. The edge of R1 is placed at 100 mils from AH128 RFin pin. (11° at 1960 MHz)
7. The edge of C10 is placed 220 mils from the edge of R1. (24° at 1960 MHz)

Performance Plots - 1930 – 1990 MHz Reference Design

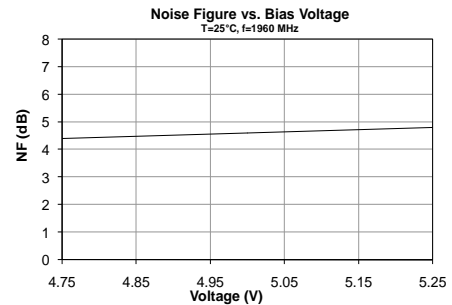
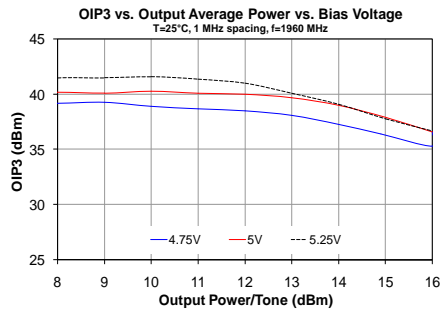
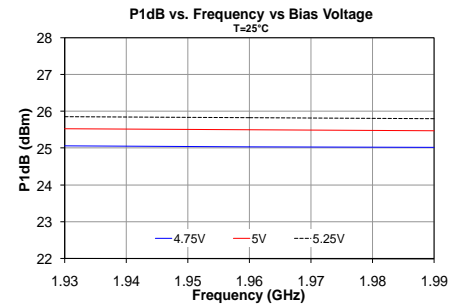
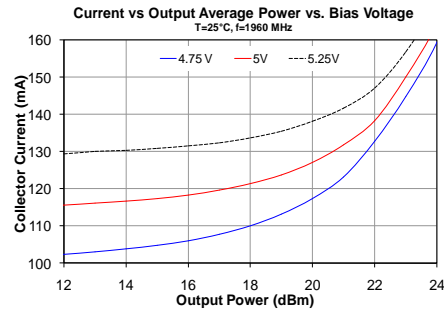
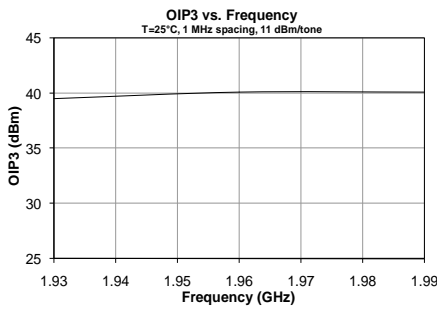
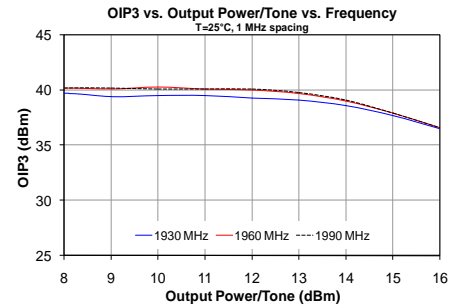
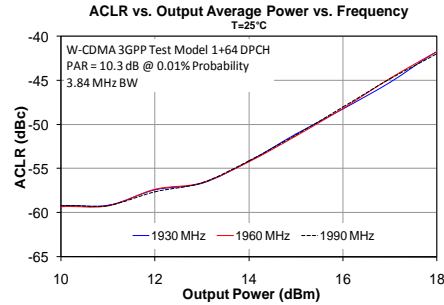
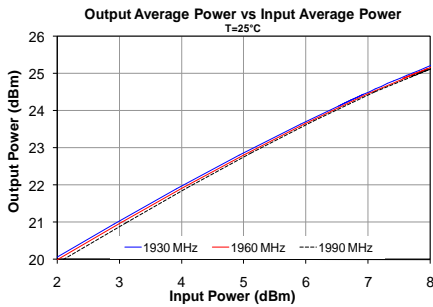
Test conditions unless otherwise noted: V<sub>CC</sub>=+5 V, I<sub>CQ</sub> = 115 mA, Temp=+25 °C, 50 Ω system  
 W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.3 dB @ 0.01% Probability, 3.84 MHz BW



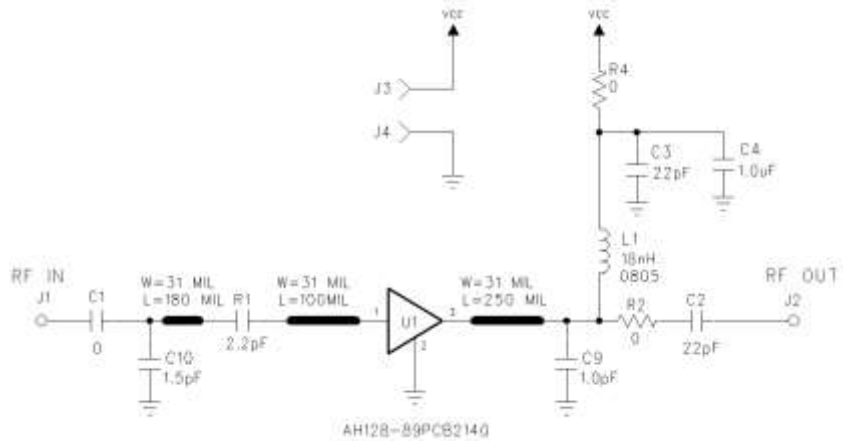
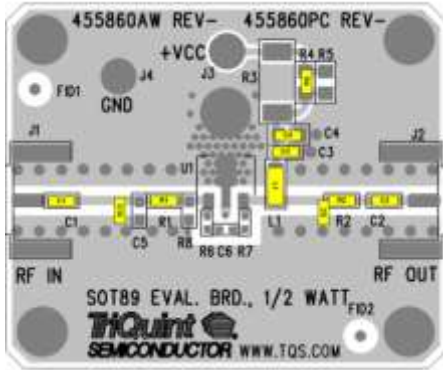


Performance Plots - 1930 – 1990 MHz Reference Design (cont'd)

Test conditions unless otherwise noted:  $V_{CC}=+5V$ ,  $I_{CQ} = 115\text{ mA}$ ,  $Temp=+25^\circ\text{C}$ ,  $50\ \Omega$  system



2110 – 2170 MHz Reference Design



Typical W-CDMA Performance at 25 °C

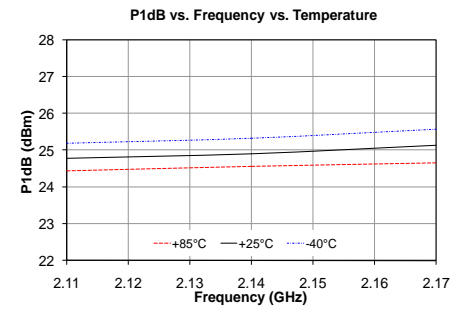
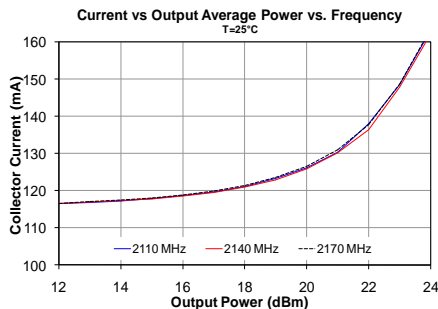
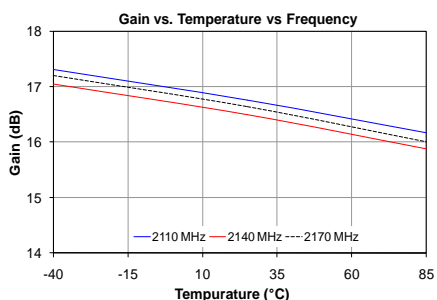
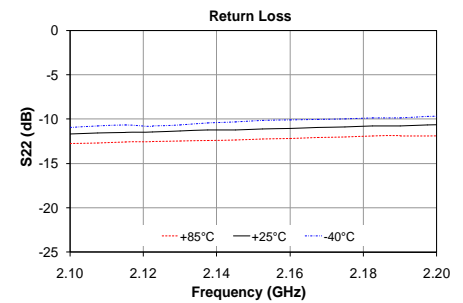
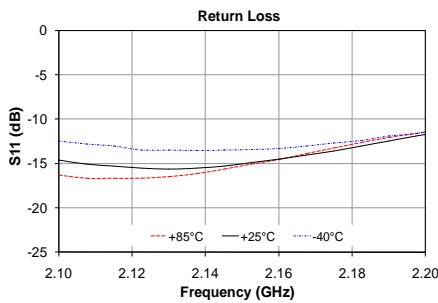
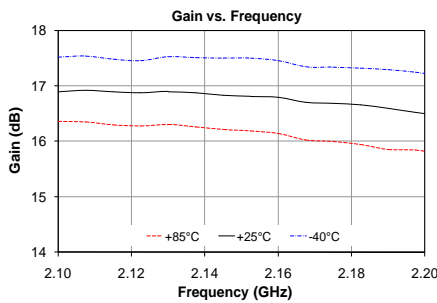
Frequency (MHz)	2110	2140	2170	Units
Gain	16.9	16.9	16.7	dB
Input Return Loss	15	15	14	dB
Output Return Loss	12	11	11	dB
ACLR (Pout=+15 dBm)	-49	-50	-49	%
Output P1dB	+24.8	+25	+25	dBm
Output IP3 (Pout=+10 dBm/tone, Δf=1MHz)	+40	+40	+39	dBm
Noise Figure	4.6	4.6	4.7	dB

Notes:

1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of C9 is placed at 250 mils from AH128 RFout pin. (29.6° at 2140 MHz)
5. The edge of R1 is placed at 100 mils from AH128 RFin pin. (12° at 2140 MHz)
6. The edge of C10 is placed 180 mils from the edge of R1. (21.3° at 2140 MHz)

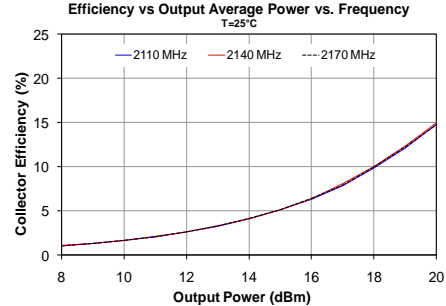
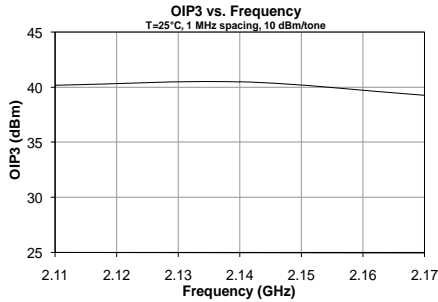
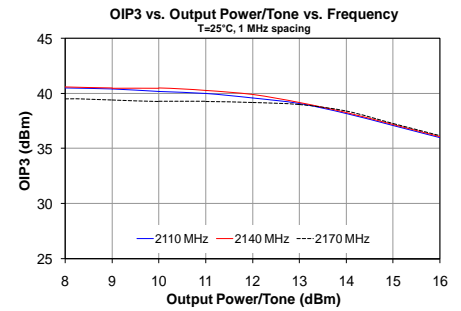
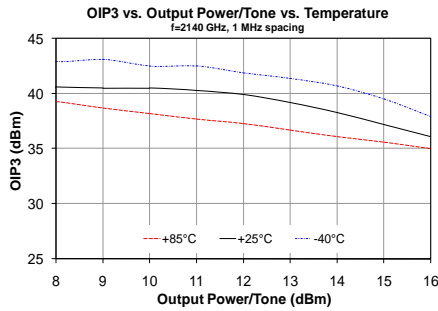
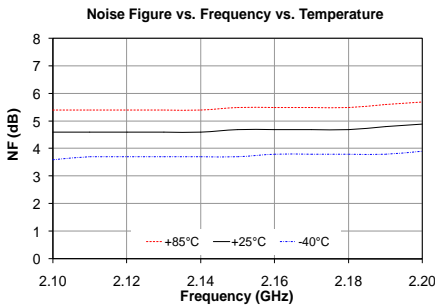
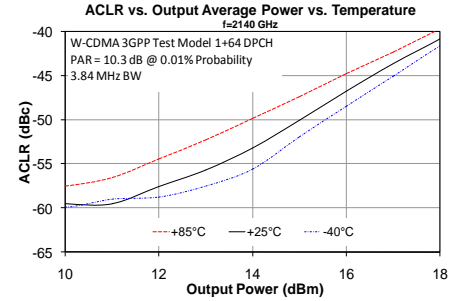
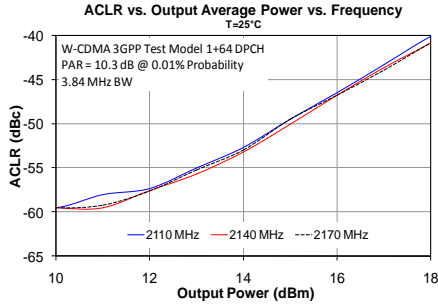
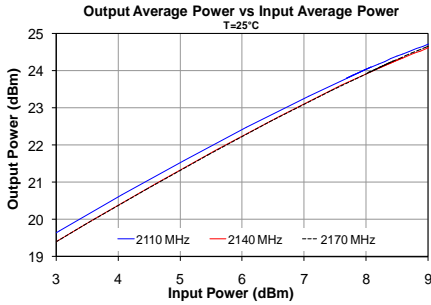
Performance Plots - 2110 – 2170 MHz Reference Design

Test conditions unless otherwise noted: V<sub>CC</sub>=+5 V, I<sub>CQ</sub> = 115 mA, Temp=+25 °C, 50 Ω system W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.3 dB @ 0.01% Probability, 3.84 MHz BW

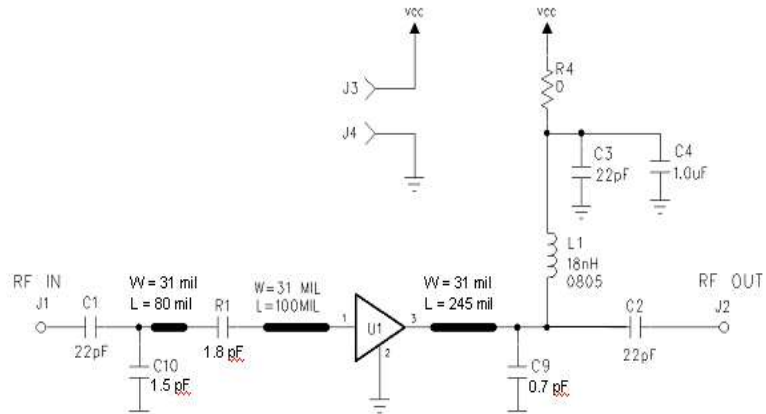
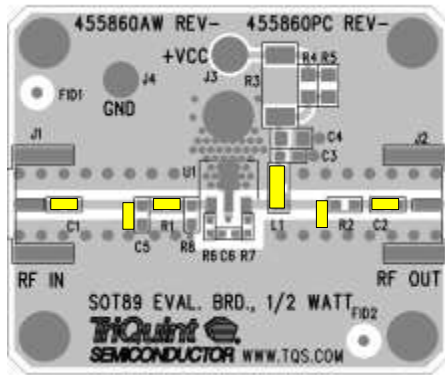


Performance Plots - 2110 – 2170 MHz Reference Design (cont'd)

Test conditions unless otherwise noted:  $V_{CC}=+5\text{ V}$ ,  $I_{CQ} = 115\text{ mA}$ ,  $T_{emp}=+25\text{ }^{\circ}\text{C}$ ,  $50\ \Omega$  system



2300 – 2400 MHz Reference Design



Typical O-FDMA Performance at 25 °C

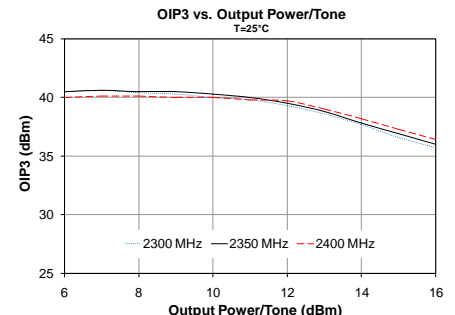
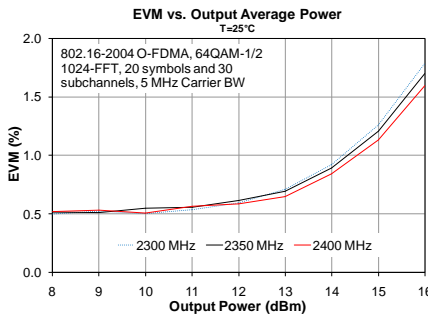
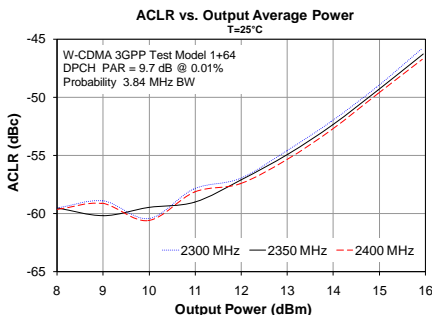
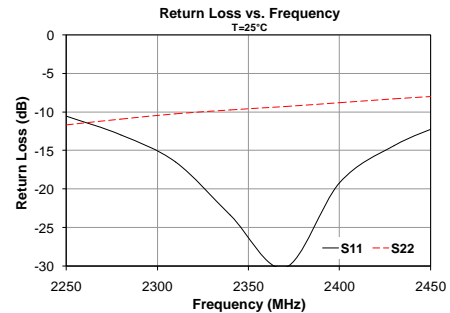
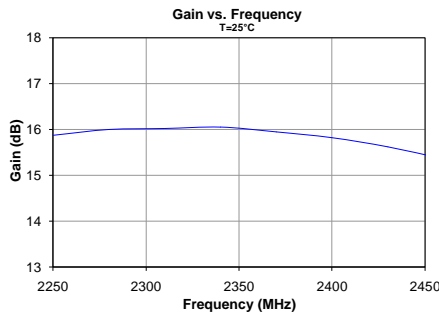
Frequency (MHz)	2300	2350	2400	Units
Gain	16.0	16.0	15.8	dB
Input Return Loss	15	27	19	dB
Output Return Loss	10.4	9.5	8.8	dB
ACLR (Pout=+15 dBm)	-49	-49.3	-49.5	%
EVM (Pout=+15 dBm)	1.26	1.2	1.13	
Output P1dB	+25	+25	+25	dBm
Output IP3 (Pout=+10 dBm/tone, Δf=1MHz)	+40.0	+40.3	+40.0	dBm

Notes:

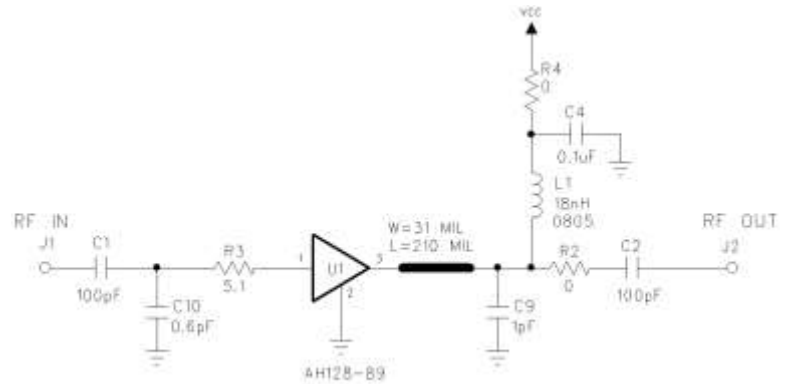
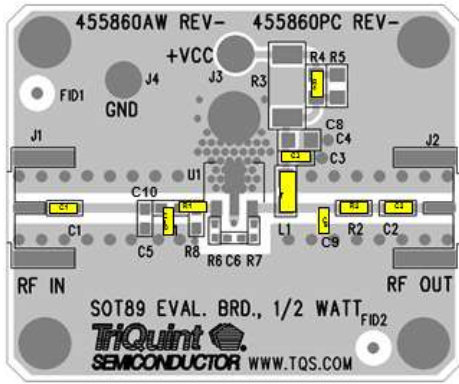
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of C9 is placed at 245 mils from AH128 RFout pin (31.9° at 2350 MHz).
5. The edge of R1 is placed at 100 mils from AH128 RFin pin (13.0° at 2350 MHz).
6. The edge of C10 is placed 80 mils from the edge of R1 (10.4° at 2350 MHz).

Performance Plots - 2300 – 2400 MHz Reference Design

Test conditions unless otherwise noted: V<sub>CC</sub>=+5 V, I<sub>CQ</sub> = 115 mA, Temp=+25 °C, 50 Ω system  
802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels, 5 MHz Carrier BW



1.8 – 2.7 GHz Reference Design



Typical Performance at 25 °C

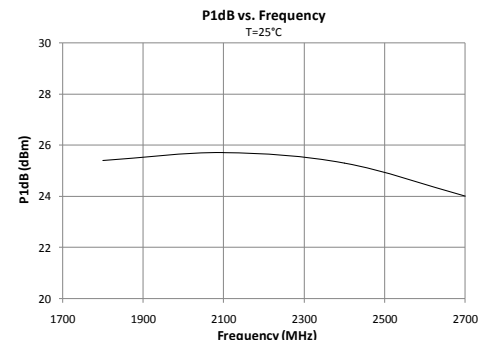
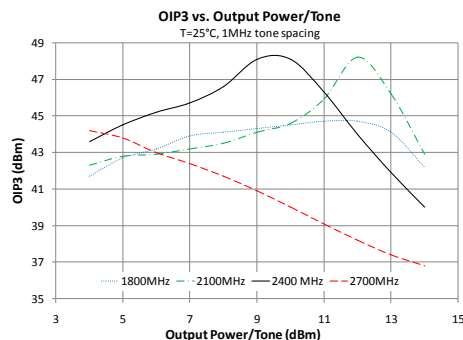
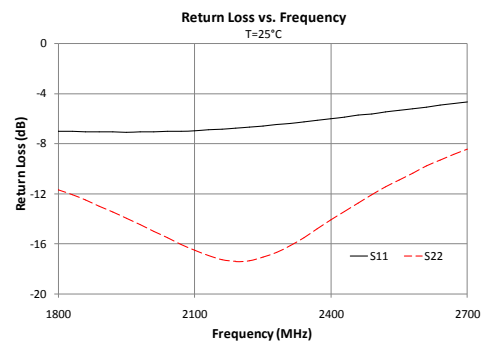
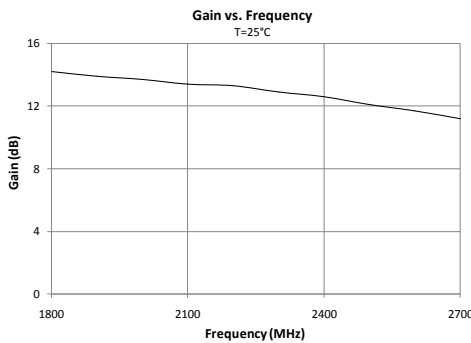
Frequency (GHz)	1.8	2.1	2.4	2.7	Units
Gain	14.2	13.4	12.6	11.2	dB
Input Return Loss	7.1	7.0	6.0	4.8	dB
Output Return Loss	11.7	16.5	14.1	8.9	dB
Output P1dB	+25.4	+25.7	+25.3	+24.0	dBm
Output IP3 (Pout=+11 dBm/tone, Δf=1MHz)	+45	+46	+46	+39	dBm

Notes:

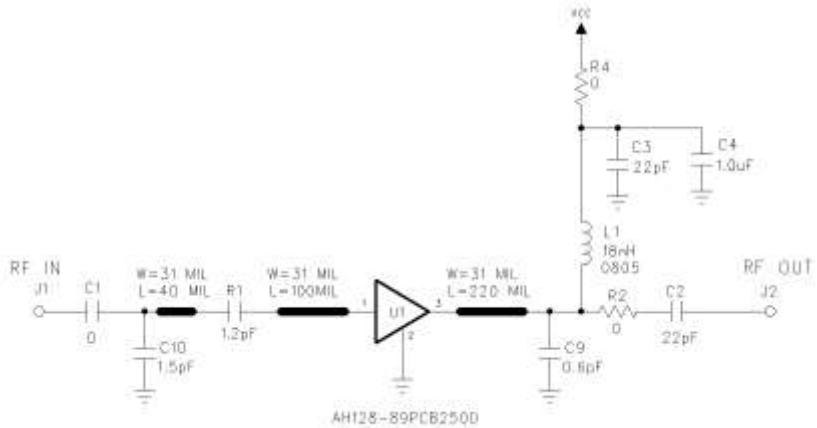
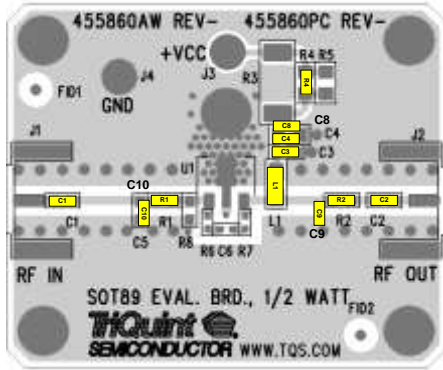
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The left edge of C9 is placed at 210 mils from AH128 RFout pin (27.9° at 2400 MHz).
5. The right edge of R3 is placed adjacent to the AH128 RFin pin.
6. The right edge of C10 is placed adjacent to the left edge of R3.

Performance Plots - 1.8 – 2.7 GHz Reference Design

Test conditions unless otherwise noted: V<sub>CC</sub>=+5 V, I<sub>CQ</sub> = 115 mA, Temp=+25 °C, 50 Ω system



2.5–2.7 GHz Reference Design



Typical O-FDMA Performance at 25 °C

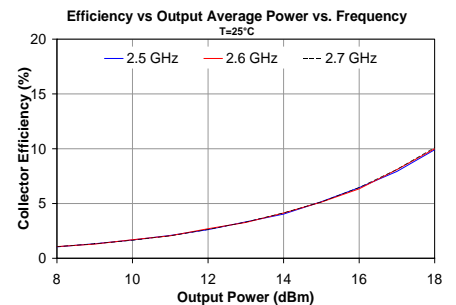
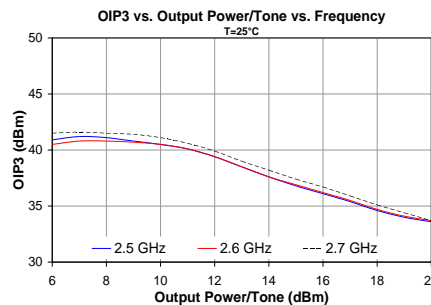
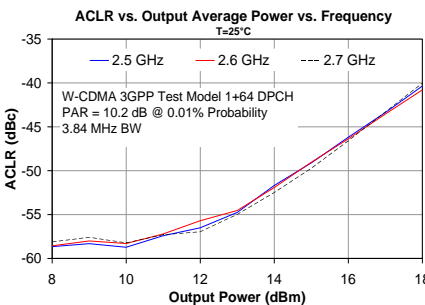
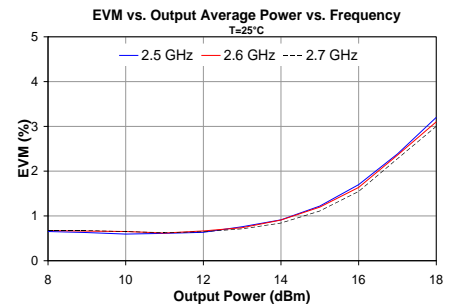
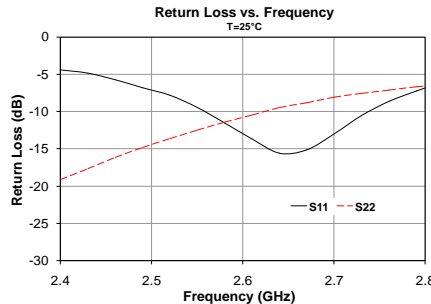
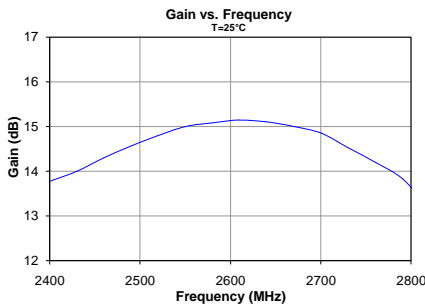
Frequency (GHz)	2.5	2.6	2.7	Units
Gain	14.7	15.1	14.9	dB
Input Return Loss	7.1	13	13	dB
Output Return Loss	15	10	8.1	dB
EVM (Pout=+17 dBm)	2.4	2.4	2.3	%
Output P1dB	+24.5	+24.8	+24.7	dBm
Output IP3 (Pout=+8 dBm/tone, Δf=1MHz)	+41.1	+40.8	+41.5	dBm

Notes:

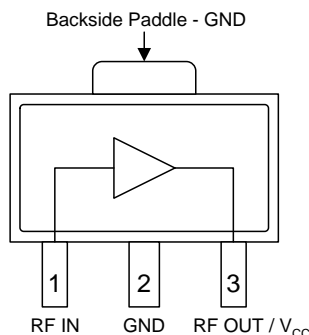
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. 0 Ω jumpers can be replaced with copper trace in target application.
4. The edge of C9 is placed at 230 mils from AH128 RFout pin. (32° at 2.5 GHz)
5. The edge of R1 is placed at 100 mils from AH128 RFin pin. (14° at 2.5 GHz)
6. The edge of C10 is placed 45 mils from the edge of R1. (6.2° at 2.5 GHz)

Performance Plots - 2.5–2.7 GHz Reference Design

Test conditions unless otherwise noted: V<sub>CC</sub>=+5 V, I<sub>CQ</sub> = 115 mA, Temp=+25 °C, 50 Ω system  
802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels, 5 MHz Carrier BW



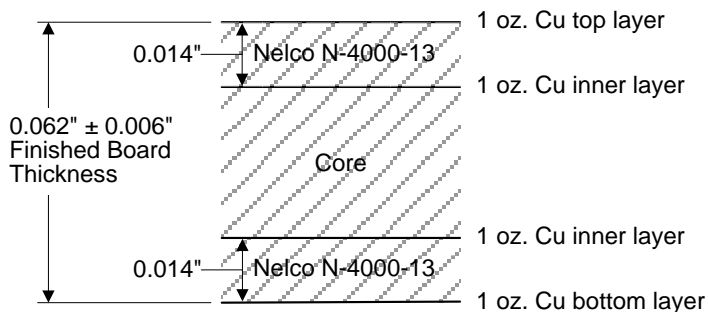
**Pin Configuration and Description**



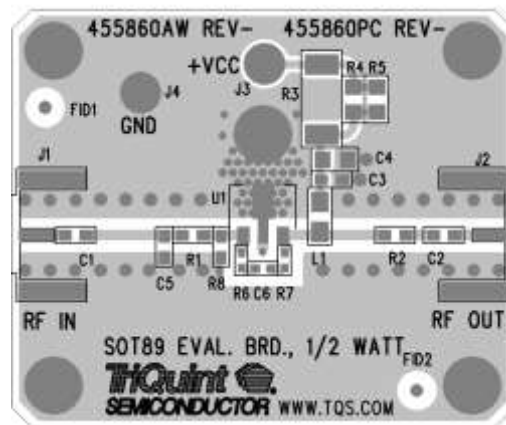
Pin No.	Label	Description
1	RF IN	RF Input. External DC Block required. Requires conjugate match for optimal performance.
2, Backside Paddle	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.
3	RF OUT / V <sub>CC</sub>	RF output, matched to 50 ohms. External DC Block and bias voltage required.

**Evaluation Board PCB Information**

TriQuint PCB 455860 Material and Stack-up

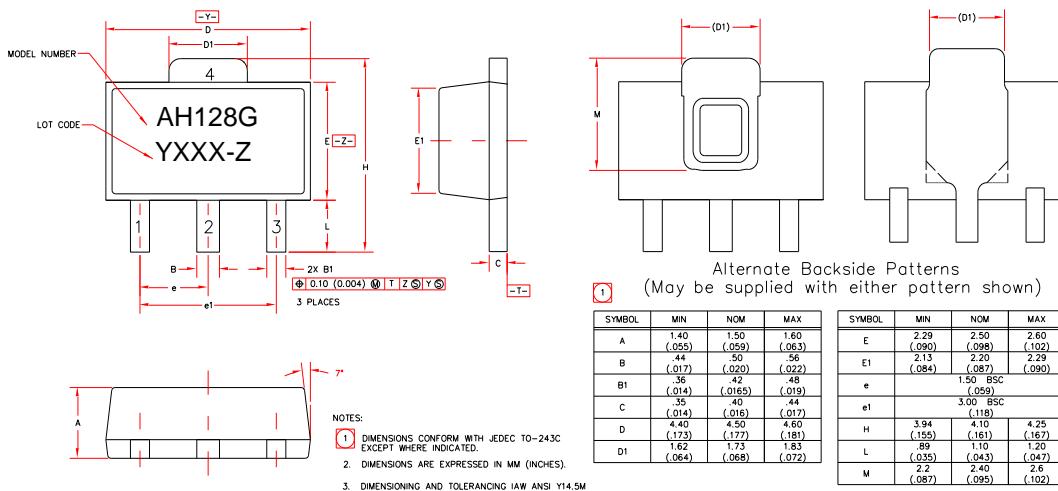


50 Ohm Lines: Width=28 mils  
Spacing=28 mils



**Package Marking and Dimensions**

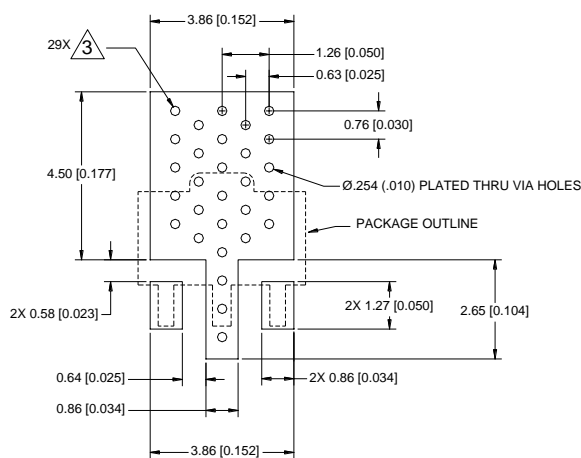
Marking: Part Identifier – AH128G  
Lot Code – YXXX-Z



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
4. Contact plating: NiPdAu

**PCB Mounting Pattern**



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation.
4. Do not remove or minimize via hole structure in the PCB. Thermal and RF grounding is critical.
5. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
6. Ensure good package backside solder attach for reliable operation and best electrical performance.



## Product Compliance Information

### ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: Class 2  
Value: /2000V to <4000V  
Test: Human Body Model (HBM)  
Standard: JEDEC Standard JS-001-2012

ESD Rating: Class C3  
Value: Passes  $\geq$  2000V min  
Test: Charged Device Model (CDM)  
Standard: JEDEC Standard JESD22-C101

### MSL Rating

MSL Rating: 3  
Test: +260°C convection reflow  
Standard: JEDEC standard IPC/JEDEC J-STD-020

### Solderability

Compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes.

Package lead plating: NiPdAu

### RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Web:** [www.triquint.com](http://www.triquint.com)

**Tel:** 877-800-8584

**Email:** [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

For information about the merger of RFMD and TriQuint as Qorvo:

**Web:** [www.qorvo.com](http://www.qorvo.com)

For technical questions and application information:

**Email:** [sjcappliations.engineering@qorvo.com](mailto:sjcappliations.engineering@qorvo.com)

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