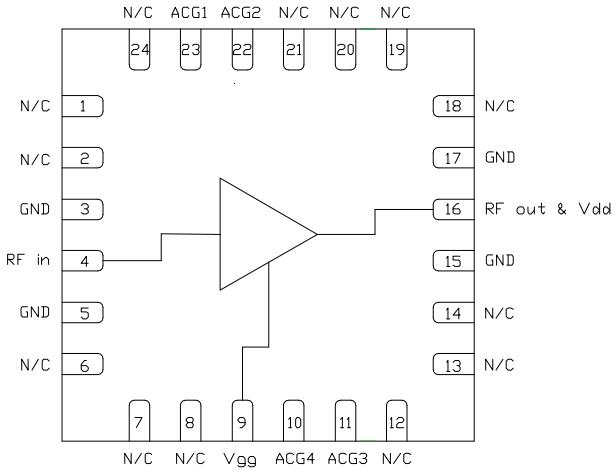
CMD275P4

DC-26.5 GHz Low Phase Noise Amplifier

Features

- Ultra wideband performance
- Low phase noise
- Low current consumption
- Pb-free RoHs compliant 4x4 mm QFN package

Functional Block Diagram



Description

The CMD275P4 is a wideband GaAs MMIC low phase noise amplifier housed in a leadless surface mount package that is ideally suited for military, space and communications systems. At 10 GHz the device delivers 16 dB of gain, a saturated output power of +20.5 dBm and a noise figure of 5.5 dB. Also with an input signal of 10 GHz the amplifier provides low phase noise performance of -165 dBc/Hz at 10 kHz offset. The CMD275P4 is a 50 ohm matched design which eliminates the need for RF port matching.

Electrical Performance – V_{dd} = 5.0 V, V_{gg} = 3.0 V, T_A = 25 °C, F = 10 GHz

Parameter	Min	Typ	Max	Units
Frequency Range		DC – 26.5		GHz
Gain		16		dB
Input Return Loss		18		dB
Output Return Loss		20		dB
Noise Figure		5.5		dB
Output P1dB		18		dBm
Saturated Output Power		20.5		dBm
Phase Noise @ 10 kHz Offset		-165		dBc/Hz
Supply Current		74		mA

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Specifications

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage, Vdd	7.5 V
Gate Voltage, Vgg	3.5 V
RF Input Power	+10 dBm
Channel Temperature, Tch	150 °C
Power Dissipation, Pdiss	495 mW
Thermal Resistance, Θ_{JC}	131 °C/W
Operating Temperature	-40 to 85 °C
Storage Temperature	-55 to 150 °C

Exceeding any one or combination of the maximum ratings may cause permanent damage to the device.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Vdd	4.0	5.0	7.0	V
Idd		74		mA
Vgg	0	3.0	3.3	V
Igg		3.7		mA

Electrical performance is measured at specific test conditions. Electrical specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications – V_{dd} = 5.0 V, V_{gg} = 3.0 V, T_A = 25 °C

Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Frequency Range	DC – 10			10 – 20			20 – 26			GHz
Gain	13	15.5		13	16		13	16.5		dB
Noise Figure		6			5			6		dB
Input Return Loss		13			15			10		dB
Output Return Loss		18			18			13		dB
Output P1dB	15.5	18.5		13	17		11	15		dBm
Saturated Output Power		21			19			17.5		dBm
Output IP3		29			28.5			25		dBm
Phase Noise @ 10 kHz Offset		-165			-165			-165		dBc/Hz
Supply Current	52	74	110	52	74	110	52	74	110	mA

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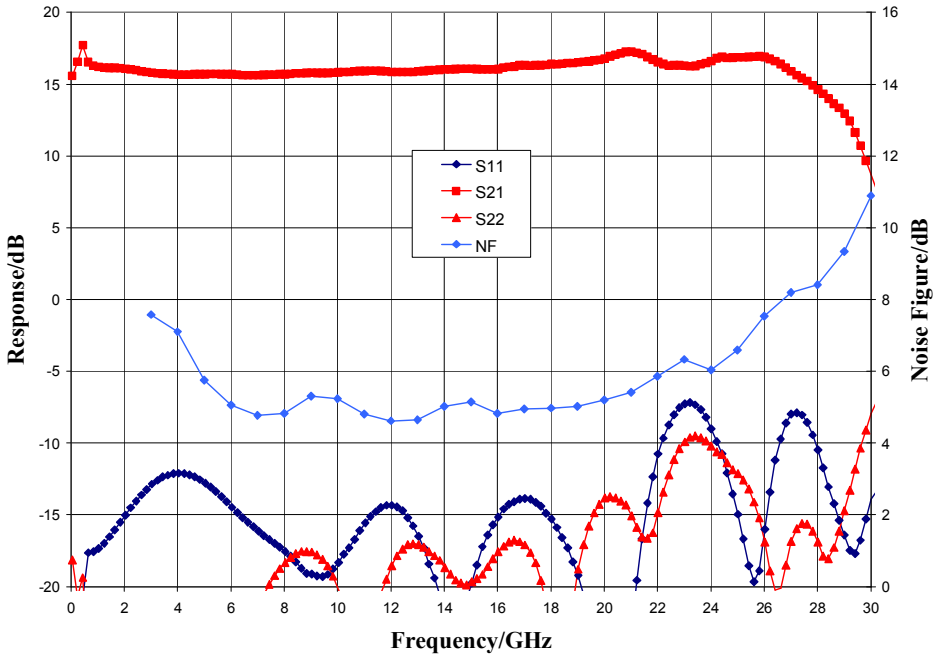
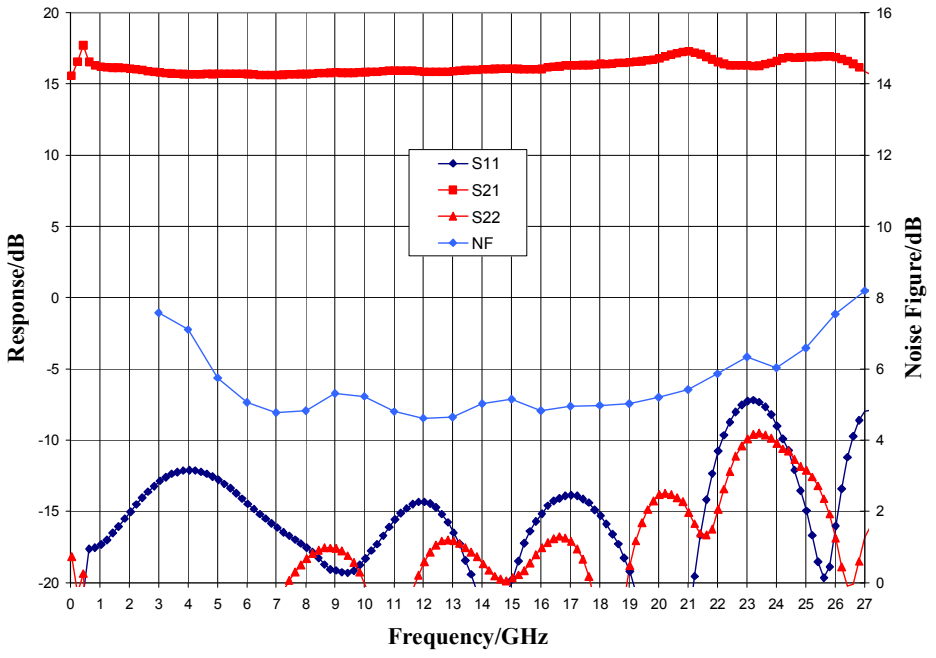
Typical Performance

Broadband Performance, V_{dd} = 5.0 V, V_{gg} = 3.0 V, I_{dd} = 74 mA, T_A = 25 °C



Narrow-band Performance, V_{dd} = 5.0 V, V_{gg} = 3.0 V, I_{dd} = 74 mA, T_A = 25 °C



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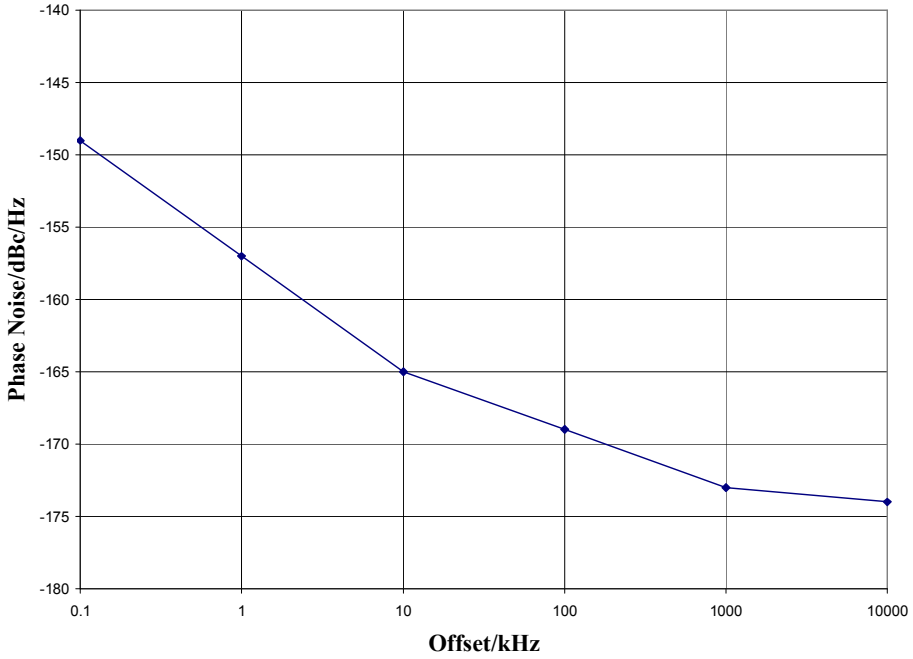
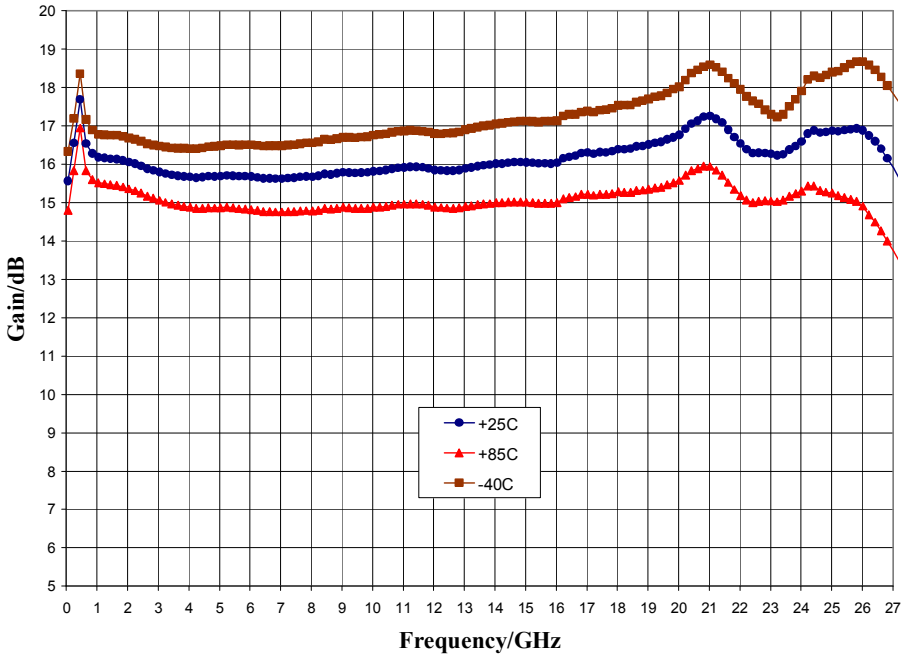
Typical Performance

Additive Phase Noise @ Psat, V_{dd} = 5.0 V, V_{gg} = 3.0 V, T_A = 25 °C



Gain vs. Temperature, V_{dd} = 5.0 V, V_{gg} = 3.0 V



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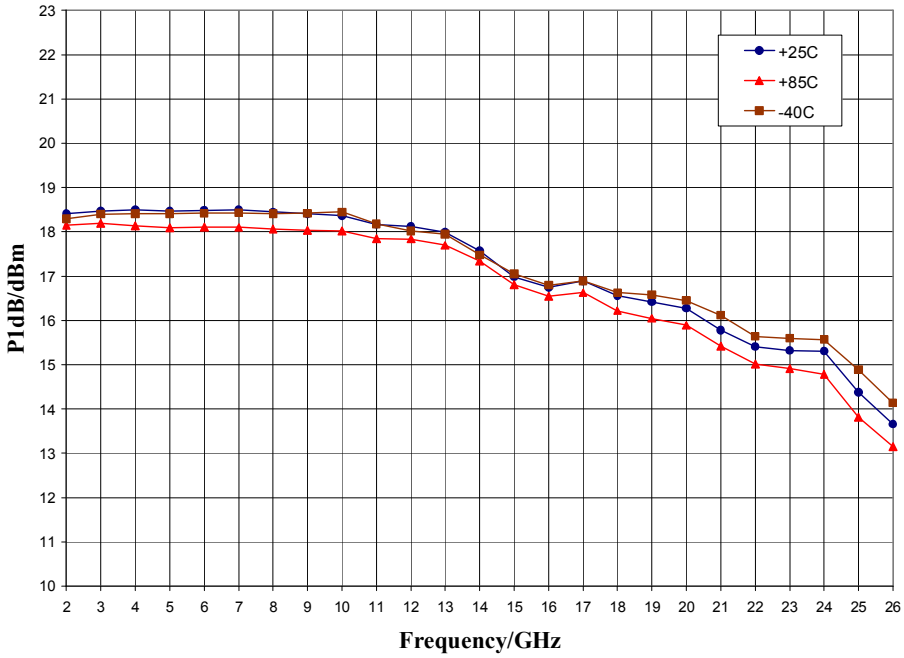
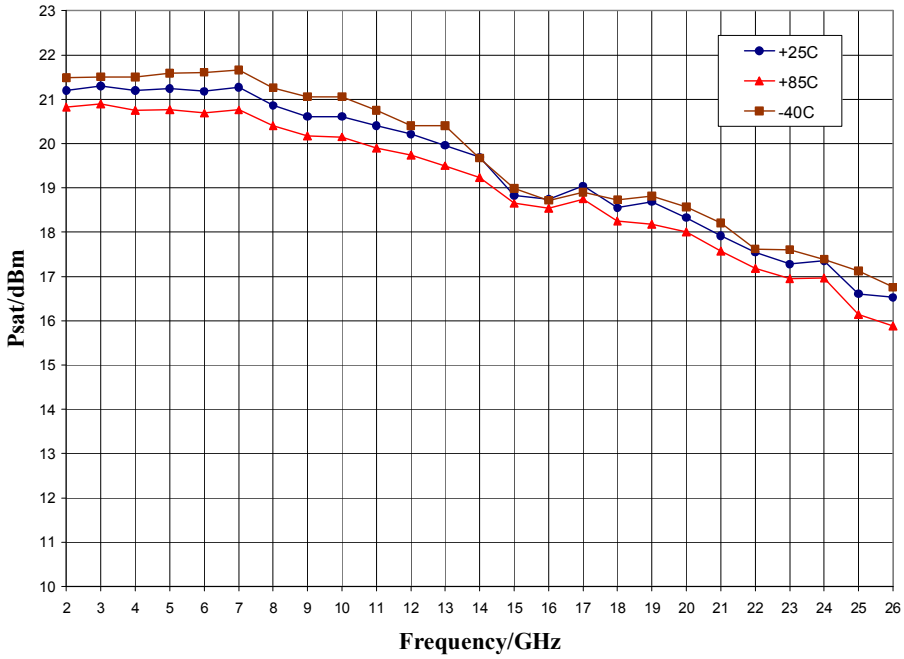
Typical Performance

P1dB vs. Temperature, V_{dd} = 5.0 V, V_{gg} = 3.0 V



Psat vs. Temperature, V_{dd} = 5.0 V, V_{gg} = 3.0 V



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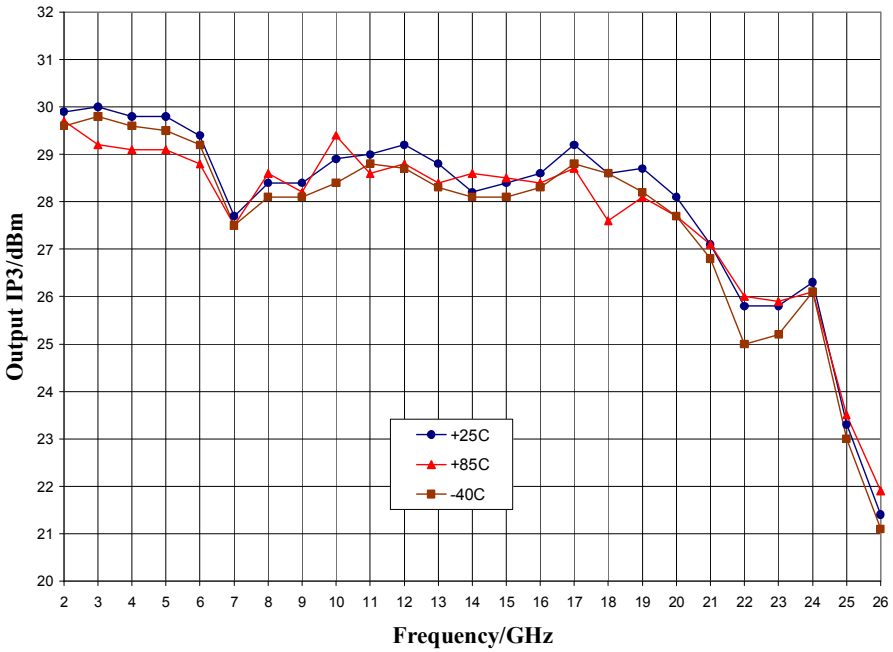
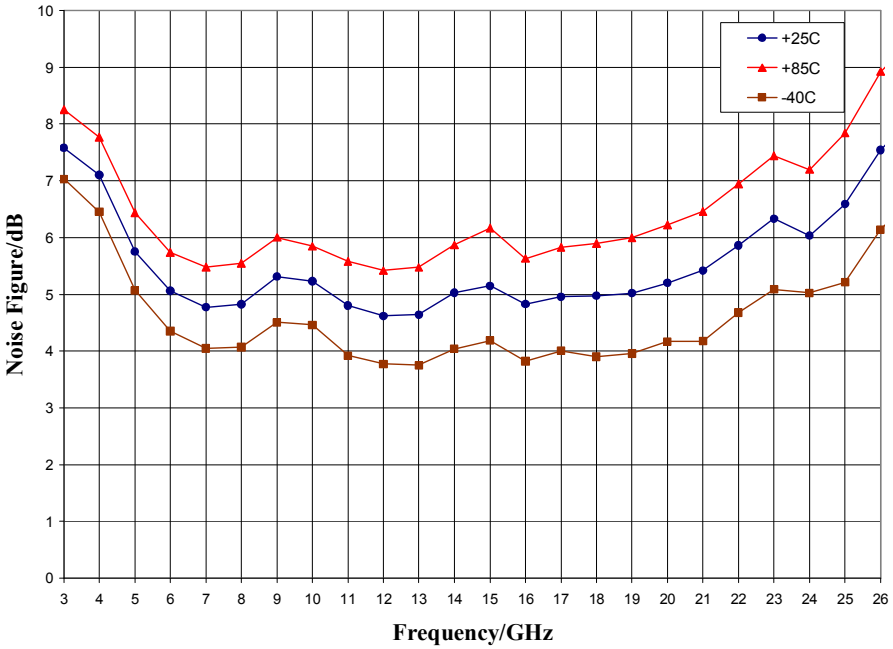
Typical Performance

Output IP3 vs. Temperature, V_{dd} = 5.0 V, V_{gg} = 3.0 V



Noise Figure vs. Temperature, V_{dd} = 5.0 V, V_{gg} = 3.0 V



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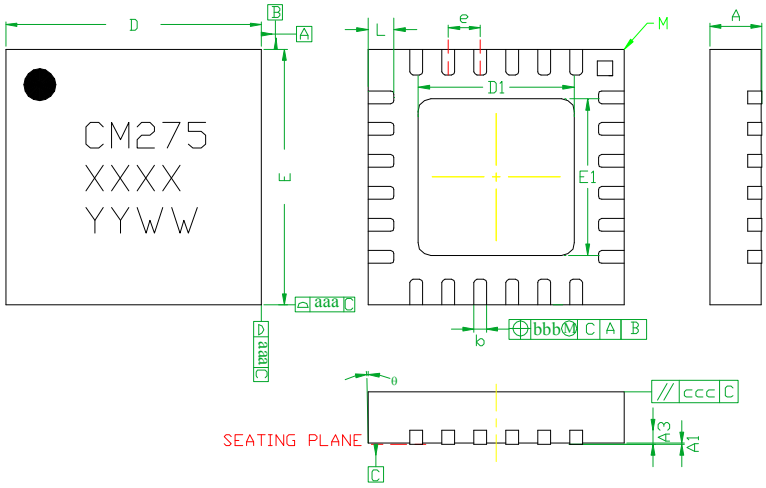
Mechanical Information

Package Information and Dimensions



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	----	0.25REF.	----
b	0.18	0.23	0.30
D	3.85	4.00	4.15
D1	2.40	2.50	2.60
E	3.85	4.00	4.15
E1	2.40	2.50	2.60
e	----	0.50BSC	----
L	0.30	0.40	0.50
θ	0	----	12
aaa	----	0.25	----
bbb	----	0.10	----
ccc	----	0.10	----
M	----	----	0.05

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS
2. RoHs COMPLIANT MOLD COMPOUND
3. LEADFRAME MATERIAL: COPPER ALLOY
4. LEAD FINISH: 100% MATTE Sn
5. INDICATED DIMENSION/TOLERANCE APPLIES TO LEADS AND EXPOSED PAD

Recommended PCB Land Pattern

Custom MMIC Design Services recommends that the user develop the land pattern that will provide the best design for proper solder reflow and device attach for their specific application. Please review CMDS Application Note AN 105 for a recommended land pattern approach.

Recommended Solder Reflow Profile

Custom MMIC Design Services recommends screen printing with belt furnace reflow to ensure proper solder reflow and device attach. Please review CMDS Application Note AN 102 for a recommended solder reflow profile.

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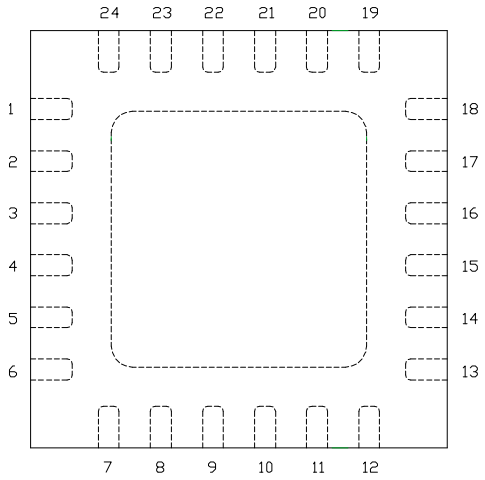
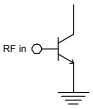
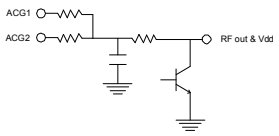
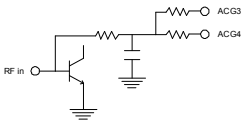
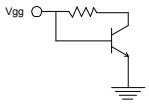
Pin Description

Pin Diagram



Functional Description

Pin	Function	Description	Schematic
1, 2, 6-8, 12-14, 18-21, 24	N/C	No connection required. These pins may be connected to RF/DC ground	
4	RF in	50 ohm matched input	
22, 23	ACG2, 1	Low frequency termination. Attach bypass capacitors per application circuit	
16	RF out & Vdd	Power supply voltage and 50 ohm matched output	
10, 11	ACG4, 3	Low frequency termination. Attach bypass capacitors per application circuit	
9	Vgg	Power supply voltage Decoupling and bypass caps required	
3, 5, 15, 17 and die paddle	Ground	Connect to RF / DC ground	

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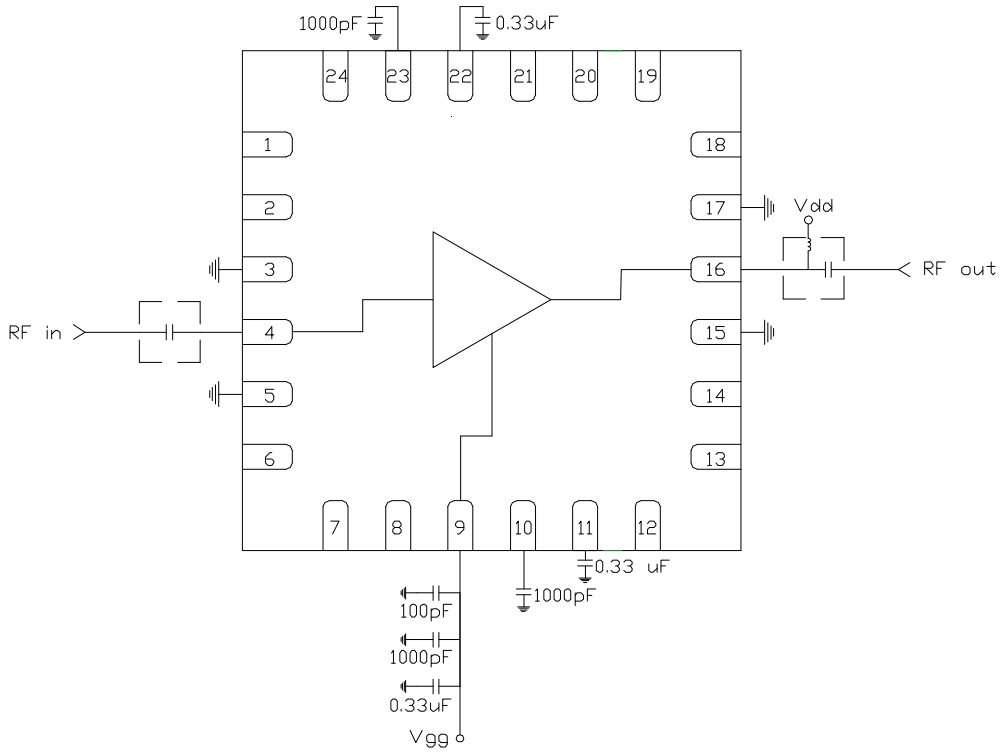
Applications Information

Application Circuit



Biasing and Operation

The CMD275P4 is biased with a positive drain supply and positive gate supply. Performance is optimized when the drain voltage is set to +5.0 V. The recommended gate voltage is +3.0 V. The preferred biasing procedure is as follows:

Turn ON procedure:
Apply the drain voltage Vdd and set it to +5V then apply gate voltage Vgg and set it to +3V.

Turn OFF procedure:
Turn off the gate voltage Vgg and then turn off the drain voltage Vdd.

The preferred biasing procedure has been proven to be robust, and should be used whenever possible. However, the CMD275P4 does allow for simultaneous biasing (applying Vdd and Vgg at the same time), and the use of a single voltage supply.

Refer to Application Note 103: Amplifier Biasing Techniques for instructions on how to implement a single supply biasing scheme.

For either approach, RF power can be applied at any time.

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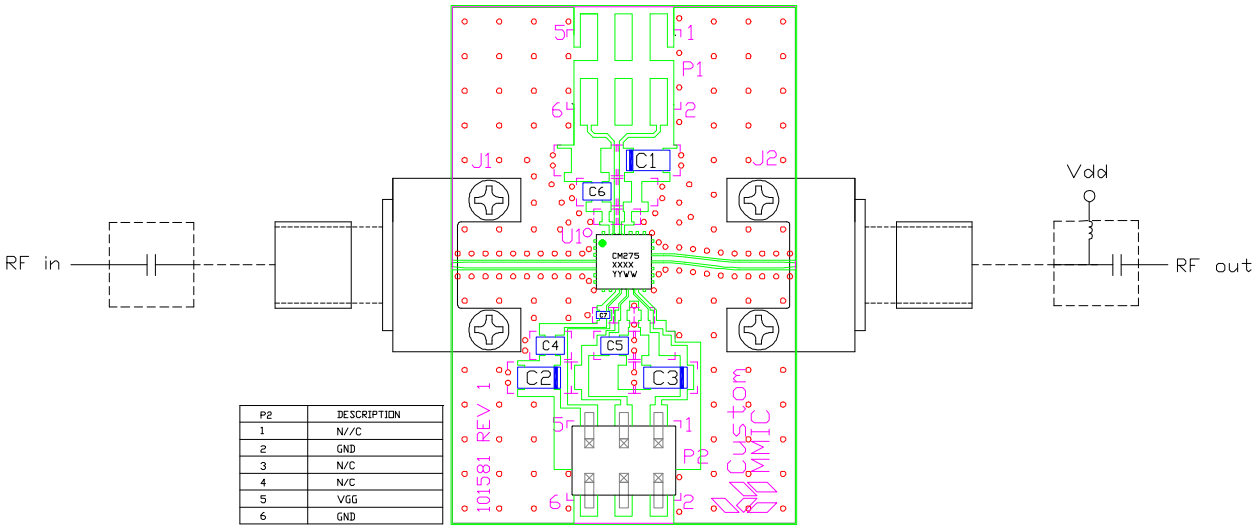
Applications Information

Evaluation Board



Bill of Material

Designator	Value	Description
J1, J2		SMA End Launch Connector
P2		6 Pin DC Header
C1-C3	0.33 µF	Capacitor, Tantalum
C4-C6	1000 pF	Capacitor, 0603
C7	100 pF	Capacitor, 0402
U1		CMD275P4 Driver Amplifier
PCB		101581 Evaluation PCB

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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