



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

1 Product Overview

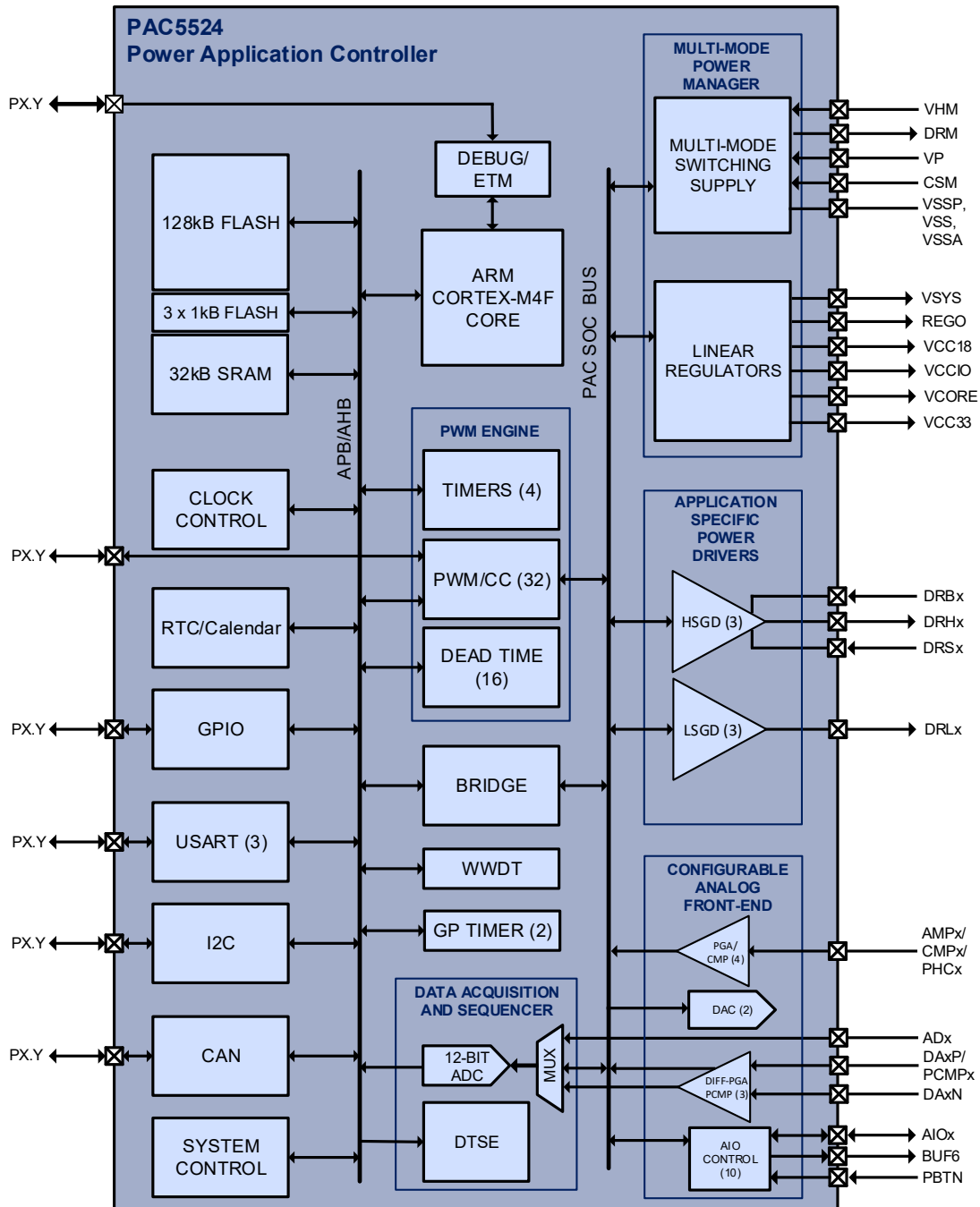
The PAC5524 is a Power Application Controller[®] (PAC) product that is optimized for high-pin count and high-speed BLDC motor control. The PAC5524 integrates a 150MHz Arm[®] Cortex[®]-M4F 32-bit microcontroller core with Active-Semi's proprietary and patent-pending Multi-Mode Power Manager[™], Configurable Analog Front-End[™] and Application Specific Power Drivers[™] to form the most compact microcontroller-based power and motor control solution available.

The PAC5524 microcontroller features 128kB of embedded FLASH and 32kB of SRAM memory, a 2.5MSPS analog-to-digital converter (ADC) with programmable auto-sampling of up to 24 conversion sequences, 3.3V IO, flexible clock control system, PWM and general-purpose timers and several serial communications interfaces.

The Multi-Mode Power Manager (MMPM) provides "all-in-one" efficient power management solution for multiple types of power sources. It features a configurable multi-mode switching supply controller capable of operating a buck or SEPIC converter and up to four linear regulated voltage supplies. The Application Specific Power Drivers (ASPD) are power drivers designed for half bridge, H-bridge, 3-phase, and general-purpose driving. The Configurable Analog Front End (CAFE) comprises differential programmable gain amplifiers, single-ended programmable gain amplifiers, comparators, digital-to-analog converters, and I/Os for programmable and interconnectible signal sampling, feedback amplification, and sensor monitoring of multiple analog input signals.

The PAC5524 is packaged in an 8x8mm, 64-lead QFN package with for compact battery-powered BLDC motor applications.

2 Functional Block Diagram



3 Key Features

Multi-Mode Power Manager™ (MMPM)

- Optional multi-mode switching supply controller configurable for DC/DC Buck or SEPIC topologies
- Direct DC supply up to 20V
- Integrated LDOs for MCU core, IO, analog with power and hibernate management
- Power and temperature monitor, warning and fault detection
- Low-power total hibernate mode, $I_Q = 18\mu A$

Configurable Analog Front-End™ (CAFE)

- 3 Differential Programmable-gain Amplifiers
- 4 Single-ended Programmable-gain Amplifiers
- 2.5V ADC reference
- Programmable over-current shutdown
- Hibernate push-button wake-up
- Power supply monitoring via ADC

Application Specific Power Drivers™ (ASPD)

- Integrated level shifters and pre-drivers
- 3 Low-side and 3 High-Side gate drivers with 1.5A gate driving capacity
- Break-before-make (BBM) hardware dead-time enforcement to prevent shoot-through
- Configurable propagation delay and fault protection
- OC, UV protection

MCU

- 150MHz Arm® Cortex®-M4F MCU
- Hardware multiplier and divider
- Single-precision Floating Point Unit (FPU)
- Nested Vectored Interrupt Controller (NVIC) with 32 interrupts and 8 priority levels
- Clock-gating for low-power operation
- Embedded Trace Macrocell (ETM) for in-system debugging in real-time without breakpoints

Memory

- 128kB FLASH, 32kB SRAM with ECC
- 2 x 1kB INFO FLASH for manufacturing information
- 1 x 1kB INFO FLASH for user parameter storage and application configuration code
- 4-level user-configurable code protection

ADC

- 12-bit 2.5MSPS SAR ADC
- Dynamic Triggering and Sequence Engine (DTSE)
 - Up to 16 configurable sequences
 - Dedicated memory for conversion results

IO

- 3.3V digital input/output or analog input for ADC
- Configurable weak pull-up or pull-down
- Configurable drive strength (6mA to 25mA minimum)
- Flexible peripheral MUX allowing each IO pin to select from up to 8 peripheral functions
- Flexible interrupt controller

Flexible Clock Control System (CCS)

- 300MHz PLL from internal 2% oscillator
- 20MHz ring oscillator
- Optional 20MHz external clock input

Timing Generators

- Four 16-bit PWM timers with up to 8 CCR output units each
- 24-bit SysTick count-down timer
- Windowed Watch-dog Timer (WWDT)
- 24-bit Real-Time Clock (RTC) with calendar and alarm
- 2 x 24-bit General-purpose count-down timers with interrupt
- Hibernate wake-up timer for sleep modes from 0.125s to 8s

Communication Peripherals

- 3 x USART (UART or SPI)
- I2C master/slave
- SPI master/slave, up to 25MHz
- CAN 2.0B Controller
- SWD or JTAG serial debug interfaces
- Embedded Trace Macrocell (ETM)

8b/16b CRC Engine

96-bit Unique ID

Physical

- $T_A = -40C$ to $125C$
- QFN 8x8mm 64-pin package
 - Exposed pad for thermal management



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

4 Ordering Information

| Part Number | Temperature Range | Package | Pins | Packaging |
|-------------|-------------------|------------|------------------|----------------------------|
| PAC5524QF | -40°C to 125°C | TQFN88-64L | 64 + Exposed Pad | Tray (2600 piece) |
| PAC5524QF-T | | | | Tape and Reel (3000 piece) |



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

Table of Contents

| | | |
|-------|--|----|
| 1 | Product Overview | 1 |
| 2 | Functional Block Diagram | 2 |
| 3 | Key Features | 3 |
| 4 | Ordering Information | 4 |
| 5 | Absolute Maximum Ratings | 10 |
| 6 | Multi-Mode Power Manager (MMPM) | 11 |
| 6.1 | Features | 11 |
| 6.2 | System Block Diagram | 11 |
| 6.3 | Functional Description | 12 |
| 6.3.1 | Multi-Mode Switching Supply (MMSS) Controller | 12 |
| 6.3.2 | Linear Regulators | 13 |
| 6.3.3 | Power-up Sequence | 14 |
| 6.3.4 | Hibernate Mode | 16 |
| 6.3.5 | Power and Temperature Monitor | 16 |
| 6.3.6 | Voltage Reference | 16 |
| 6.4 | Electrical Characteristics | 17 |
| 6.4.1 | MMSS Electrical Characteristics | 17 |
| 6.4.2 | Linear Regulators Electrical Characteristics | 18 |
| 6.4.3 | Power Monitor Electrical Characteristics | 19 |
| 6.5 | Typical Performance Characteristics | 20 |
| 7 | Configurable Analog Front-End (CAFE) | 21 |
| 7.1 | Features | 21 |
| 7.2 | System Block Diagram | 22 |
| 7.3 | Functional Description | 23 |
| 7.3.1 | Differential Programmable Gain Amplifier (DA) | 23 |
| 7.3.2 | Single-Ended Programmable Gain Amplifier (AMP) | 23 |
| 7.3.3 | General-Purpose Comparator (CMP) | 23 |
| 7.3.4 | Phase Comparator (PHC) | 23 |
| 7.3.5 | Protection Comparator (PCMP) | 24 |
| 7.3.6 | Analog Output Buffer (BUF) | 24 |
| 7.3.7 | Analog Front End I/O (AIO) | 24 |
| 7.3.8 | Push Button (PBTN) | 24 |
| 7.3.9 | HP DAC and LP DAC | 24 |



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

| | | |
|--------|--|----|
| 7.3.10 | ADC Analog Input | 25 |
| 7.3.11 | Configurable Analog Signal Matrix (CASM) | 26 |
| 7.3.12 | Configurable Digital Signal Matrix (CDSM) | 26 |
| 7.3.13 | Temperature Protection | 26 |
| 7.4 | Electrical Characteristics | 27 |
| 7.4.1 | Differential Programmable Gain Amplifier (DA) | 27 |
| 7.4.2 | Single-Ended Programmable Gain Amplifier (SA) | 28 |
| 7.4.3 | General Purpose Comparator (CMP) | 28 |
| 7.4.4 | Phase Comparator (PHC) | 29 |
| 7.4.5 | Protection Comparator (PCMP) | 29 |
| 7.4.6 | Analog Output Buffer (BUF) | 29 |
| 7.4.7 | Analog Front End (AIO) Electrical Characteristics | 30 |
| 7.4.8 | Push-Button (PBTN) Electrical Characteristics | 30 |
| 7.4.9 | HP DAC and LP DAC Electrical Characteristics | 30 |
| 7.4.10 | Temperature Protection Electrical Characteristics | 31 |
| 7.5 | Typical Performance Characteristics | 32 |
| 8 | Application Specific Power Drivers (ASPD) | 33 |
| 8.1 | Features | 33 |
| 8.2 | System Block Diagram | 33 |
| 8.3 | Functional Description | 34 |
| 8.4 | Low-Side Gate Drivers | 34 |
| 8.5 | High-Side Gate Drivers | 34 |
| 8.6 | High-Side Switching Transients | 35 |
| 8.7 | Power Drivers Control | 35 |
| 8.8 | Gate Driver Fault Protection | 36 |
| 8.9 | Electrical Characteristics | 37 |
| 8.9.1 | Low-Side Gate Drivers | 37 |
| 8.9.2 | High-Side Gate Drivers | 37 |
| 8.9.3 | High-Side and Low-Side Gate Driver Propagation Delay | 38 |
| 8.10 | Typical Performance Characteristics | 39 |
| 9 | SOC Control Signals | 41 |
| 9.1 | High-side and Low-Side Gate Drivers | 41 |
| 9.2 | SPI SOC Bus | 44 |
| 9.3 | ADC EMUX | 44 |



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

| | | |
|--------|---|----|
| 9.4 | Analog Interrupts | 44 |
| 10 | ADC/DTSE | 45 |
| 10.1 | Features | 45 |
| 10.2 | System Block Diagram | 45 |
| 10.3 | Functional Description | 46 |
| 10.3.1 | ADC | 46 |
| 10.3.2 | Dynamic Triggering and Sample Engine (DTSE) | 46 |
| 10.3.3 | EMUX Control | 46 |
| 10.4 | Electrical Characteristics | 47 |
| 11 | Memory System | 48 |
| 11.1 | Features | 48 |
| 11.2 | System Block Diagram | 48 |
| 11.3 | Functional Description | 49 |
| 11.3.1 | Program FLASH | 49 |
| 11.3.2 | INFO FLASH | 49 |
| 11.3.3 | SRAM | 49 |
| 11.3.4 | Code Protection | 50 |
| 11.4 | Electrical Characteristics | 51 |
| 12 | System and Clock Control (SCC) | 52 |
| 12.1 | Features | 52 |
| 12.2 | System Block Diagram | 52 |
| 12.3 | Functional Description | 53 |
| 12.4 | Clock Sources | 53 |
| 12.4.1 | Ring Oscillator | 53 |
| 12.4.2 | Reference Clock | 53 |
| 12.4.3 | External Clock Input | 53 |
| 12.5 | PLL | 53 |
| 12.6 | Clock Tree | 53 |
| 12.6.1 | FRCLK | 53 |
| 12.6.2 | SCLK | 53 |
| 12.6.3 | PCLK | 54 |
| 12.6.4 | ACLK | 54 |
| 12.6.5 | HCLK | 54 |
| 12.7 | Electrical Characteristics | 55 |



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

| | | |
|--------|--|----|
| 13 | Arm® Cortex®-M4F MCU Core | 56 |
| 13.1 | Features | 56 |
| 13.2 | System Block Diagram | 56 |
| 13.3 | Functional Description | 57 |
| 13.4 | Application Typical Current Consumption | 58 |
| 13.5 | Electrical Characteristics | 60 |
| 14 | IO Controller | 61 |
| 14.1 | Features | 61 |
| 14.2 | System Block Diagram | 61 |
| 14.3 | Functional Description | 62 |
| 14.3.1 | IO Controller | 62 |
| 14.3.2 | GPIO Current Injection | 62 |
| 14.3.3 | Peripheral MUX | 63 |
| 14.4 | Electrical Characteristics | 64 |
| 15 | Serial Interface | 65 |
| 15.1 | Features | 65 |
| 15.2 | System Block Diagram | 65 |
| 15.3 | Functional Description | 66 |
| 15.4 | I ² C Controller | 66 |
| 15.5 | USART | 66 |
| 15.5.1 | USART SPI Mode | 66 |
| 15.5.2 | USART UART Mode | 66 |
| 15.6 | CAN | 67 |
| 15.7 | Dynamic Characteristics | 68 |
| 15.7.1 | Serial Interface | 68 |
| 15.7.2 | I ² C Dynamic Characteristics | 69 |
| 15.7.3 | I ² C Timing Diagram | 70 |
| 16 | PWM Timers | 71 |
| 16.1 | Features | 71 |
| 16.2 | System Block Diagram | 73 |
| 16.3 | Functional Description | 74 |
| 17 | General Purpose Timers | 75 |
| 17.1 | Features | 75 |
| 17.2 | System Block Diagram | 75 |



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

| | | |
|--------|-------------------------------------|----|
| 17.3 | Functional Description | 76 |
| 17.3.1 | SOC Bus Watchdog Timer | 76 |
| 17.3.2 | Wake-up Timer | 76 |
| 17.3.3 | Real-time Clock with Calendar (RTC) | 76 |
| 17.3.4 | Windowed Watchdog Timer (WWDT) | 76 |
| 17.3.5 | GP Timer (GPT) | 76 |
| 18 | CRC | 77 |
| 18.1 | Features | 77 |
| 18.2 | System Block Diagram | 77 |
| 18.3 | Functional Description | 77 |
| 19 | Application Block Diagram | 78 |
| 20 | Thermal Characteristics | 80 |
| 21 | Pin Configuration and Description | 81 |
| 21.1 | MMPM and System Pin Descriptions | 82 |
| 21.2 | CAFE Pin Descriptions | 83 |
| 21.3 | ASPD Pin Descriptions | 84 |
| 21.4 | I/O Ports Pin Descriptions | 85 |
| 22 | Mechanical Information | 86 |
| 23 | Handling Precautions | 87 |
| 24 | Solderability | 87 |
| 25 | Contact Information | 88 |
| 26 | Important Notice | 88 |



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

5 Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|--|---|--------------------|------|
| Power Manager | | | |
| VHM, DRM to VSS | Supply Input and DC/DC Gate Drive Voltage | -0.3 to 72 | V |
| VP to VSS | Gate Drive Voltage | -0.3 to 20 | V |
| CSM, REGO to VSS | DC/DC current sense and VSYS regulator output | -0.3 to VP + 0.3 | V |
| VSYS, VCCIO, AIO6 to VSS | | -0.3 to 6 | V |
| VCC33 to VSS | Analog Supply Voltage | -0.3 to 4.1 | V |
| VCC18 to VSS | MCU FLASH Supply Voltage | -0.3 to 2.5 | V |
| VCORE to VSS | MCU Core Supply Voltage | -0.3 to 1.44 | V |
| Signal Manager | | | |
| AIO[0..5, 7..9] to VSS | AIO Input Voltage | -0.3 to VSYS + 0.3 | V |
| AIO6 to VSS | AIO6 Input Voltage | -0.3 to 6 | V |
| Driver Manager | | | |
| DRLx to VSS | Low-side Gate Drive Voltage | -0.3 to VP + 0.3 | V |
| DRBx to VSS | Boot-strap Gate Drive Voltage | -0.3 to 84 | V |
| DRSx to VSS | High-side Gate Drive Voltage | -6 to 72 | V |
| dVDRSx/dt | DRSx allowable offset slew rate | 5 | V/ns |
| DRBx, DRHx to respective DRSx | Floating gate drive offset | -0.3 to 20 | V |
| VSS, VSYS, DRLx, DRHx, VSYSW RMS current | | 0.2 | ARMS |
| VSS RMS current | | 0.4 | ARMS |
| VP RMS current | | 0.6 | ARMS |
| IO | | | |
| PCx, PDx, PEx, PFx, PGx to VSS | MCU IO Pin Voltage | -0.3 to 4.6 | V |
| IPCx, IPDx, IPEx, IPFx, IPGx | Pin injection current | 25 | mA |
| $\sum I_{PCx}, \sum I_{PDx}, \sum I_{PEx}, \sum I_{PFx}, \sum I_{PGx}$ | Sum of all pin injection current | 50 | mA |
| Temperature | | | |
| T _A | Ambient Temperature | -40 to 125 | °C |
| T _{STG} | Storage Temperature | -55 to 150 | °C |
| Electro-static Discharge (ESD) | | | |
| Human Body Model (HBM) | All pins | 2 | kV |
| Charge Device Model (CDM) | All pins | 1 | kV |

Operation of this device outside the parameter ranges given above may cause permanent damage.

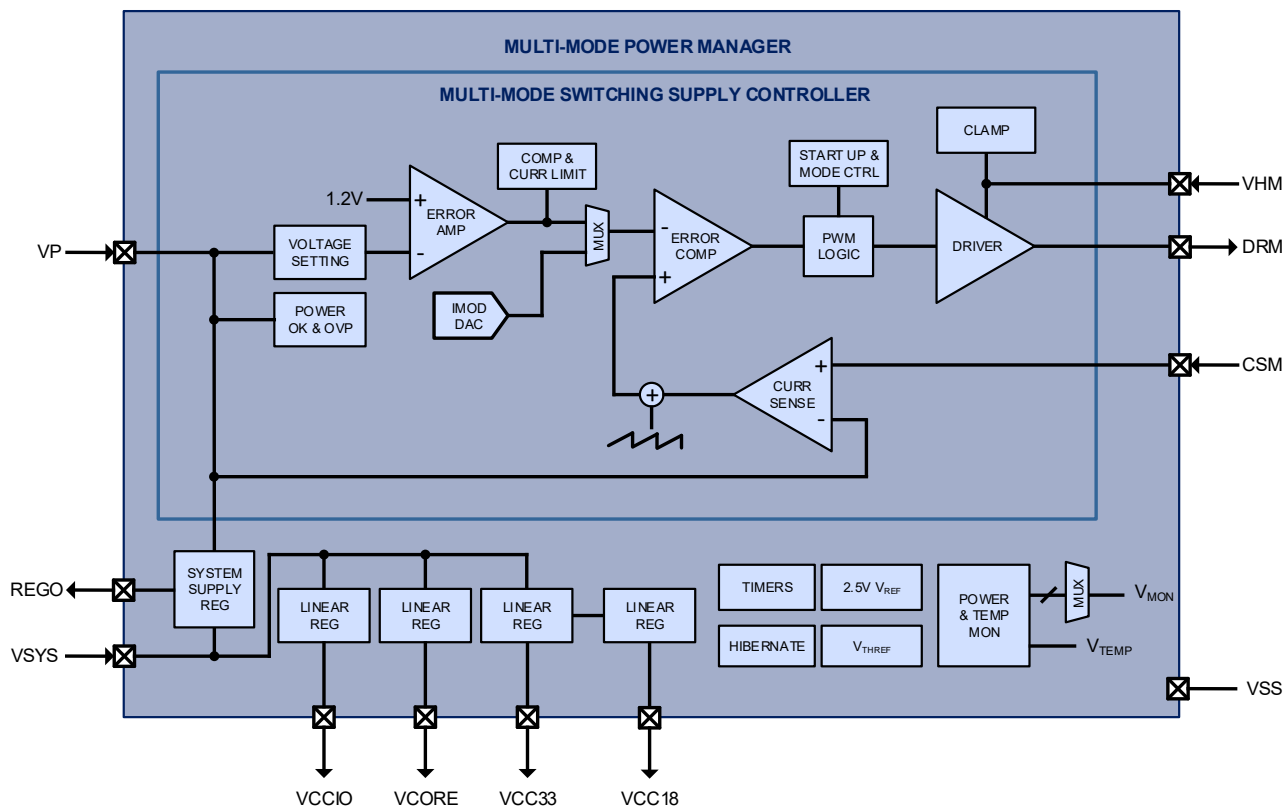
6 Multi-Mode Power Manager (MPPM)

6.1 Features

- Multi-mode switching supply controller configurable as Buck or SEPIC
- DC supply up to 70V input
- Direct DC input of up to 20V with no DC/DC
- 5 linear regulators with power and hibernate management, including VREF for ADC
- Power and temperature monitor, warning, and fault detection
- Very low-power total hibernate mode

6.2 System Block Diagram

Figure 1 MPPM System Block Diagram



6.3 Functional Description

The Multi-Mode Power Manager is optimized to efficiently provide “all-in-one” power management required by the PAC and associated application circuitry. It incorporates a dedicated multi-mode switching supply (MMSS) controller operable as a Buck or SEPIC converter to efficiently convert power from a DC input source to generate a main supply output VP. Five linear regulators provide VCC18, VSYS, VCCIO, VCC33, and VCORE supplies for MCU FLASH, 5V system, 3.3V I/O, 3.3V mixed signal, and 1.2V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

6.3.1 Multi-Mode Switching Supply (MMSS) Controller

The MMSS controller drives an external power transistor for pulse-width modulation switching of an inductor or transformer for power conversion. The DRM output drives the gate of the N-CH MOSFET between the VHM on state and VSSP off state at proper duty cycle and switching frequency to ensure that the main supply voltage VP is regulated. The VP regulation voltage is initially set to 15V during start up and can be reconfigured to be 9V or 12V by the microcontroller after initialization. When VP is lower than the target regulation voltage, the internal feedback control circuitry causes the inductor current to increase to raise VP. Conversely, when VP is higher than the regulation voltage, the feedback loop control causes the inductor current to decrease to lower VP. The feedback loop is internally stabilized. The output current capability of the switching supply is determined by the external current sense resistor. In the high-side current sense buck or SEPIC mode, the inductor current signal is sensed differentially between the CSM pin and VP and has a peak current limit threshold of 0.26V.

The MMSS controller is flexible and configurable as a buck or SEPIC converter. Input sources include battery supply for buck mode or SEPIC mode as shown below. The MMSS controller operational mode is determined by external configuration and register settings from the microcontroller after power up. It can operate in either high-side or low-side current sense mode and does not require external feedback loop compensation circuitry.

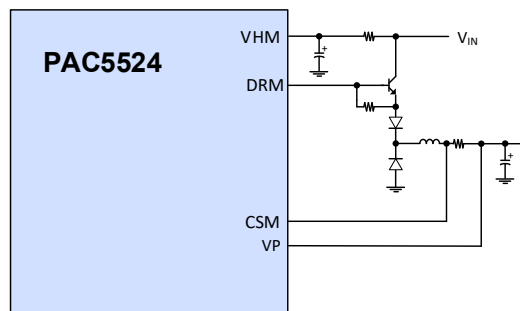


Figure 2 Buck Mode

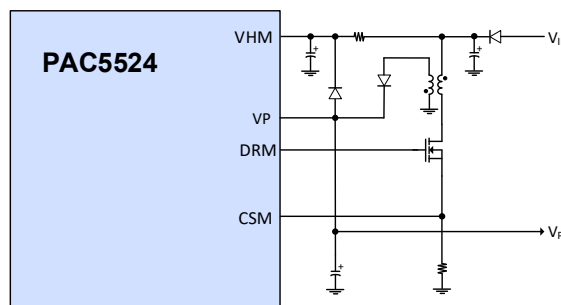


Figure 3 SEPIC Mode

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

The MMSS detects and selects between high-side and low-side mode during start up based on the placement of the current sense resistor and the CSM pin voltage. It employs a safe start up mode with a 9.5kHz switching frequency until VP exceeds 4.3V under-voltage-lockout threshold, then transitions to the 45kHz default switching frequency for at least 6ms to bring VP close to the target voltage, before enabling the linear regulators. Any extra load should only be applied after the supplies are available and the microprocessor has initialized. The switching frequency can be reconfigured by the microprocessor to be 181kHz to 500kHz in the high switching frequency mode for battery-based applications, and to be 45kHz to 125kHz in the low switching frequency mode. Upon initialization, the microcontroller must reconfigure the MMSS to the desired settings for VP regulation voltage, switching mode, switching frequency, and VHM clamp. Refer to the PAC application notes and user guide for MMSS controller design and programming.

If a stable external 5V to 20V power source is available, it can power the VP main supply and all the linear regulators directly without requiring the MMSS controller to operate. In such applications, VHM can be connected directly to VP and the microcontroller should disable the MMSS upon initialization to reduce power loss.

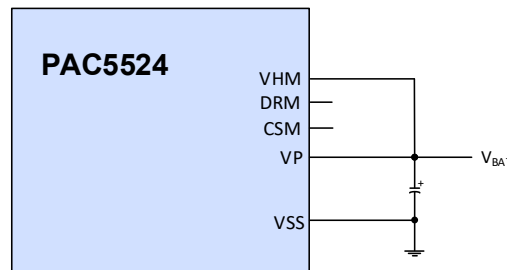


Figure 4 Direct Battery Supply

6.3.2 Linear Regulators

The MMPM includes four linear regulators. The system supply regulator (VSYS) is a medium voltage regulator that takes the VP supply and sources up to 200mA at REGO until VSYS, externally coupled to REGO, reaches 5V. This allows a properly rated external resistor to be connected from REGO to VSYS to close the loop and offload power dissipation between VP and VSYS.

Once VSYS is above 4V, the four additional linear regulators for VCC18, VCCIO, VCC33, and VCORE supplies sequentially power up. Figure 10 5 shows typical circuit connections for the linear regulators. The VCC18 regulator generates a dedicated 1.8V supply for FLASH on the MCU. The VCCIO regulator generates a dedicated 3.3V supply for IO. The VCC33 and VCORE regulators generate 3.3V and 1.2V, respectively. When VSYS, VCCIO, VCC33, and VCORE are all above their respective power good thresholds, and the configurable power on reset duration has expired, the microcontroller is initialized.

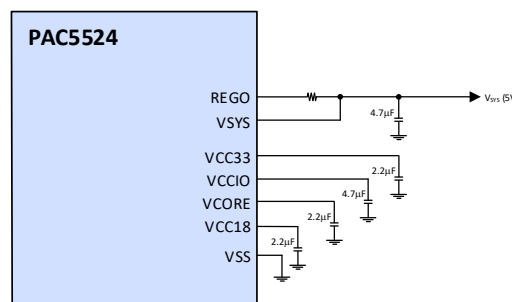


Figure 5 Linear Regulators Connections

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

6.3.3 Power-up Sequence

The MMPM follows a typical power up sequence with a DC/DC as shown below.

A typical sequence begins with input power supply being applied, followed by the safe start up and start up durations to bring the switching supply output VP to 15V, before the linear regulators are enabled. When all the supplies are ready, the internal clocks become available, and the microcontroller starts executing from the program memory. During initialization, the microcontroller can reconfigure the switching supply to a different VP regulation voltage such as 9V or 12V and to an appropriate switching frequency and switching mode. The total loading on the switching supply must be kept below 25% of the maximum output current until after the reconfiguration of the switching supply is complete.

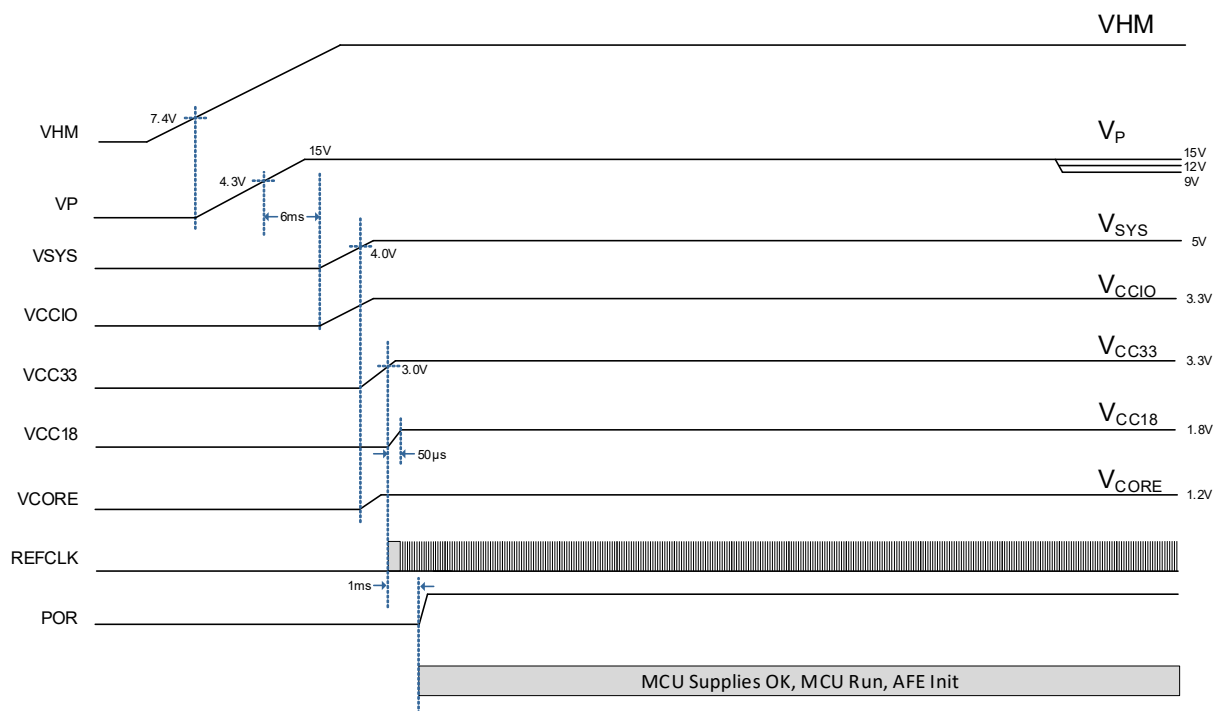


Figure 6 Power-up Sequence with DC/DC

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

If the PAC5524 is used without a DC/DC by directly supplying the IC and connecting the VP and VHM supply pins on the device, the power supply start-up sequence is slightly different. This case is shown below.

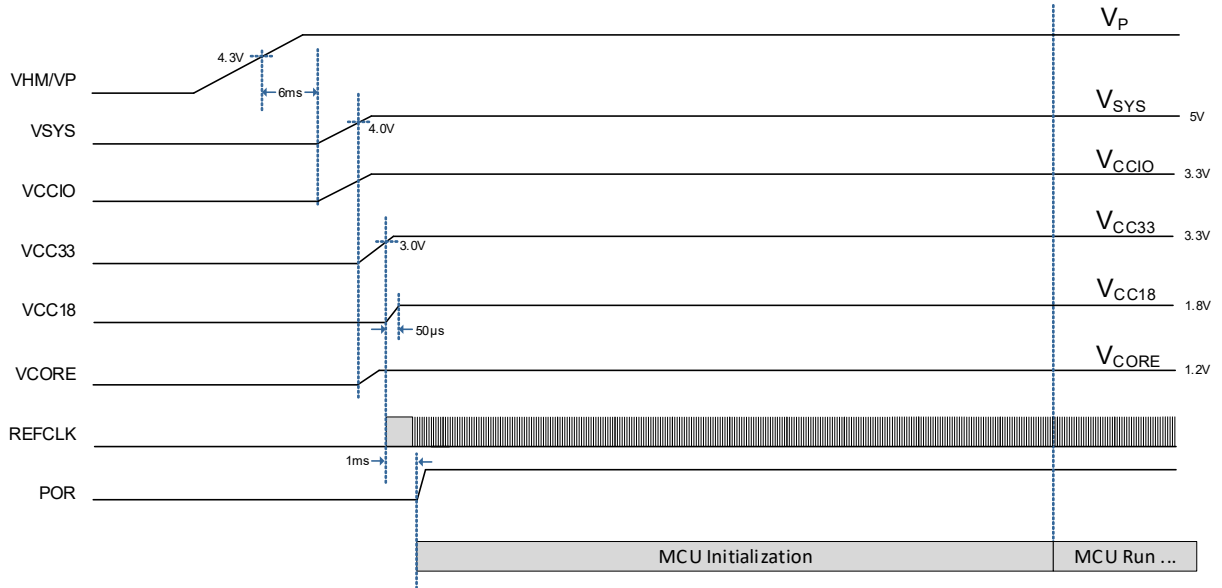


Figure 7 Power-up Sequence with direct DC supply

6.3.4 Hibernate Mode

The IC can go into an ultra-low power hibernate mode via the microcontroller firmware or via the optional push button (PBTN). In hibernate mode, only a minimal amount (typically 18 μ A) of current is used by V_P , and the MMSS controller and all internal regulators are shut down to eliminate power drain from the output supplies. The system exits hibernate mode after a wake-up timer duration (configurable from 125ms to 8s or infinite) has expired or, if push button enabled, after an additional push button event has been detected. When exiting the hibernate mode, the power manager goes through the start up cycle and the microcontroller is reinitialized. Only the persistent power manager status bits (resets and faults) are retained during hibernation.

6.3.5 Power and Temperature Monitor

Whenever any of the V_{SYS} , V_{CCIO} , V_{CC33} , or V_{CORE} power supplies falls below their respective power good threshold voltage, a fault event is detected and the microcontroller is reset. The microcontroller stays in the reset state until V_{SYS} , V_{CCIO} , V_{CC33} , and V_{CORE} supply rails are all good again and the reset time has expired. A microcontroller reset can also be initiated by a maskable temperature fault event that occurs when the IC temperature reaches 170°C. The fault status bits are persistent during reset, and can be read by the microcontroller upon re-initialization to determine the cause of previous reset.

A power monitoring signal V_{MON} is provided onto the ADC pre-multiplexer for monitoring various internal power supplies. V_{MON} can be set to be V_{CORE} , $0.4 \cdot V_{CC33}$, $0.4 \cdot V_{CCIO}$, $0.4 \cdot V_{SYS}$, $0.1 \cdot V_{REGO}$, $0.1 \cdot V_P$, or the internal compensation voltage V_{COMP} for switching supply power monitoring.

For power and temperature warning, an IC temperature warning event at 140°C are provided as a maskable interrupt to the microcontroller. This warning allows the microcontroller to safely power down the system.

In addition to the temperature warning interrupt and fault reset, a temperature monitor signal $V_{TEMP} = 1.5 + 5.04e-3 \cdot (T - 25^\circ C)$ (V) is provided onto the ADC pre-multiplexer for IC temperature measurement.

6.3.6 Voltage Reference

The reference block includes a 2.5V high precision reference voltage that provides the 2.5V reference voltage for the ADC, the DACs, and the 4-level programmable threshold voltage V_{THREF} (0.1V, 0.2V, 0.5V, and 1.25V).

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

6.4 Electrical Characteristics

The Electrical Characteristics for the MMPM are shown below.

6.4.1 MMSS Electrical Characteristics

Table 1 HVCP Manager Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--|--|--|------|-------|------|-------|
| Input Supply (VM) | | | | | | |
| I _{HIB;VHM} | VHM hibernate mode supply current | Hibernate mode active | | 18 | 36 | μA |
| I _{SU;VHM} | VHM start-up supply current | VHM < V _{UVLOR;VHM} | | 75 | 120 | μA |
| I _{OP;VHM} | VHM operating supply current | DRM floating | | 0.3 | 0.5 | mA |
| V _{OP;VHM} | VHM operating voltage range | | 5 | | 70 | V |
| V _{UVLOR;VHM} | VHM under-voltage lockout rising | VHM rising | 6.8 | 7.4 | 8 | V |
| V _{UVLOF;VHM} | VHM under-voltage lockout falling | VHM falling | 6 | 6.6 | 7 | V |
| V _{CLAMP;VHM} | VHM clamp voltage | Clamp enabled, sink current = 100 μA | 14.5 | 16.9 | 19.5 | V |
| I _{CLAMP;VHM} | VHM clamp sink current limit | Clamp enabled | | 4 | | mA |
| Output Supply and Feedback (VP) | | | | | | |
| V _{REG;VP} | VP output regulation voltage | Programmable to 9V, 12V, 15V; Load = 0 to 500mA | -7 | -1 | 5 | % |
| K _{POK;VP} | VP power OK threshold | VP rising, hysteresis = 10% | 82 | 87 | 92 | % |
| K _{OVP;VP} | VP over-voltage protection threshold | VP rising, hysteresis = 15%; MMPM controller enabled | | 136 | | % |
| Switching Control | | | | | | |
| f _{SWM;DRM} | Switching frequency programmable range | High-frequency mode, 8 settings | 181 | | 500 | kHz |
| | | Low-frequency mode, 8 settings | 45 | | 125 | kHz |
| f _{SSU;DRM} | Safe start-up switching frequency | | | 9.5 | | kHz |
| t _{ONMIN;DRM} | DRM Minimum on-time | | | 440 | | ns |
| t _{OFFMIN;DRM} | DRM Minimum off-time | Low duty-cycle and low-frequency mode | | 25 | | % |
| | | Low duty-cycle and high-frequency mode | | 440 | | ns |
| | | High duty-cycle mode | | 820 | | ns |
| Current Sense (CSM pin) | | | | | | |
| V _{DET;CSM} | CSM mode detection threshold | Rising, hysteresis = 50mV | 0.40 | 0.55 | 0.69 | V |
| V _{HSLIM;CSM} | High-side current limit threshold | 181kHz, duty = 50%, relative to VP | 0.17 | 0.26 | 0.35 | V |
| V _{LSLIM;CSM} | Low-side current limit threshold | 45kHz, duty = 25% | 0.7 | 1 | 1.48 | V |
| t _{BLANK;CSM} | Current sense blanking time | | | 200 | | ns |
| V _{PROT;CSM} | Low-side abnormal current sense protection threshold | VP < 4.3V | | 0.8 | | V |
| | | VP > 4.3V | | 1.9 | | V |
| Gate Driver Output (DRM pin) | | | | | | |
| V _{OH;DRM} | High-level output voltage | 5% I _{OH} , relative to VHM | | VHM-1 | | V |



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

| | | | | |
|--------------|----------------------------------|------------------------------|------|----|
| $V_{OL,DRM}$ | Low-level output voltage | 5% I_{OL} | 0.6 | V |
| $I_{OH,DRM}$ | High-level output source current | $V_{DRM} = V_{HM} - 5V$ | -0.3 | A |
| $I_{OL,DRM}$ | Low-level output sink current | $V_{DRM} = 5V$ | 0.5 | A |
| $t_{PD,DRM}$ | Strong pull-down pulse width | High-side current sense mode | 240 | ns |

$V_{HM} = 24V$ and $T_A = -40^{\circ}C$ to $125^{\circ}C$ unless otherwise specified

6.4.2 Linear Regulators Electrical Characteristics

Table 2 Linear Regulators Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-----------------|------------------------------------|-------------------------------------|------|------|------|---------|
| $V_{OP,VP}$ | VP operating voltage range | | 4.5 | | 20 | V |
| $V_{UVLO,VP}$ | VP under-voltage lockout threshold | VP rising, hysteresis = 0.2V | 4 | 4.3 | 4.6 | V |
| $I_{Q,VP}$ | VP quiescent supply current | MMPM only, including $I_{Q,VSYS}$ | | 400 | 750 | μA |
| $I_{Q,VSYS}$ | VSYS quiescent supply current | VCCIO, VCC33, VCORE regulators only | | 350 | 600 | μA |
| V_{SYS} | VSYS output voltage | Load = 10 μA to 200mA | 4.8 | 5.0 | 5.18 | V |
| V_{CCIO} | VCCIO output voltage | Load = 10mA | 3.15 | 3.3 | 3.4 | V |
| V_{CC33} | VCC33 output voltage | Load = 10mA | 3.15 | 3.3 | 3.4 | V |
| V_{CORE} | VCORE output voltage | Load = 10mA | 1.14 | 1.2 | 1.26 | V |
| $I_{LIM,VSYS}$ | VSYS regulator current limit | | 220 | 330 | | mA |
| $I_{LIM,VCCIO}$ | VCCIO regulator current limit | | 45 | 80 | | mA |
| $I_{LIM,VCC33}$ | VCC33 regulator current limit | | 45 | 80 | | mA |
| $I_{LIM,VCORE}$ | VCORE regulator current limit | | 45 | 80 | | mA |
| K_{SCFB} | Short-circuit fold-back | | | 50 | | % |
| $V_{DO,VSYS}$ | VSYS drop-out voltage | VP = 5V, $I_{VSYS} = 100mA$ | | 350 | 680 | mV |
| $V_{UVLO,VSYS}$ | VSYS UVLO threshold | VSYS rising, hysteresis = 0.2V | 3.5 | 4 | 4.4 | V |
| $K_{POK,VCCIO}$ | VCCIO power OK threshold | VCCIO rising, hysteresis = 10% | 79 | 85 | 91 | % |
| $K_{POK,VCC33}$ | VCC33 power OK threshold | VCC33 rising, hysteresis = 10% | 79 | 85 | 91 | % |
| $K_{POK,VCORE}$ | VCORE power OK threshold | VCORE rising, hysteresis = 10% | 79 | 85 | 91 | % |
| $t_{POK,VCC18}$ | VCC18 power OK time | $C_{VCC18} = 1\mu F$ | | | 50 | μS |

$V_{HM} = 12V$ and $T_A = -40^{\circ}C$ to $125^{\circ}C$ unless otherwise specified

6.4.3 Power Monitor Electrical Characteristics

Table 3 Power Monitor Electrical Characteristics

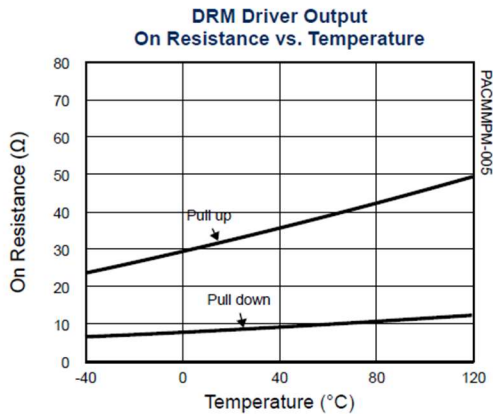
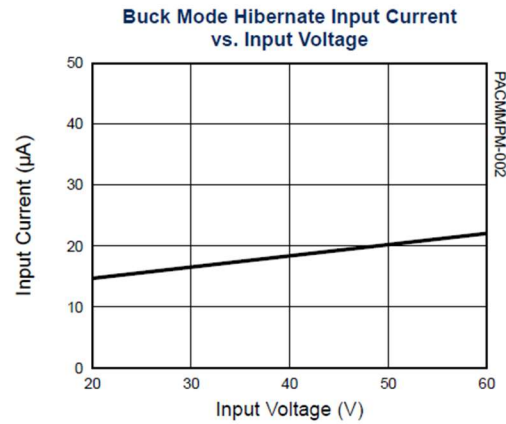
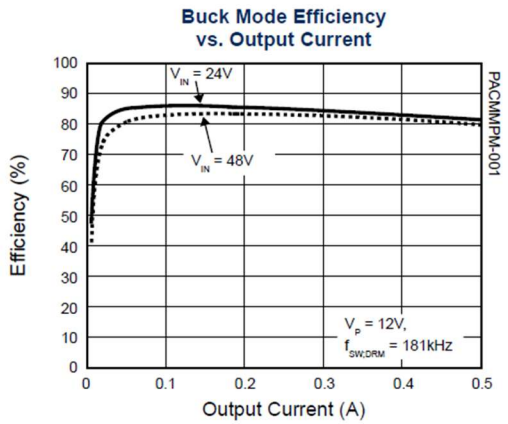
| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-------------------|--------------------------------------|--|-------|------|-------|-------|
| V _{REF} | Reference Voltage | T _A = 25°C | 2.487 | 2.5 | 2.513 | V |
| | | T _A = -40°C to 125°C | 2.463 | 2.5 | 2.537 | V |
| K _{MON} | Power Monitoring Voltage coefficient | V _{CORE} | | 1 | | V / V |
| | | V _{SYS} , V _{CCIO} , V _{CC33} | | 0.4 | | V / V |
| | | V _P , V _{REGO} | | 0.1 | | V / V |
| V _{TEMP} | Temperature monitor voltage | T _A = 25C, at ADC | 1.475 | 1.5 | 1.54 | V |
| K _{TEMP} | Temperature monitoring coefficient | At ADC | | 5.04 | | mV/K |

V_{HM} = 12V and T_A = -40°C to 125°C unless otherwise specified

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

6.5 Typical Performance Characteristics

VHM = 12V and $T_A = -40^{\circ}\text{C}$ to 125°C unless otherwise specified





PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

7 Configurable Analog Front-End (CAFE)

7.1 Features

- 3 Differential Programmable-Gain Amplifiers (DA)
- 4 Single-Ended Programmable-Gain Amplifiers (SA)
- 10 5V IO pins
- Over-Current Protection and Shutdown Comparators
- Power Monitoring
- Hibernate Push-Button Wake-up

7.2 System Block Diagram

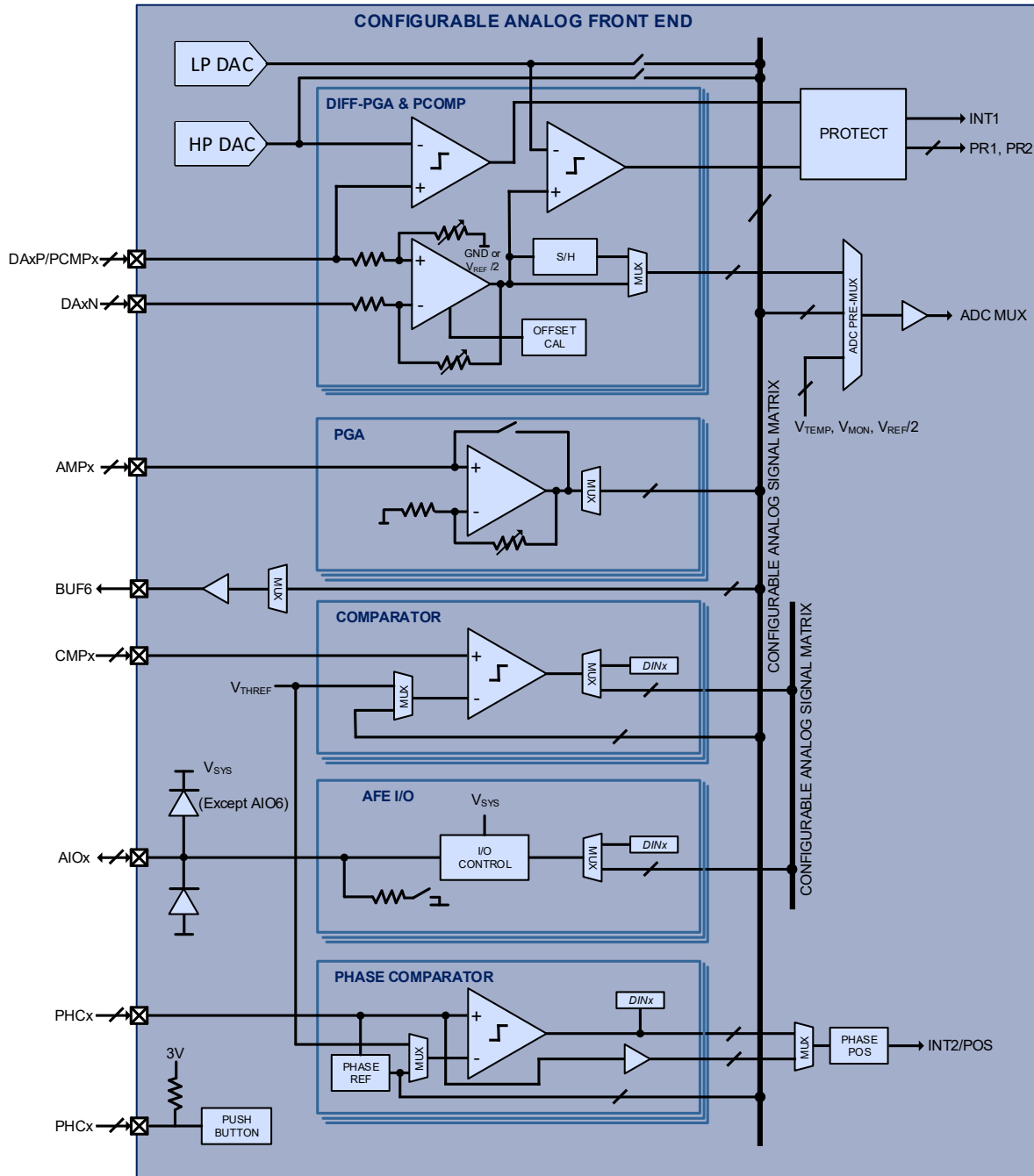


Figure 8 CAFE System Block Diagram

7.3 Functional Description

The device includes a Configurable Analog Front End™ that is accessible through 10 analog and I/O pins (AIO<9:0>). These pins can be configured to form flexible interconnected circuitry made up of 3 differential programmable gain amplifiers, 4 single-ended programmable gain amplifiers, 4 general purpose comparators, 3 phase comparators, 10 protection comparators, and one buffer output. These pins can also be programmed as analog feed-through pins, or as analog front end I/O pins that can function as digital inputs or digital open-drain outputs. The PAC proprietary configurable analog signal matrix (CASM) and configurable digital signal matrix (CDSM) allow real time asynchronous analog and digital signals to be routed in flexible circuit connections for different applications. A push-button function is provided for optional push button on, hibernate, and off power management function.

The CAFE also contains a power monitor MUX that allows all available power supplies to be sampled by the ADC for control and operation of the application.

7.3.1 Differential Programmable Gain Amplifier (DA)

The DAXP and DAXN pin pair are positive and negative inputs, respectively, to a differential programmable gain amplifier. The differential gain can be programmable to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x for zero-ohm signal source impedance. The differential programmable gain amplifier has -0.3V to 3.5V input common mode range, and its output can be configured for routing directly to the ADC pre-multiplexer, or through a sample-and-hold circuit synchronized with the ADC auto-sampling mechanism. Each differential amplifier is accompanied by offset calibration circuitry, and two protection comparators for protection event monitoring. The programmable gain differential amplifier is optimized for use with signal source impedance lower than 500Ω and with matched source impedance on both positive and negative inputs for minimal offset. The effective gain is scaled by $13.5k / (13.5k + R_{SOURCE})$, where R_{SOURCE} is the matched source impedance of each input.

7.3.2 Single-Ended Programmable Gain Amplifier (AMP)

Each AMPx input goes to a single-ended programmable gain amplifier with signal relative to V_{SS} . The amplifier gain can be programmed to be 1x, 2x, 4x, 8x, 16x, 32x, and 48x, or as analog feed-through. The programmable gain amplifier output is routed via a multiplexer to the configurable analog signal matrix CASM.

7.3.3 General-Purpose Comparator (CMP)

The general-purpose comparator takes the CMPx input and compares it to either the programmable threshold voltage (V_{THREF}) or a signal from the configurable analog signal matrix CASM. The comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed via a multiplexer to either a data input bit or the configurable digital signal matrix CDSM. Each general-purpose comparator has two mask bits to prevent or allow rising or falling edge of its output to trigger second microcontroller interrupt INT2, where INT2 can be configured to active protection event PR1.

7.3.4 Phase Comparator (PHC)

The phase comparator takes the PHCx input and compares it to either the programmable threshold voltage (V_{THREF}) or a signal from the configurable analog signal matrix CASM. The comparison signal can be set to a phase reference signal generated by averaging the PHCx input voltages. In a three-phase motor control application, the phase reference signal acts as a virtual center tap for BEMF detection. The PHCx inputs are optionally fed through to the CASM. The PHC inputs can be compared to the virtual center-tap, or phase to phase for the most efficient BEMF zero-cross detection. The phase comparators have configurable asymmetric hysteresis.

The phase comparator has 0V to V_{SYS} input common mode range, and its polarity-selectable output is routed to a data input bit and to the phase/position multiplexer synchronized with the auto-sampling sequencers.

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

7.3.5 Protection Comparator (PCMP)

Two protection comparators are provided in association with each differential programmable gain amplifier, with outputs available to trigger protection events and accessible as read-back output bits. The high-speed protection (HP) comparator compares the PCMPx pin to the 8-bit HP DAC output voltage, with full scale voltage of 2.5V. The limit protection (LP) comparator compares the differential programmable gain amplifier output to the 10-bit LP DAC output voltage, with full scale voltage of 2.5V.

Each protection comparator has a mask bit to prevent or allow it to trigger the main microcontroller interrupt INT1. Each protection comparator also has one mask bit to prevent or allow it to activate protection event PR1, and another mask bit to prevent or allow it to activate protection event PR2. These two protection events can be used directly by protection circuitry in the Application Specific Power Driver™ (ASPD) to protect devices being driven.

7.3.6 Analog Output Buffer (BUF)

A subset of the signals from the configurable analog signal matrix CASM can be multiplexed to the BUF6 pin for external use. The buffer offset voltage can be minimized with the built-in swap function.

7.3.7 Analog Front End I/O (AIO)

There are 10 AIOx pins that are available in the device. When the AIO pins are in I/O mode, the pin can be configured to be a digital input or digital open-drain output. The AIOx input or output signal can be set to a data input or output register bit or multiplexed to one of the signals in the configurable digital signal matrix CDSM. The signal can be set to active high (default) or active low, with V_{SYS} as the supply rail. AIO<9:6> support microcontroller interrupts for external signals. Each of these I/Os has two mask bits to prevent or allow rising or falling edge of its corresponding digital input to trigger second microcontroller interrupt INT2.

7.3.8 Push Button (PBTN)

AIO6 may be configured as a push-button input that is used to wake-up the PAC5524 when it is in hibernate mode. Before entering hibernate mode, the MCU can configure AIO6 to be a wake-up source to exit hibernate mode. When a high-to-low transition is observed on AIO6, the CAFE will wake-up the device.

In addition, the PBTN may be used as a hardware reset for the MCU when it is held low for longer than 8s during normal operation.

The PBTN input is active-low and a 55k resistor that is pulled-up to 3V. Pulling this signal to ground externally will raise the push-button event.

7.3.9 HP DAC and LP DAC

The 8-bit HP DAC can be used as the comparison voltage for the high-speed protection (HP) comparators or routed for general purpose use via the AB2 signal in the CASM. The HP DAC output full scale voltage is 2.5V.

The 10-bit LP DAC can be used as the comparison voltage for the limit protection (LP) comparators or routed for general purpose use via the AB3 signal in the CASM. The LP DAC output full scale voltage is 2.5V.

7.3.10 ADC Analog Input

The PAC5524 has several different analog input channels that may be used for analog-to-digital conversions using the MCU ADC. The diagram below shows the hierarchy of MUXes that are available for analog signal sampling.

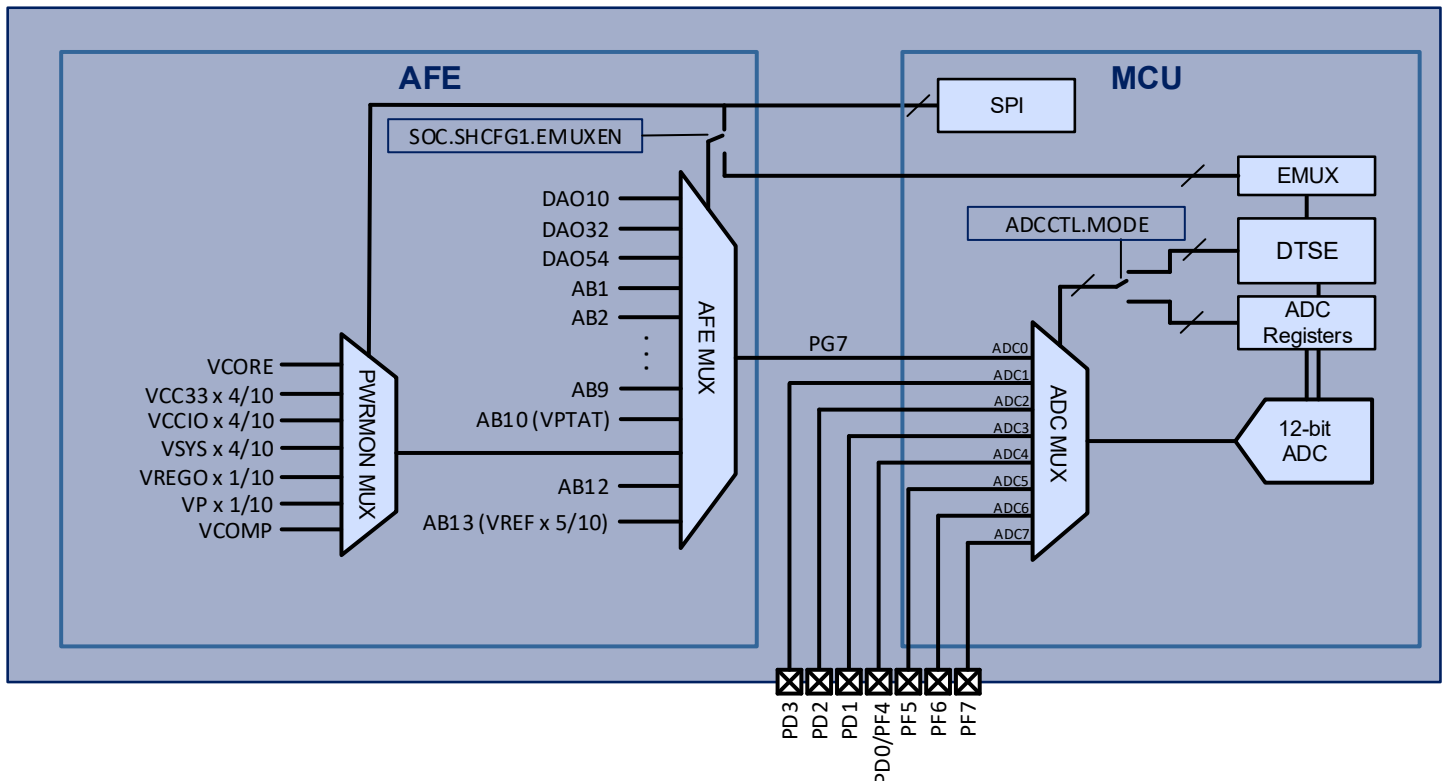


Figure 9 ADC Analog Input

The PAC5524 contains three analog MUXes as shown in the figure above:

- ADC MUX
- AFE MUX
- PWRMON MUX

The ADC MUX is an 8-channel MUX local to the ADC on the MCU that is directly controlled either by registers in the MCU, or automatically by the ADC DTSE. The output of the ADC MUX is sampled by the ADC. The ADC0 input to the ADC MUX is connected to the AFE MUX through the PG7 IO (which is internal to the device). ADC MUX input channels ADC1-ADC7 are directly connected to the pins on the PAC5524 on the IOs shown in the figure above

The AFE MUX is a 16-to-1 MUX that selects between the DA outputs, analog bus channels, voltage reference and the internal temperature sensor (VPTAT). This allows the ADC to rapidly sample the motor phase current, external voltage and temperature signals and the internal device temperature using the hardware sequencer on the device (DTSE).

The PWRMON MUX is a 8-to-1 MUX that selects between the power supply rails and comparator outputs. This MUX may be changed using the SPI bus by changing the MUX select register for this MUX.

For more information on controlling the various MUXes using the ADC and DTSE, see the PAC5524 User Guide.

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

7.3.11 Configurable Analog Signal Matrix (CASM)

The CASM has 12 general purpose analog signals labeled AB1 through AB12 that can be used for:

- Routing the single-ended programmable gain amplifier or analog feed-through output to AB1 through AB9
- Routing an analog signal via AB1, AB2, or AB3 to the negative input of a general-purpose comparator or phase comparator
- Routing the 8-bit HP DAC output to AB2
- Routing the 10-bit LP DAC output to AB3
- Routing analog signals via AB1 through AB12 to the ADC pre-multiplexer
- Routing phase comparator feed-through signals to AB7, AB8, and AB9, and averaged voltage to AB1

7.3.12 Configurable Digital Signal Matrix (CDSM)

The CDSM has 7 general purpose bi-directional digital signals labeled DB1 through DB7 that can be used for:

- Routing the AIOx input to or output signals from DB1 through DB7
- Routing the general-purpose comparator output signals to DB1 through DB7

7.3.13 Temperature Protection

The PAC5524 has two level of temperature protection. When the device reaches an internal temperature of 140°C, there is a mask-able interrupt that may be generated on IRQ1 to the MCU. The MCU may use this information to change the application behavior or disable the motor. The temperature warning status is cleared when the internal temperature falls below the temperature warning hysteresis threshold after the blanking time.

When the device reaches an internal temperature of 170C, the device will shut down all power supplies and gate drivers. The device will re-start when the internal temperature falls below the temperature fault hysteresis threshold after the blanking time.

7.4 Electrical Characteristics

The Electrical Characteristics for the CAFE are shown below.

7.4.1 Differential Programmable Gain Amplifier (DA)

Table 4 DA Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------------|---|--|------|------|-----------------|------------|
| $I_{CC,DA}$ | Operating supply current | Each enabled amplifier | | 150 | 300 | μ A |
| $V_{ICMR,DA}$ | Input common mode range | | -0.3 | | 3.5 | V |
| $V_{OLR,DA}$ | Output linear range | | 0.1 | | $V_{SYS} - 0.1$ | V |
| $V_{SHR,DA}$ | Sample and hold range | | 0.1 | | 3.5 | |
| $V_{OS,DA}$ | Input offset voltage | Gain = 48x, $V_{DAxP}=V_{DAxN}=0V$, $T_A=25^\circ C$ | -8 | | 8 | mV |
| $A_{VZI,DA}$ | Differential amplifier gain (zero ohm source impedance) | Gain = 1x | | 1 | | |
| | | Gain = 2x | | 2 | | |
| | | Gain = 4x | | 4 | | |
| | | Gain = 8x, $V_{DAxP}=V_{DAxN}=0V$, $T_A = 25^\circ C$ | | 8 | | |
| | | | -2 | | 2 | % |
| | | Gain = 16x | | 16 | | |
| | | Gain = 32x | | 32 | | |
| $K_{CMRR,DA}$ | Common mode rejection ratio | Gain = 8x, $V_{DAxP}=V_{DAxN}=0V$, $T_A = 25^\circ C$ | | 55 | | dB |
| $R_{INDIF,DA}$ | Differential input impedance | | | 27 | | k Ω |
| | Slew rate ¹ | Gain = 8x | 7 | 10 | | V/ μ s |
| $t_{ST,DA}$ | Settling time ¹ | To 1% of final value | | 200 | 400 | ns |

$T_A = -40^\circ C$ to $125^\circ C$ unless otherwise specified

¹ Guaranteed by design

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

7.4.2 Single-Ended Programmable Gain Amplifier (SA)

Table 5 SA Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------------|----------------------------|--|------|------|-----------------|------------|
| $I_{CC,AMP}$ | Operating supply current | Each enabled amplifier | | 80 | 140 | μA |
| $V_{ICMR,AMP}$ | Input common mode range | | 0 | | V_{SYS} | V |
| $V_{OLR,AMP}$ | Output linear range | | 0.1 | | $V_{SYS} - 0.1$ | V |
| $V_{OS,AMP}$ | Input offset voltage | Gain = 1x, $T_A=25^\circ C$, $V_{AMPX}=2.5V$ | -10 | | 10 | mV |
| $A_{V,AMP}$ | Amplifier gain | Gain = 1x | | 1 | | |
| | | Gain = 2x | | 2 | | |
| | | Gain = 4x | | 4 | | |
| | | Gain = 8x, $V_{AMPX}=125mV$, $T_A = 25^\circ C$ | -2 | | 2 | % |
| | | Gain = 16x | | 16 | | |
| | | Gain = 32x | | 32 | | |
| | | Gain = 48x | | 48 | | |
| $I_{IN,AMP}$ | Input current | | | 0 | 1 | μA |
| | Slew rate ² | Gain = 8x | 8 | 12 | | V/ μs |
| $t_{ST,AMP}$ | Settling time ² | To 1% of final value | | 150 | 300 | ns |

$T_A = -40^\circ C$ to $125^\circ C$ unless otherwise specified

7.4.3 General Purpose Comparator (CMP)

Table 6 CMP Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------------|-------------------------------|------------------------------------|------|------|-----------|---------|
| $I_{CC,CMP}$ | Operating supply current | Each enabled amplifier | | 35 | 110 | μA |
| $V_{ICMR,CMP}$ | Input common mode range | | 0 | | V_{SYS} | V |
| $V_{OS,CMP}$ | Input offset voltage | $V_{CMPX}=2.5V$, $T_A=25^\circ C$ | -10 | | 10 | mV |
| $V_{HYS,CMP}$ | Hysteresis | | | 20 | | mV |
| $I_{IN,CMP}$ | Input current | | | 0 | 1 | μA |
| $t_{DEL,CMP}$ | Comparator delay ² | | | | 100 | ns |

$T_A = -40^\circ C$ to $125^\circ C$ unless otherwise specified.

² Guaranteed by design



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

7.4.4 Phase Comparator (PHC)

Table 7 PHC Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-----------------------|-------------------------------|--|------|------|------------------|-------|
| I _{CC,PHC} | Operating supply current | Each enabled amplifier | | 35 | 110 | μA |
| V _{ICMR,PHC} | Input common mode range | | 0 | | V _{sys} | V |
| V _{OS,PHC} | Input offset voltage | V _{PCMPx} =2.5V, T _A =25°C | -10 | | 10 | mV |
| V _{HYS,PHC} | Hysteresis | | | 20 | | mV |
| I _{IN,PHC} | Input current | | | 0 | 1 | μA |
| t _{DEL,PHC} | Comparator delay ³ | | | | 100 | ns |

T_A = -40°C to 125°C unless otherwise specified.

7.4.5 Protection Comparator (PCMP)

Table 8 PCMP Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|------------------------|-------------------------------|--|------|------|---------------------|-------|
| I _{CC,PCMP} | Operating supply current | Each enabled comparator | | 35 | 100 | μA |
| V _{ICMR,PCMP} | Input common mode range | | 0.3 | | V _{sys} -1 | V |
| V _{OS,PCMP} | Input offset voltage | V _{PCMPx} =2.5V, T _A =25°C | -10 | | 10 | mV |
| V _{HYS,PCMP} | Hysteresis | | | 20 | | mV |
| I _{IN,PCMP} | Input current | | | 0 | 1 | μA |
| t _{DEL,PCMP} | Comparator delay ¹ | | | | 100 | ns |

T_A = -40°C to 125°C unless otherwise specified.

7.4.6 Analog Output Buffer (BUF)

Table 9 BUF Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-----------------------|--------------------------|--|------|------|------|-------|
| I _{CC,BUF} | Operating supply current | No load | | 35 | 100 | μA |
| V _{ICMR,BUF} | Input common mode range | | 0 | | 3.5 | V |
| V _{OLR,AMP} | Output linear range | | 0.1 | | 3.5 | V |
| V _{OS,BUF} | Offset voltage | V _{BUF} = 2.5V, T _A = 25°C | -18 | | 18 | mV |
| I _{OMAX} | Maximum output current | C _L = 0.1nF | 0.8 | 1.3 | | mA |

T_A = -40°C to 125°C unless otherwise specified.

³ Guaranteed by design

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

7.4.7 Analog Front End (AIO) Electrical Characteristics

Table 10 AIO Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---------------------|-----------------------------------|--|------|------|------|-------|
| V _{AIO} | Pin voltage range | | 0 | | 5 | V |
| V _{IH;AIO} | High-level input voltage | | 2.2 | | | V |
| V _{IL;AIO} | Low-level input voltage | | | | 0.8 | V |
| R _{PD;AIO} | Pull-down resistance | Input mode | 0.5 | 1 | 1.8 | MΩ |
| V _{OL;AIO} | Low-level output voltage | I _{AIO<9,7,3,1>=7mA} , open-drain output mode | | | 0.4 | V |
| | | I _{AIO<6,0>=7mA} , open-drain output mode | | | 0.5 | |
| I _{OL;AIO} | Low-level output sink current | V _{AIOx} = 0.4V, open-drain output mode | 6 | 14 | | mA |
| I _{LK;AIO} | High-level output leakage current | V _{AIOx} = 5V, open-drain output mode | | 0 | 10 | μA |

T_A = -40°C to 125°C unless otherwise specified

7.4.8 Push-Button (PBTN) Electrical Characteristics

Table 11 PBTN Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------------------|--------------------------|-------------------------------|------|------|------|-------|
| V _{I;PBTN} | Input voltage range | | 0 | | 5 | V |
| V _{IH;PBTN} | High-level input voltage | | 2 | | | V |
| V _{IL;PBTN} | Low-level input voltage | | | | 0.35 | V |
| R _{PU;PBTN} | Pull-up resistance | To 3V, push-button input mode | 40 | 55 | 95 | kΩ |

T_A = -40°C to 125°C unless otherwise specified

7.4.9 HP DAC and LP DAC Electrical Characteristics

Table 12 HPDAC and LPDAC Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---------------------|--------------------------------|---------------------------------|-------|------|-------|-------|
| V _{DACREF} | DAC reference voltage | T _A = 25°C | 2.48 | 2.5 | 2.52 | V |
| | | T _A = -40°C to 125°C | 2.453 | 2.5 | 2.547 | |
| | HP 8-bit DAC INL ⁴ | | -1 | | 1 | LSB |
| | HP 8-bit DAC DNL ⁴ | | -0.5 | | 0.5 | LSB |
| | LP 10-bit DAC INL ⁴ | | -2 | | 2 | LSB |
| | LP 10-bit DAC DNL ⁴ | | -1 | | 1 | LSB |

T_A = -40°C to 125°C unless otherwise specified

⁴ Guaranteed by design



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

7.4.10 Temperature Protection Electrical Characteristics

Table 13 PBTN Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|--------------------------------|------------|------|------|------|-------|
| T _{WARN} | Temperature warning threshold | | | 140 | | °C |
| T _{WARN;HYS} | Temperature warning hysteresis | | | 10 | | °C |
| T _{WARN;BLANK} | Temperature warning blanking | | | 10 | | μs |
| T _{FAULT} | Temperature fault threshold | | | 165 | | °C |
| T _{FAULT;HYS} | Temperature fault hysteresis | | | 10 | | °C |
| T _{FAULT;BLANK} | Temperature fault blanking | | | 10 | | μs |

7.5 Typical Performance Characteristics

(T_A = -25°C unless otherwise specified)

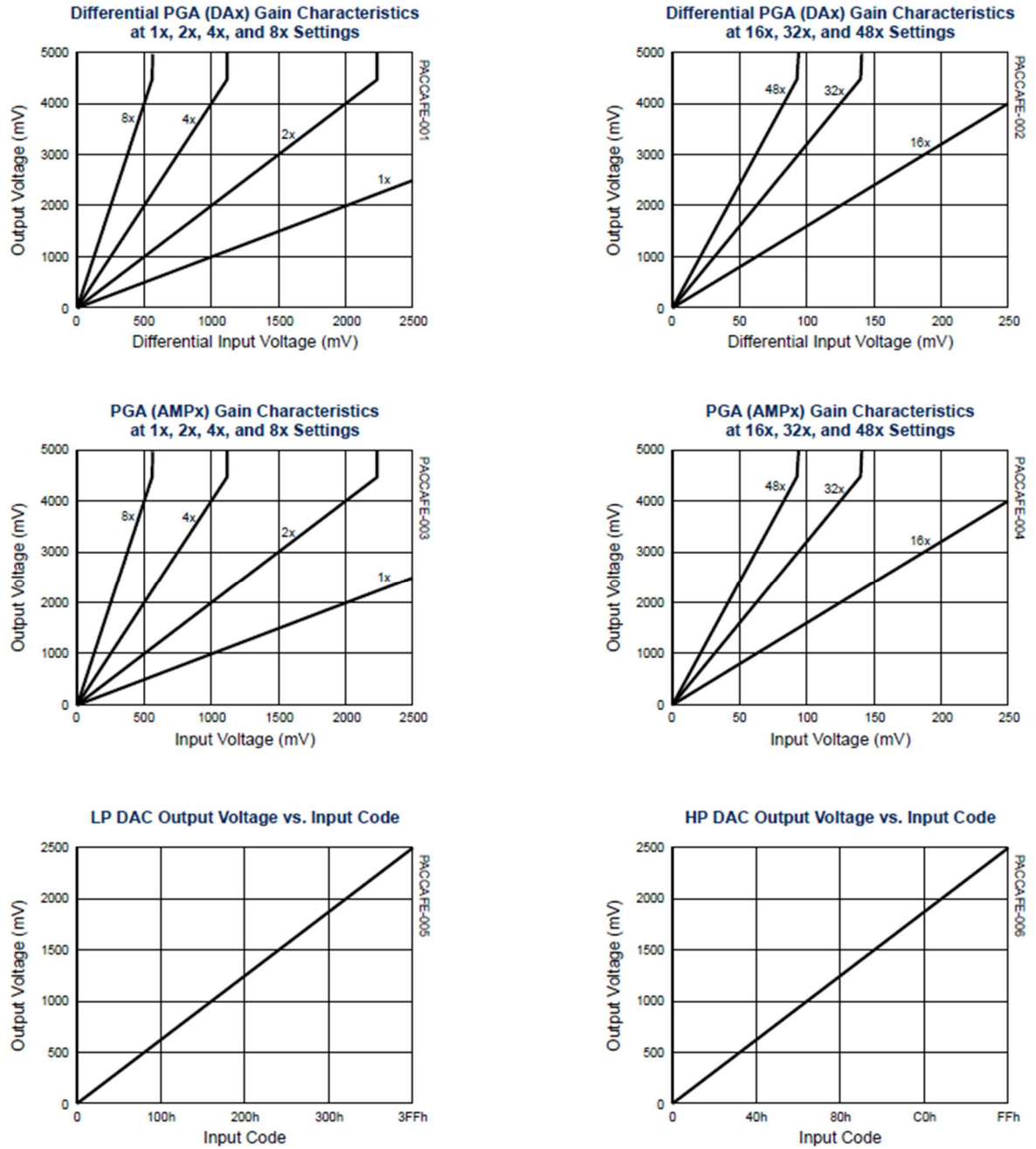


Figure 10 PGA Typical Performance Characteristics

8 Application Specific Power Drivers (ASPD)

8.1 Features

- 3 low-side and 3 high-side gate drivers
- 1.5A gate driving capability
- Break-before-make Dead-Time Enforcement
- OC, UV and OV Protection

8.2 System Block Diagram

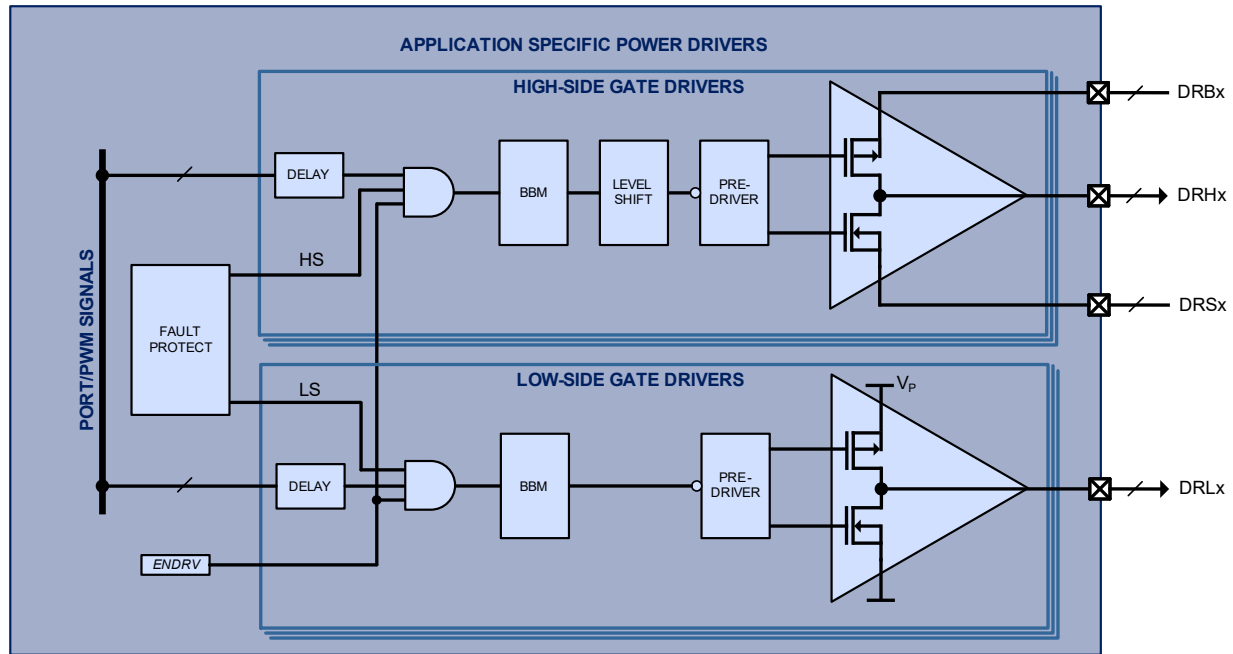


Figure 11 ASPD System Block Diagram

8.3 Functional Description

The Application Specific Power Drivers™ (ASPD) module handles power driving for power and motor control applications. The ASPD contains three low-side gate drivers (DRLx), three high-side gate drivers (DRHx). Each gate driver can drive an external MOSFET or IGBT switch in response to high-speed control signals from the microcontroller ports, and a pair of high-side and low-side gate drivers can form a half-bridge driver.

The ASPD includes built-in configurable fault protection for the internal gate drivers.

The figure below shows typical gate driver connections. The ASPD gate drivers support up to a 70V supply.

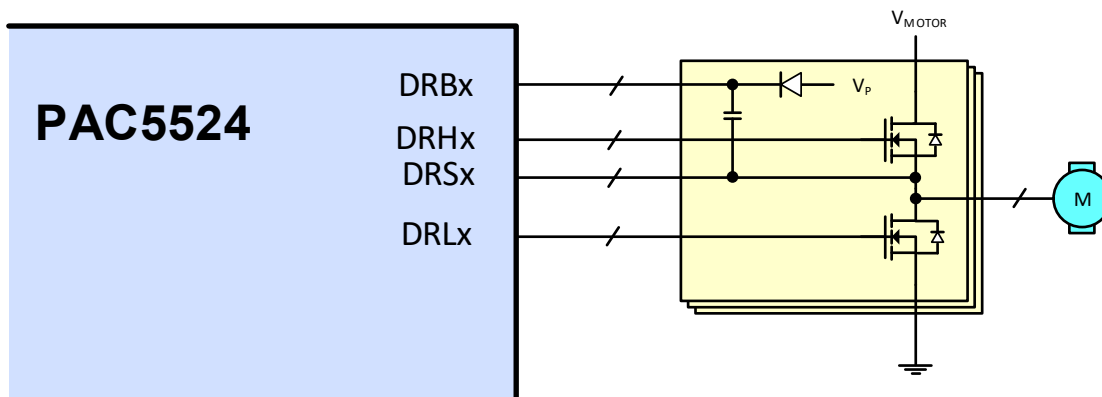


Figure 12 Typical Gate Driver Connections

8.4 Low-Side Gate Drivers

The DRLx low-side gate driver drives the gate of an external MOSFET or IGBT switch between the low-level power ground rail and high-level VP supply rail. The DRLx output pin has sink and source output current capability of 1.5A. Each low-side gate driver is controlled by a microcontroller port signal with 4 configurable levels of propagation delay.

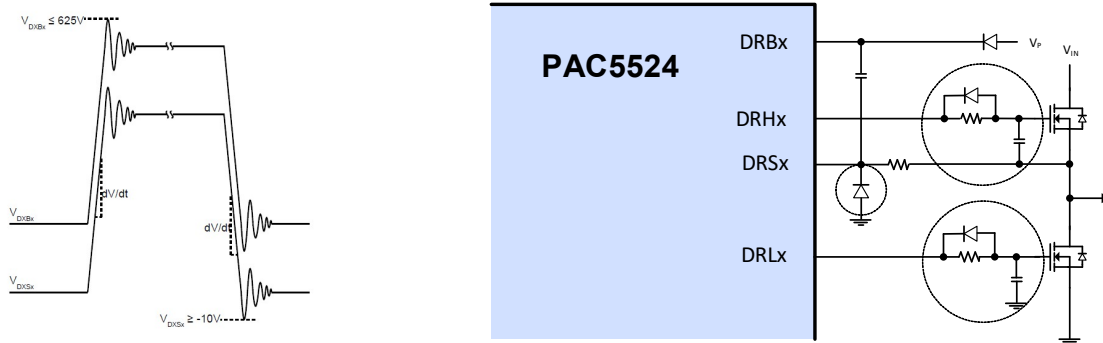
8.5 High-Side Gate Drivers

The DRHx high-side gate driver drives the gate of an external MOSFET or IGBT switch between its low-level DRSx driver source rail and its high-level DRBx bootstrap rail. The DRSx pin can go up to 70V steady state. The DRHx output pin has sink and source output current capability of 1.5A. The DRBx bootstrap pin can have a maximum operating voltage of 16V relative to the DRSx pin, and up to 82V steady state. The DRSx pin is designed to tolerate momentary switching negative spikes down to -5V without affecting the DRHx output state. Each high-side gate driver is controlled by a microcontroller port signal with 4 configurable levels of propagation delay.

For bootstrapped high-side operation, connect an appropriate capacitor between DRBx and DRSx and a properly rated bootstrap diode from VP to DRBx. To operate the DRHx output as a low-side gate driver, connect its DRBx pin to VP and its DRSx pin to VSS.

8.6 High-Side Switching Transients

Typical high-side switching transients are shown below. To ensure functionality and reliability, the DRSx and DRBx pins must not exceed the peak and undershoot limit values shown. This should be verified by probing the DRBx and DRSx pins directly relative to VSS pin. A small resistor and diode clamp for the DRSx pin can be used to make sure that the pin voltage stays within the negative limit value. In addition, the high-side slew rate dV/dt must be kept within $\pm 5V/ns$ for DRSx. This can be achieved by adding a resistor-diode pair in series, and an optional capacitor in parallel with the power switch gate. The parallel capacitor also provides a low impedance and close gate shunt against coupling from the switch drain. These optional protections and slew rate control are shown in the figure below.



(a) High-Side Switching Transients

(b) Optional Transient Protection and Slew Rate Control

Figure 13 High-Side Switching Transients and Optional Circuitry

8.7 Power Drivers Control

All power drivers are initially disabled from power-on-reset. To enable the power drivers, the microprocessor must first set the driver enable bit to '1'. The gate drivers are controlled by the microcontroller ports and/or PWM signals as shown in **Error! Reference source not found.** The drivers have configurable delays as shown in Table 14 Power Driver Delay Configuration. Refer to the PAC application notes and user guide for additional information on power drivers control programming.

Table 14 Power Driver Delay Configuration

| Delay Setting | DRLx | | DRHx | |
|---------------|--------|---------|--------|---------|
| | Rising | Falling | Rising | Falling |
| 00b | 130ns | 140ns | 160ns | 140ns |
| 01b | 170ns | 180ns | 200ns | 180ns |
| 10b | 230ns | 250ns | 260ns | 240ns |
| 11b | 360ns | 380ns | 380ns | 370ns |



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

8.8 Gate Driver Fault Protection

The ASPD incorporates a configurable fault protection mechanism using protection signal from the Configurable Analog Front End (CAFE), designated as protection event 1 (PR1) signal. The DRL0/DRL1/DRL2 drivers are designated as low-side group 1. The DRH3/DRH4/DRH5 gate drivers are designated as high-side group 1. The PR1 signal from the CAFE can be used to disable low-side group 1, high-side group 1, or both depending on the PR1 mask bit settings.

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

8.9 Electrical Characteristics

The Electrical Characteristics for the ASPD are shown below.

8.9.1 Low-Side Gate Drivers

Table 15 Low-Side Gate Drivers Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------------|---------------------------------------|---------------------------|-----------|------------|------|-------|
| $V_{OH;DRL}$ | High-level output voltage | $I_{DRLx} = -50\text{mA}$ | $V_P-0.5$ | $V_P-0.25$ | | V |
| $V_{OL;DRL}$ | Low-level output voltage | $I_{DRLx} = 50\text{mA}$ | | 0.175 | 0.35 | V |
| $I_{OHPK;DRL}$ | High-level pulsed peak source current | 10 μs pulse | | -1.5 | | A |
| $I_{OLPK;DRL}$ | Low-level pulsed peak sink current | 10 μs pulse | | 1.5 | | A |

$V_P = 12\text{V}$ and $T_A = -40^\circ\text{C}$ to 125°C unless otherwise specified

8.9.2 High-Side Gate Drivers

Table 16 High-Side Gate Drivers Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------------|---|--|----------------|------------------|-----------------|---------------|
| V_{DRS} | Level-shift driver source voltage range | Repetitive, 10 μs pulse | -5 | | 71 | V |
| | | Steady state | 0 | | 66 | V |
| V_{DRB} | Bootstrap pin voltage range | Repetitive, 10 μs pulse | 3 | | 83 | V |
| | | Steady state | 5.2 | | 78 | V |
| $V_{BS;DRB}$ | Bootstrap supply voltage range | V_{DRBx} , relative to respective V_{DRSx} | 5.2 | | 16 | V |
| $V_{UVLO;DRB}$ | Bootstrap UVLO threshold | V_{DRBx} rising, relative to respective V_{DRSx} , hysteresis = 1V | | 3.5 | 4.5 | V |
| $I_{BS;DRB}$ | Bootstrap circuit supply current | Gate Driver Disabled | | 23 | 35 | μA |
| | | Gate Driver Enabled | | 30 | 45 | |
| $I_{OS;DRB}$ | Offset supply current | Gate Driver Disabled | | 0.5 | 10 | μA |
| | | Gate Driver Enabled | | 0.5 | 10 | |
| $V_{OH;DRH}$ | High-Level output voltage | $I_{DRHx} = -50\text{mA}$ | $V_{DRBx}-0.6$ | $V_{DRBx}-0.2$ | | V |
| $V_{OL;DRH}$ | Low-level output voltage | $I_{DRHx} = 50\text{mA}$ | | $V_{DRSx}+0.175$ | $V_{DRSx}+0.35$ | V |
| $I_{OHPK;DRH}$ | High-level pulsed peak source current | 10 μs pulse | | -1.5 | | A |
| $I_{OLPK;DRL}$ | Low-level pulsed peak sink current | 10 μs pulse | | 1.5 | | A |

$V_P = 12\text{V}$ and $T_A = -40^\circ\text{C}$ to 125°C unless otherwise specified

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

8.9.3 High-Side and Low-Side Gate Driver Propagation Delay

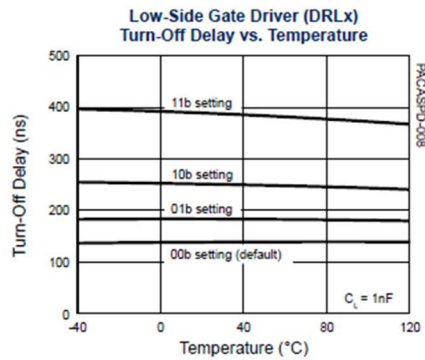
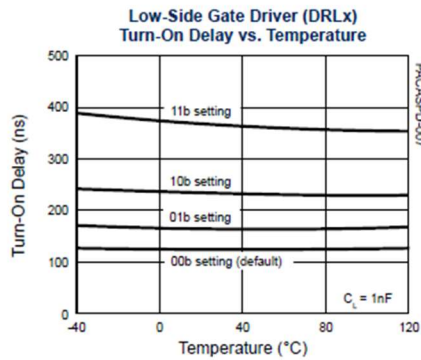
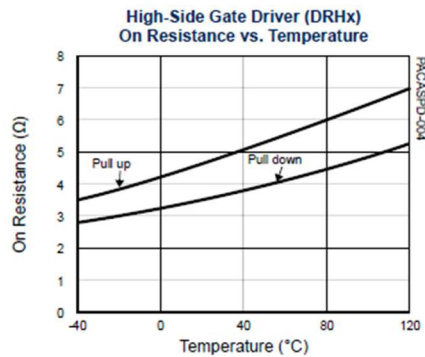
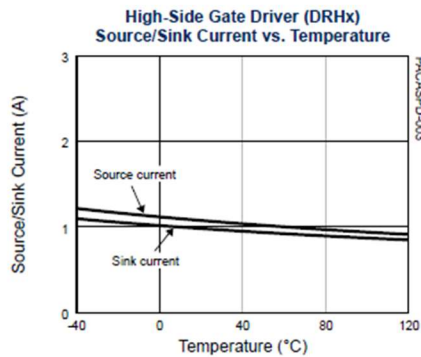
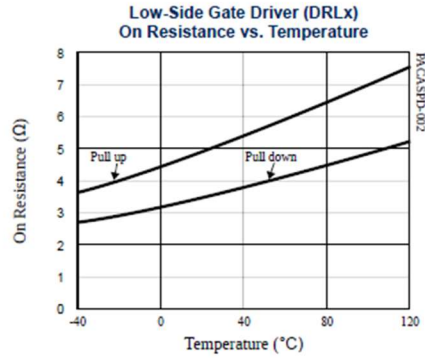
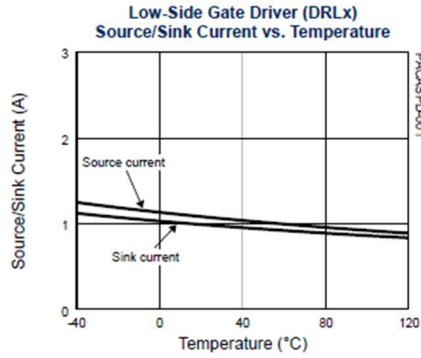
Table 17 Gate Driver Propagation Delay Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------|-------------------|-------------------|------|------|------|-------|
| t_{PD} | Propagation Delay | Delay setting 00b | | 10 | | ns |
| | | Delay setting 01b | | 50 | | ns |
| | | Delay setting 10b | | 120 | | ns |
| | | Delay setting 11b | | 250 | | ns |

$V_P = 12V$ and $T_A = -40^{\circ}C$ to $125^{\circ}C$ unless otherwise specified

8.10 Typical Performance Characteristics

(VP = 12V and TA = -25°C unless otherwise specified)



High Pin-Count 70V Motor Controller and Driver for BLDC Motors

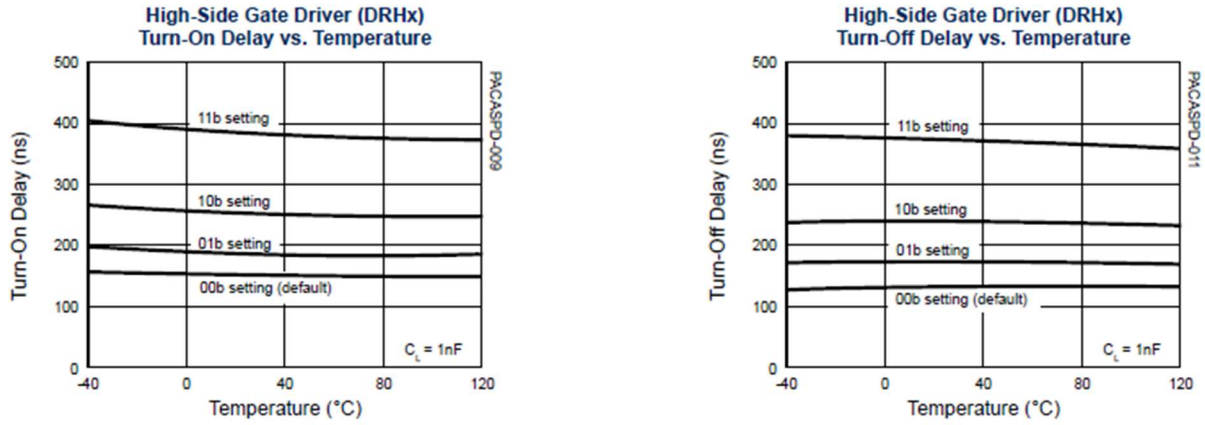


Figure 14 ASPD Gate Driver Typical Performance Characteristics

9 SOC Control Signals

The MCU has access to the Analog Sub-system on the PAC5524 through certain digital peripherals. The functions that the MCU may access from the Analog Sub-System are:

- High-side and Low-side Gate Drivers
- SPI Interface for Analog Register Access
- ADC EMUX
- Analog Sub-system Interrupts

9.1 High-side and Low-Side Gate Drivers

The high-side and low-side gate drivers on the PAC5524 are controlled by PWM outputs of the timer peripherals on the MCU. The timer peripheral generates the PWM output. The PWM timer may be configured to generate a complementary PWM output (high-side and low-side gate drive signals) with hardware controlled dead-time.

These signals are sent to the gate drivers in the Analog Sub-system that create the high and low side gate drivers for the external inverter.

The user may choose to enable or not enable the DTG (Dead-time Generator). The diagram below shows the block diagram of the PWM timer, DTG and ASPD gate drivers.

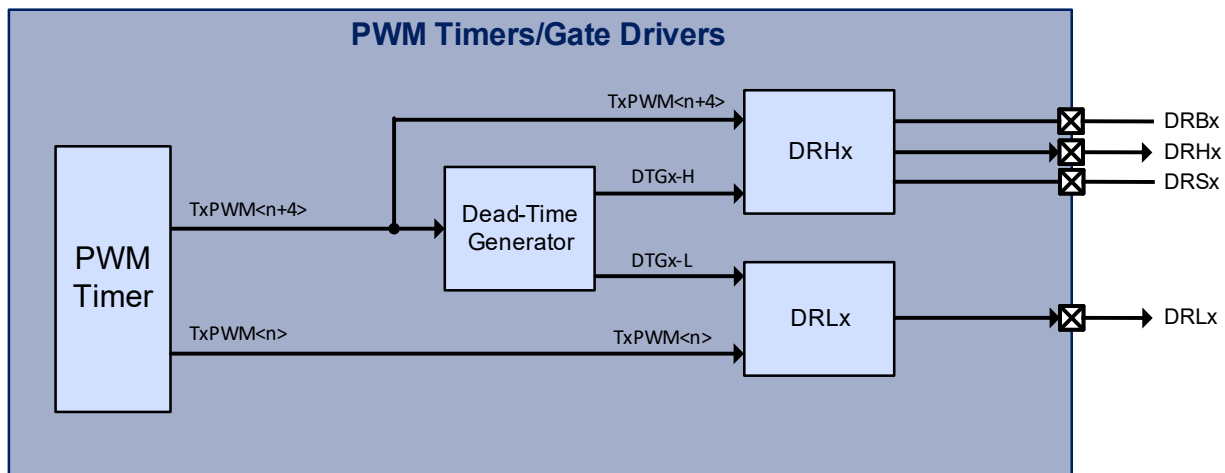


Figure 15 SOC Signals for Gate Drivers

Each timer peripheral that drives the DTG and ASPD Gate Drivers has two PWM outputs that are connected to the gate drivers: $TxPWM<n>$ and $TxPWM<n+4>$. If the Dead-Time Generator is disabled $TxPWM<n>$ is connected to the DRLx gate driver output and $TxPWM<n+4>$ is connected to the DRHx gate driver output.

If the DTG is enabled, the $TxPWM<n+4>$ is used to generate the complementary high-side and low-side output ($DTGx-H$ and $DTGx-L$). $DTGx-H$ is connected to the DRHx output and $DTGx-L$ is connected to the DRLx output.

The MCU allows flexibility the assignment of PWM outputs to ASPD gate drivers. The tables below shows which PWM outputs are available for each gate driver.



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

For applications that drive half-bridge or full-bridge topologies, the DTG will be enabled to allow a complementary output with dead-time insertion.

Table 18 PWM to ASPD Gate Driver Options (DTG Enabled)

| Gate Driver | PWM Input Options |
|-------------|--|
| DRH3/DRL0 | TAPWM4 TBPWM4 TCPWM0 TCPWM4 TDPWM4 |
| DRH4/DRL1 | TAPWM5 TBPWM5 TCPWM1 TCPWM5 TDPWM5 |
| DRH5/DRL2 | TAPWM6 TBPWM6 TCPWM2 TCPWM6 TDPWM6 |



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

For applications that are not driving half-bridge topologies, the DTG is disabled and the PWM outputs are directly connected to the gate drivers.

Table 19 PWM to ASPD Gate Driver Options (DTG Enabled)

| Gate Driver | PWM Input Options |
|-------------|--|
| DRH3 | TAPWM4 TBPWM4 TCPWM0 TCPWM4 TDPWM4 |
| DRH4 | TAPWM5 TBPWM5 TCPWM1 TCPWM5 TDPWM5 |
| DRH5 | TAPWM6 TBPWM6 TCPWM2 TCPWM6 TDPWM6 |
| DRL0 | TAPWM0 TBPWM0 TCPWM0 TDPWM0 |
| DRL1 | TAPWM1 TBPWM1 TCPWM1 TDPWM1 |
| DRL2 | TAPWM2 TBPWM2 TCPWM2 TDPWM2 |

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

9.2 SPI SOC Bus

The SPI SOC bus is used for reading and writing registers in the Analog Sub-System. The PAC5524 allows both USARTA and USARTB to be used as the SPI master to read and write registers in the Analog Sub-System.

The table below shows which peripherals and which IO pins should be used for this interface.

Table 20 SPI SOC Bus Connections

| SPI Signal | USART Signal | IO Pin |
|------------|--------------|--------|
| SCLK | USASCLK | PA3 |
| | USBCLK | PA3 |
| MOSI | USAMOSI | PA4 |
| | USBMOSI | PA4 |
| MISO | USAMISO | PA5 |
| | USBMISO | PA5 |
| SS | USASS | PA6 |
| | USBSS | PA6 |

9.3 ADC EMUX

The ADC EMUX is a write-only serial bus that the ADC DTSE uses for instructing the CAFE to perform MUX changes, activate Sample and Hold, etc.

The table below shows the MCU pins that are used by the ADC EMUX in the PAC5524.

Table 21 ADC EMUX SOC Bus Connections

| SPI Signal | USART Signal | IO Pin |
|------------|--------------|--------|
| SCLK | USASCLK | PA3 |
| | USBCLK | PA3 |

9.4 Analog Interrupts

The Analog sub-system has two interrupts that it can generate for different conditions. The table below shows the two different interrupts, the interrupt conditions and the IO pin that the interrupts are connected to.

Table 22 Analog Interrupt SOC Bus Connections

| SPI Signal | USART Signal | IO Pin |
|------------|--|--------|
| nIRQ1 | HPCOMP/LPCOMP Comparator Protection for Over-current and Over-Voltage events | PA7 |
| nIRQ2 | BEMF and Special Mode Comparator, including phase to phase comparator, AIO6/AIO7/AIO8/AIO9 interrupt | PA0 |

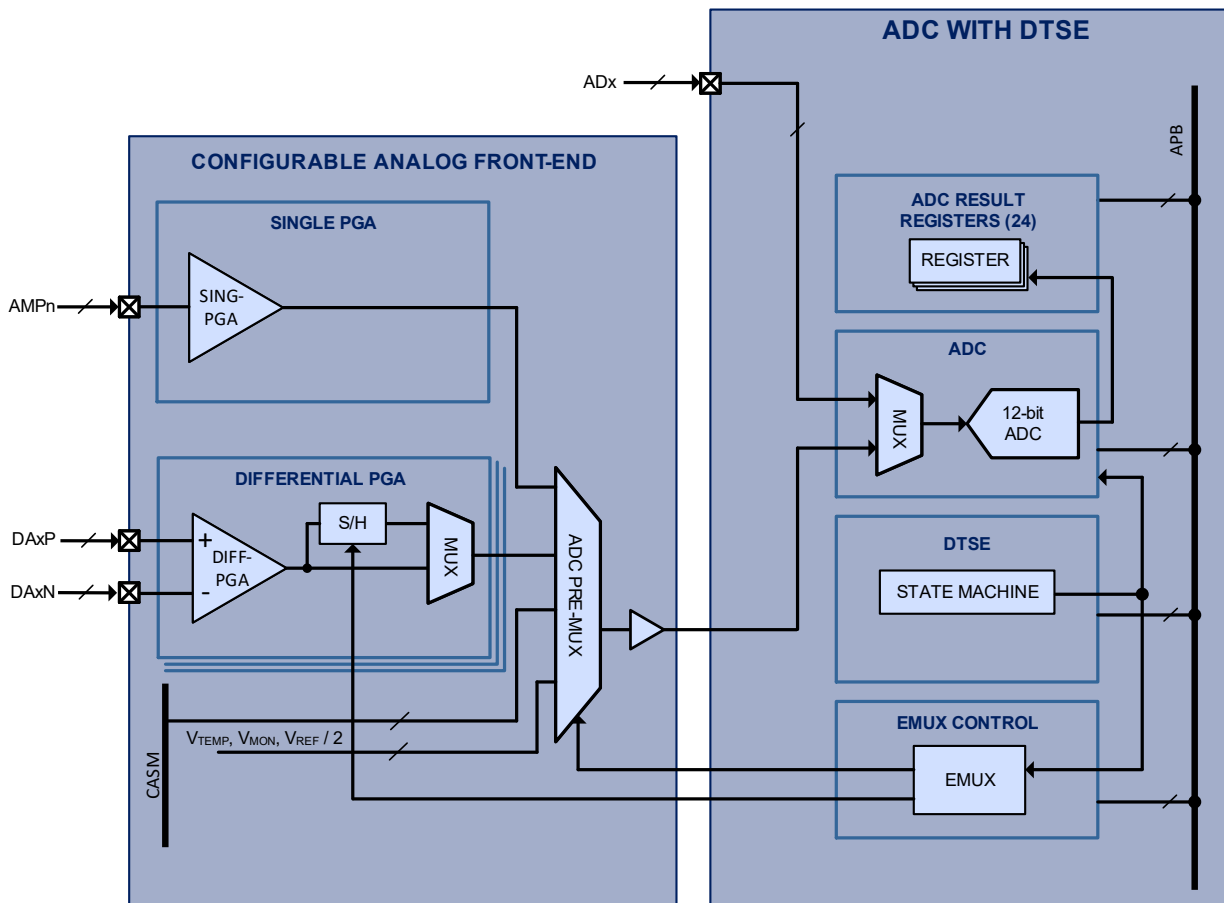
10 ADC/DTSE

10.1 Features

- 10-bit 1MSPS SAR ADC
- Configurable Dynamic Triggering and Sequence Engine (DTSE)
- High-speed sample and hold for current measurement
- Current, power and temperature monitoring using DTSE

10.2 System Block Diagram

Figure 16 ADC/DTSE System Block Diagram



10.3 Functional Description

10.3.1 ADC

The analog-to-digital converter (ADC) is a 12-bit successive approximation register (SAR) ADC with 400ns conversion time and up to 2.5 MSPS capability. The integrated analog multiplexer allows selection from up to 8 direct ADx inputs, and from up to 10 analog inputs signals in the Configurable Analog Front End (CAFE), including up to 3 differential input pairs as well as temperature and $V_{REF} / 2$.

The ADC contains a power down mode, and the user may configure the ADC to interrupt the MCU for the completion of a conversion when in manual mode. The ADC may be configured for either repeating or non-repeating conversions or conversion sequences.

10.3.2 Dynamic Triggering and Sample Engine (DTSE)

The Dynamic Triggering and Sample Engine (DTSE) is a highly-configurable automatic sequencer that allows the user to configure automatic sampling of their application-specific analog signals without any interaction from the micro-controller core. The DTSE also contains a pseudo-DMA engine that copies each of up to 24 conversion results to dedicated memory space and can interrupt the MCU when complete.

The DTSE has up to 32 input triggers, from PWM Timers A, B, C and D for either the rising, falling or rising and falling PWM edges. The user may also force any trigger sequence by writing a register via firmware. The user can configure the DTSE to chain from 1 to 24 conversions to any PWM trigger.

The DTSE has a flexible interrupt structure that allows up to 24 interrupts to be configured at the completion of any individual conversion. The user may configure one of four different IRQ signals when generating an interrupt during sequence conversions. The IRQ may be generated at the end of a conversion sequence, or at the end of a series of conversions. The user may select one of four IRQs for conversions, and each may be assigned a different interrupt priority.

Each of the 24 conversions has dedicated results registers, so that the pseudo-DMA engine has dedicated storage for each of the conversion results.

10.3.3 EMUX Control

A dedicated low latency interface controllable by the DTSE or register control allows changing the ADC pre-multiplexer and asserting/de-asserting the S/H circuit in the Configurable Analog Front-End (CAFE), allowing back to back conversions of multiple analog inputs without microcontroller interaction.

For more information on the ADC and DTSE, see the PAC55XX Family User Guide.

10.4 Electrical Characteristics

The Electrical Characteristics for the ADC and DTSE are shown below.

Table 23 ADC/DTSE Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|------------------------------|--------------------------------------|--|------|------------|------|--------|
| f_{ADCCLK} | ADC conversion clock input | | | | 40 | MHz |
| $f_{ADCCONV}$ | ADC conversion time | $f_{ADCCLK} = 40\text{MHz};$ PCx, PDx, PEx, PFx, PGx pins | | | 16 | ADCCLK |
| | | | | | 400 | ns |
| $t_{ADC;SH}$ t_{ADCSH} | ADC sample and hold time | $f_{ADCCLK} = 40\text{MHz};$ AIO[9:0] pins | | | 800 | ns |
| | ADC sample and hold time | | | | 100 | ns |
| $t_{ADC;CVT}$ C_{ADCIC} | ADC analog conversion time | ADC MUX input | | | 4 | ADCCLK |
| | ADC input capacitance | | | 1 | | pF |
| | ADC resolution | | | 12 | | bits |
| | ADC effective resolution | | 10.5 | | | bits |
| | ADC differential non-linearity (DNL) | $F_{ADCCLK} = 25\text{MHz}$ | | ± 0.5 | | LSB |
| | ADC resolution | $F_{ADCCLK} = 40\text{MHz}$ | | ± 0.75 | | LSB |
| | ADC integral non-linearity (INL) | $F_{ADCCLK} = 25\text{MHz}$ | | ± 0.5 | | LSB |
| | ADC differential non-linearity (DNL) | $F_{ADCCLK} = 40\text{MHz}$ | | ± 0.75 | | LSB |
| | ADC offset error | | | 0.6 | | %FS |
| | ADC gain error | | | 0.12 | | %FS |
| V_{REFADC} | ADC reference input voltage | $V_{REF} = 2.5\text{V}$ | | 2.5 | | V |
| $f_{EMUXCLK}$ | EMUX engine clock input | | | | 50 | MHz |

$T_A = -40^\circ\text{C}$ to 125°C unless otherwise specified

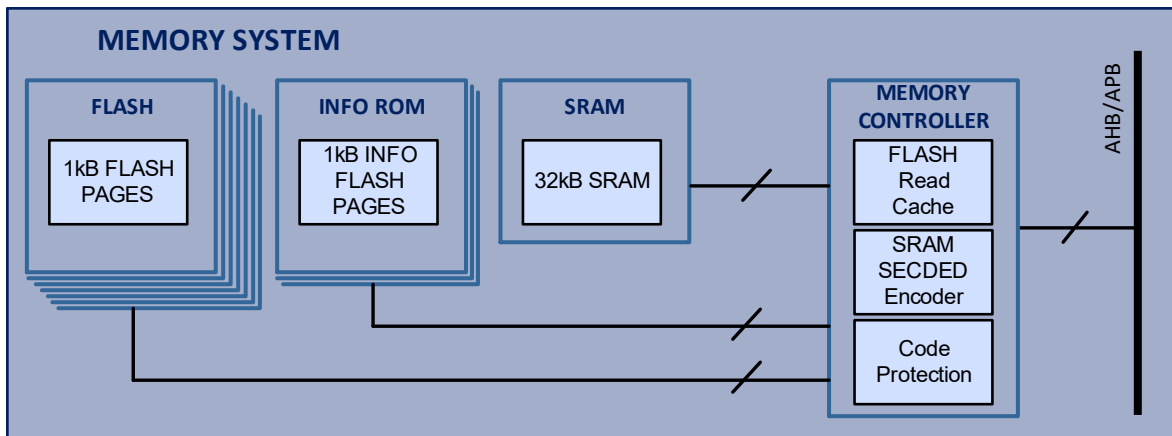
11 Memory System

11.1 Features

- 128kB Program FLASH
 - 30k Program/Erase cycles
 - 10 years data retention
 - FLASH look-ahead buffer for optimizing access
- 1kB INFO-1 FLASH
- 1kB INFO-2 FLASH
 - Device ID, Unique ID, trim and manufacturing data
- 32kB SRAM
 - 150MHz access for code or data
 - SECDE for read/write operations
- User-configurable Code Protection

11.2 System Block Diagram

Figure 17 Memory System Block Diagram



11.3 Functional Description

The PAC5524 contains multiple banks of FLASH memory, SRAM memory as well as peripheral control registers that are accessible to the MCU in a flat memory map.

11.3.1 Program FLASH

The PAC55XX Memory Controller provides access to 128 1kB pages of main program FLASH for a total of 128kB of FLASH through the system AHB bus. Each page may be individually erased or written while the MCU is executing instructions from SRAM.

The PAC55XX Memory Controller provides a FLASH read buffer that optimizes access from the MCU to the FLASH memory. This look ahead buffer monitors the program execution and fetches instructions from FLASH before they are needed to optimize access to this memory.

11.3.2 INFO FLASH

The PAC55XX Memory Controller provides access to the INFO-1, INFO-2 and INFO-3 FLASH memories, which are each a single 1kB page for a total of 3kB of memory.

INFO-1 and INFO-2 are read-only memories that contains device-specific information such as the device ID, a unique ID, trimming and calibration data that may be used by programs executing on the PAC55XX.

INFO-3 is available to the user for data or program storage.

11.3.3 SRAM

The PAC55XX Memory Controller provides access to the 32kB SRAM for non-persistent data storage. The SRAM memory supports word (4B), half-word (2B) and byte addresses.

The PAC55XX Memory Controller can read or write data from RAM up to 150MHz. This can be a benefit for time-critical applications. This memory can also be used for program execution when modifying the contents of FLASH, INFO-1 or INFO-2 FLASH.

The PAC55XX Memory Controller also has an SECDED encoder, capable of detecting and correcting single-bit errors, and detecting double-bit errors. The user may read the status of the encoder, to see if a single-bit error has occurred. The user may also enable an interrupt upon detection of single-bit errors. Dual-bit errors can be configured to generate an interrupt in the PAC55XX.⁵

For more information on the PAC55XX Memory Controller, see the PAC55XX Family User Guide.

⁵ Note that when writing half-word or single bytes to SRAM, the memory controller must perform a read-modify write to memory to perform the SECDED calculation. These operations will take more than one clock cycle to perform for this reason.

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

11.3.4 Code Protection

The PAC5524 allows the user to configure a 4-level code protection scheme to secure code from being read from the device.

There are four levels of code protection available as shown in the table below.

Table 24 Code Protection Levels

| Level | Name | Features |
|-------|--------------------------|--|
| 0 | UNLOCKED | <ul style="list-style-type: none"> No restrictions |
| 1 | RW PROTECTION | <ul style="list-style-type: none"> SWD enabled Programmable protection of up to 64 regions of FLASH User-specified Read or Write per region |
| 2 | SWD DISABLED | <ul style="list-style-type: none"> SWD disabled Programmable protection of up to 64 regions of FLASH User-specified Read or Write per region |
| 3 | SWD PERMANENTLY DISABLED | <ul style="list-style-type: none"> SWD disabled Programmable protection of up to 64 regions of FLASH User-specified Read or Write per region No recovery |

11.4 Electrical Characteristics

The Electrical Characteristics for the Memory System are shown below.

Table 25 Memory System Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---------------------------|----------------------------|--|------|------|------|---------------|
| FLASH | | | | | | |
| $t_{\text{READ;FLASH}}$ | FLASH word read time | | 40 | | | ns |
| $t_{\text{WRITE;FLASH}}$ | FLASH work write time | | 30 | | | μs |
| $t_{\text{PERASE;FLASH}}$ | FLASH page erase time | | | | 2 | ms |
| $t_{\text{MERASE;FLASH}}$ | FLASH mass erase time | | | | 10 | ms |
| $N_{\text{PERASE;FLASH}}$ | FLASH program/erase cycles | | 30k | | | cycles |
| $t_{\text{DF;FLASH}}$ | FLASH data retention | | 10 | | | years |
| SRAM | | | | | | |
| $t_{\text{ACC;SRAM}}$ | SRAM access time | HCLK = 150MHz; Word (32-bits), aligned | 6.67 | | | ns |
| | | HCLK = 150MHz; Half-word (16-bits), byte (8-bits), aligned | 6.67 | | | ns |

$T_A = -40^\circ\text{C}$ to 125°C unless otherwise specified

12 System and Clock Control (SCC)

12.1 Features

- 20MHz Ring Oscillator
- High-accuracy 2% trimmed 4MHz RC oscillator
- External Clock Input for External Clocks up to 20MHz
- PLL with 1MHz to 50MHz input, 62.5MHz to 300MHz output
- Clock dividers for all system clocks
- Clock gating for power conservation during low-power operation

12.2 System Block Diagram

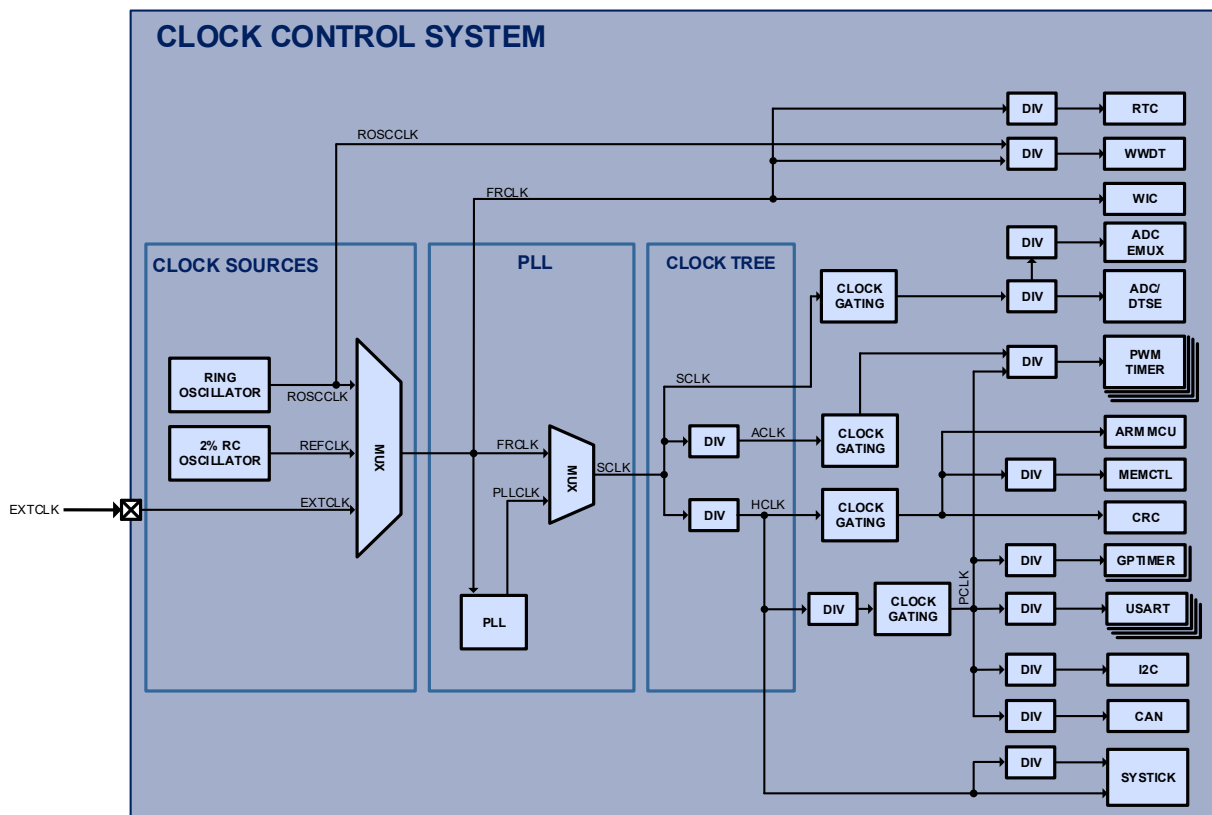


Table 26 Clock Control System Block Diagram

12.3 Functional Description

The Clock Control System (CCS) controls the clock system and clock gating for the PAC5524. There are three independent clock sources: the Ring Oscillator, Reference Clock and External Clock Input.

12.4 Clock Sources

12.4.1 Ring Oscillator

The Ring Oscillator (ROSC) is an integrated 20MHz clock oscillator that is the default system clock, and is available by default when the PAC55XX comes out of reset. The output of the ROSC is the **ROSCCLK** clock. The **ROSCCLK** may be selected as the **FRCLK** clock and may supply the WWDT, for applications that need an independent clock source or need to continue to be clocked when the system is in a low-power mode.

The ROSC may be disabled by the user by a configuration register.

12.4.2 Reference Clock

The Reference Clock (**REFCLK**) is an integrated 2% trimmed 4MHz RC clock. This clock is suitable for many applications. This clock may be selected as the **FRCLK** and can be used as the input to the PLL and is used to derive the clock for the MMPM.

12.4.3 External Clock Input

The External Clock Input (EXTCLK) is a clock input available through the digital peripheral MUX, and allows the drive the clock system by a 50% duty cycle clock of up to 20MHz. This clock may be selected as FRCLK and can be used as the input the PLL (as long as the accuracy is better than +/- 2%).

12.5 PLL

The PAC55XX contains a Phase Lock Loop (PLL) that can generate very high clock frequencies up to 300MHz for the peripherals and timers in the device. The input to the PLL is the **FRCLK** and must be from the **EXTCLK** or **REFCLK** clock sources

The input to the PLL must be between 1MHz – 50MHz and the output can be configured to be from 62.5MHz to 300MHz. The user can configure the PLL to generate the desired clock output based on a set of configuration registers in the CCS. The output of the PLL is the **PLLCLK** clock. The user may configure a MUX to generate the SCLK clock from **PLLCLK** or from **FRCLK**.

In addition to configuring the PLL output frequency, the PLL may be enabled, disabled and bypassed through a set of configuration registers in the CCS.

12.6 Clock Tree

The following are the system clocks available in the clock tree. See the section below to see which clocks are available for each of the digital peripherals in the system.

12.6.1 FRCLK

The free-running clock (**FRCLK**) is generated from one of the four clock sources (**ROSCCLK**, **EXTCLK** or **REFCLK**). This clock may be used by the WWDT and the RTC, for configurations that turn off all other system clocks during low power operation.

The **FRCLK** or **PLLCLK** is selected via a MUX and the output becomes **SCLK**.

12.6.2 SCLK

The System Clock (**SCLK**) generates two system clocks: **ACLK** and **HCLK**. Each of these system clocks has their own 3b clock divider and is described below.



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

12.6.3 PCLK

The Peripheral Clock (**PCLK**) is used by most of the digital peripherals in the PAC55XX. This clock has a 3b clock divider and also has clock gating support, which allows this clock output to be disabled before the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

As shown above, most of the peripherals that use **PCLK** also have their own clock dividers so that this clock can be further divided down to meet the application's needs.

12.6.4 ACLK

The Auxiliary Clock (**ACLK**) may be optionally used by the PWM timer block in the PAC55XX in order to generate a very fast clock for PWM output to generate the best possible accuracy and edge generation.

This clock has a 3b clock divider and also has clock gating support, which disables this clock output when the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

As shown above, the **ACLK** is an optional input for just the PWM timer block in the PAC55XX.

12.6.5 HCLK

The AHB Clock (**HCLK**) is used by the Arm® Cortex®-M4 MCU and Memory Controller peripheral. This clock has a 3b divider and also has clock gating support, which allows this clock output to be disabled before the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

HCLK supplies PCLK with its clock source.

12.7 Electrical Characteristics

The Electrical Characteristics for the System and Clock Control module are shown below.

Table 27 System and Clock Control Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--|---|--|------|------|-------|---------------|
| Clock Tree (FRCLK, FCLK, PCLK, ACLK, HCLK) | | | | | | |
| f_{FRCLK} | Free-running clock frequency | | | | 25 | MHz |
| f_{SCLK} | System clock frequency | | | | 300 | MHz |
| f_{PCLK} | Peripheral clock frequency | After PCLK divider | | | 150 | MHz |
| f_{ACLK} | Auxiliary clock frequency | After ACLK divider | | | 300 | MHz |
| f_{HCLK} | High-speed clock frequency | After HCLK divider | | | 150 | MHz |
| Internal Oscillators | | | | | | |
| $f_{ROSCCLK}$ | Ring oscillator frequency | | | 20 | | MHz |
| $f_{TRIM;REFCLK}$ | Trimmed RC oscillator frequency | $T_A = 25^\circ\text{C}$ | -2% | 4 | 2% | MHz |
| | | $T_A = -40^\circ\text{C}$ to 125°C | -3% | 4 | 3% | MHz |
| $f_{JITTER;REFCLK}$ | Trimmed RC oscillator clock jitter | $T_A = -40^\circ\text{C}$ to 85°C | | 0.5 | | % |
| PLL | | | | | | |
| $f_{IN;PLL}$ | PLL input frequency range | | 1 | | 50 | MHz |
| $f_{OUT;PLL}$ | PLL output frequency range | | 62.5 | | 300 | MHz |
| $t_{SETTLE;PLL}$ | PLL setting time | $T_A = 25^\circ\text{C}$, PLL settled | | | 15 | μs |
| | | $T_A = 25^\circ\text{C}$, PLLLOCK = 1 | | 200 | 500 | μs |
| $t_{JITTER;PLL}$ | PLL period jitter | RMS | | 25 | | ps |
| | | Peak to peak | | | 100 | ps |
| | PLL duty cycle | | 40 | 50 | 60 | % |
| External Clock Input (EXTCLK) | | | | | | |
| f_{EXTCLK} | External Clock Input Frequency | | | | 20 | MHz |
| | External Clock Input Duty Cycle | | 40 | | 60 | % |
| $V_{IH;EXTCLK}$ | External Clock Input high-level input voltage | | 2.1 | | | V |
| $V_{IL;EXTCLK}$ | External Clock Input low-level input voltage | | | | 0.825 | V |

$T_A = -40^\circ\text{C}$ to 125°C unless otherwise specified

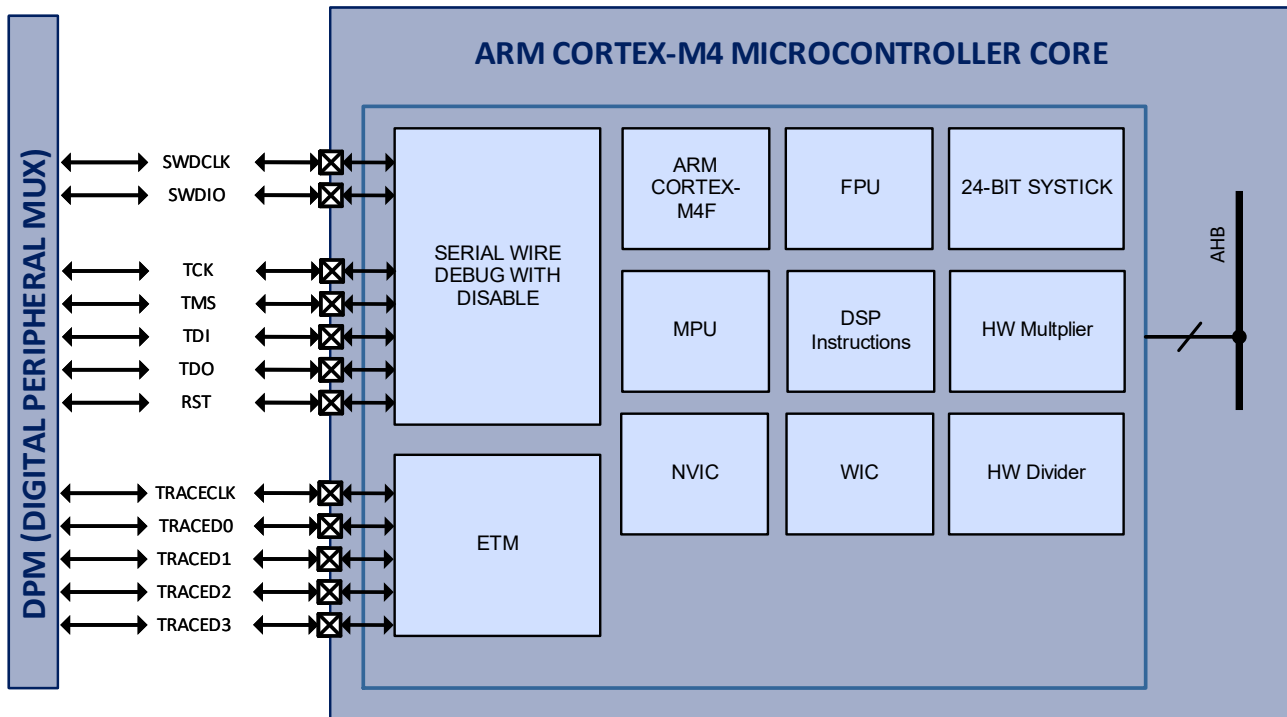
13 Arm® Cortex®-M4F MCU Core

13.1 Features

- Arm® Cortex®-M4F core
- SWD or JTAG Debug
- SWD/JTAG code security
- Embedded Trace Module (ETM) for instruction tracing
- Memory Protection Unit (MPU)
- Nested Vectored Interrupt Controller (NVIC) with 29 user interrupts and 8 levels of priority
- Floating Point Unit (FPU)
- Wakeup Interrupt Controller (WIC)
- 24-bit SysTick Count-down Timer
- Hardware Multiply and Divide Instructions

13.2 System Block Diagram

Figure 18 Arm Cortex-M4F MCU System Block Diagram



13.3 Functional Description

The Arm® Cortex®-M4F microcontroller core is configured for little endian operation and includes hardware support for multiplication and division, DSP instructions as well as an IEEE754 single-precision Floating Point Unit (FPU).

The MCU also contains an 8-region Memory Protection Unit (MPU), as well as a Nested Vector Interrupt Controller (NVIC) that supports 29 user interrupts with 8 levels of priority. There is a 24-bit SysTick count-down timer.

The Arm® Cortex®-M4F supports sleep and deep sleep modes for low power operation. In sleep mode, the Arm® Cortex®-M4F is disabled. In deep sleep mode, the MCU as well as many peripherals are disabled. The Wakeup Interrupt Controller (WIC) can wake up the MCU when in deep sleep mode by using any GPIO interrupt, the Real-Time Clock (RTC) or Windowed Watchdog Timer (WWDT). The PAC55XX also supports clock gating to reduce power during deep sleep operation.

The debugger supports 4 breakpoint and 2 watch-point unit comparators using the SWD or JTAG protocols. The debug serial interfaces may be disabled to prevent memory access to the firmware during customer production.

For more information on the detailed operation of the Microcontroller Core in the PAC55XX, see the PAC55XX Family User Guide.

13.4 Application Typical Current Consumption

The MCU clock configuration and peripheral configuration have a large influence on the amount of load that the power supplies in the PAC55XX will have.

The table below shows a number of popular configurations and what the typical power consumption will be on the VSYS and VCORE power supplies in the PAC55XX.

Table 28 PAC55XX Application Typical Current Consumption

| CLOCK CONFIGURATION | MCU PERIPHERALS | MCU STATE | IVSYS | IVCORE | IVCC33 |
|--|------------------------------------|--------------|--------|--------|--------|
| CLKREF = 4MHz PLL Disabled ACLK=HCLK=PCLK=SCLK=MCLK = 16MHz ROSCCLK Enabled FRCLK MUX = ROSCCLK | All peripherals disabled | Halted | 9.5mA | 2.3mA | n/a |
| CLKREF = 4MHz PLLCLK = 30MHz ACLK=HCLK=PCLK=SCLK= 16MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF | All peripherals disabled | Halted | 10.5mA | 3.5mA | n/a |
| CLKREF = 4MHz PLLCLK = 150MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF | All peripherals disabled | Halted | 20mA | 13.5mA | n/a |
| CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF | All peripherals disabled | Halted | 22mA | 15mA | n/a |
| CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF ADCCLK = 40MHz | ADC enabled (repeated conversions) | Halted | 36mA | 16mA | 13.5mA |
| CLKREF = 4MHz | All peripherals disabled | CPU Executes | 8.5mA | 2.2mA | n/a |



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

| | | | | | |
|--|--|----------------------------|------|------|-----|
| PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF | | instructions from FLASH | | | |
| CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF | Timer A enabled; TAPWM[7:0] enabled; Fs = 100kHz; 50% duty cycle | Halted | 22mA | 15mA | n/a |

13.5 Electrical Characteristics

The Electrical Characteristics for the System and Clock Control module are shown below.

Table 29 System and Clock Control Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|------------------|------------------------------|---|------|------|------|-------|
| f_{HCLK} | MCU Clock | | | | 50 | MHz |
| $I_{Q;V_{CORE}}$ | V_{CORE} quiescent current | Arm® Cortex®-M4F Sleep/Deep Sleep Modes | | | 2 | mA |
| | | PAC5524 Hibernate Mode | | | 0 | mA |
| $I_{Q;V_{SYS}}$ | V_{SYS} quiescent current | Arm® Cortex®-M4F Sleep/Deep Sleep Modes | | | 8 | mA |
| | | PAC5524 Hibernate Mode | | | 15 | μA |
| $I_{Q;V_{CCIO}}$ | VCCIO quiescent current | Arm® Cortex®-M4F Sleep/Deep Sleep Modes | | | 0.15 | mA |
| | | PAC5524 Hibernate Mode | | | 0 | mA |
| $I_{Q;V_{CC33}}$ | VCC33 quiescent current | Arm® Cortex®-M4F Sleep/Deep Sleep Modes | | | 0.4 | mA |
| | | PAC5524 Hibernate Mode | | | 0 | mA |

14 IO Controller

14.1 Features

- 3.3V Input/Output, 4.6V input tolerant
- Push-Pull Output, Open-Drain Output or High-Impedance Input for each IO
- Configurable Pull-up and Pull-down for each IO (60k)
- Configurable Drive Strength for each IO (up to 24mA)
- Analog Input for some IOs
- Edge-sensitive or level-sensitive interrupts
- Rising edge, falling edge or both edge interrupts
- Peripheral MUX allowing up to 8 peripheral selections for each IO
- Configurable De-bouncing Circuit for each IO

14.2 System Block Diagram

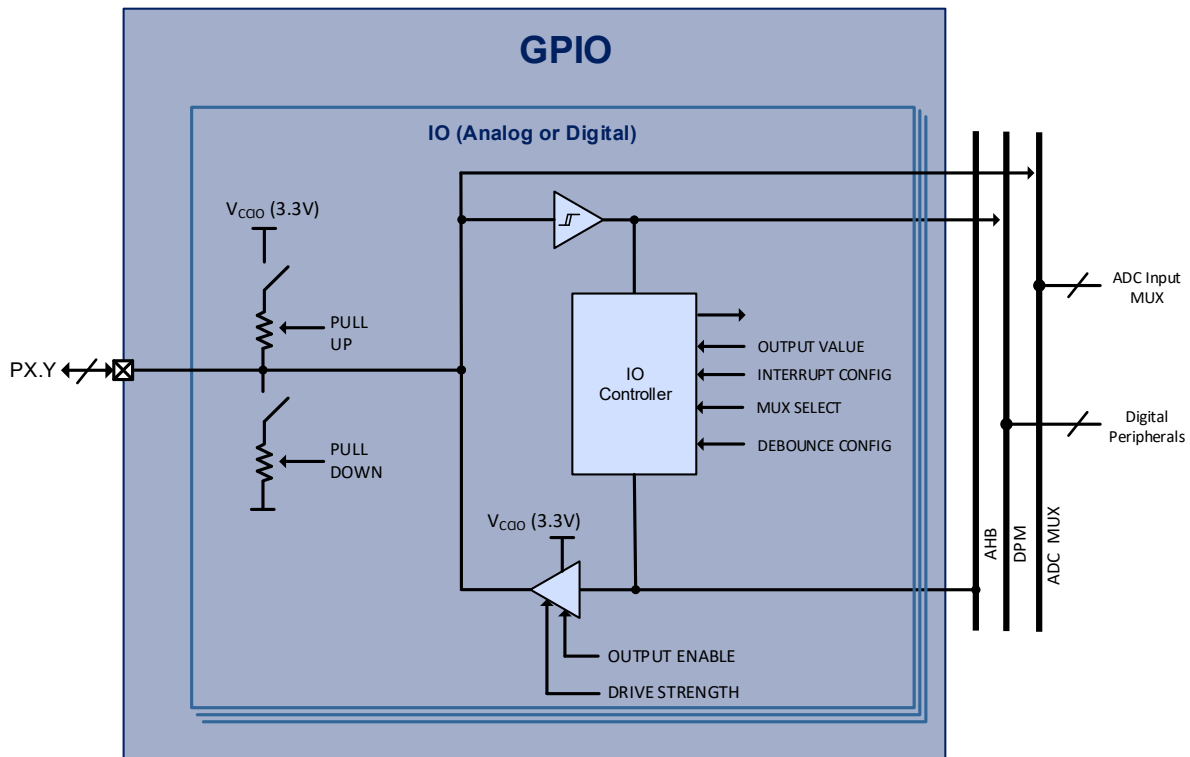


Figure 19 IO Controller System Block Diagram

14.3 Functional Description

14.3.1 IO Controller

The PAC55XX IO cells can be used for digital input/output and analog input for the ADC. All IOs are supplied by the V_{CCIO} (3.3V) power supply.

Each IO can be configured for digital push-pull output, open-drain output or high-impedance input. Each IO also has a configurable 60k weak pull-up or weak pull-down that can be enabled.

NOTE: Configuring both pull-up and pull-down at the same time may cause device damage and should be avoided.

Each IO has a configurable de-bouncing filter that can be enabled or disabled, to help filter out noise.

All IO have interrupt capability. Each pin can be configured for either level or edge sensitive interrupts, and can select between rising edge, falling edge and both edges for interrupts. Each pin has a separate interrupt enable and interrupt flag.

Some of the IO on the PAC5524 can be configured as an analog input to the ADC.

14.3.2 GPIO Current Injection

Under normal operation, there should not be current injected into the GPIOs on the device due to the GPIO voltage below ground or above the GPIO supply (V_{CCIO}). Current will be injected into the GPIO when the GPIO pin voltage is less than $-0.3V$ or when greater than $GPIO\ supply + 0.3V$.

In order provide a robust solution when this situation occurs, the PAC52XX family of products allows a small amount of injected current into the GPIO pins, to avoid excessive leakage or device damage.

For information on the GPIO current injection thresholds, see the absolute maximum parameters for this device.

Sustained operation with the GPIO pin voltage greater than the GPIO supply or when the GPIO pin voltage is less than $-0.3V$ may result in reduced lifetime of the device. GPIO current injection should only be a temporary condition.



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

14.3.3 Peripheral MUX

The Peripheral MUX (DPM) allows the IO controller to select one of up to four peripheral functions for each IO pin. Note that if the pin is configured for analog input, the peripheral MUX is bypassed.

The Peripheral MUX for the PAC5524 is shown below.

Table 30 Peripheral MUX settings

| PIN | PERIPHERAL MUX SETTINGS | | | | | | | | ADC CH |
|-----|-------------------------|--------|--------|-----------|----------|---------|----------|----------|--------|
| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | |
| PC0 | GPIOC0 | TBPWM0 | TCPWM0 | TBQEPIDX | USBMOSI | USCSCLK | CANRXD | I2CSCL | |
| PC1 | GPIOC1 | TBPWM1 | TCPWM1 | TBQEPPHA | USBMISO | USCSS | CANTXD | I2CSDA | |
| PC2 | GPIOC2 | TBPWM2 | TCPWM2 | TBQEPPHB | USBSCLK | USCMOSI | | EMUXD | |
| PC3 | GPIOC3 | TBPWM3 | TCPWM3 | | USBSS | USCMISO | | EMUXC | |
| PC4 | GPIOC4 | TBPWM4 | TCPWM4 | TCQEPIDX | USBMOSI | USCSCLK | CANRXD | I2CSDL | |
| PC5 | GPIOC5 | TBPWM5 | TCPWM5 | TCQEPPHA | USBMISO | USCSS | CANTXD | I2CSDA | |
| PC6 | GPIOC6 | TBPWM6 | TCPWM6 | TCQEPPHB | USBSCLK | USCMOSI | | EMUXD | |
| PC7 | GPIOC7 | TBPWM7 | TCPWM7 | | USBSS | USCMISO | FRCLK | EMUXC | |
| PD0 | GPIOD0 | TBPWM0 | TCPWM0 | TDQEPIDX | | USCSCLK | CANTXD | EMUXD | AD4 |
| PD1 | GPIOD1 | TBPWM1 | TCPWM1 | TDQEPPHA | | USCSS | CANRXD | EMUXC | AD3 |
| PD2 | GPIOD2 | TBPWM2 | TCPWM2 | TDQEPPHB | | USCMOSI | | | AD2 |
| PD3 | GPIOD3 | TBPWM3 | TCPWM3 | | | USCMISO | FRCLK | TRACED3 | AD1 |
| PD4 | GPIOD4 | TBPWM4 | TCPWM4 | TDQEPIDX | TBQEPIDX | USDCLK | TRACED3 | USDMSI | |
| PD5 | GPIOD5 | TBPWM5 | TCPWM5 | TDQEPPHA | TBQEPPHA | USDSS | CANRXD | USDMSO | |
| PD6 | GPIOD6 | TBPWM6 | TCPWM6 | TDQEPPHB | TBQEPPHB | USDMSI | CANTXD | I2CSDA | |
| PE0 | GPIOE0 | TCPWM4 | TDPWM0 | TAQEPIDX | TBQEPIDX | USCLK | I2CSCL | EMUXC | |
| PE1 | GPIOE1 | TCPWM5 | TDPWM1 | TAQEPPHA | TBQEPPHA | USCSS | I2CSDA | EMUXD | |
| PE2 | GPIOE2 | TCPWM6 | TDPWM2 | TAQEPPHB | TBQEPPHB | USCMOSI | CANRXD | EXTCLK | |
| PE3 | GPIOE3 | TCPWM7 | TDPWM3 | FRCLK | | USCMISO | CANTXD | | |
| PF0 | GPIOF0 | TCPWM0 | TDPWM0 | TCK/SWDCL | TBQEPIDX | USBSCLK | TRACED2 | TRACECLK | |
| PF1 | GPIOF1 | TCPWM1 | TDPWM1 | TMS/SWDIO | TBQEPPHA | USBSS | TRACED1 | TRACED0 | |
| PF2 | GPIOF2 | TCPWM2 | TDPWM2 | TDI | TBQEPPHB | USBMOSI | TRACED0 | TRACED1 | |
| PF3 | GPIOF3 | TCPWM3 | TDPWM3 | TDO | FRCLK | USBMISO | TRACECLK | TRACED2 | |
| PF4 | GPIOF4 | TCPWM4 | TDPWM4 | | TCQEPIDX | USDCLK | TRACED3 | EMUXC | AD4 |
| PF5 | GPIOF5 | TCPWM5 | TDPWM5 | | TCQEPPHA | USDSS | | EMUXD | AD5 |
| PF6 | GPIOF6 | TCPWM6 | TDPWM6 | | TCQEPPHB | USDMSI | CANRXD | I2CSCL | AD6 |
| PF7 | GPIOF7 | TCPWM7 | TDPWM7 | | | USDMSO | CANTXD | I2CSDA | AD7 |
| PG0 | GPIOG0 | TCPWM0 | TDPWM0 | EMUXC | | USDCLK | TRACECLK | TCQEPIDX | |
| PG1 | GPIOG1 | TCPWM1 | TDPWM1 | EMUXD | | USDSS | TRACED0 | TCQEPPHA | |
| PG2 | GPIOG2 | TCPWM2 | TDPWM2 | FRCLK | | USDMSI | TRACED1 | TCQEPPHB | |
| PG3 | GPIOG3 | TCPWM3 | TDPWM3 | | | USDMSO | TRACED2 | | |

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

14.4 Electrical Characteristics

The Electrical Characteristics for the IO Controller are shown below.

Table 31 IO Controller Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units | |
|-----------------------|--|--|-----------|------|-------|------------|----|
| V_{IH} | High-level input voltage | | 2.1 | | | V | |
| V_{IL} | Low-level input voltage | | | | 0.825 | V | |
| I_{OL} | Low-level output sink current (Limited by $I_{V_{SYS}}$ and $I_{V_{CCIO}}$) | $V_{OL} = 0.4V$ | DS = 6mA | 6 | | | mA |
| | | | DS = 8mA | 8 | | | |
| | | | DS = 11mA | 11 | | | |
| | | | DS = 14mA | 14 | | | |
| | | | DS = 17mA | 17 | | | |
| | | | DS = 20mA | 20 | | | |
| | | | DS = 22mA | 22 | | | |
| | | | DS = 25mA | 25 | | | |
| I_{OH} | High-level output source current (Limited by $I_{V_{SYS}}$ and $I_{V_{CCIO}}$) | $V_{OH} = 2.4V$ | DS = 6mA | | | -6 | mA |
| | | | DS = 8mA | | | -8 | |
| | | | DS = 11mA | | | -11 | |
| | | | DS = 14mA | | | -14 | |
| | | | DS = 17mA | | | -17 | |
| | | | DS = 20mA | | | -20 | |
| | | | DS = 22mA | | | -22 | |
| | | | DS = 25mA | | | -25 | |
| I_{IL} | Input leakage current | | -2 | | 0.95 | μA | |
| R_{PU} | Weak pull-up resistance | When pull-up enabled | 45 | 60 | 100 | k Ω | |
| R_{PD} | Weak pull-down resistance | When pull-down enabled | 45 | 60 | 115 | k Ω | |
| $I_{INJ;GPIO}$ | GPIO pin current injection | $V_{GPIO} < -0.3V$ or $V_{GPIO} > V_{CCIO} + 0.3V$ | -15 | | 15 | mA | |
| $\Sigma I_{INJ;GPIO}$ | Sum of all GPIO pin current injection | $V_{GPIO} < -0.3V$ or $V_{GPIO} > V_{CCIO} + 0.3V$ | -40 | | 40 | mA | |

$T_A = -40^\circ C$ to $125^\circ C$ unless otherwise specified

15 Serial Interface

15.1 Features

- USART (UART or SPI master/slave)
- I2C master/slave
- CAN 2.0B controller

15.2 System Block Diagram

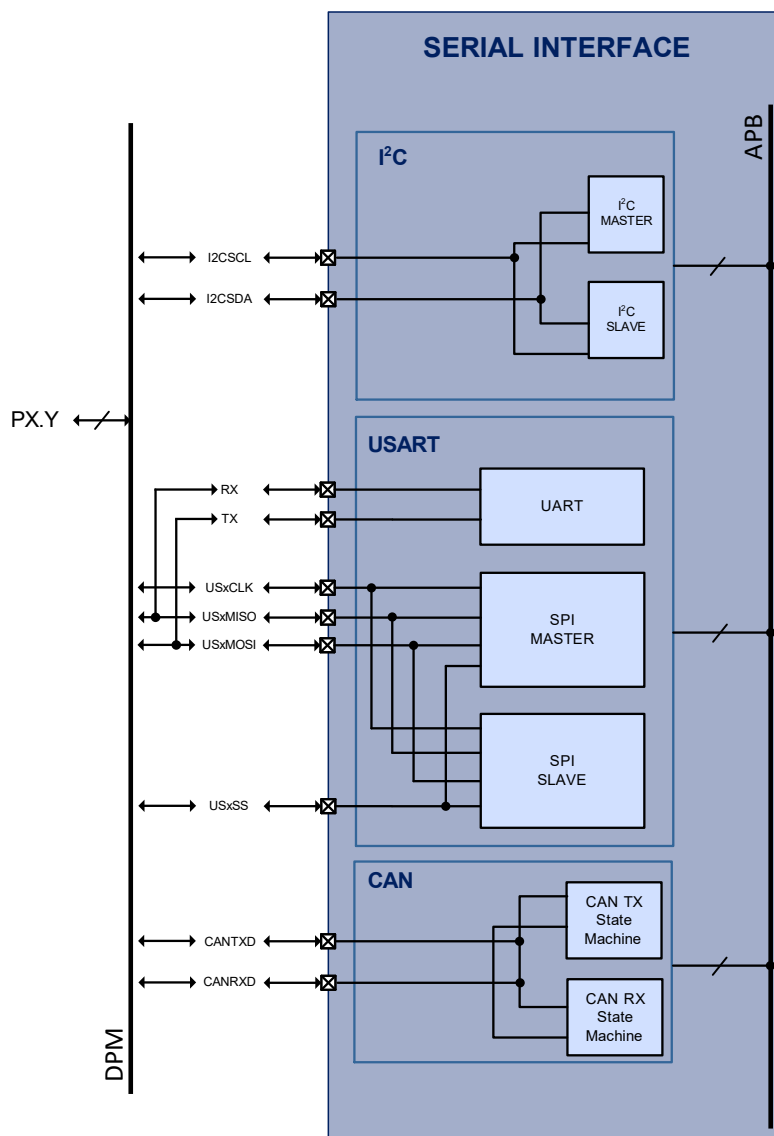


Figure 20 Serial Interfaces System Block Diagram

15.3 Functional Description

The PAC55XX has three types of serial interfaces: I²C, USART and CAN. The PAC55XX has one I²C controller, one CAN controller and up to 3 USARTs.

15.4 I²C Controller

The PAC55XX contains one I²C controller. This is a configurable APB peripheral and the clock input is PCLK. This peripheral has an input clock divider that can be used to generate various master clock frequencies. The I²C controller can support various modes of operation:

- I²C master operation
 - Standard (100kHz), full-speed (400kHz), fast (1MHz) or high-speed modes (3.4MHz)
 - Single and multi-master
 - Synchronization (multi-master)
 - Arbitration (multi-master)
 - 7-bit or 10-bit slave addressing
- I²C slave operation
 - Standard (100kHz), full-speed (400kHz), fast (1MHz) or high-speed modes (3.4MHz)
 - Clock stretching
 - 7-bit or 10-bit slave addressing

The I²C peripheral may operate either by polling or can be configured to be interrupt driven for both receive and transmit operations.

15.5 USART

The PAC55XX contains up to 2 Universal Synchronous Receive Transmit (USART) peripherals. Each USART is a configurable APB bus client and input clock is PCLK. These peripherals have a configurable clock divider that can be used to produce various frequencies for the UART or SPI master peripheral.

The number of these peripherals depends on the peripheral MUX configuration. See the IO Controller section on information on how to configure the peripheral MUX with the USART peripheral.

The USART peripheral supports two main modes: SPI mode and UART mode.

15.5.1 USART SPI Mode

- Master or slave mode operation
- 8-bit, 16-bit or 32-bit word transfers
- Configurable clock polarity (active high or active low)
- Configurable data phase (setup/sample or sample/setup)
- Interrupts and status flags for RX and TX operations
- Support for up to 25MHz SPI clock

15.5.2 USART UART Mode

- 8-bit data
- Programmable data bit rate



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

- Maximum baud rate of 1Mbaud
- RX and TX FIFOs
- Configurable stop bits (1 or 2)
- Configurable parity: even, odd, none
 - Mark/space support for 9-bit addressing protocols
- Interrupt and status flags for RX and TX operations

15.6 CAN

The PAC55XX contains one Controller Area Network (CAN) peripheral. The CAN peripheral is a configurable APB bus client and input clock is PCLK. This peripheral has a configurable clock divider that can be used to produce various frequencies for the CAN peripheral.

- CAN 2.0B support
- 1Mb/s data rate
- 64-byte receive FIFO
- 16-byte transmit buffer
- Standard and extended frame support
- Arbitration
- Overload frame generated on FIFO overflow
- Normal and Listen Only modes supported
- Interrupt and status flags for RX and TX operations

15.7 Dynamic Characteristics

The Dynamic Characteristics for the Serial Interfaces on the PAC5524 are shown below.

15.7.1 Serial Interface

Table 32 Serial Interface Dynamic Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|--|-----------------------------------|-------|------|---------------|-------|
| I2C | | | | | | |
| f_{I2CCLK} | I ² C input clock frequency | Standard mode (100kHz) | 2.8 | | | MHz |
| | | Full-speed mode (400kHz) | 2.8 | | | MHz |
| | | Fast mode (1MHz) | 6.14 | | | MHz |
| | | High-speed mode (3.4MHz) | 20.88 | | | MHz |
| USART (UART mode) | | | | | | |
| $f_{UARTCLK}$ | USART input clock frequency | | | | $f_{PCLK}/16$ | MHz |
| $f_{UARTBAUD}$ | UART baud rate | $f_{USARTCLK} = 7.1825\text{MHz}$ | | | 1 | Mbps |
| USART (SPI mode) | | | | | | |
| f_{SPICLK} | USART input clock frequency | Master mode | | | 50 | MHz |
| | | Slave mode | | | 50 | MHz |
| $f_{USARTSPICLK}$ | USART SPI clock frequency | Master mode | | | 25 | MHz |
| | | Slave mode | | | 25 | MHz |
| CAN | | | | | | |
| f_{CANCLK} | CAN input clock frequency | | | | 50 | MHz |
| f_{CANTX} | CAN transmit clock frequency | | | | 1 | Mbps |
| f_{CANRX} | CAN receive clock frequency | | | | 1 | Mbps |

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

15.7.2 I2C Dynamic Characteristics

Table 33 I2C Dynamic Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------------|--|--------------------------------|------|------|------|---------|
| f_{SCL} | SCL clock frequency | Standard mode | 0 | | 100 | kHz |
| | | Full-speed mode | 0 | | 400 | kHz |
| | | Fast mode | 0 | | 1 | MHz |
| t_{LOW} | SCL clock low | Standard mode | 4.7 | | | μ s |
| | | Full-speed mode | 1.3 | | | μ s |
| | | Fast mode | 0.5 | | | μ s |
| t_{HIGH} | SCL clock high | Standard mode | 4.0 | | | μ s |
| | | Full-speed mode | 0.6 | | | μ s |
| | | Fast mode | 0.26 | | | μ s |
| $t_{HD;STA}$ | Hold time for a repeated START condition | Standard mode | 4.0 | | | μ s |
| | | Full-speed mode | 0.6 | | | μ s |
| | | Fast mode | 0.26 | | | μ s |
| $t_{SU;STA}$ | Set-up time for a repeated START condition | Standard mode | 4.7 | | | μ s |
| | | Full-speed mode | 0.6 | | | μ s |
| | | Fast mode | 0.26 | | | μ s |
| $t_{HD;DAT}$ | Data hold time | Standard mode | 0 | | 3.45 | μ s |
| | | Full-speed mode | 0 | | 0.9 | μ s |
| | | Fast mode | 0 | | | μ s |
| $t_{SU;DAT}$ | Data setup time | Standard mode | 250 | | | ns |
| | | Full-speed mode | 100 | | | ns |
| | | Fast mode | 50 | | | ns |
| $t_{SU;STO}$ | Set-up time for STOP condition | Standard mode | 4.0 | | | μ s |
| | | Full-speed mode | 0.6 | | | μ s |
| | | Fast mode | 0.26 | | | μ s |
| t_{BUF} | Bus free time between a STOP and START condition | Standard mode | 4.7 | | | μ s |
| | | Full-speed mode | 1.3 | | | μ s |
| | | Fast mode | 0.5 | | | μ s |
| t_r | Rise time for SDA and SCL | Standard mode | | | 1000 | ns |
| | | Full-speed mode | 20 | | 300 | ns |
| | | Fast mode | | | 120 | ns |
| t_f | Fall time for SDA and SCL | Standard mode | | | 300 | ns |
| | | Full-speed mode | | | 300 | ns |
| | | Fast mode | | | 120 | ns |
| C_b | Capacitive load for each bus line | Standard mode, full-speed mode | | | 400 | pF |
| | | Fast mode | | | 550 | pF |

15.7.3 I2C Timing Diagram

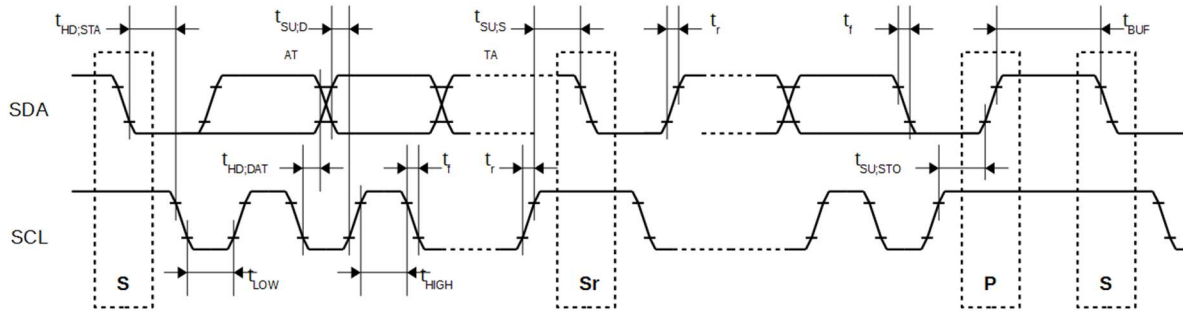


Figure 21 I2C Timing Diagram

16 PWM Timers

16.1 Features

- Base timer features:
 - Configurable input clock source: PCLK or ACLK
 - Up to 300MHz input clock
 - 3-bit Input clock divider
 - Timer counting modes
 - Up, up/down and asymmetric
 - Timer latch modes
 - Latch when counter = 0
 - Latch when counter = period
 - Latch when CCR value written
 - Latch all CCR values at same time
 - Base timer interrupts
 - Single shot or auto-reload
- CCR/PWM Timer
 - PWM output or capture input
 - CCR interrupt enable
 - CCR interrupt skips
 - SW force CCR interrupt
 - CCR interrupt type
 - Rising, falling or both
 - CCR compare latch modes
 - Latch when counter = 0
 - Latch when counter = period
 - Latch immediate
 - CCR capture latch modes
 - Latch on rising edge
 - Latch on falling edge
 - Latch on both rising and falling edges
 - Invert CCR output
 - CCR phase delay for phase shifted drive topologies
 - ADC trigger outputs
 - PWM rising edge or falling edge
- Dead-time Generators (DTG)
 - DTG enabled
 - 12-bit rising edge delay



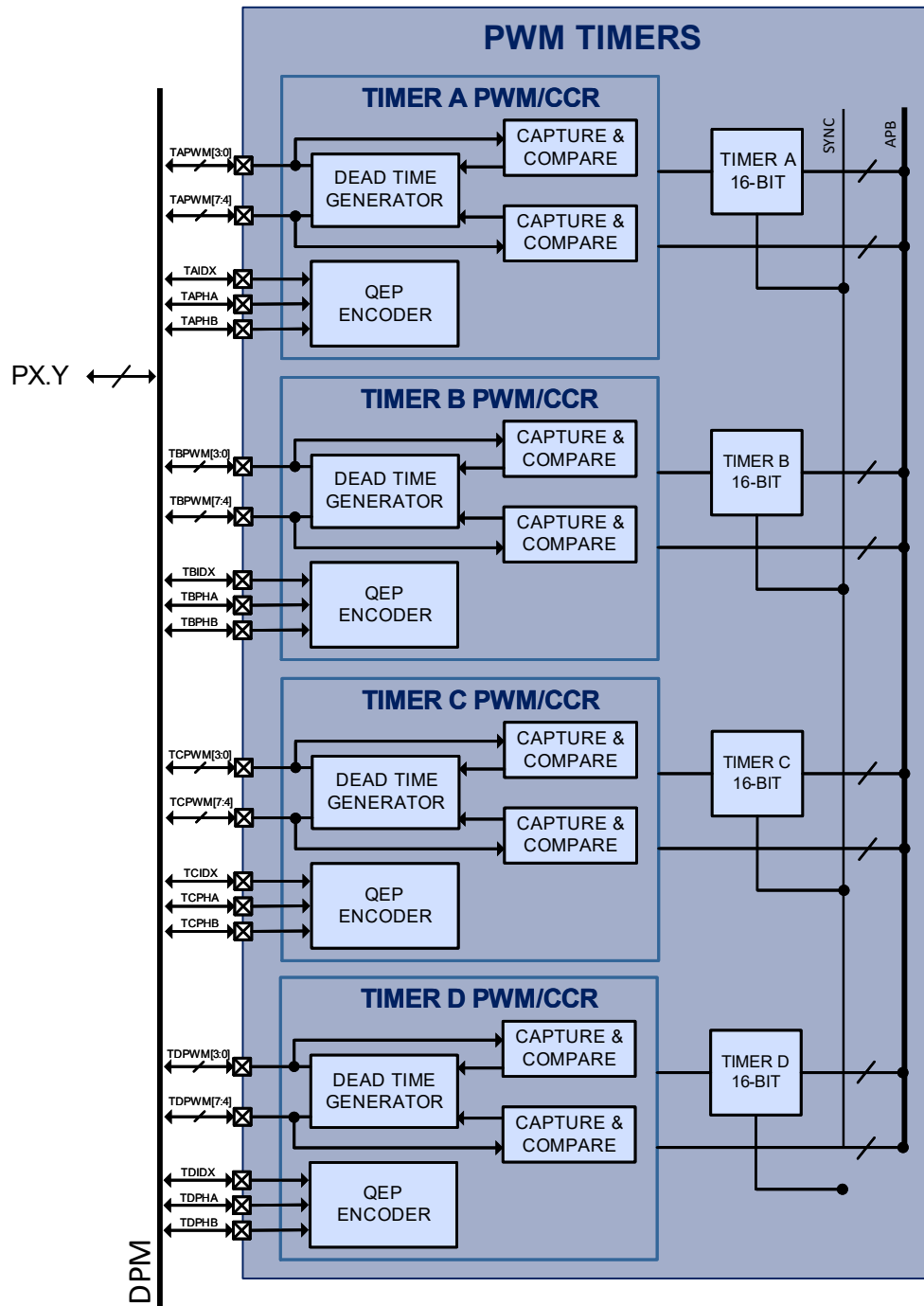
PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

- 12-bit falling edge delay
- QEP Decoder
 - QEP encoder enabled
 - Direction status
 - Configurable Interrupts:
 - Phase A rising edge
 - Phase B rising edge
 - Index event
 - Counter wrap
 - 4 different counting modes for best resolution, range and speed performance

16.2 System Block Diagram

Figure 22 PWM Timers System Block Diagram



16.3 Functional Description

The PAC5524 contains four 16-bit timer units that may be used for PWM output and capture input. Each timer has a 16-bit time-base that may configure the counting style to up, up/down and up/down asymmetric modes. These modes can be used to support different drive topologies such as 120° trapezoidal and 180° sinusoidal.

Each base timer block may be clocked by either PCLK or ACLK. Configuring the timer to clock using ACLK allows higher PWM edge resolution by offering a clock that is up to 2X higher than the system clock. The base timer supports interrupts as well as single shot or auto-reload modes for maximum flexibility.

Each base timer has up to 8 CCR units that may be used for PWM output or capture input. When configured for PWM output, the user may configure a delay in order to support phase delay drive topologies. The CCR output may also be inverted in order to support full-bridge topologies.

The user may configure each CCR output rising or falling edge to interrupt the DTSE to begin a sequence of conversions.

17 General Purpose Timers

17.1 Features

- SOC Bus Watchdog Timer
- Hibernate Wake-up Timer
- Real-Time Clock with Calendar and Alarm
- Windowed Watchdog Timer (WWDT)
- 24-Bit General-purpose Timers

17.2 System Block Diagram

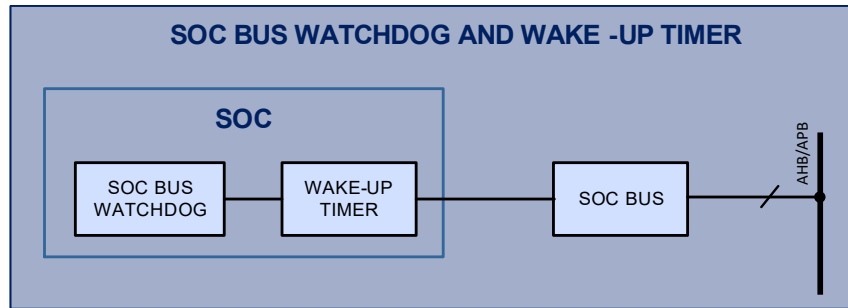


Figure 23 SOC and WWDT System Block Diagrams

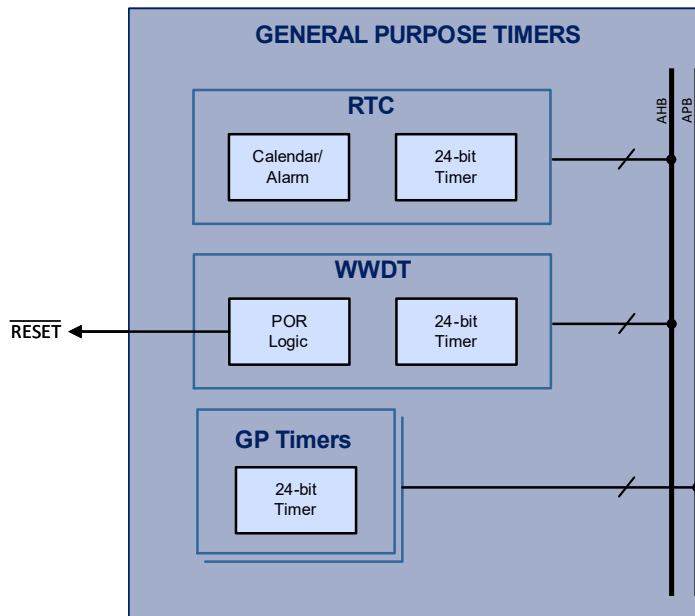


Figure 24 General-Purpose Timers System Block Diagrams

17.3 Functional Description

17.3.1 SOC Bus Watchdog Timer

The SOC Bus Watchdog Timer is used to monitor internal SOC Bus communication. It will trigger a device reset if there is no SOC Bus communication to the AFE for 4s or 8s.

17.3.2 Wake-up Timer

The wake-up timer can be used for very low power hibernate and sleep modes to wake up the micro controller periodically. It can be configured to be 125ms, 250ms, 500ms, 1s, 2s, 4, or 8s.

17.3.3 Real-time Clock with Calendar (RTC)

The 24-bit real-time clock with calendar (RTC) is an AHB bus client and may also be used to measure long time periods and periodic wake up from sleep mode.

The RTC uses FRCLK as its clock source and has a divider that can be configured up to a /65536 input clock divider. In order to count accurately, the input clock divider must be configured to generate a 1MHz clock to the RTC.

The RTC counts the time (seconds, minutes, hours, days) since enabled. It also allows the user to set a calendar date to set an alarm function that can be configured to generate an interrupt to the NVIC when it counts to that value.

17.3.4 Windowed Watchdog Timer (WWDT)

The 24-bit windowed watchdog timer (WWDT) is an AHB bus client and can be used for long time period measurements or periodic wake up from sleep mode. Its primary use is to reset the system via a POR if it is not reset at a certain periodic interval.

The WWDT can be configured to use FRCLK or ROSCCLK as its clock source and has a divider that be configured up to a /65536 input clock divider.

The WWDT can be configured to allow only a small window when it is valid to reset the timer, to maximize application security and catch any stray code operating on the MCU.

The WWDT may be configured to enable an interrupt for the MCU, and the timer can be disabled when unused to save energy for low power operations.

17.3.5 GP Timer (GPT)

The PAC55XX contains two General Purpose (GP) Timers.

These timers are 24-bit timers and are both APB bus clients. These count-down timers use PCLK as their input clock and have a configurable divider of up to /32768. Each of the GPT can be configured to interrupt the MCU when they count down to 0.

18 CRC

18.1 Features

- 8-bit or 16-bit CRC
- User may select the polynomial through configuration:
 - CCITT CRC-16
 - IBM/ANSI CRC-16
 - Dallas/Maxim CRC-8
- Input data width: 8b or 32b
- Reflect input
- Reflect output
- Specify seed value

18.2 System Block Diagram

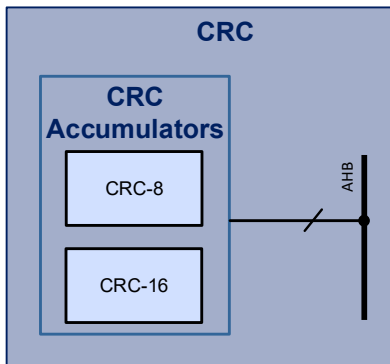


Figure 25 CRC System Block Diagram

18.3 Functional Description

The CRC peripheral can perform CRC calculation on data through registers from the MCU to accelerate the calculation or validation of a CRC for communications protocols or data integrity checks.

The CRC peripheral allows the calculation of both CRC-8 and CRC-16 on data. The CRC peripheral also allows the user to specify a seed value, select the data input to be 8b or 32b and to reflect the final output for firmware efficiency.

19 Application Block Diagram

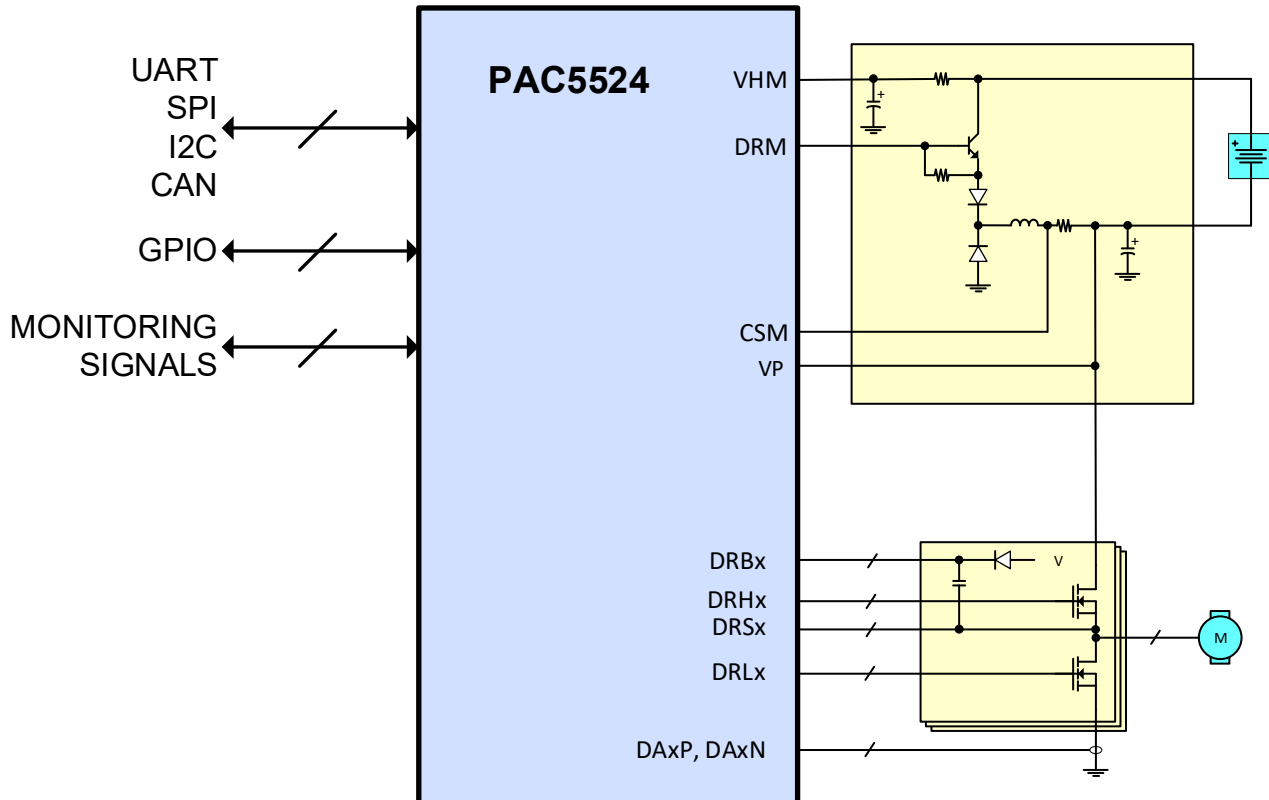


Figure 26 PAC5524 Application Block Diagram



PAC5524

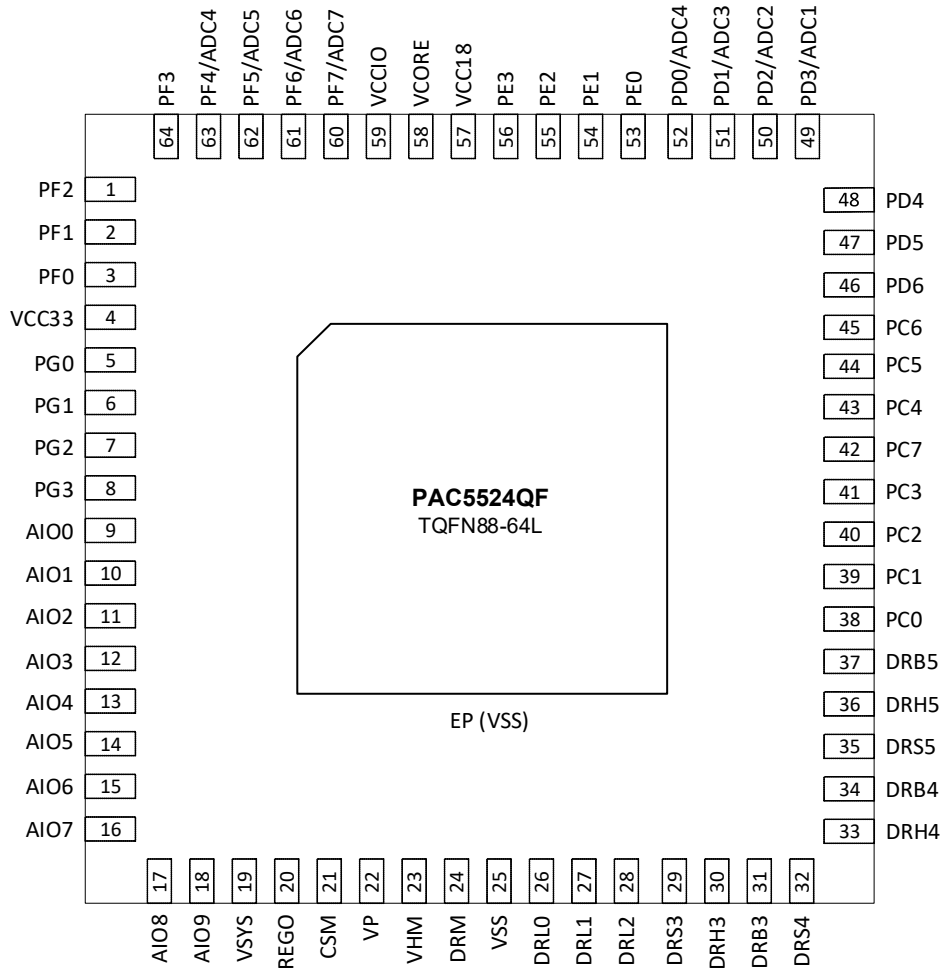
High Pin-Count 70V Motor Controller and Driver for BLDC Motors

20 Thermal Characteristics

Table 34 Thermal Characteristics

| SYMBOL | PARAMETER | VALUE | UNIT |
|---------------|--|------------|------|
| T_A | Operating ambient temperature range | -40 to 105 | °C |
| T_J | Operating junction temperature range | -40 to 125 | °C |
| T_{STG} | Storage temperature range | -55 to 150 | °C |
| | Lead temperature (Soldering, 10 seconds) | 300 | °C |
| Θ_{JC} | Junction-to-case thermal resistance | 2.897 | °C/W |
| Θ_{JA} | Junction-to-ambient thermal resistance | 23.36 | °C/W |

21 Pin Configuration and Description



Top View

21.1 MPPM and System Pin Descriptions

| Pin Number | Pin Name | Description |
|------------|----------|---|
| 4 | VCC33 | Internally generated 3.3V power supply. Connect to a 2.2 μ F or higher value ceramic capacitor from V _{CC33} to V _{SSA} . |
| 19 | VSYS | 5V System power supply. Connect to a 6.8 μ F (20%) or higher ceramic capacitor from V _{SYS} to V _{SS} . |
| 20 | REGO | System regulator output. Connect to V _{SYS} directly or through an external power-dissipating resistor. |
| 21 | CSM | Switching supply current sense input. Connect to the positive side of the current sense resistor. |
| 22 | VP | Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 0.1 μ F ceramic capacitor from V _P to V _{SS} for voltage loop stabilization. This pin requires good capacitive bypassing to V _{SS} , so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin. |
| 23 | VHM | Switching supply controller supply input. Connect a 1 μ F or higher value ceramic capacitor, or a 0.1 μ F ceramic capacitor in parallel with a 10 μ F or higher electrolytic capacitor from V _{HM} to V _{SSP} . This pin requires good capacitive bypassing to V _{SSP} , so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin. |
| 24 | DRM | Switching supply driver output. Connect to the base or gate of the external power NPN or n-channel MOSFET. See User Guide and application notes. |
| 25 | VSS | Ground. |
| 57 | VCC18 | Internally generated 1.8V power supply. Connect a 2.2 μ F or higher value ceramic capacitor from V _{CC18} to V _{SSA} . |
| 58 | VCORE | Internally generated 1.2V core power supply. Connect a 2.2 μ F or higher value ceramic capacitor from V _{CORE} to V _{SSA} . |
| 59 | VCCIO | Internally generated digital I/O 3.3V power supply. Connect a 4.7 μ F or higher value ceramic capacitor from V _{CCIO} to V _{SSA} . |
| EP | EP (VSS) | Exposed pad. Must be connected to V _{SS} in a star ground configuration. Connect to a large PCB copper area for power dissipation heat sinking. |
| 4 | VCC33 | Internally generated 3.3V power supply. Connect to a 2.2 μ F or higher value ceramic capacitor from V _{CC33} to V _{SSA} . |
| 19 | VSYS | 5V System power supply. Connect to a 6.8 μ F (20%) or higher ceramic capacitor from V _{SYS} to V _{SS} . |
| 20 | REGO | System regulator output. Connect to V _{SYS} directly or through an external power-dissipating resistor. |
| 21 | CSM | Switching supply current sense input. Connect to the positive side of the current sense resistor. |
| 22 | VP | Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 0.1 μ F ceramic capacitor from V _P to V _{SS} for voltage loop stabilization. This pin requires good capacitive bypassing to V _{SS} , so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin. |
| 23 | VHM | Switching supply controller supply input. Connect a 1 μ F or higher value ceramic capacitor, or a 0.1 μ F ceramic capacitor in parallel with a 10 μ F or higher electrolytic capacitor from V _{HM} to V _{SSP} . This pin requires good capacitive bypassing to V _{SSP} , so the ceramic capacitor must be connected with a shorter than 10mm trace from the pin. |
| 24 | DRM | Switching supply driver output. Connect to the base or gate of the external power NPN or n-channel MOSFET. See User Guide and application notes. |
| 25 | VSS | Ground. |
| 57 | VCC18 | Internally generated 1.8V power supply. Connect a 2.2 μ F or higher value ceramic capacitor from V _{CC18} to V _{SSA} . |
| 58 | VCORE | Internally generated 1.2V core power supply. Connect a 2.2 μ F or higher value ceramic capacitor from V _{CORE} to V _{SSA} . |
| 59 | VCCIO | Internally generated digital I/O 3.3V power supply. Connect a 4.7 μ F or higher value ceramic capacitor from V _{CCIO} to V _{SSA} . |
| EP | EP (VSS) | Exposed pad. Must be connected to V _{SS} in a star ground configuration. Connect to a large PCB copper area for power dissipation heat sinking. |



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

21.2 CAFE Pin Descriptions

| Pin Number | Pin Name | Function | Type | Description |
|------------|----------|----------|--------|------------------------------------|
| 9 | AIO0 | AIO0 | I/O | Analog front end I/O 0. |
| | | DA0N | Analog | Differential PGA 0 negative input. |
| 10 | AIO1 | AIO1 | I/O | Analog front end I/O 1. |
| | | DA0P | Analog | Differential PGA 0 positive input. |
| 11 | AIO2 | AIO2 | I/O | Analog front end I/O 2. |
| | | DA1N | Analog | Differential PGA 1 negative input. |
| 12 | AIO3 | AIO3 | I/O | Analog front end I/O 3. |
| | | DA1P | Analog | Differential PGA 1 positive input. |
| 13 | AIO4 | AIO4 | I/O | Analog front end I/O 4. |
| | | DA2N | Analog | Differential PGA 2 negative input. |
| 14 | AIO5 | AIO5 | I/O | Analog front end I/O 5. |
| | | DA2P | Analog | Differential PGA 2 positive input. |
| 15 | AIO6 | AIO6 | I/O | Analog front end I/O 6. |
| | | AMP6 | Analog | PGA input 6. |
| | | CMP6 | Analog | Comparator input 6. |
| | | BUF6 | Analog | Buffer output 6. |
| | | PBTN | Analog | Push button input. |
| 16 | AIO7 | AIO7 | I/O | Analog front end I/O 7. |
| | | AMP7 | Analog | PGA input 7. |
| | | CMP7 | Analog | Comparator input 7. |
| | | PHC7 | Analog | Phase comparator input 7. |
| 17 | AIO8 | AIO8 | I/O | Analog front end I/O 8. |
| | | AMP8 | Analog | PGA input 8. |
| | | CMP8 | Analog | Comparator input 8. |
| | | PHC8 | Analog | Phase comparator input 8. |
| 18 | AIO9 | AIO9 | I/O | Analog front end I/O 9. |
| | | AMP9 | Analog | PGA input 9. |
| | | CMP9 | Analog | Comparator input 9. |
| | | PHC9 | Analog | Phase comparator input 9. |



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

21.3 ASPD Pin Descriptions

| Pin Number | Pin Name | Type | Description |
|------------|----------|--------|------------------------------------|
| 26 | DRL0 | Analog | Low-side gate driver 0. |
| 27 | DRL1 | Analog | Low-side gate driver 1. |
| 28 | DRL2 | Analog | Low-side gate driver 2. |
| 29 | DRS3 | Analog | High-side gate driver source 3. |
| 30 | DRH3 | Analog | High-side gate driver 3. |
| 31 | DRB3 | Analog | High-side gate driver bootstrap 3. |
| 32 | DRS4 | Analog | High-side gate driver source 4. |
| 33 | DRH4 | Analog | High-side gate driver 4. |
| 34 | DRB4 | Analog | High-side gate driver bootstrap 4. |
| 35 | DRS5 | Analog | High-side gate driver source 5. |
| 36 | DRH5 | Analog | High-side gate driver 5. |
| 37 | DRB5 | Analog | High-side gate driver bootstrap 5. |



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

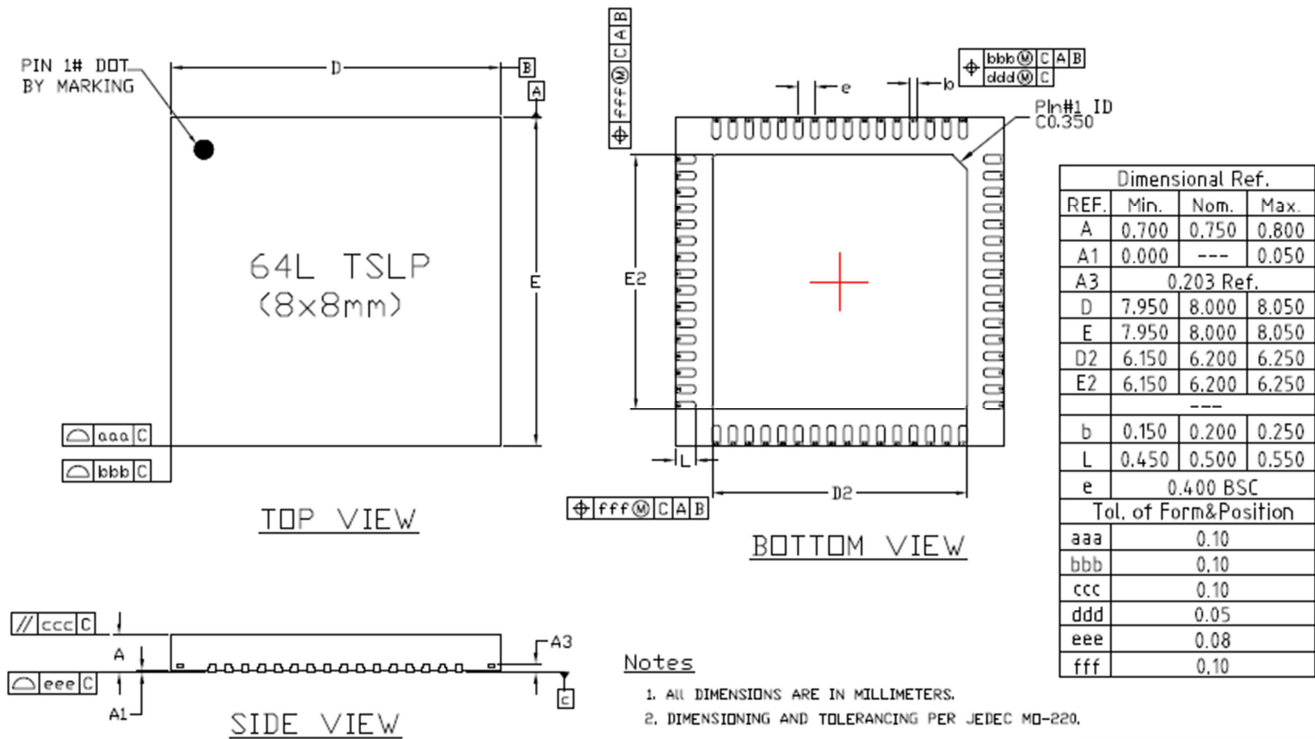
21.4 I/O Ports Pin Descriptions

| Pin Number | Pin Name | Function | Type | Description |
|------------|----------|----------|--------------|-------------------|
| 1 | PF2 | PF2 | I/O | I/O port PF2. |
| 2 | PF1 | PF1 | I/O | I/O port PF1. |
| 3 | PF0 | PF0 | I/O | I/O port PF0. |
| 5 | PG0 | PG0 | I/O | I/O port PG0. |
| 6 | PG1 | PG1 | I/O | I/O port PG1. |
| 7 | PG2 | PG2 | I/O | I/O port PG2. |
| 8 | PG3 | PG3 | I/O | I/O port PG3. |
| 38 | PC0 | PC0 | I/O | I/O port PC0. |
| 39 | PC1 | PC1 | I/O | I/O port PC1. |
| 40 | PC2 | PC2 | I/O | I/O port PC2. |
| 41 | PC3 | PC3 | I/O | I/O port PC3. |
| 42 | PC7 | PC7 | I/O | I/O port PC7. |
| 43 | PC4 | PC4 | I/O | I/O port PC4. |
| 44 | PC5 | PC5 | I/O | I/O port PC5. |
| 45 | PC6 | PC6 | I/O | I/O port PC6. |
| 46 | PD6 | PD6 | I/O | I/O port PD6. |
| 47 | PD5 | PD5 | I/O | I/O port PD5. |
| 48 | PD4 | PD4 | I/O | I/O port PD4. |
| 49 | PD3 | PD3 | I/O | I/O port PD3. |
| | | AD1 | Analog Input | ADC channel ADC1. |
| 50 | PD2 | PD2 | I/O | I/O port PD2. |
| | | AD2 | Analog Input | ADC channel ADC2. |
| 51 | PD1 | PD1 | I/O | I/O port PD1. |
| | | AD3 | Analog Input | ADC channel ADC3. |
| 52 | PD0 | PD0 | I/O | I/O port PD0. |
| | | AD4 | Analog Input | ADC channel ADC4. |
| 53 | PE0 | PE0 | I/O | I/O port PE0. |
| 54 | PE1 | PE1 | I/O | I/O port PE1. |
| 55 | PE2 | PE2 | I/O | I/O port PE2. |
| 56 | PE3 | PE3 | I/O | I/O port PE3. |
| 60 | PF7 | PF7 | I/O | I/O port PF7. |
| | | AD7 | Analog Input | ADC channel ADC7. |
| 61 | PF6 | PF6 | I/O | I/O port PF6. |
| | | AD6 | Analog Input | ADC channel ADC6. |
| 62 | PF5 | PF5 | I/O | I/O port PF5. |
| | | AD5 | Analog Input | ADC channel ADC5. |
| 63 | PF4 | PF4 | I/O | I/O port PF4. |
| | | AD4 | Analog Input | ADC channel ADC4. |
| 64 | PF3 | PF3 | I/O | I/O port PF3. |

22 Mechanical Information

Package Marking and Dimensions

Marking: Part number – PAC5524QF



Notes:

1. All dimensions are in mm. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

23 Handling Precautions

| Parameter | Rating | Standard |
|----------------------------------|----------|------------------------|
| ESD – Human Body Model (HBM) | Class 1A | ESDA/JEDEC JS-001-2012 |
| ESD – Charged Device Model (CDM) | Class C3 | JEDEC JESD22-C101F |
| MSL – Moisture Sensitivity Level | Level 3 | IPC/JEDEC J-STD-020 |



Caution!

ESD sensitive device

24 Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.



PAC5524

High Pin-Count 70V Motor Controller and Driver for BLDC Motors

25 Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

26 Important Notice

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