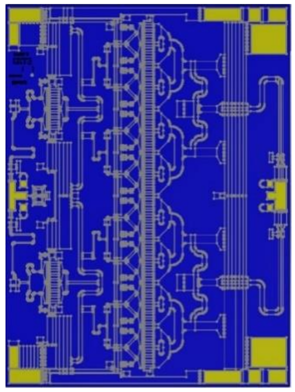
QPA1017D

5.7 – 7 GHz 50 Watt GaN Power Amplifier



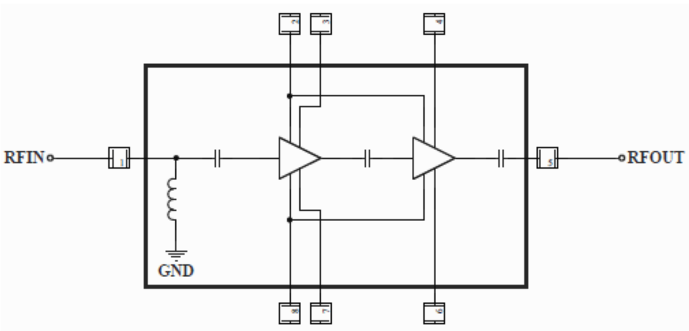
Product Overview

Qorvo's QPA1017D is a high power MMIC amplifier fabricated on Qorvo's production 0.15 um GaN on SiC process (QGaN15). The QPA1017D operates from 5.7 – 7.0 GHz, provides 50 W of saturated output power with 21 dB of large signal gain and greater than 40% power–added efficiency. For satellite communications applications, QPA1017D provides 25 W linear power with 25 dBc third order intermodulation distortion products.

To simplify system integration, QPA1017D is fully matched to 50 ohms. Input port is DC grounded for improved ESD performance, output port is AC coupled with integrated DC blocking capacitor.

Lead-free and RoHS compliant

Functional Block Diagram



Key Features

- Frequency Range: 5.7 – 7 GHz
- P_{SAT} (P_{IN} = 26 dBm): > 47 dBm
- PAE (P_{IN} = 26 dBm): > 40 %
- Power Gain (P_{IN} = 26 dBm): > 21 dB
- IM3 (P_{OUT}/Tone = 41 dBm): -25 dBc
- Small Signal Gain: > 28 dB
- Bias: V_D = +24 V, I_{DQ} = 1.5 A, V_G = -2.5 V typ.
- Die Dimensions: 4.79 x 6.45 x 0.10 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Applications

- C-Band Radar
- Satellite Communications

Ordering Information

Part No.	Description
QPA1017D	5.7 – 7 GHz 50 Watt GaN Amplifier (10 pcs.)
QPA1017DS2	Samples (2 pcs. pack)
QPA1017DEVB	Evaluation Board for QPA1017D

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-6 V to 0 V
Drain Current (I_D)	10 A
Gate Current (I_G)	See plot page 20
Power Dissipation (P_{DISS}), 85 °C	Pulsed, 180 W CW, 100 W
Input Power (P_{IN}), Pulsed and CW, 50 Ω, V_D = 24 V, I_{DQ} = 1.5 A, T_{BASE} = 85 °C,	32 dBm*
Input Power (P_{IN}), Pulsed and CW, 3:1 VSWR, V_D = 24 V, I_{DQ} = 1.5 A , T_{BASE} = 85 °C	32 dBm*
Mounting Temperature (30 seconds)	320 ºC
Storage Temperature	-55 to +150 ºC

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.
* Robustness guaranteed over 5.7-7.0 GHz. Out of band operation not recommended

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Drain Voltage (V_D)		+24	+28	V
Drain Current, Quiescent (I_{DQ})		1.5		A
Drain Current, RF (I_{D_Drive})	See chart page 4, 6			A
Gate Voltage Typ. Range (V_G)	−2 to -2.9			V
Gate Current, RF (I_{G_Drive})	See chart page 4, 6			mA
Operating Temp. Range (T_{BASE})	−40		+85	ºC

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

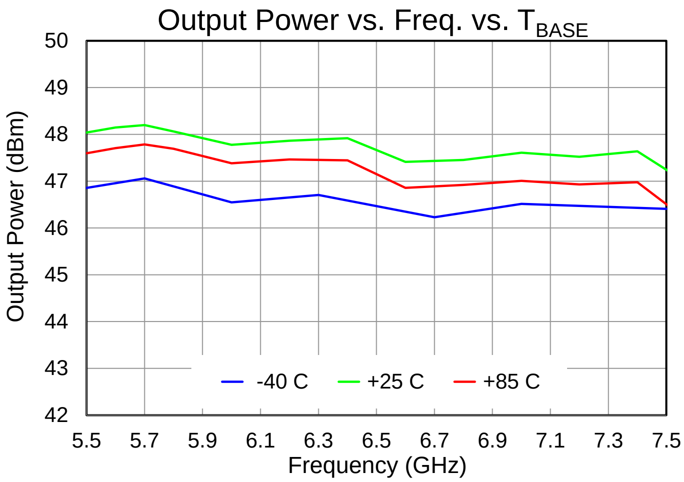
Parameter	Conditions [(1) (2)]	Min	Typ.	Max	Units
Operational Frequency Range		5.7		7	GHz
Output Power at Saturation, P_{SAT}	P_{IN} = +26 dBm, Pulsed		47		dBm
Large Signal Gain	P_{IN} = +26 dBm, Pulsed		22		dB
Small Signal Gain, S21	CW		28		dB
Input Return Loss, IRL	CW		8		dB
Output Return Loss, ORL	CW		5		dB
3RD Intermodulation Products, IM3	P_{OUT}/Tone = 41 dBm; Freq. = 5.7, 6.4, 7 GHz; Δf = 20 MHz, CW		-25		dBc
5TH Intermodulation Products, IM5	P_{OUT}/Tone = 41 dBm; Freq. = 35 GHz; Δf = 20 MHz, CW		-35		dBc
P_{SAT} Temperature Coefficient	T_{DIFF} = −40 ºC to +85 ºC; P_{IN} = +26 dBm, Pulsed		-0.007		dBm/ºC
S21 Temperature Coefficient	T_{DIFF} = −40 ºC to +85 ºC, CW		-0.065		dB/ºC

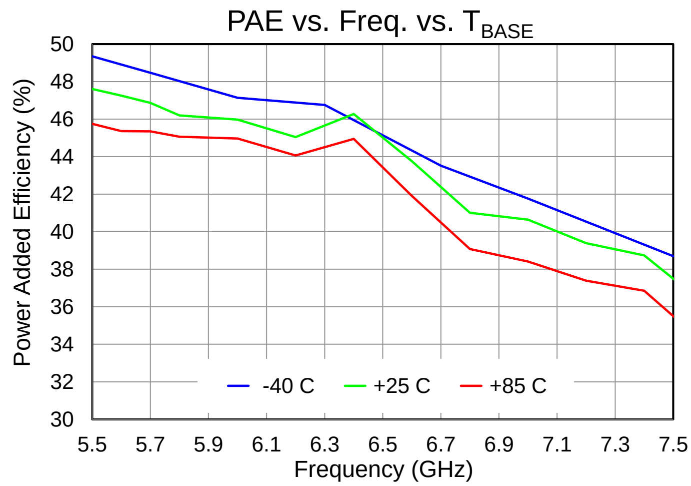
Notes:

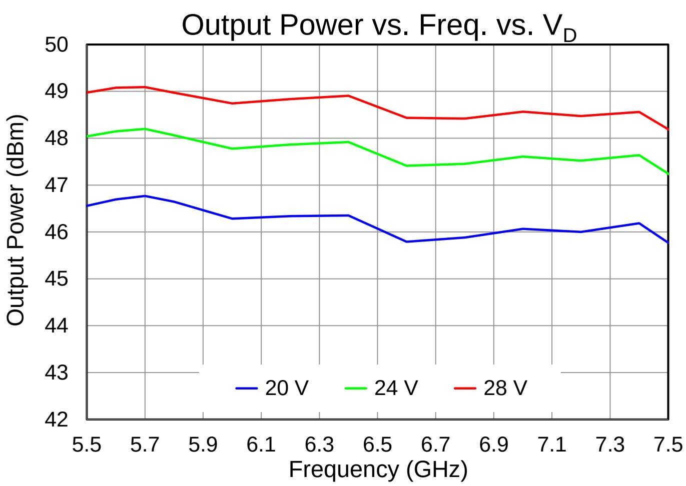
1. Test conditions unless otherwise noted: Pulsed V_D = +24 V, I_{DQ} = 1.5 A, V_G = -2.5V +/- typical, DC = 20%, PW = 150 us, T_{BASE} = +25 ºC, Z_0 = 50 Ω
2. T_{BASE} is back side of 40 mil CuMo carrier plate with AuSn solder

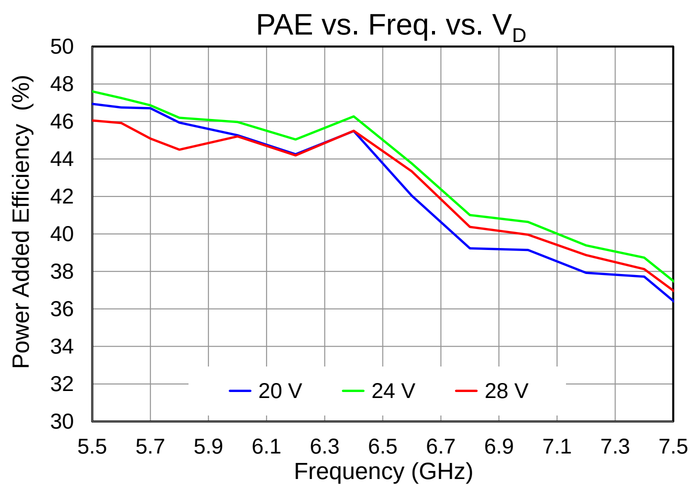
Performance Plots – Large Signal

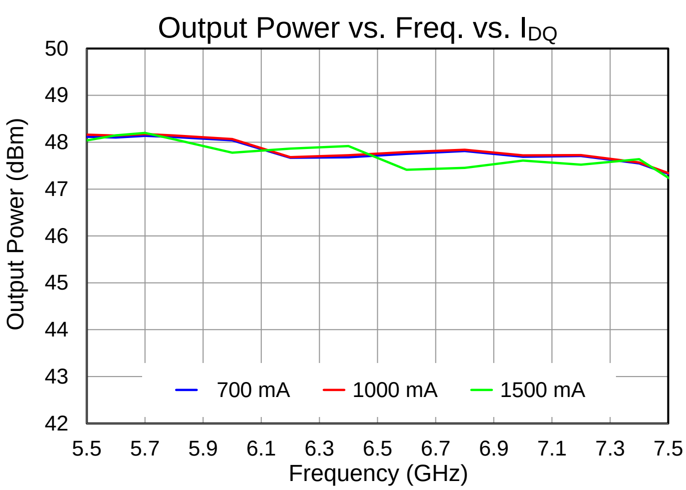
Test conditions, unless otherwise noted: **Pulsed** V_D = 24 V, I_{DQ} = 1.5 A, Duty Cycle = 20%, PW = 150 us, P_{IN} = 26 dBm, T_{BASE} = +25 ºC

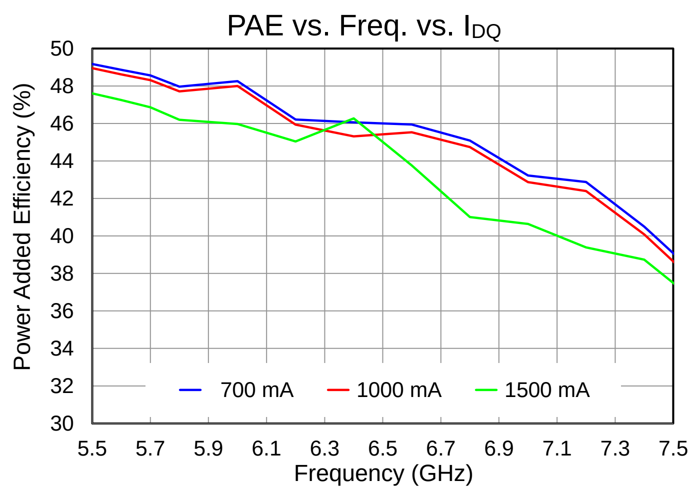








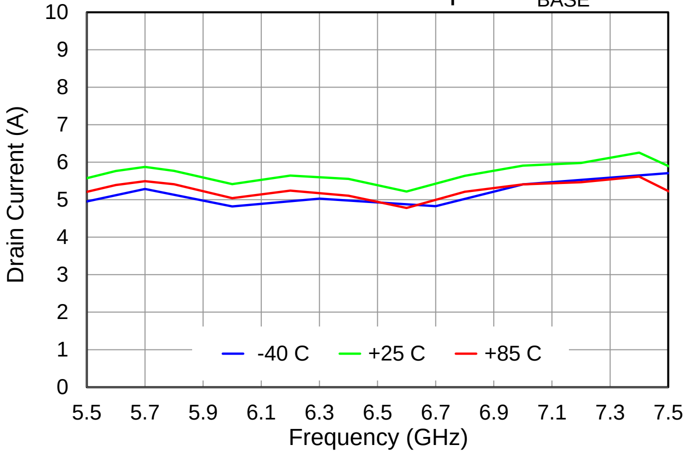




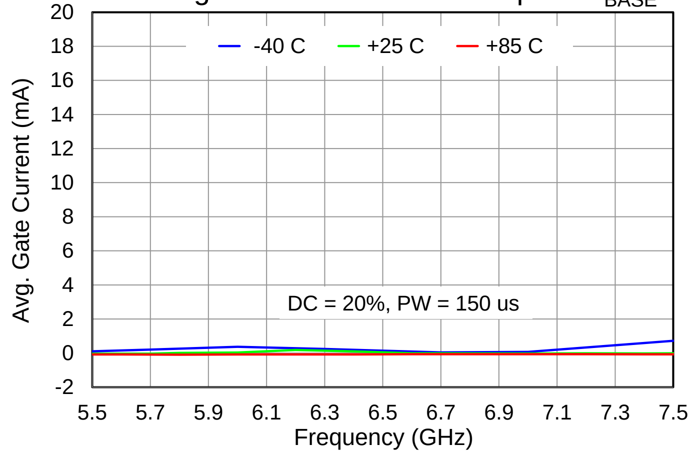
Performance Plots – Large Signal

Test conditions, unless otherwise noted: **Pulsed** V_D = 24 V, I_{DQ} = 1.5 A, Duty Cycle = 20%, PW = 150 us, P_{IN} = 26 dBm, T_{BASE} = +25 ºC

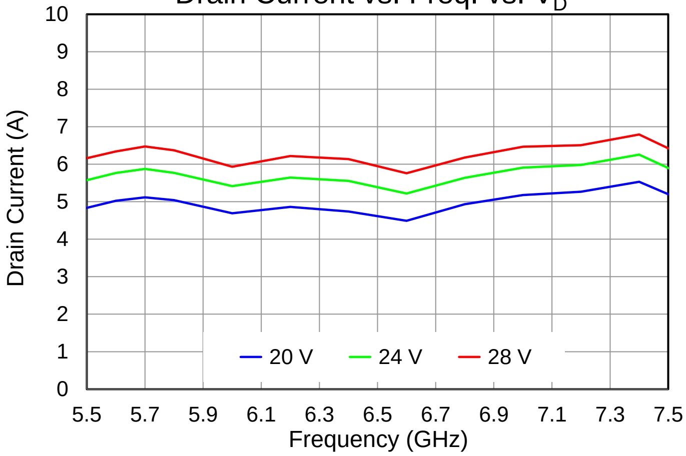
Drain Current vs. Freq. vs. T_{BASE}



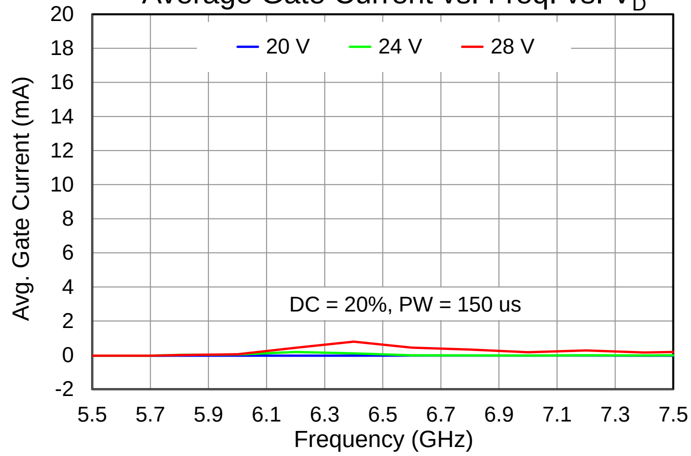
Average Gate Current vs. Freq. vs. T_{BASE}



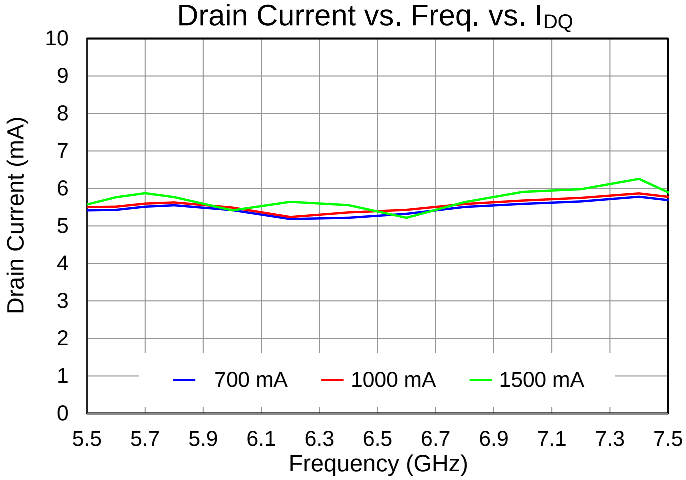
Drain Current vs. Freq. vs. V_D



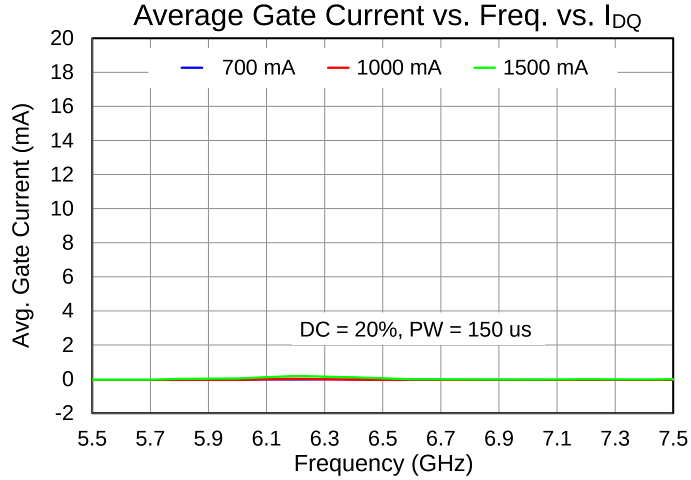
Average Gate Current vs. Freq. vs. V_D



Drain Current vs. Freq. vs. I_{DQ}



Average Gate Current vs. Freq. vs. I_{DQ}



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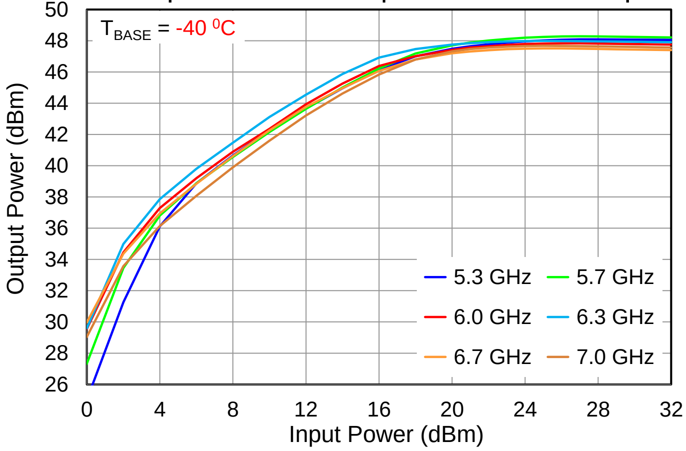
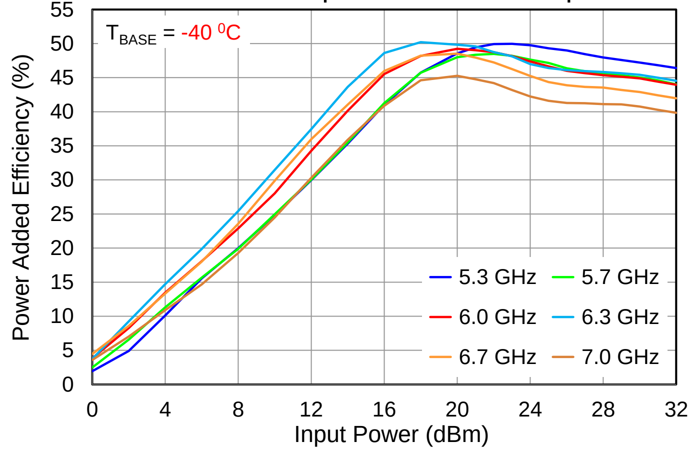
Output Power vs. Input Power vs. Freq.



PAE vs. Input Power vs. Freq.



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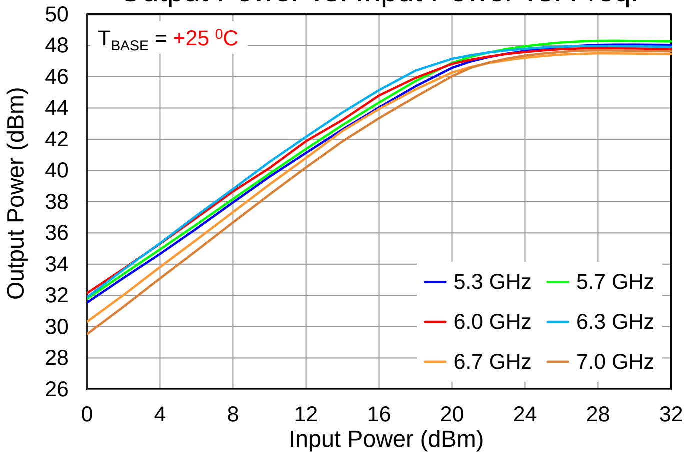

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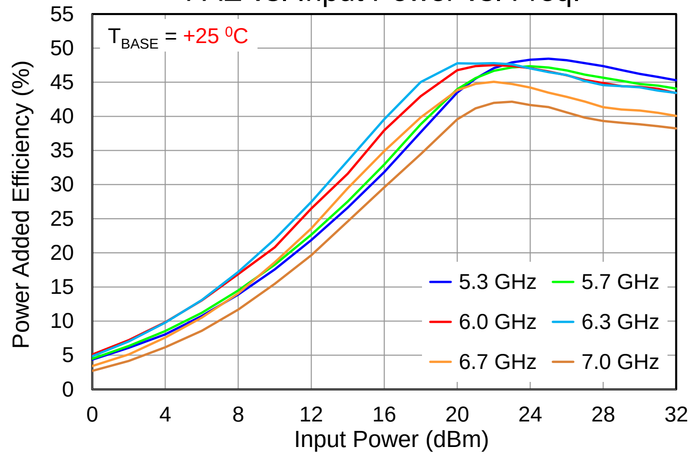

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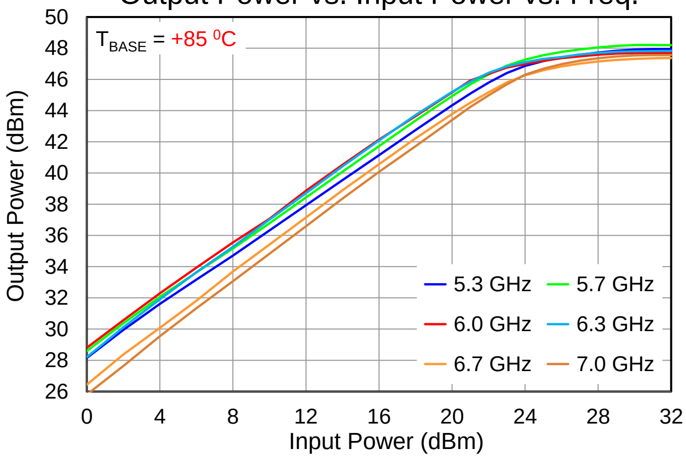

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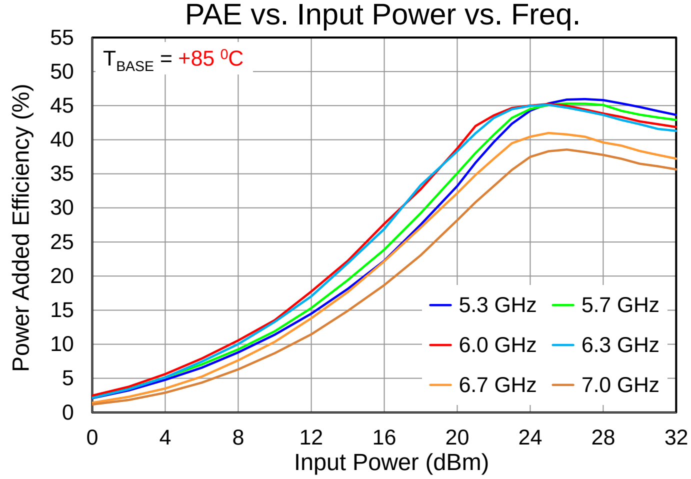

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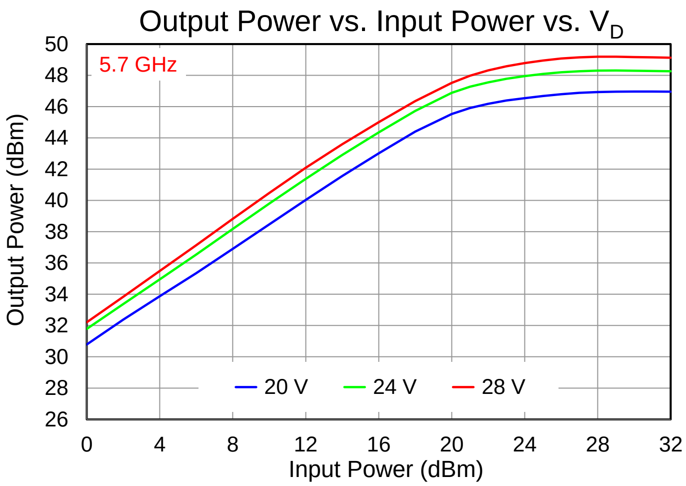

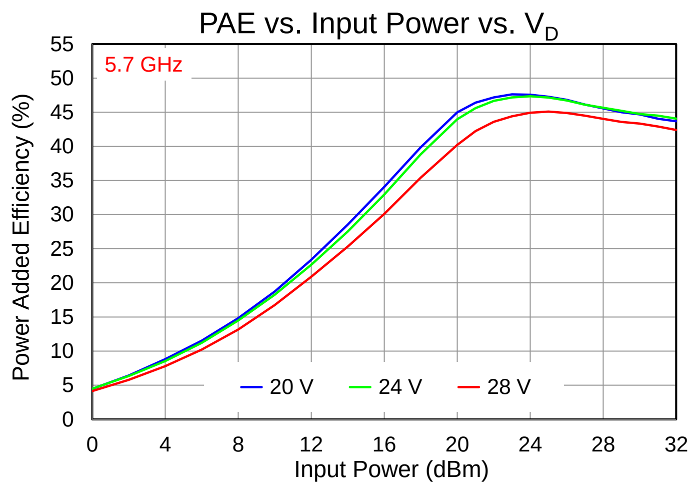

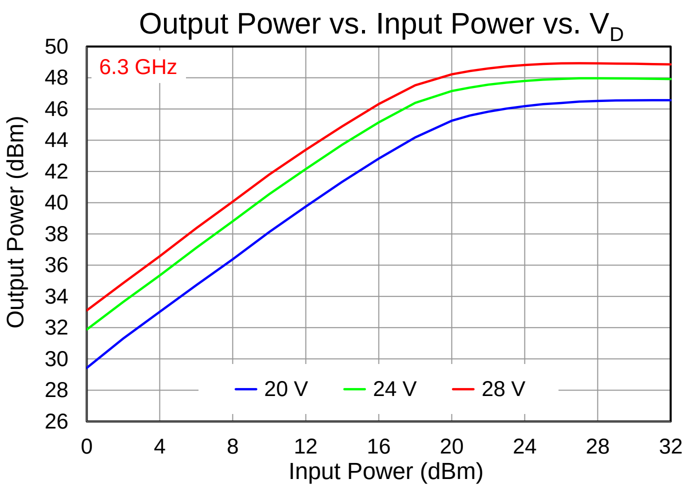

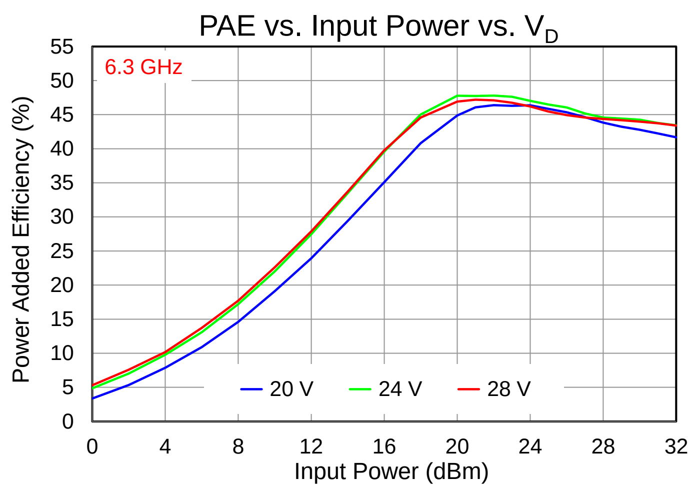

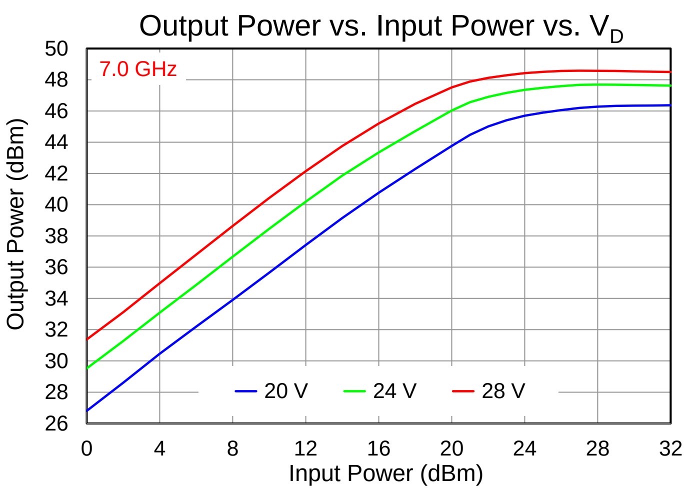

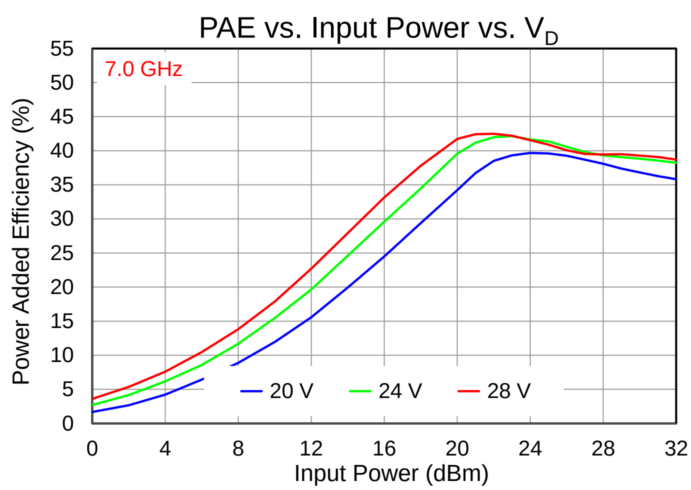

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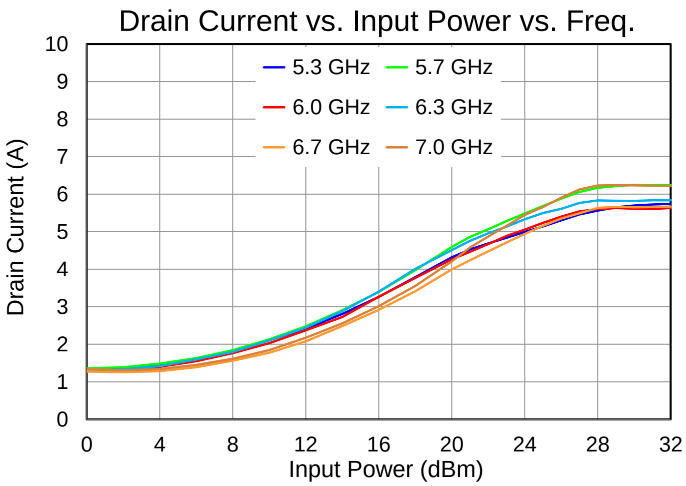

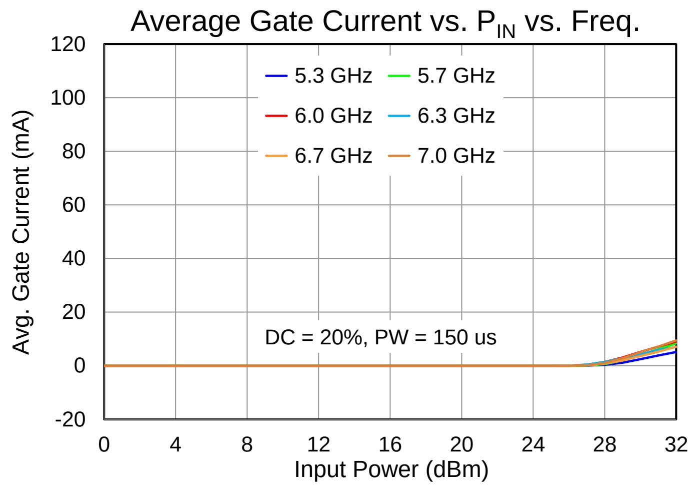

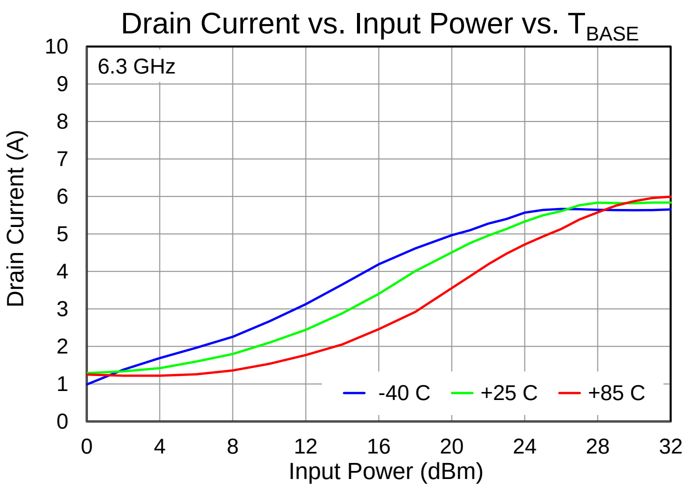

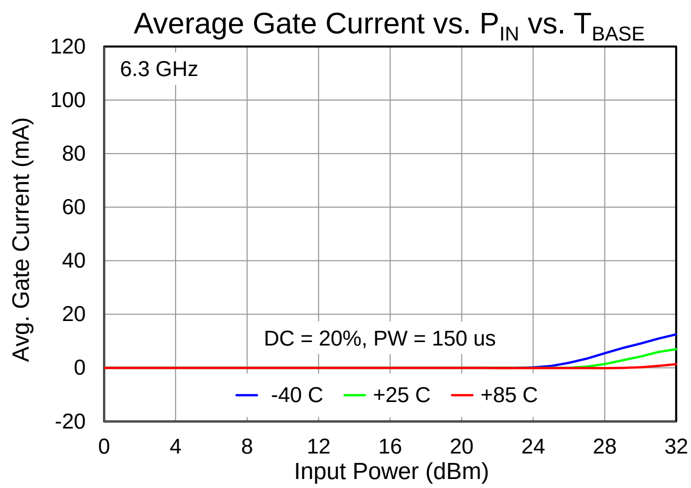

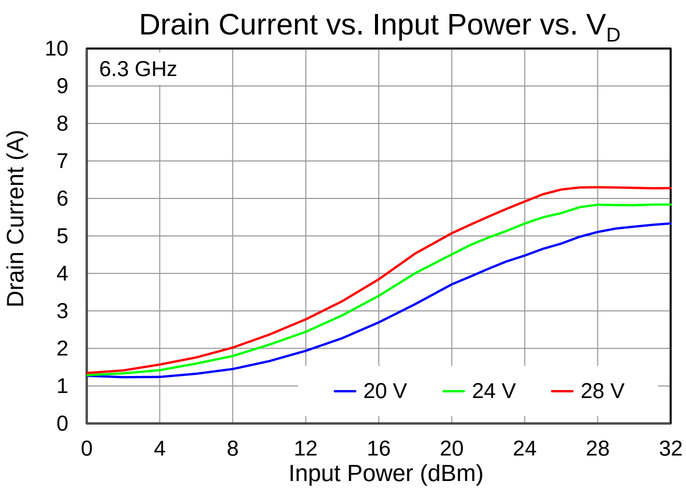

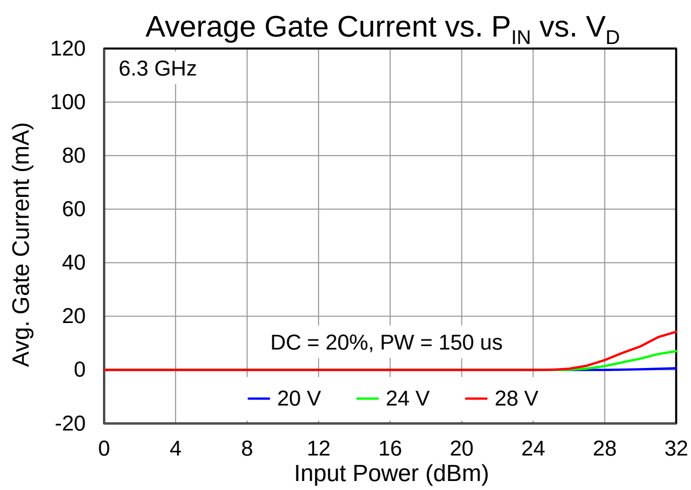

Performance Plots – Large Signal

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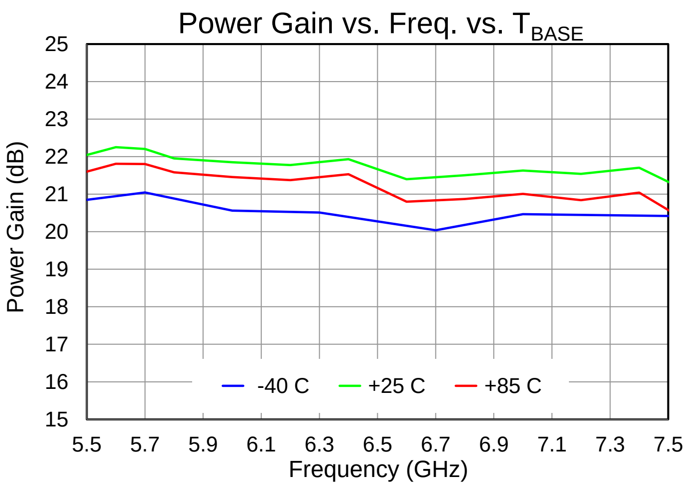
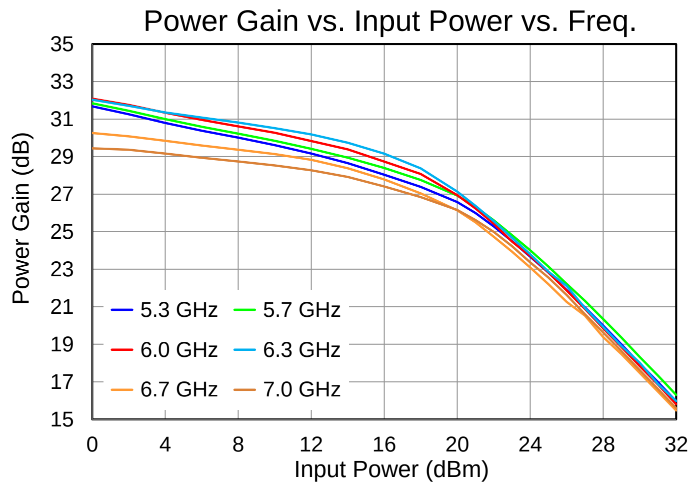
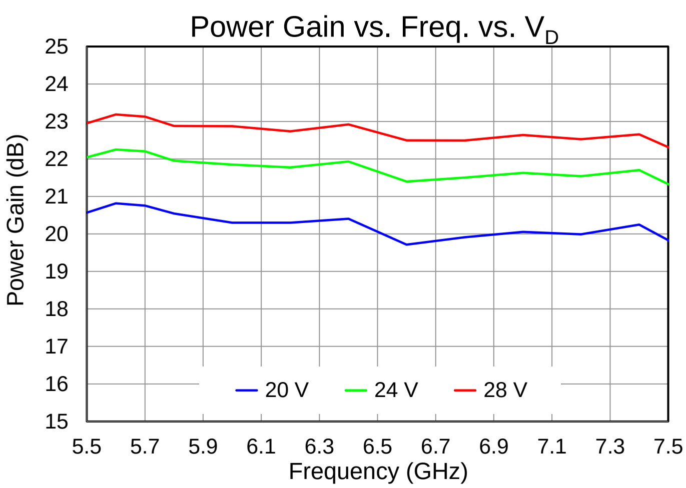
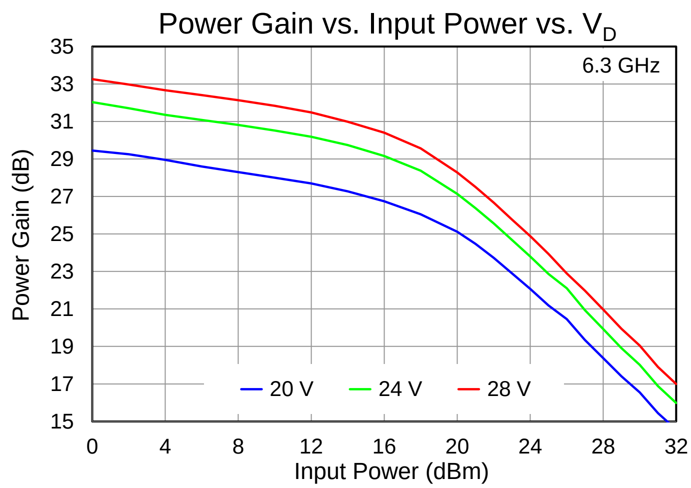
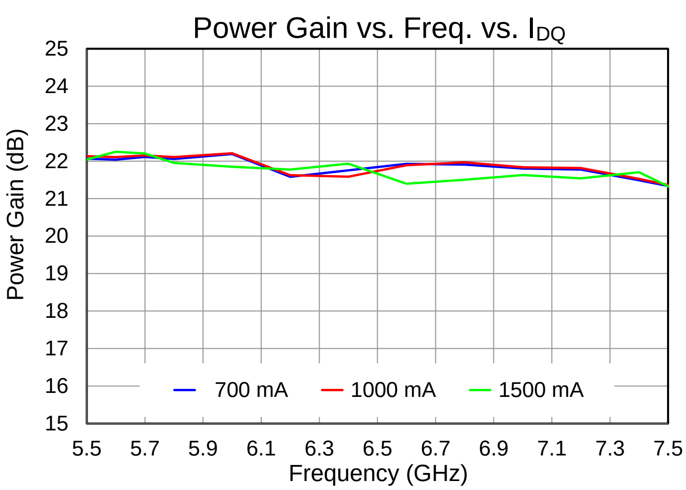
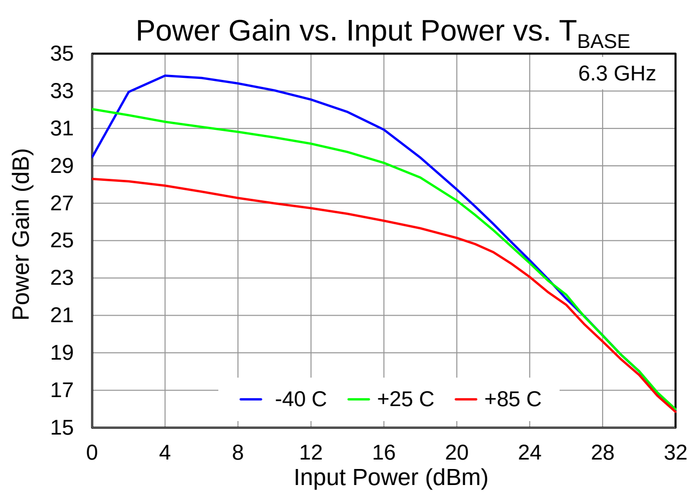






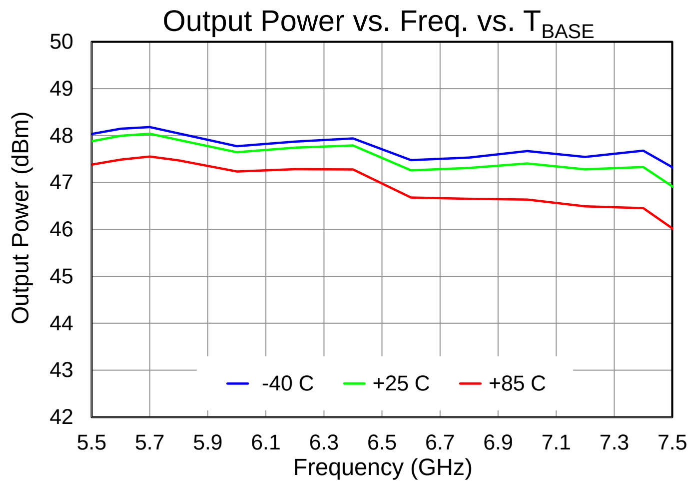


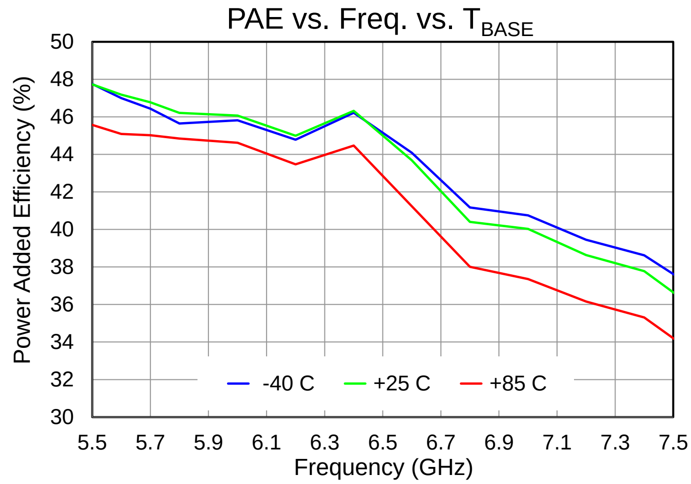


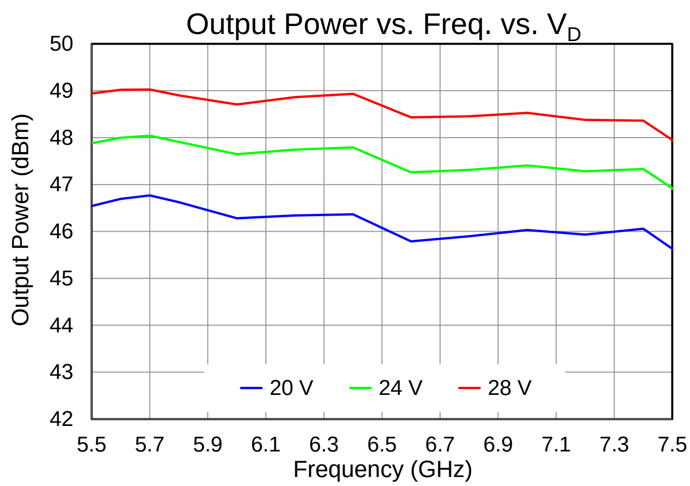


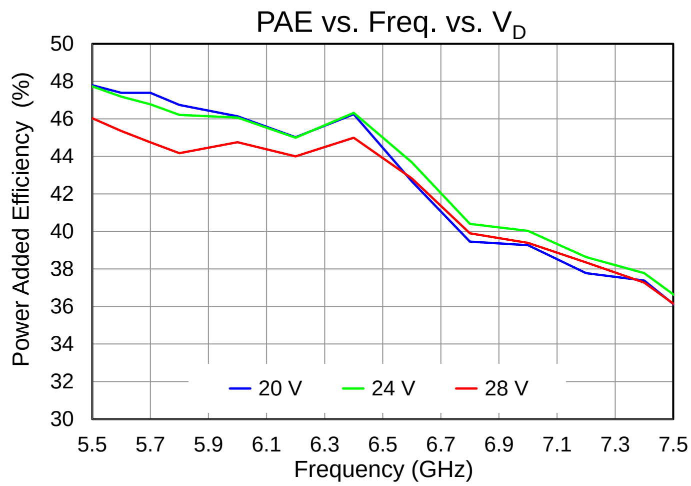
Performance Plots – Large Signal

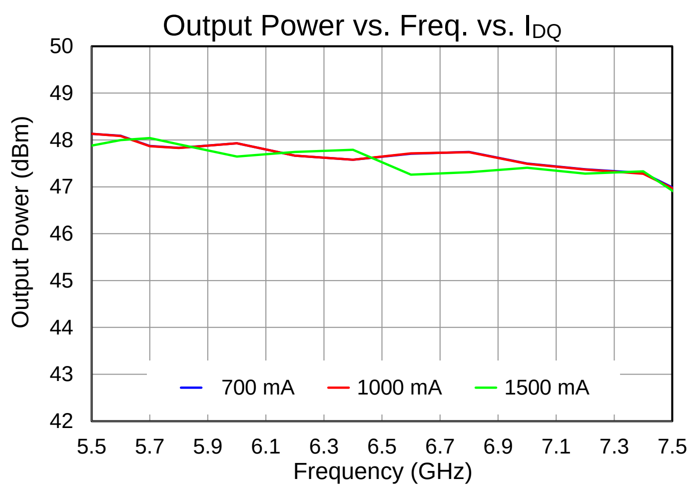
Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 1.5 A, P_{IN} = 26 dBm, T_{BASE} = +25 ºC

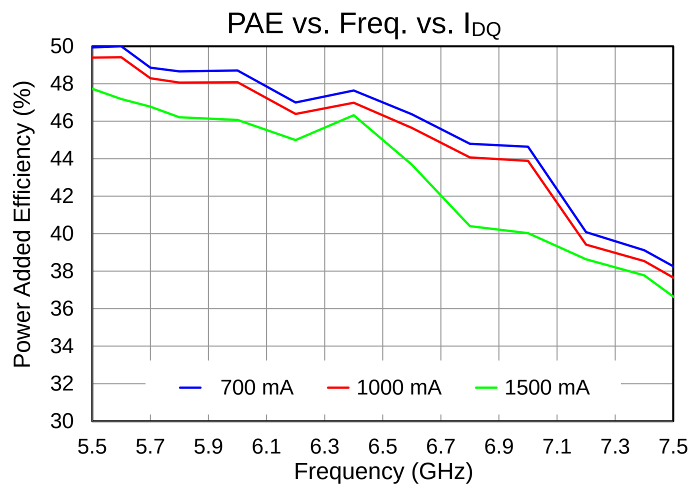






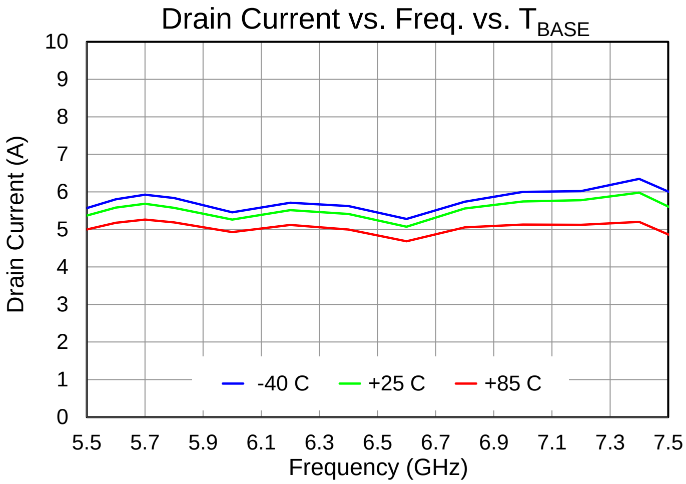


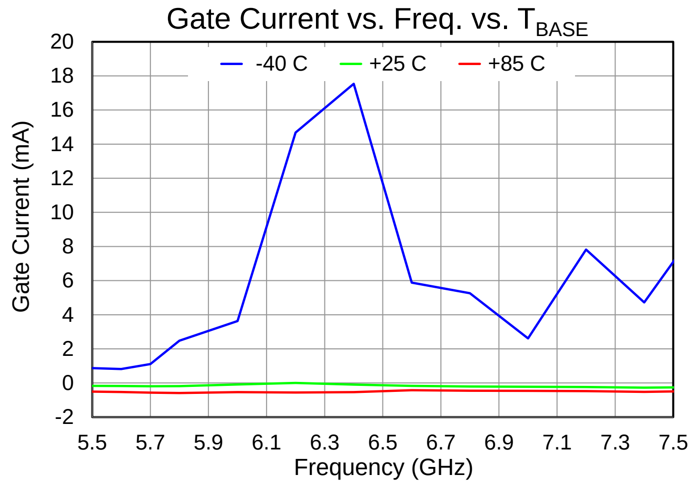


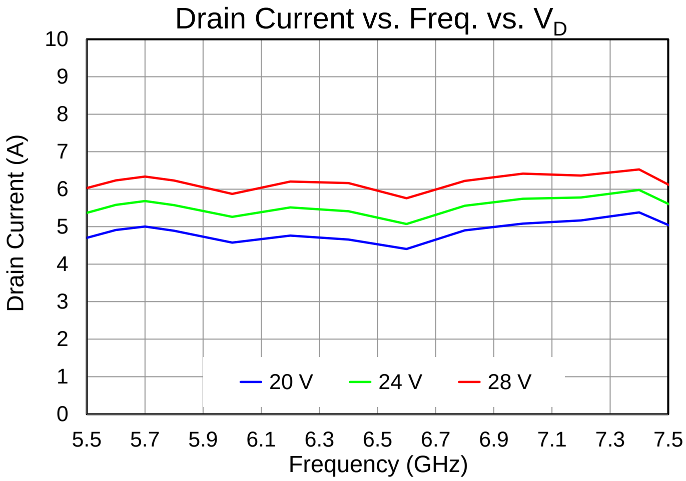


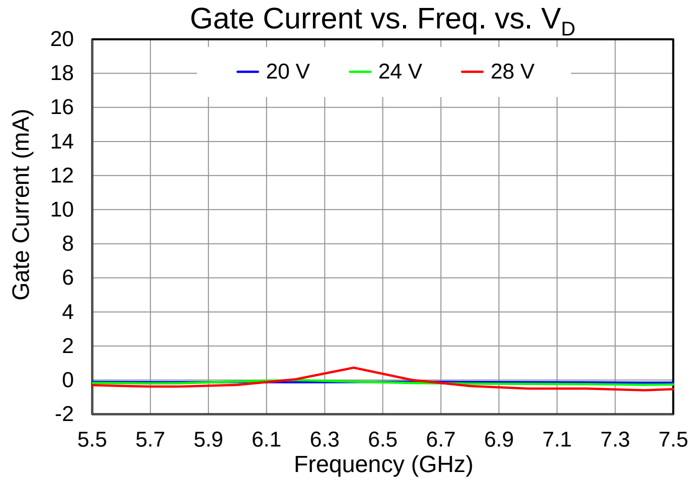
Performance Plots – Large Signal

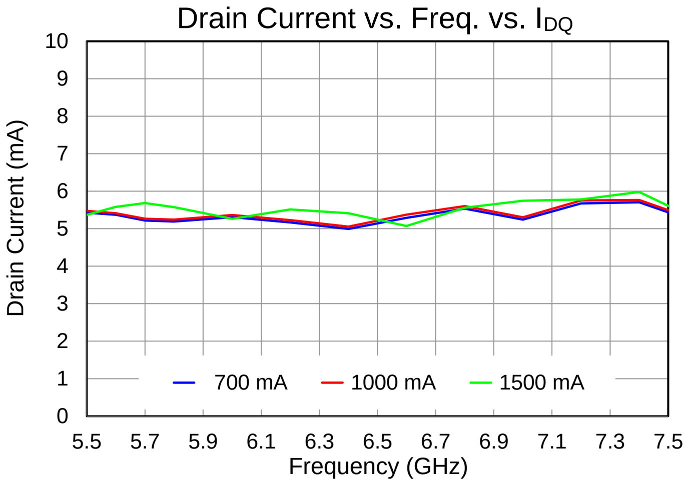
Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 1.5 A, P_{IN} = 26 dBm, T_{BASE} = +25 ºC

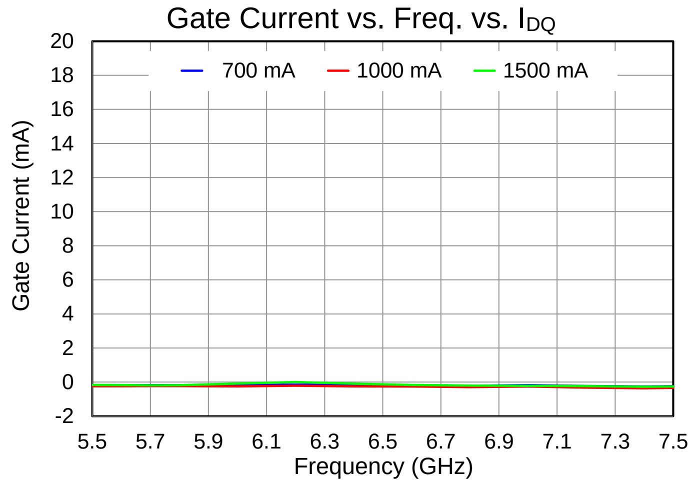








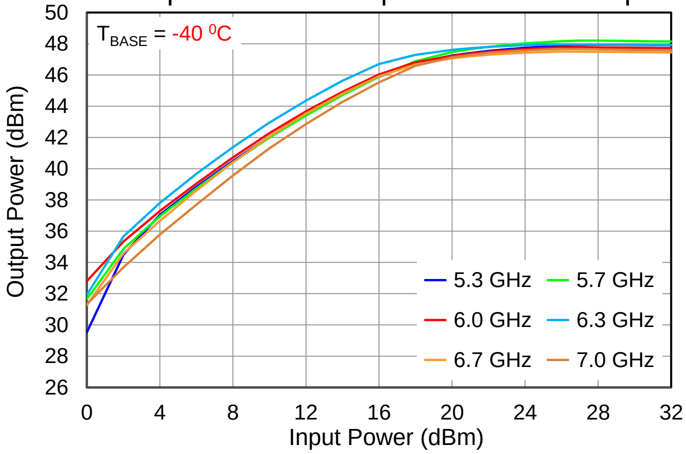




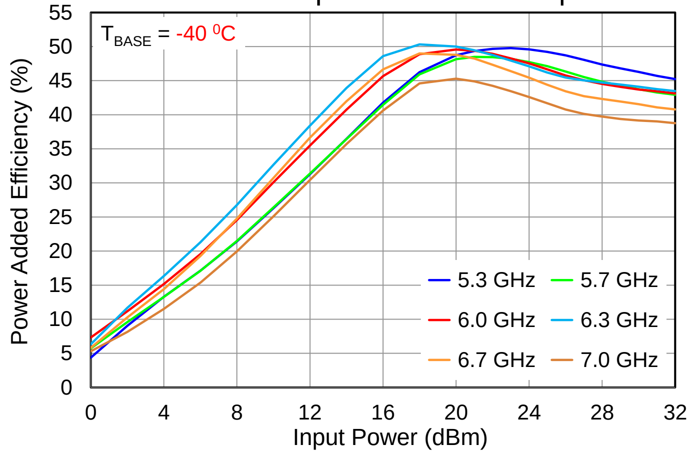
Performance Plots – Large Signal

Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 1.5 A, P_{IN} = 26 dBm, T_{BASE} = +25 ºC

Output Power vs. Input Power vs. Freq.



PAE vs. Input Power vs. Freq.



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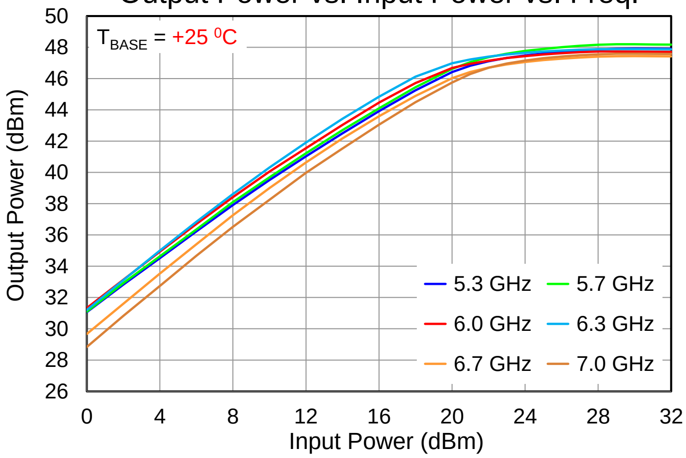
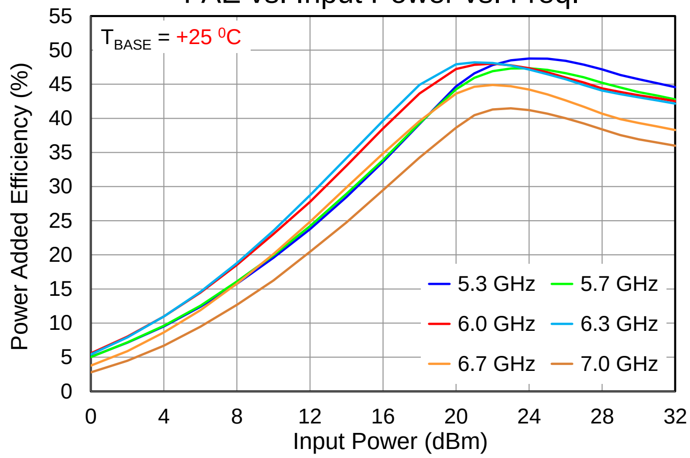


PAE vs. Input Power vs. Freq.



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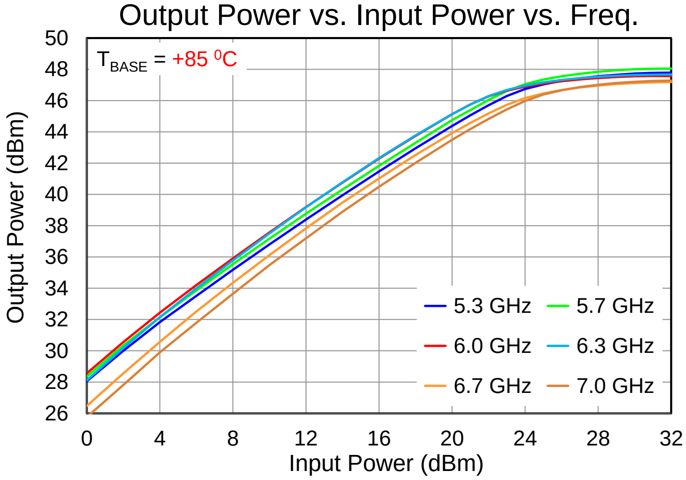

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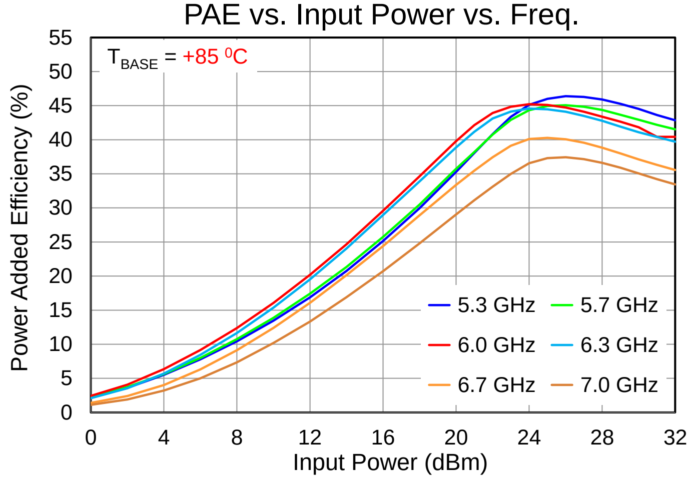

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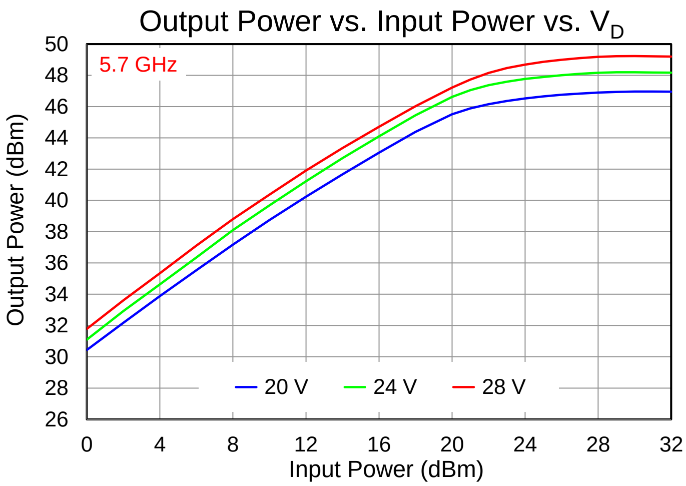
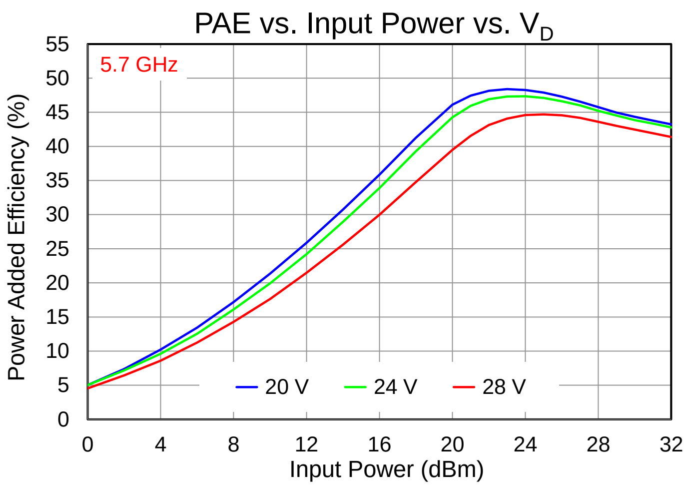
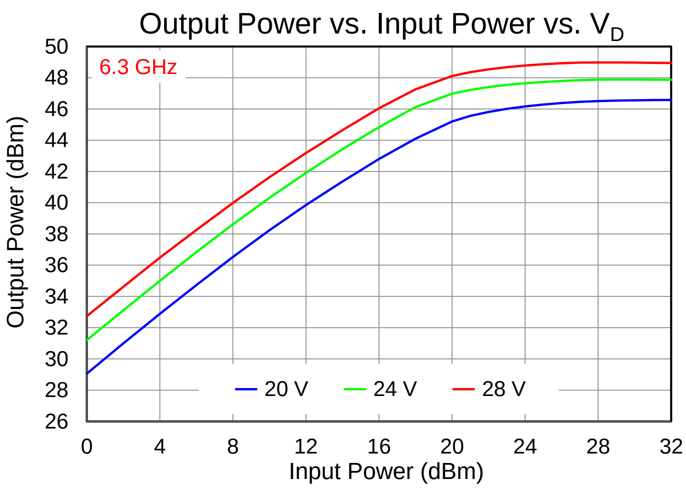
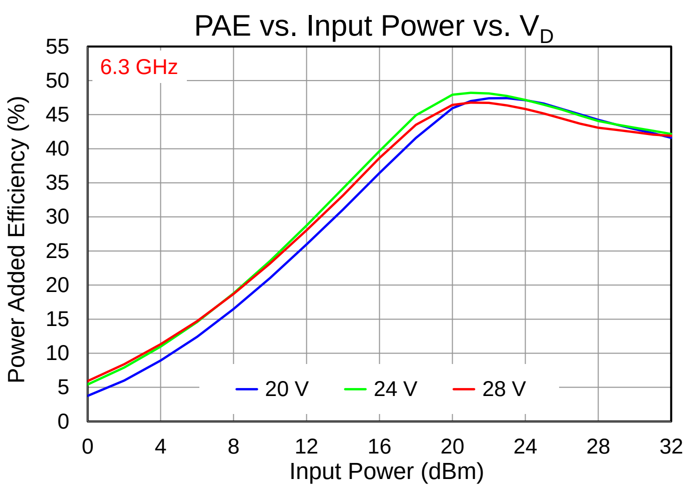
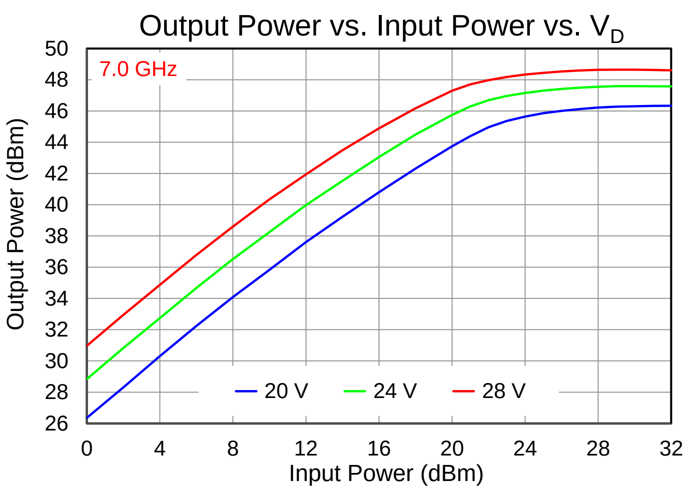
Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 1.5 A, P_{IN} = 26 dBm, T_{BASE} = +25 ºC

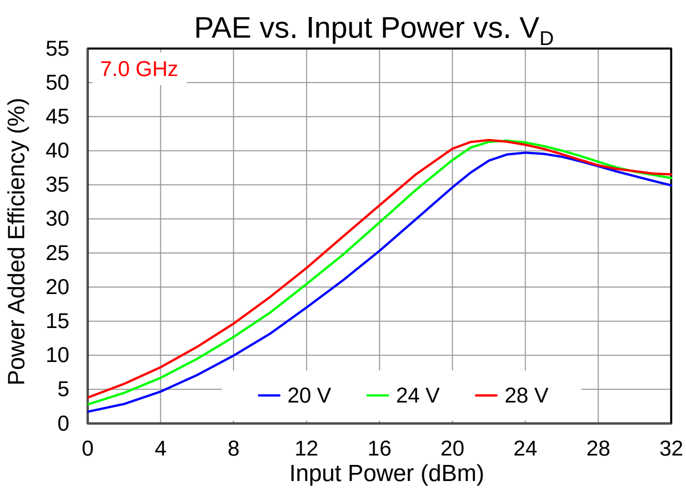






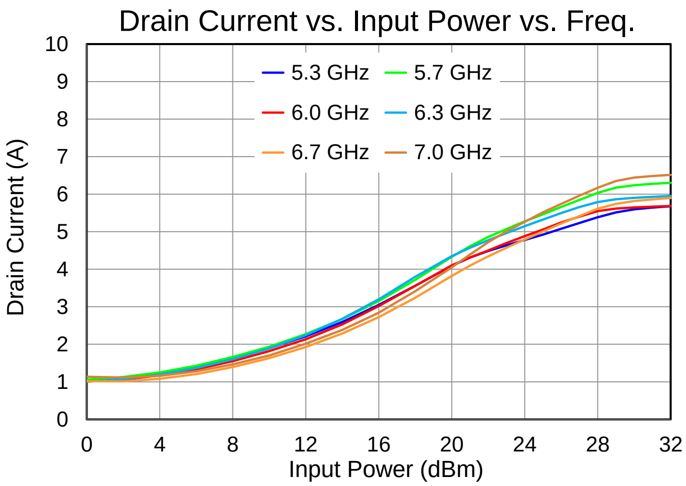


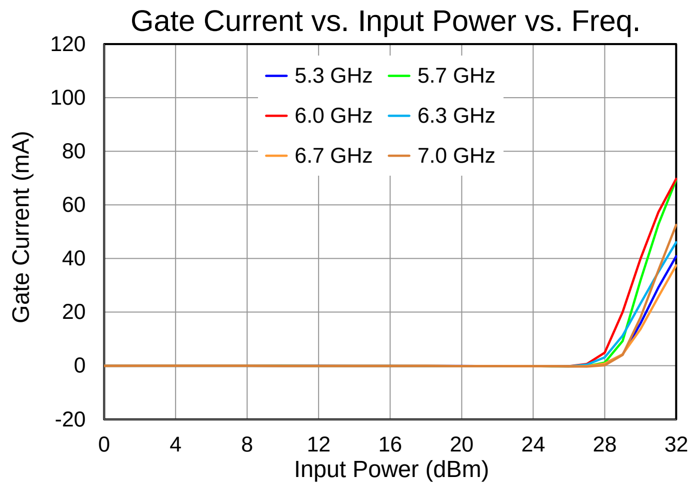


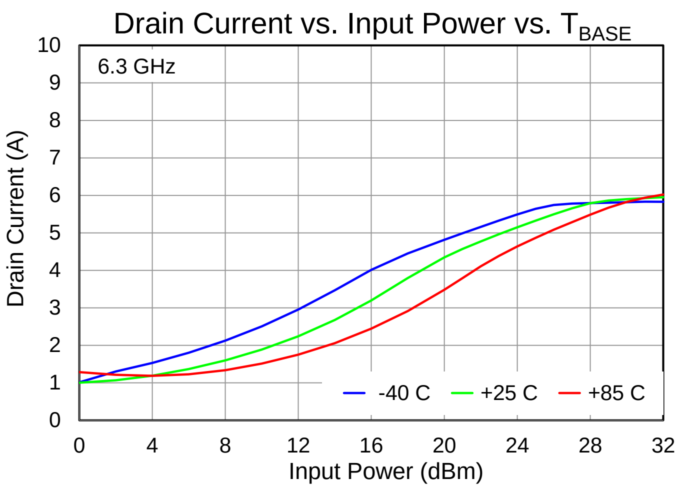


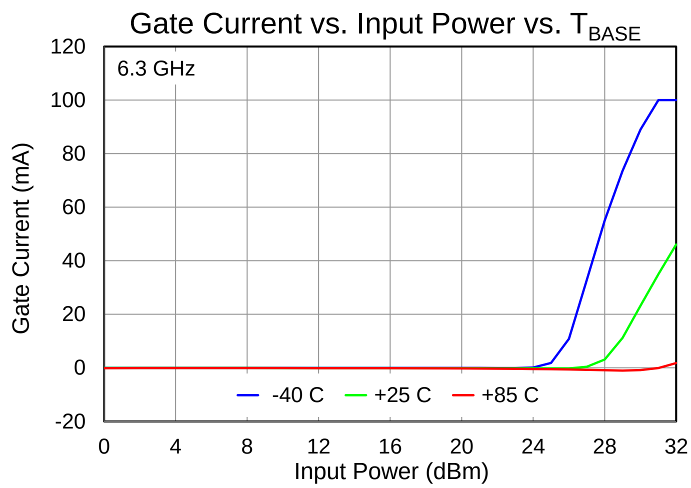
Performance Plots – Large Signal

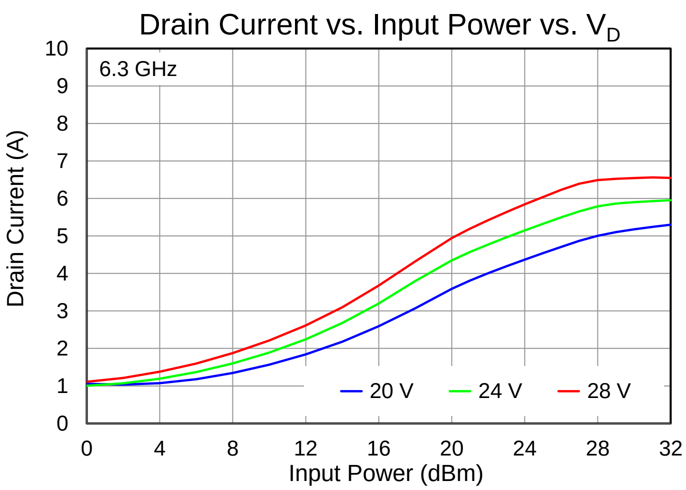
Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 1.5 A, P_{IN} = 26 dBm, T_{BASE} = +25 ºC

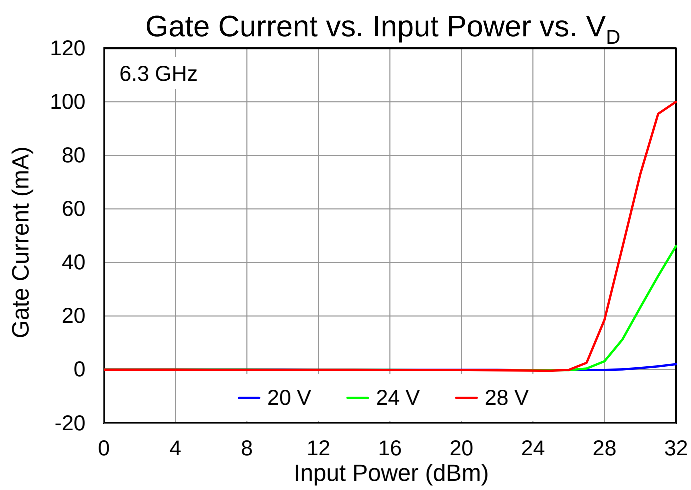






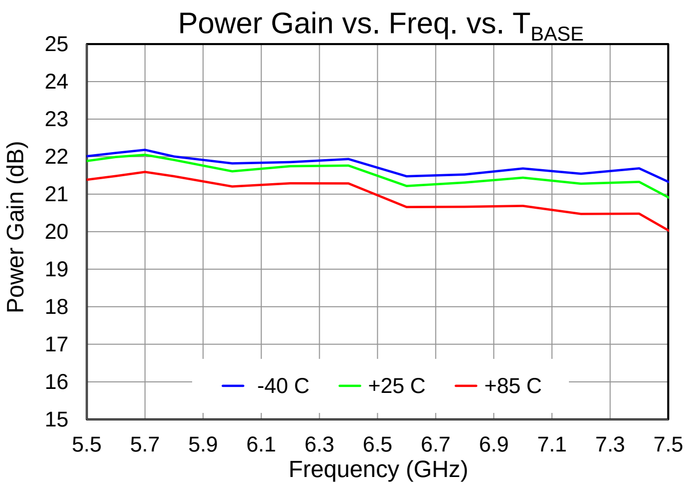


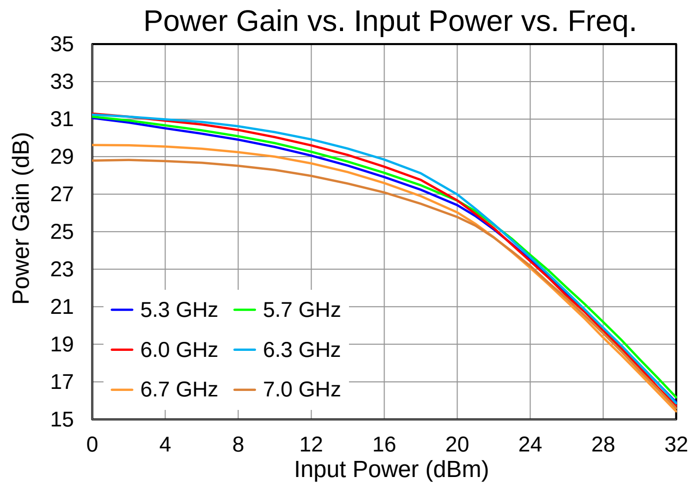


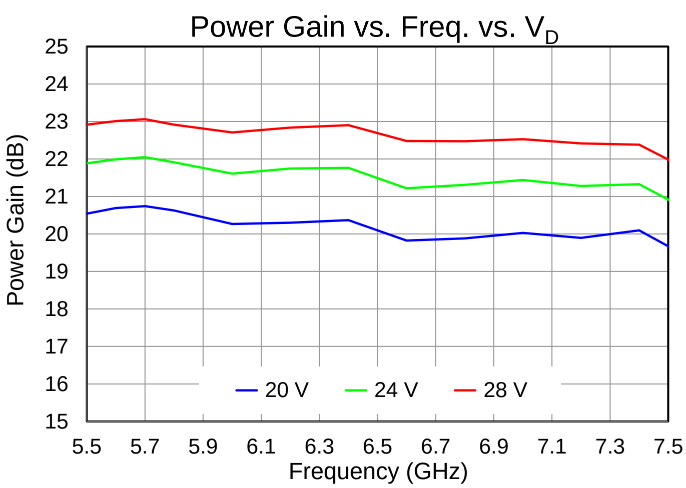


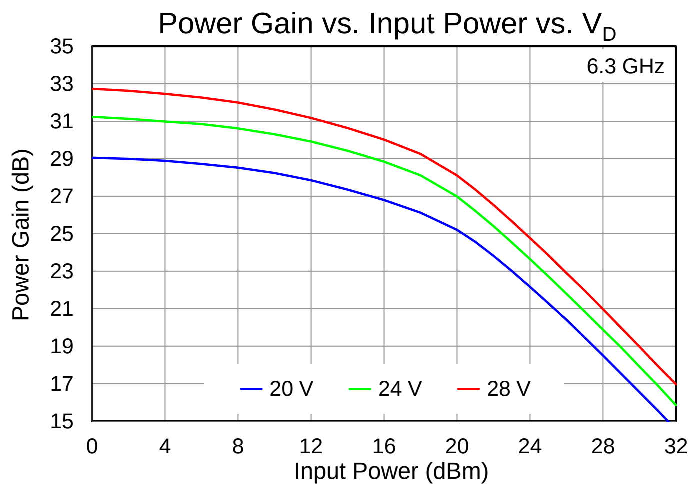
Performance Plots – Large Signal

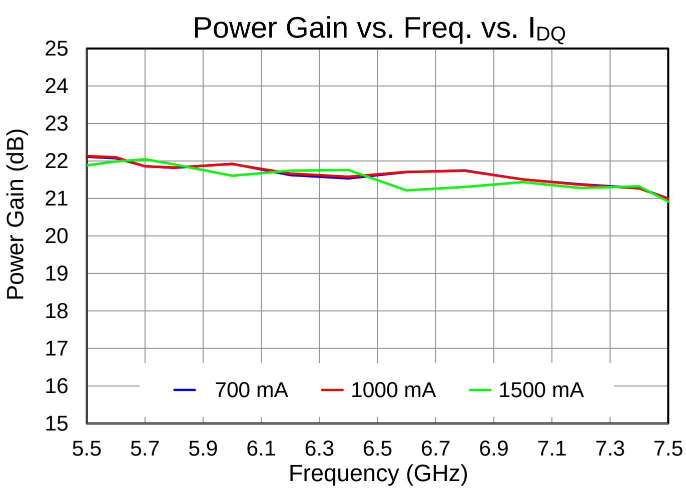
Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 1.5 A, P_{IN} = 26 dBm, T_{BASE} = +25 ºC

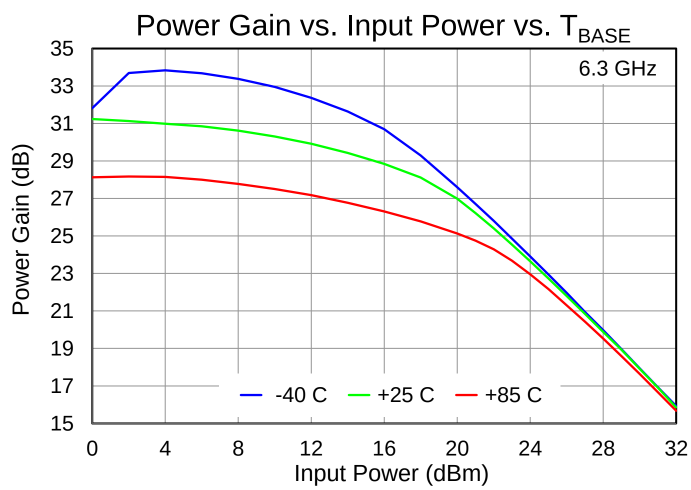






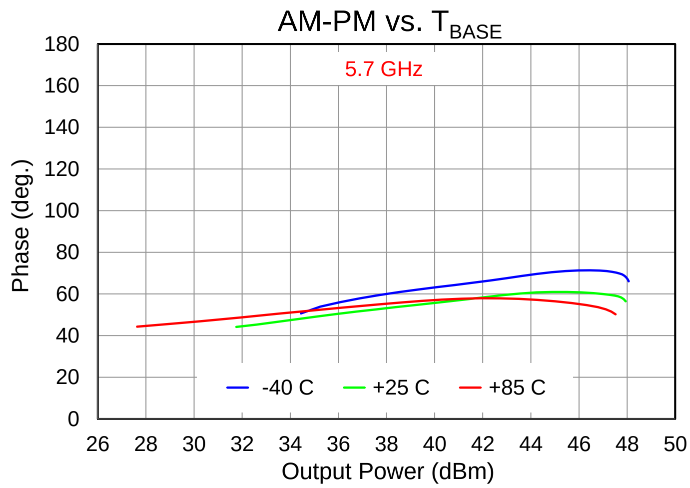


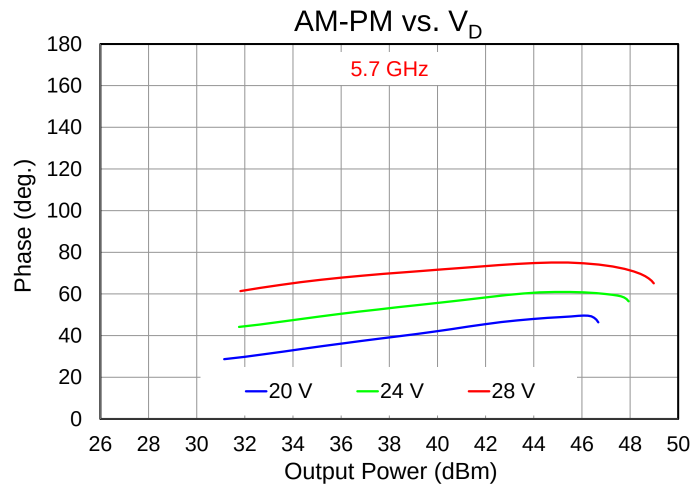


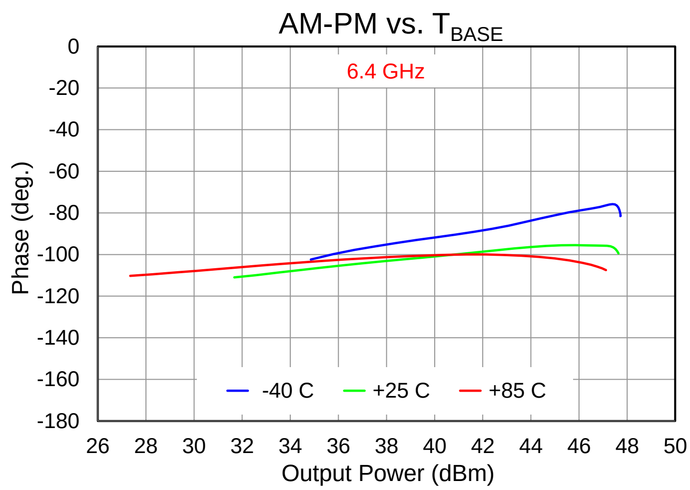


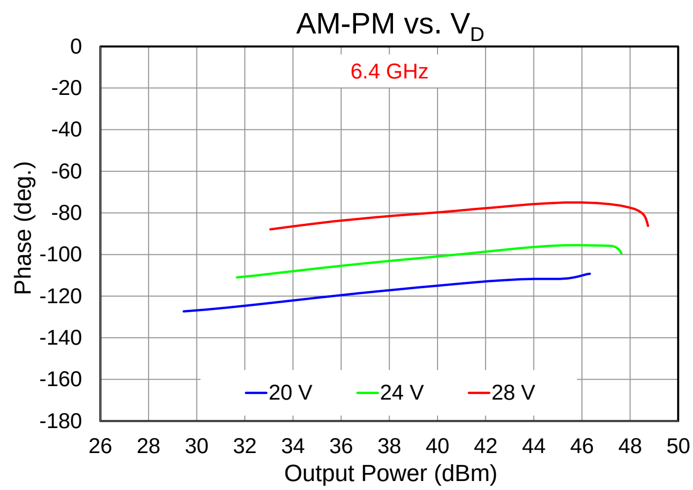
Performance Plots – Large Signal

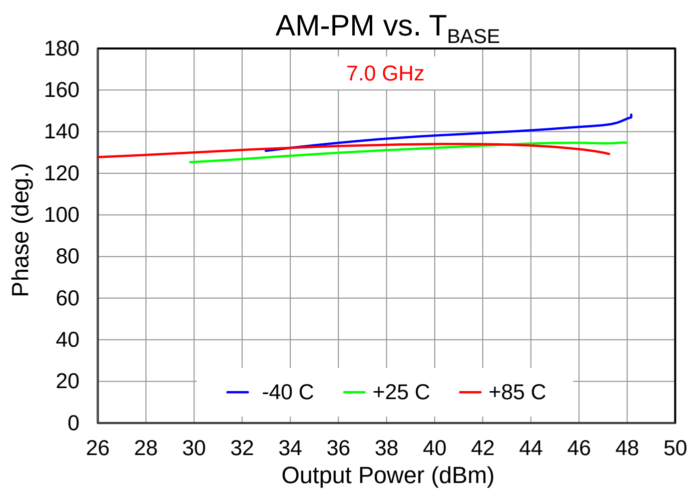
Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 1.5 A, T_{BASE} = +25 ºC

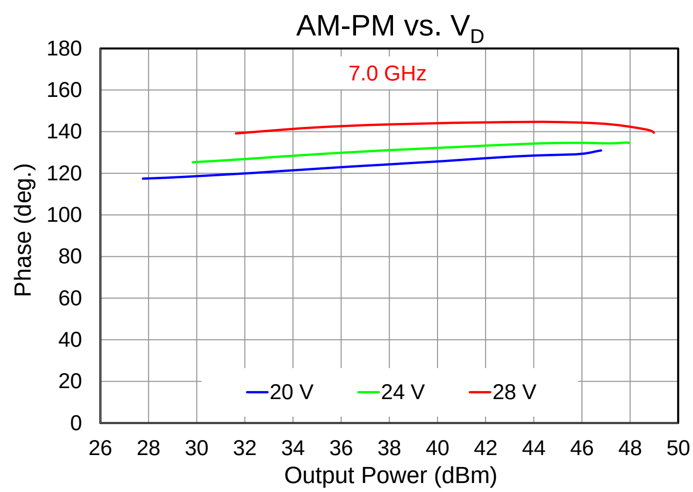






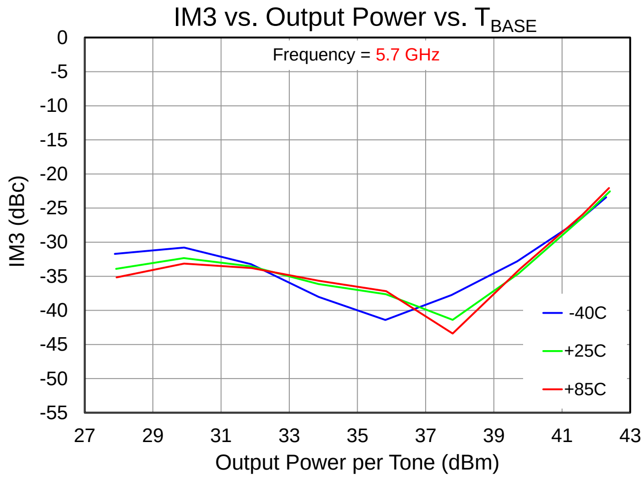


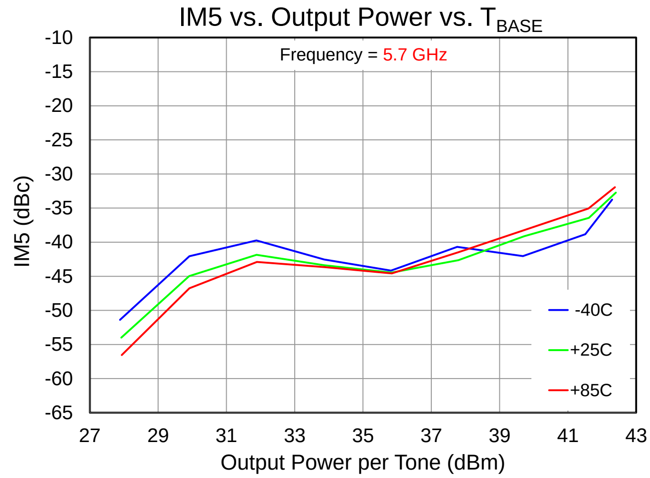


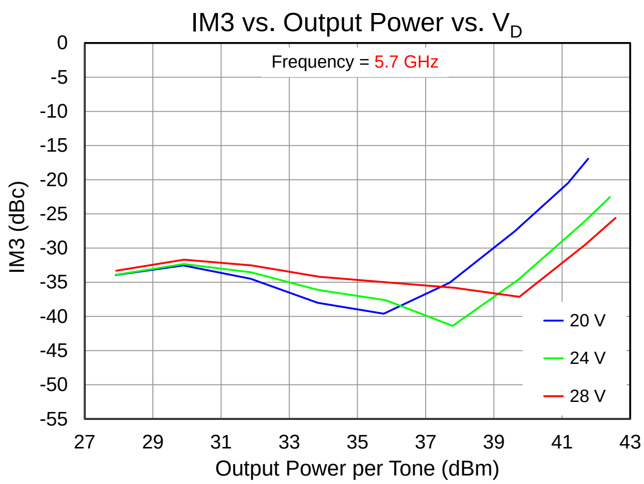


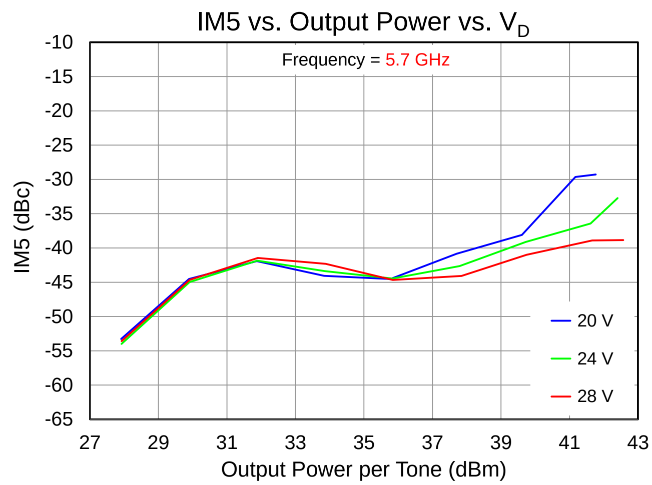
Performance Plots – Linearity

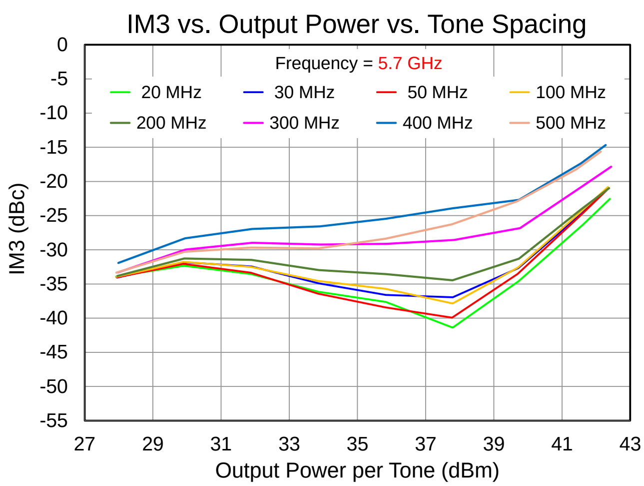
Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 1.5 A, Tone Spacing = 20 MHz, T_{BASE} = +25 ºC

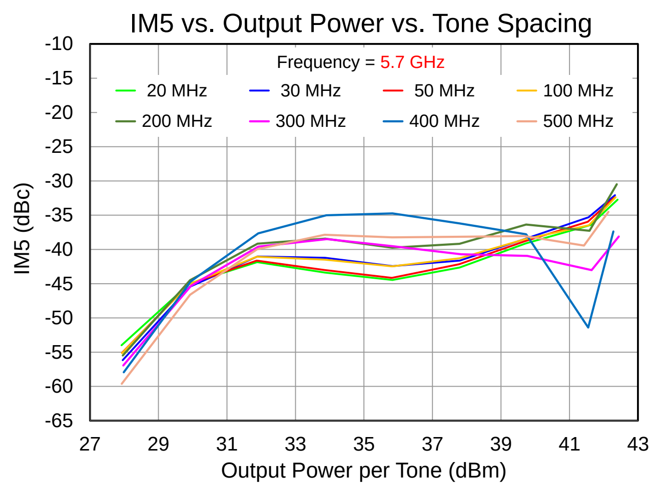








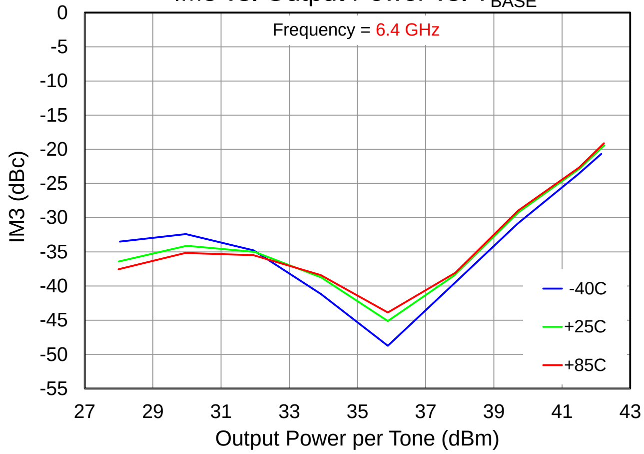




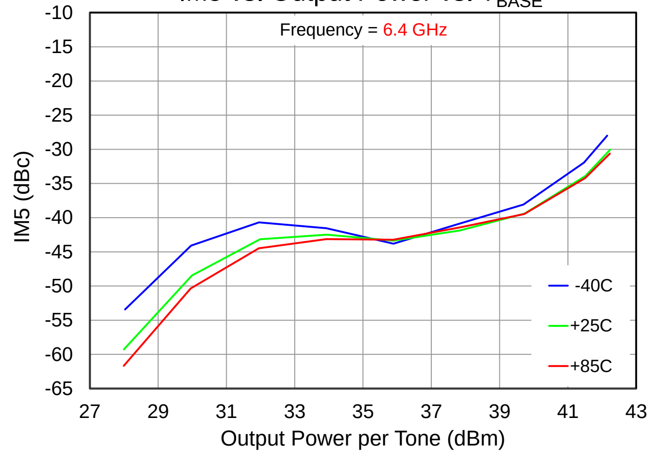
Performance Plots – Linearity

Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 1.5 A, Tone Spacing = 20 MHz, T_{BASE} = +25 ºC

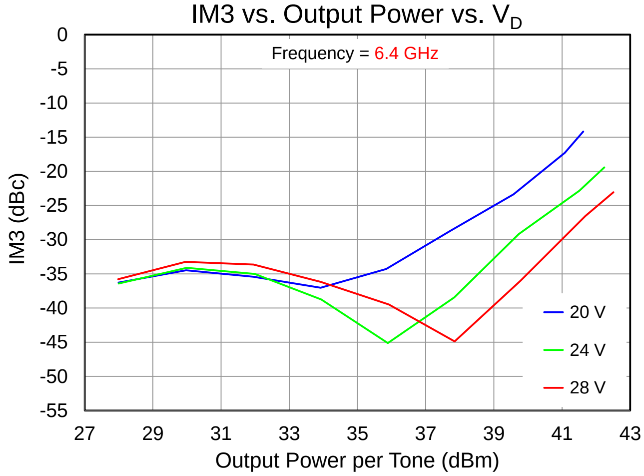
IM3 vs. Output Power vs. T_{BASE}



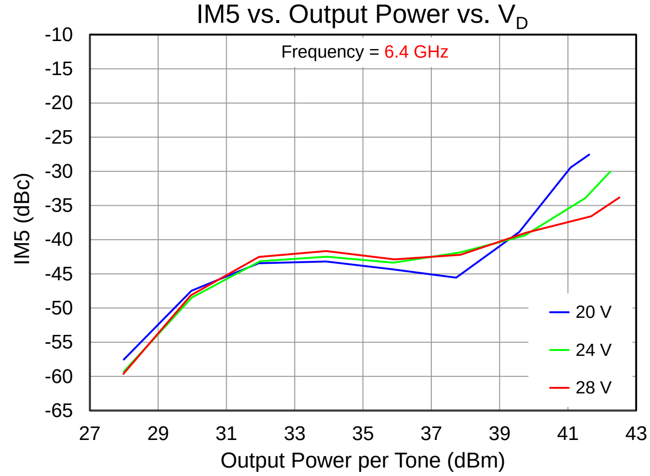
IM5 vs. Output Power vs. T_{BASE}



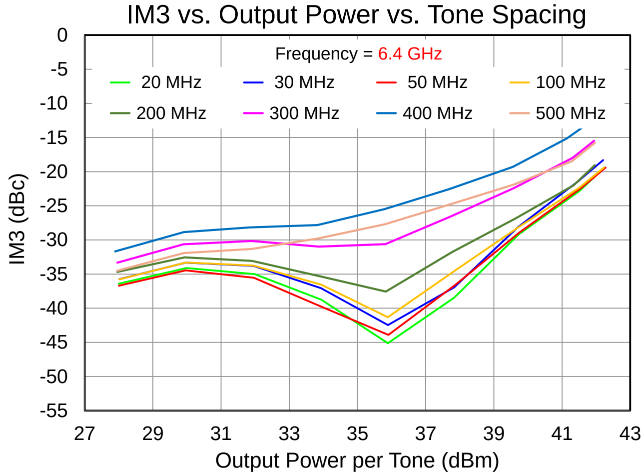
IM3 vs. Output Power vs. V_D



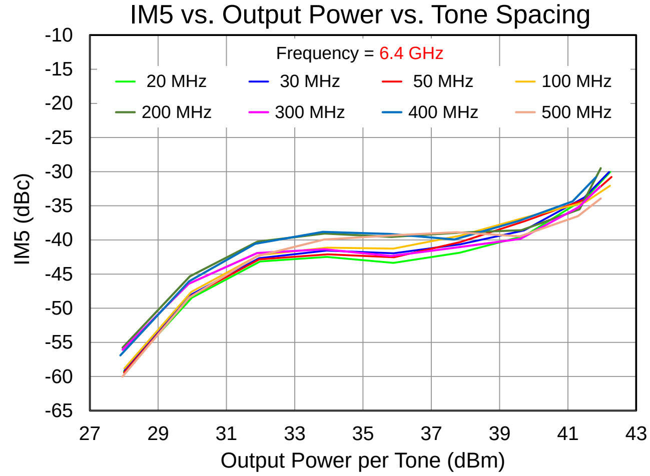
IM5 vs. Output Power vs. V_D



IM3 vs. Output Power vs. Tone Spacing



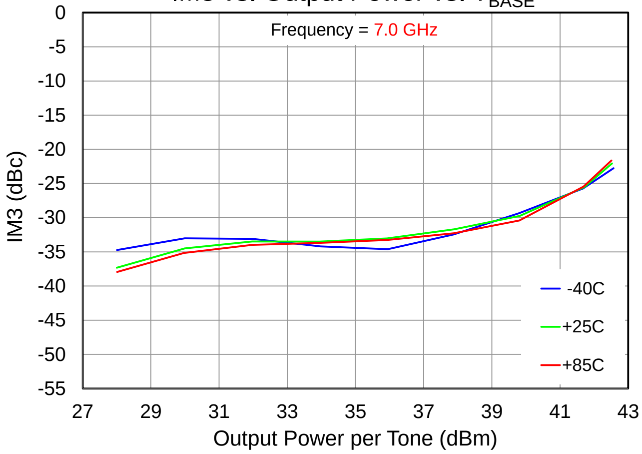
IM5 vs. Output Power vs. Tone Spacing



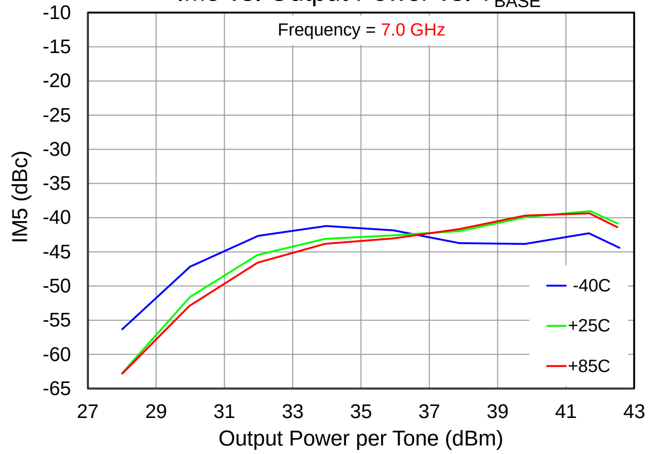
Performance Plots – Linearity

Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 1.5 A, Tone Spacing = 20 MHz, T_{BASE} = +25 ºC

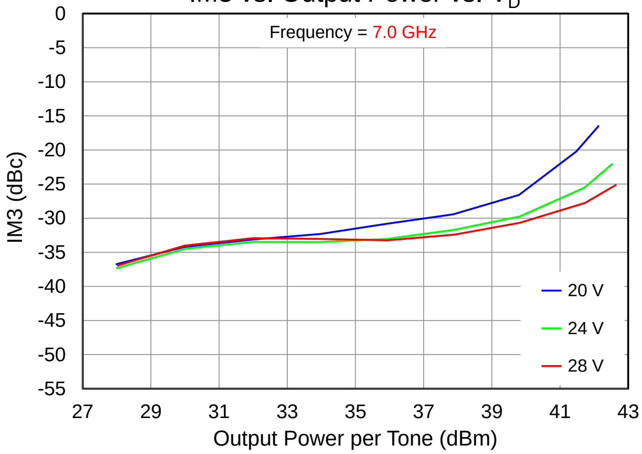
IM3 vs. Output Power vs. T_{BASE}



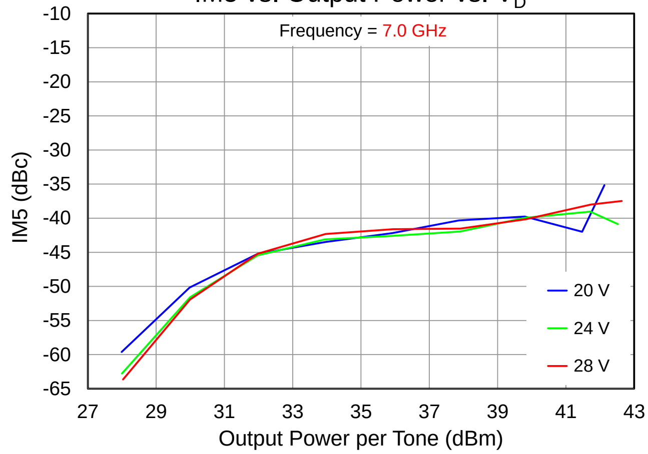
IM5 vs. Output Power vs. T_{BASE}



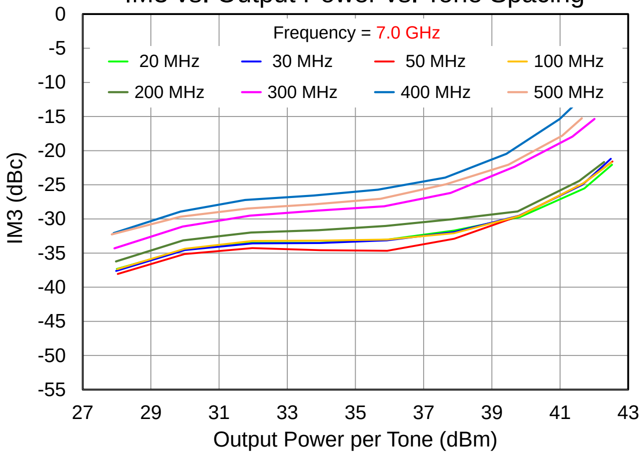
IM3 vs. Output Power vs. V_D



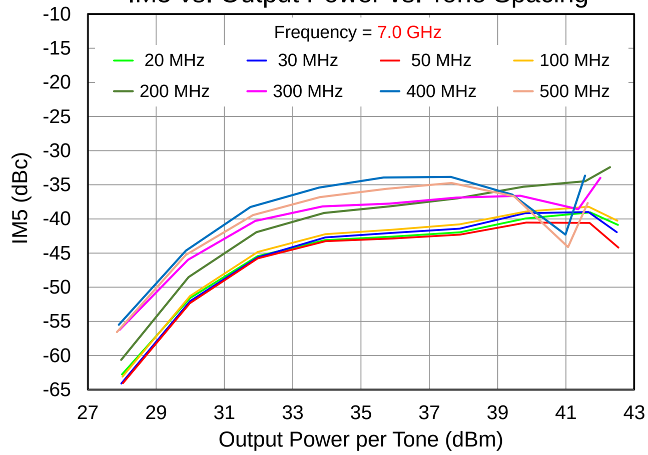
IM5 vs. Output Power vs. V_D



IM3 vs. Output Power vs. Tone Spacing



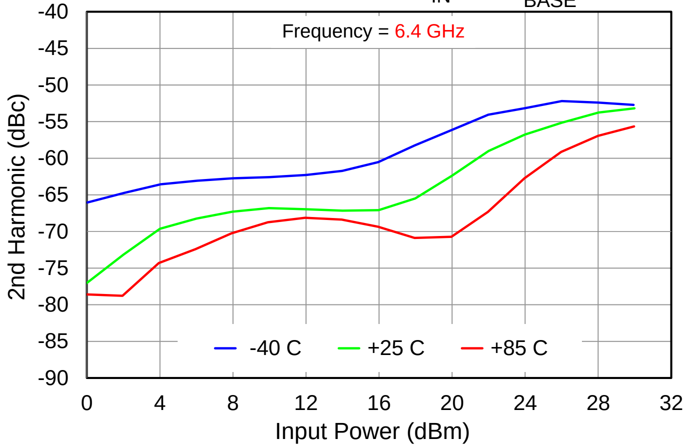
IM5 vs. Output Power vs. Tone Spacing



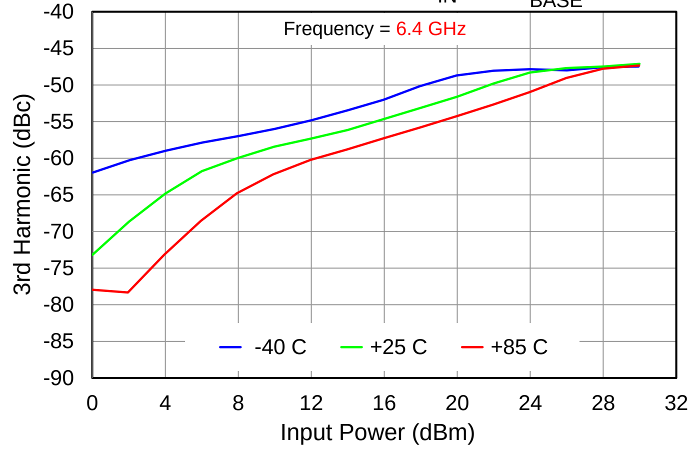
Performance Plots – Harmonics

Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 1.5 A, T_{BASE} = +25 ºC

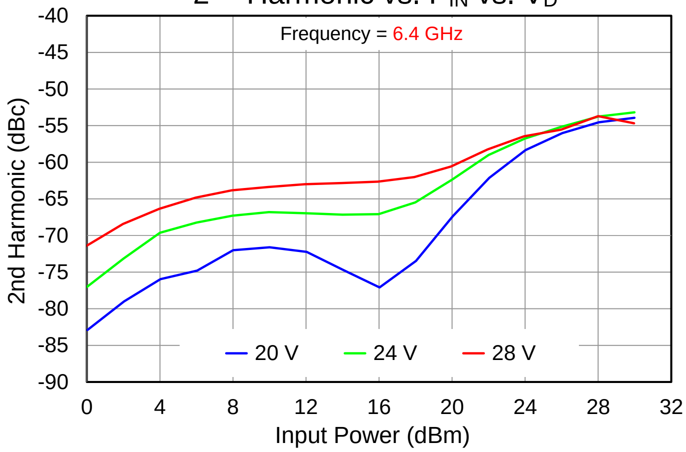
2ND Harmonic vs. P_{IN} vs. T_{BASE}



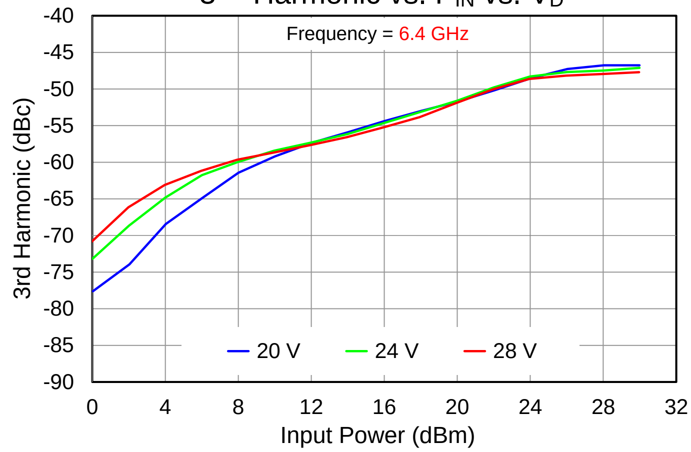
3RD Harmonic vs. P_{IN} vs. T_{BASE}



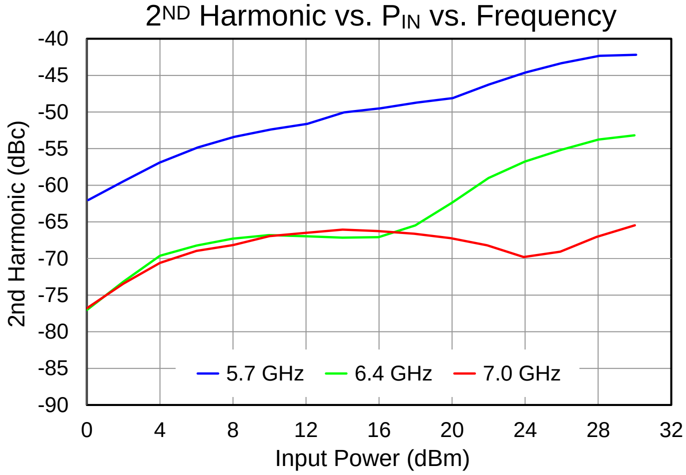
2ND Harmonic vs. P_{IN} vs. V_D



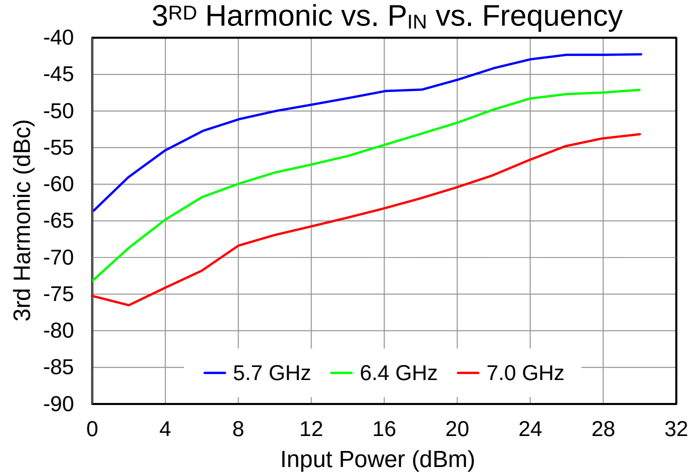
3RD Harmonic vs. P_{IN} vs. V_D



2ND Harmonic vs. P_{IN} vs. Frequency

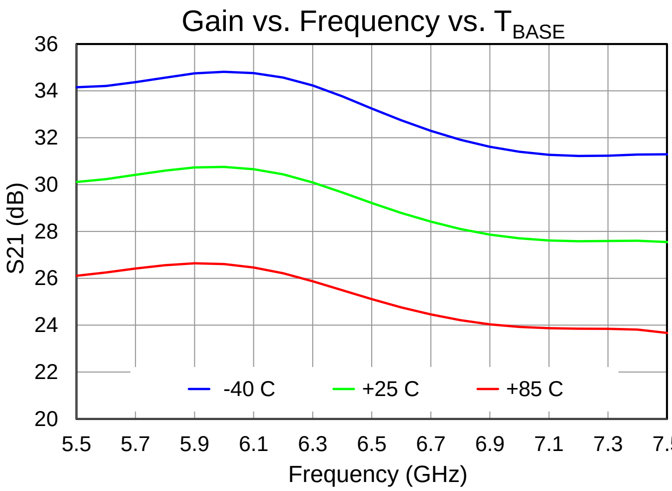


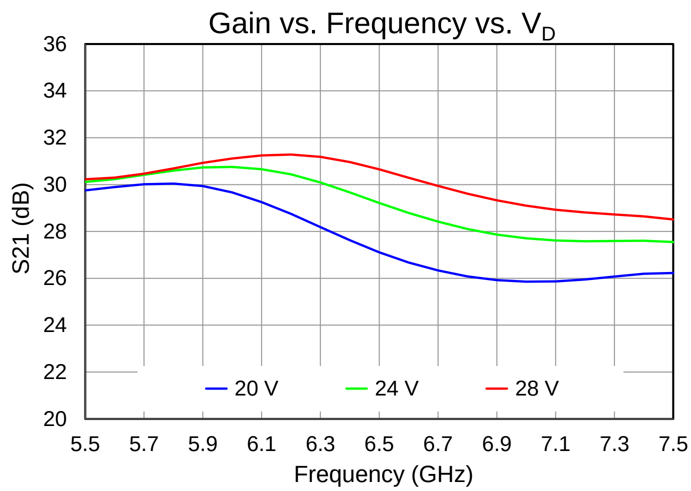
3RD Harmonic vs. P_{IN} vs. Frequency

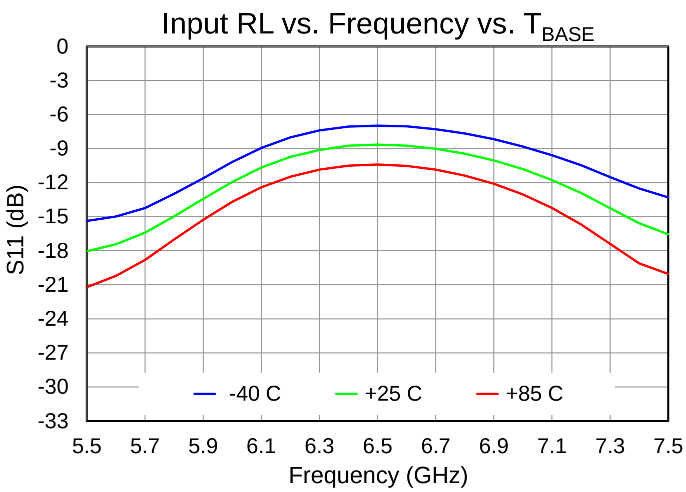


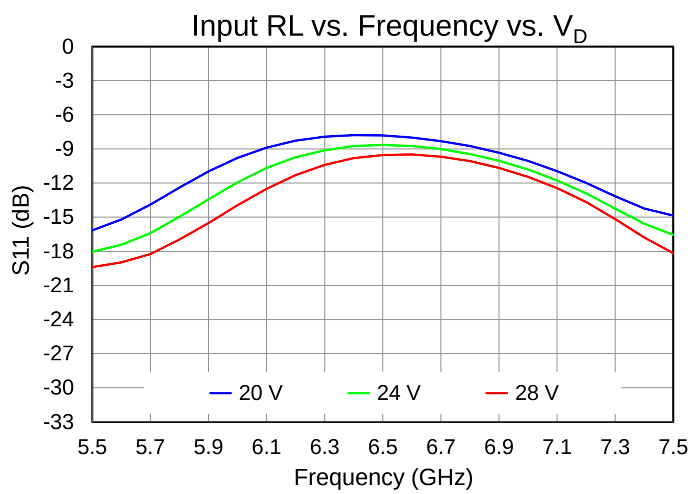
Performance Plots – Small Signal

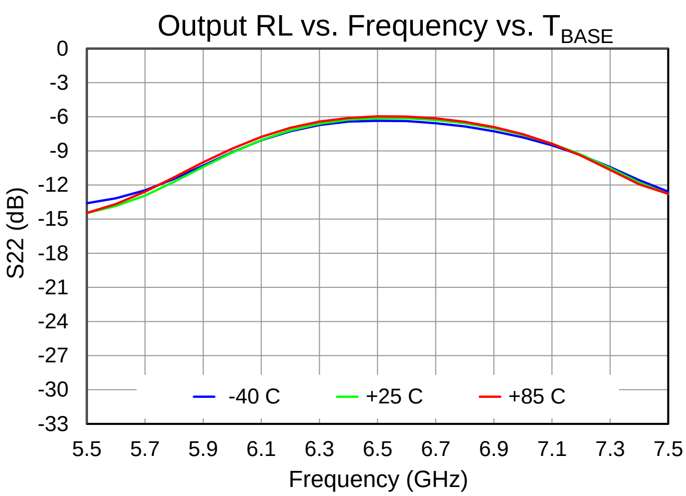
Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 1.5 A, T_{BASE} = +25 ºC

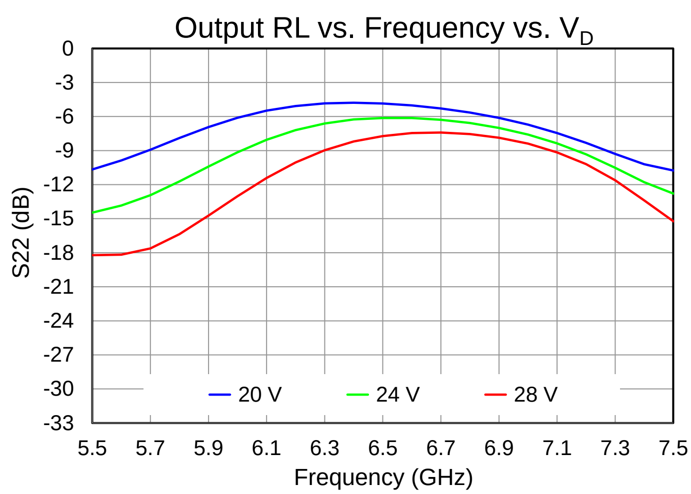






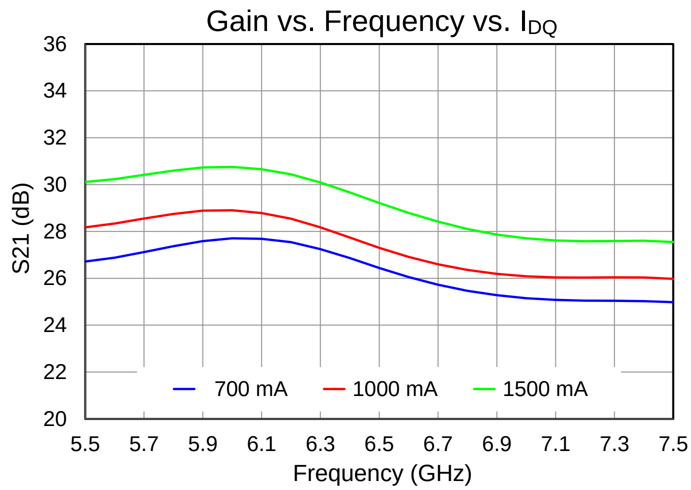


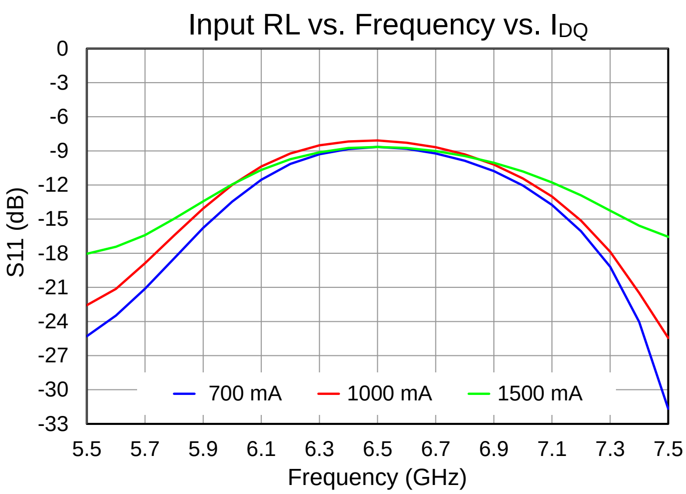


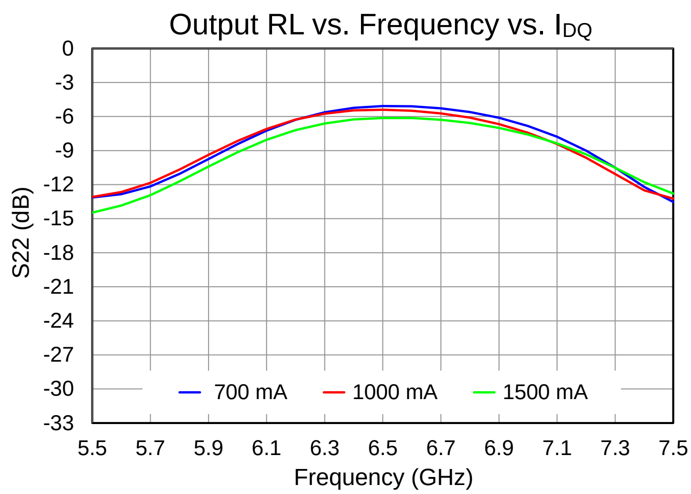


Performance Plots – Small Signal

Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 1.5 A, T_{BASE} = +25 ºC







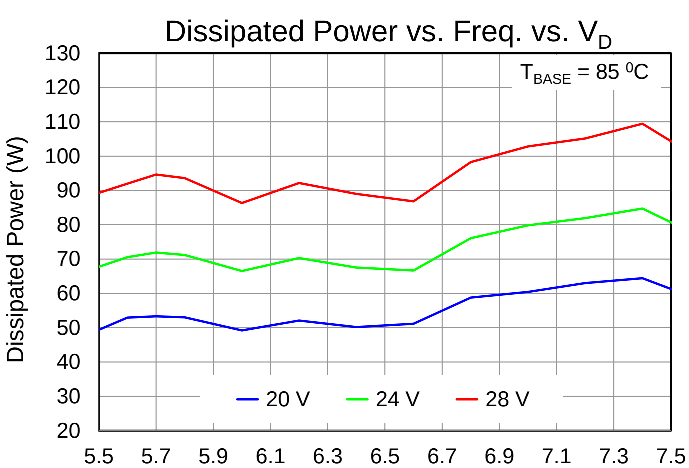
Thermal and Reliability Information

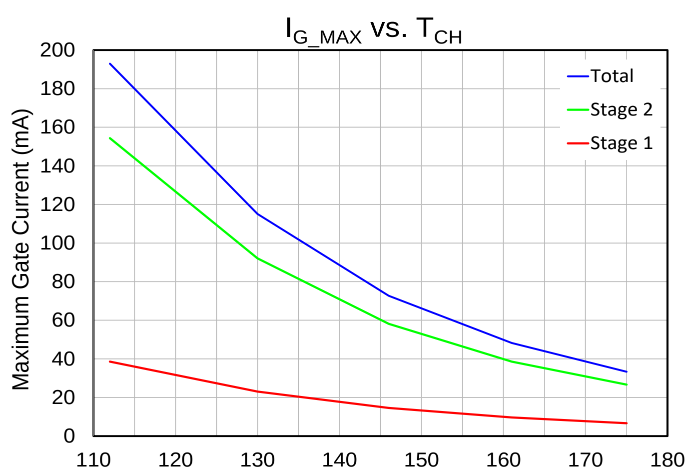
Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} (1)	Quiescent T_{base} = 85 °C, V_D = 24 V, I_{DQ} = 1.5 A P_{DISS} = 36 W	0.95	ºC/W
Channel Temperature, T_{CH} (2)		119	°C
Thermal Resistance, θ_{JC} (1)	Pulsed, T_{base} = 85 °C, V_D = 24 V, I_{DQ} = 1.5 A, Freq = 7 GHz, I_{D_Drive} = 5.4 A, DC = 20%, PW = 150 us, P_{IN} = 26 dBm, P_{OUT} = 47 dBm P_{DISS} = 80 W	0.54	ºC/W
Channel Temperature, T_{CH} (2)		128	°C
Thermal Resistance, θ_{JC} (1)	CW, T_{base} = 85 °C, V_D = 24 V, I_{DQ} = 1.5 A, Freq = 7 GHz, I_{D_Drive} = 5.1 A, P_{IN} = 26 dBm, P_{OUT} = 46.5 dBm P_{DISS} = 78 W	1.03	ºC/W
Channel Temperature, T_{CH} (2)		166	°C

Notes:

1. Thermal resistance determined to the back of package (85 °C)
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note “GaN Device TCHMAX Theta-JC and Reliability Estimates,” located here https://www.qorvo.com/products/d/da006480

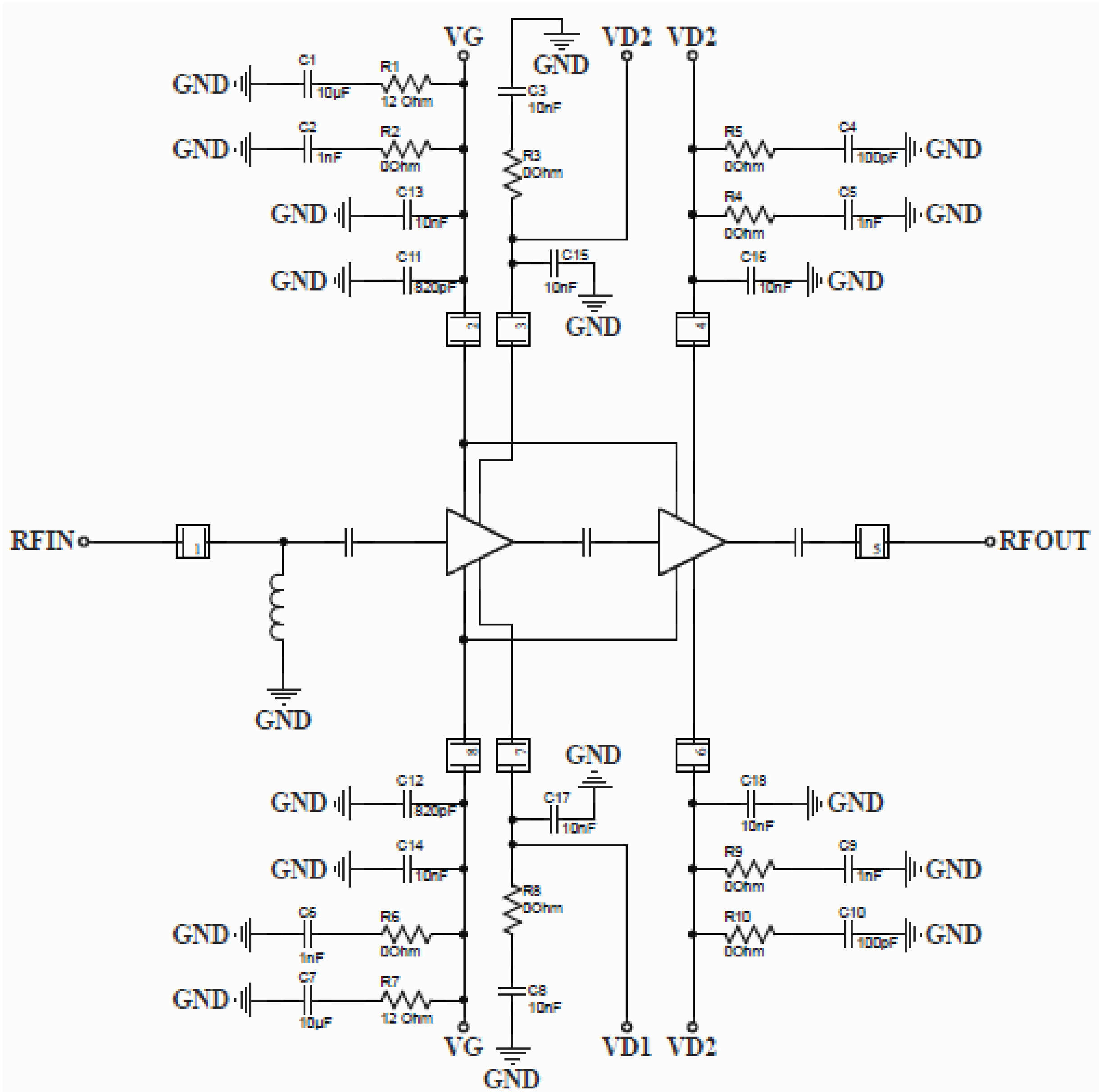
Dissipated Power and Maximum Gate Current





Test conditions, unless otherwise noted: Pulsed or CW, V_D = 24 V, I_{DQ} = 1.5 A, P_{IN} = +26 dBm, T_{BASE} = +85 ºC

Applications Information



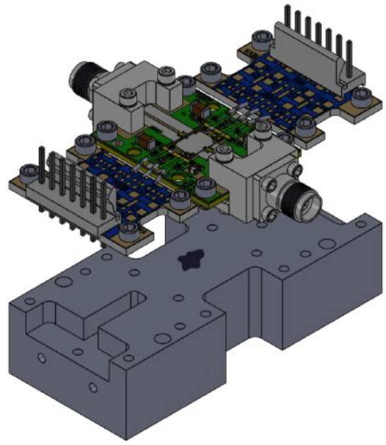
Bias-Up Procedure

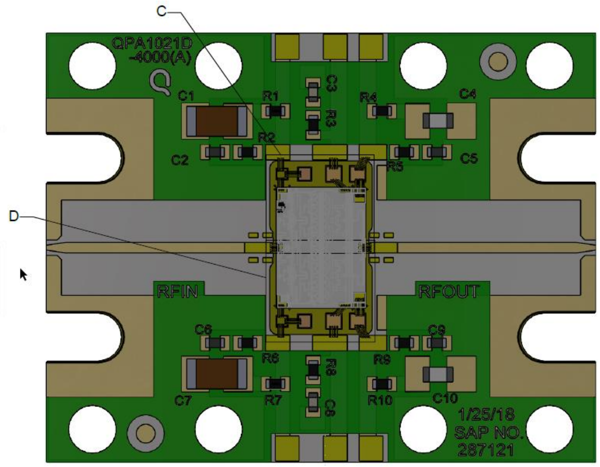
1. Set I_D limit to 100 mA, I_G limit to 9 A
2. Set V_G to −5.0 V
3. Set V_D +24 V
4. Adjust V_G more positive until I_{DQ} = 1.5 A ($V_G \approx$ -2.5V +/- typical)
5. Apply RF signal

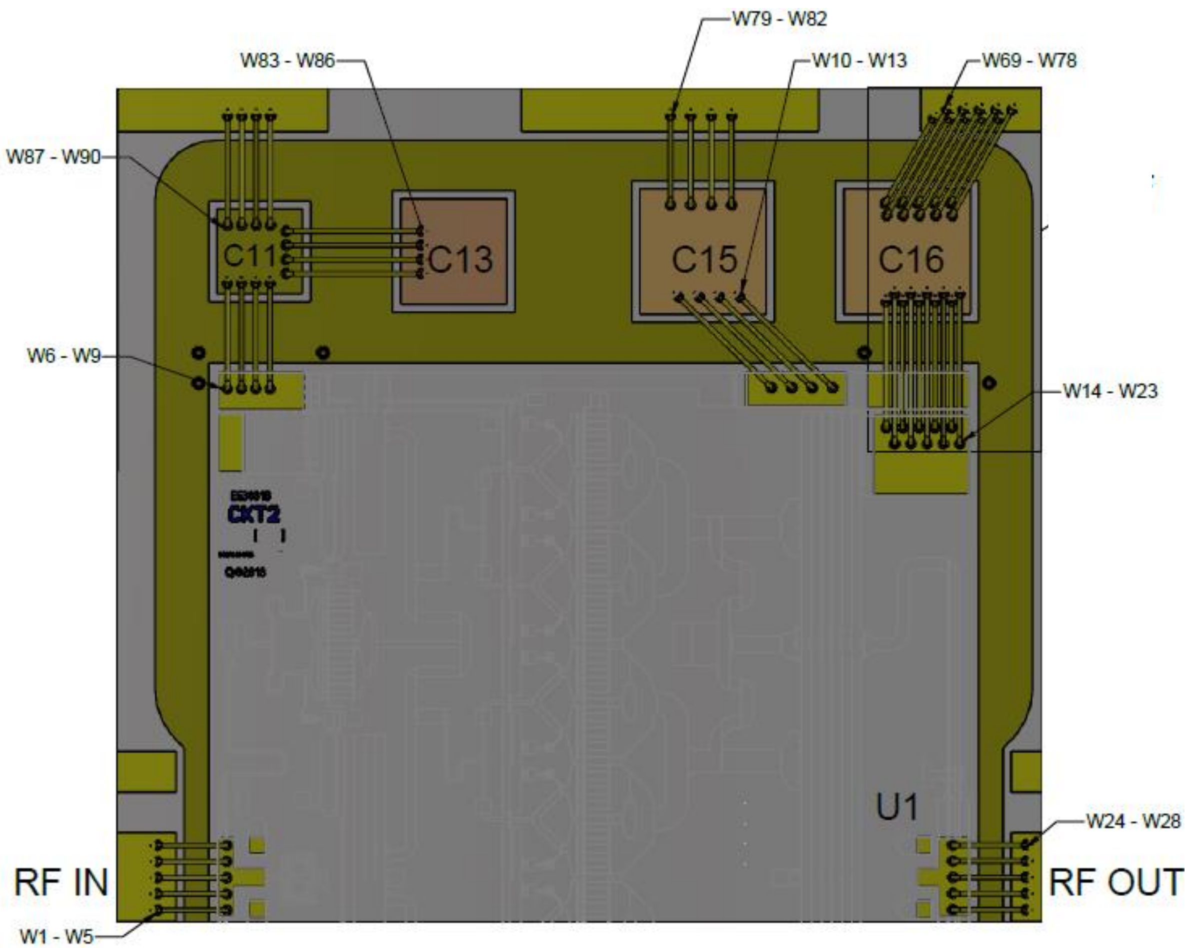
Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to −5.0 V. Ensure I_{DQ} ~ 0 mA
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_G supply

Evaluation Board (EVB) Layout Assembly

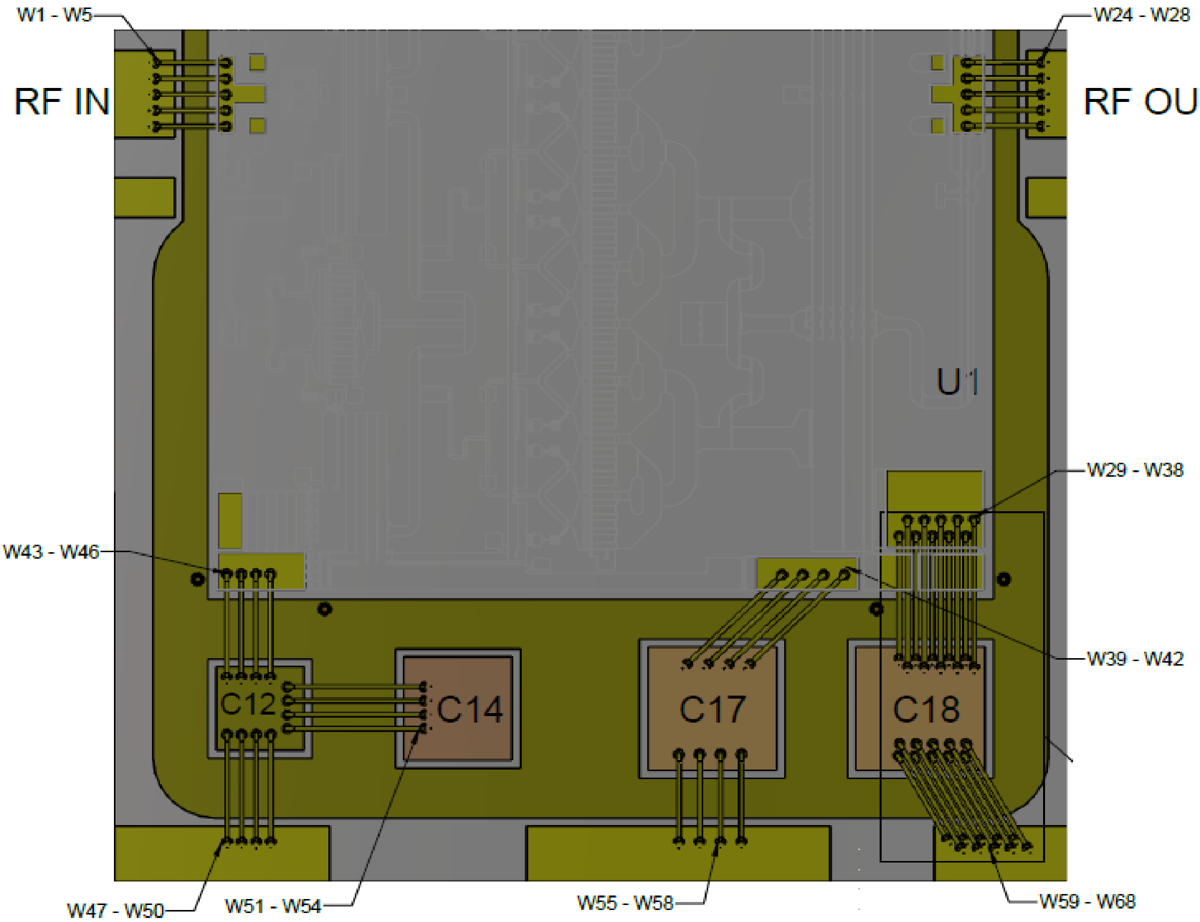






DETAIL C

Evaluation Board (EVB) Layout Assembly (con't)

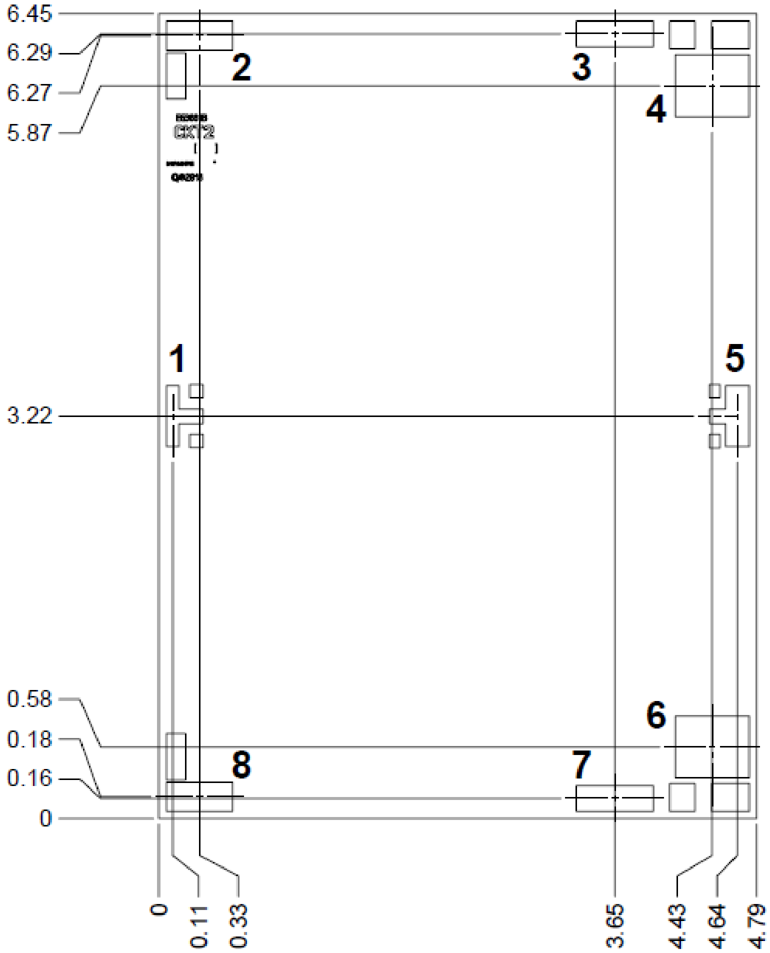


DETAIL D

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1, C7	10 uF	CAP, 10uF, 20%, 50V, 20%, X5R, 1206	Various	
C2, C5, C6, C9	1 nF	CAP, 1nF, ±10%, 50V, X7R, 0402	Various	
C3, C8	0.01 uF	CAP, 0.01uF, ±10%, 50V, X7R, 0402	Various	
C4, C10	100 pF	CAP, 100pF, 5%, 250V, C0G, 0603	Various	
C13, C14, C15, C16, C17, C18	10 nF	CAP, 10nF, 20%, 100V, X7R, 30x30, SL	Various	
R1, R7	12 Ω	RES, 12 Ohm, 5%, 1/16W, 0402	Various	
R2, R3, R4, R5, R6, R8, R9, R10	0 Ω	RES, 0 Ohm, JMPR, 0402	Various	
H1, H2	-	CONN, HDR, Male-vert, 7 PIN, 1 RAW, MTA	Various	
J1, J2	-	Connector, Female, End Launch, 1092-02A-5	Southwest Microwave	1092-02A-5
Carrier Plate	-	Carrier Plate, CuMo, 0.9 x 1.155 x 0.04T	Various	Custom
PCB_MMIC	-	PCB for MMIC (named QPA1021D), Rogers 6035 10mils, 0.5oz Ni/Au plating both sides	Various	Custom
PCB,_Bias	-	PCB for DC Bias	Various	Custom
H-Block	-	H-Block, Copper C110, 1.14 x 2.49 x 0.59T	Various	Custom

Mechanical Information



Dimensions are in mm
Thickness: 0.10
Die x, y size tolerance: ± 0.050
Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (mm)	Description
1	RF_{IN}	0.10 x 0.49	RF Input. Matched to 50 Ω, DC blocked, DC shorted to ground
2, 8	V_G	0.53 x 0.23	Gate voltage. External bypassing required; refer to page 21 for recommendation
3, 7	V_{D1}	0.62 x 0.21	Drain voltage for stage 1. External bypassing required; refer to page 21 for recommendation
4, 6	V_{D2}	0.59 x 0.50	Drain voltage for stage 2. External bypassing required; refer to page 21 for recommendation
5	RF_{OUT}	0.19 x 0.49	RF Output. Matched to 50 Ω, DC blocked

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ANSI/ESD/JEDEC JS-001

Caution!

ESD-Sensitive Device

Solderability

Use only AuSn (80/20) solder, and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_{4}O_{2}$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: **www.qorvo.com**

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Email: **customer.support@qorvo.com**

Important Notice