QPA2210D

27 – 31 GHz 7 Watt GaN Power Amplifier

Product Overview

Qorvo's QPA2210D is a Ka-band power amplifier fabricated on Qorvo's 0.15 um GaN on SiC process (QGaN15). Operating between 27 and 31 GHz, it achieves 2.5 W linear power with −25 dBc intermodulation distortion products and 25 dB small signal gain. Saturated output power is 7 W with power-added efficiency of 32%.

QPA2210D is ideally suited to support satellite communications and 5G infrastructure.

To simplify system integration, the QPA2210D is fully matched to 50 ohms with integrated DC blocking caps on both I/O ports.

The QPA2210D is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

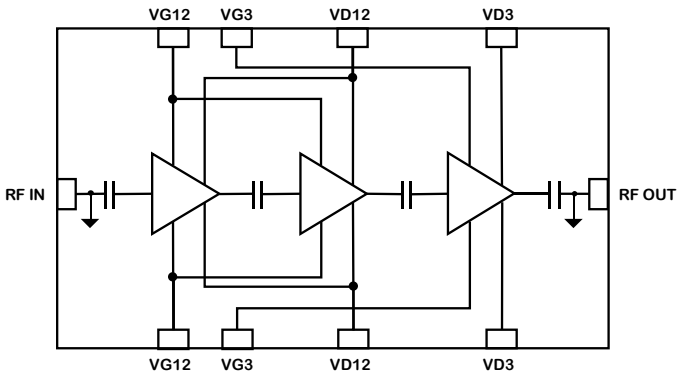
Lead-free and RoHS compliant.

Key Features

- Frequency Range: 27 – 31 GHz
- P_{SAT} (P_{IN}=21 dBm): > 38.4 dBm
- PAE (P_{IN}=21 dBm): > 32 %
- Power Gain (P_{IN}=21 dBm): > 16 dB
- IMD3 (at 31 dBm/tone): < −25 dBc
- Small Signal Gain: 25 dB
- Bias: V_D = 20 V, I_{DQ} = 200 mA
- Die Dimensions: 2.740 x 1.432 x 0.050 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- 5G Infrastructure
- Satellite Communications

Ordering Information

Part No.	Description
QPA2210D	27 – 31 GHz 7 Watt GaN Amplifier (10 Pcs.)
QPA2210DEVB01	Evaluation Board for QPA2210D

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	−5 V to 0 V
Drain Current (I_D)	2800 mA
Gate Current (I_G)	See plot pg. 17
Power Dissipation (P_{DISS}), 85 °C	20 W
Input Power (P_{IN}), 50 Ω, V_D=20 V, I_{DQ}=200 mA, 85 °C	33 dBm
Input Power (P_{IN}), 3:1 VSWR, V_D=20 V, I_{DQ}=200 mA, 85 °C	33 dBm
Soldering Temperature (30 s, max.)	320 °C
Storage Temperature	−55 to +150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value / Range
Drain Voltage (V_D)	20 V
Drain Current (I_{DQ})	200 mA
Operating Temperature	−40 to +85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

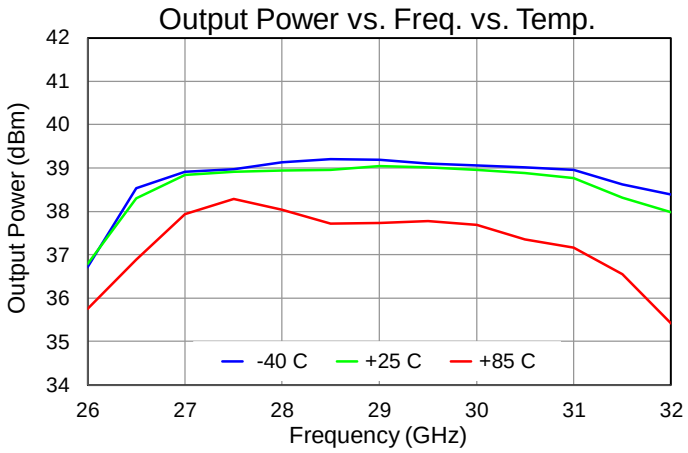
Electrical Specifications

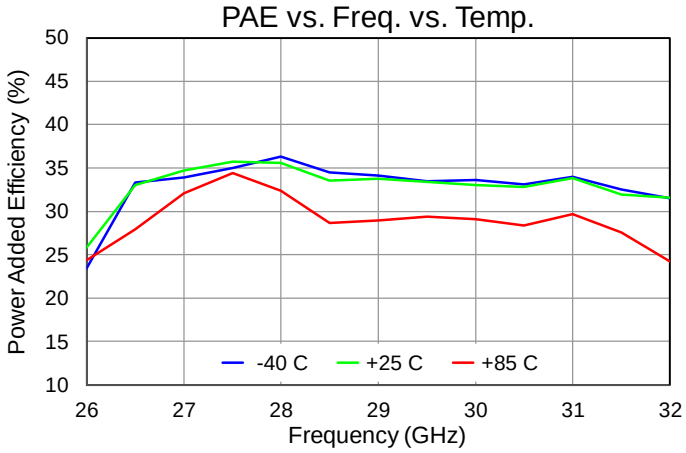
Parameter		Min	Typ	Max	Units
Operational Frequency		27		31	GHz
Output Power (P_{IN}=21 dBm)	27 GHz 29 GHz 31 GHz		38.8 39.0 38.8		dBm dBm dBm
Power Added Efficiency (P_{IN}=21 dBm)	27 GHz 29 GHz 31 GHz		34.7 33.7 33.9		% % %
Small Signal Gain	27 GHz 29 GHz 31 GHz		27.0 27.3 26.0		dB dB dB
Input Return Loss	27 GHz 29 GHz 31 GHz		20 11 14		dB dB dB
Output Return Loss	27 GHz 29 GHz 31 GHz		7 9 8		dB dB dB
IMD3 (P_{OUT}/Tone=31 dBm, 10 MHz tone spacing)	27 GHz 29 GHz 31 GHz		−34 −29 −29		dBc dBc dBc
P_{OUT} Temp. Coeff. (85 °C to 25 °C, P_{IN} = 21 dBm))			−0.020		dB/°C
Sm. Sig. Gain Temp. Coefficient (85 °C to −40 °C)			−0.094		dB/°C

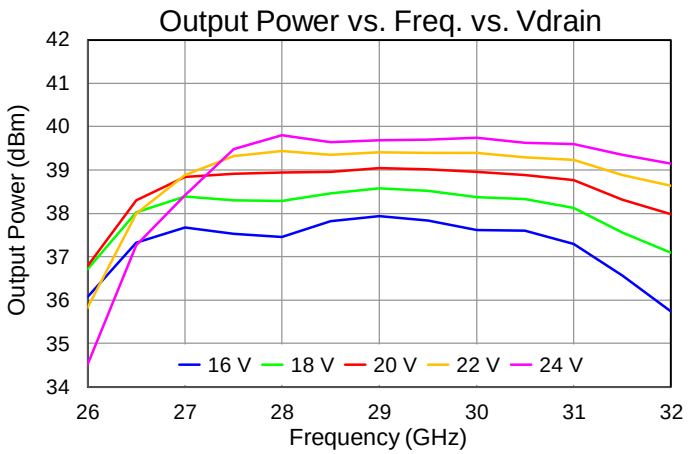
Test conditions, unless otherwise noted: T = +25 °C, V_D = 20 V, I_{DQ} = 200 mA

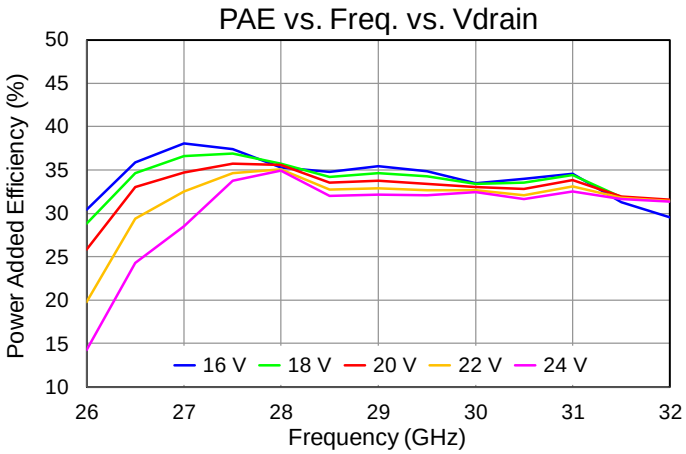
Performance Plots – Large Signal

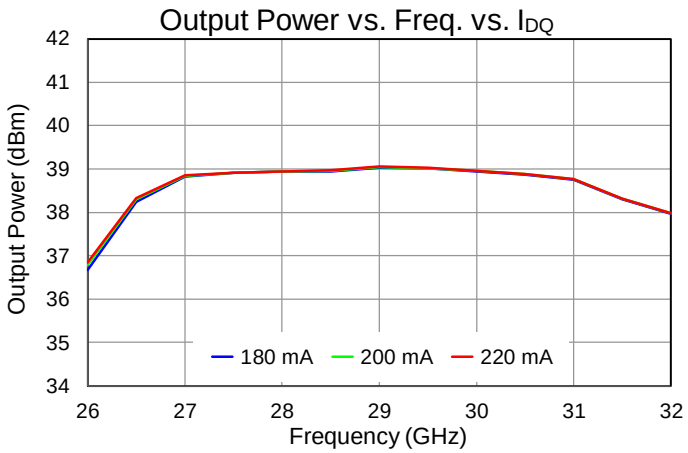
Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 200 mA, T=+25 °C, P_{IN} = 21 dBm

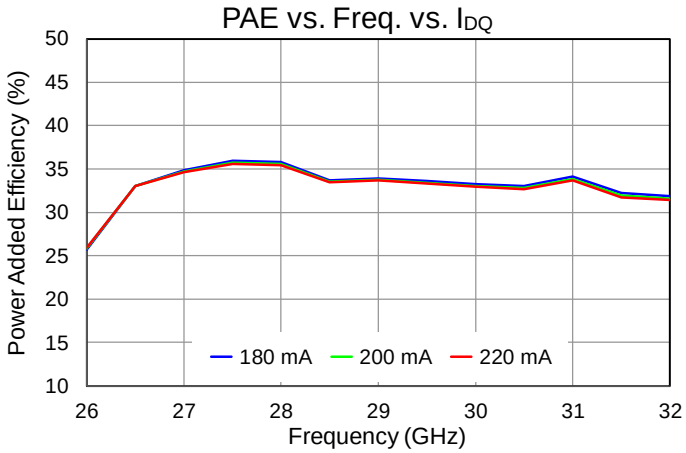








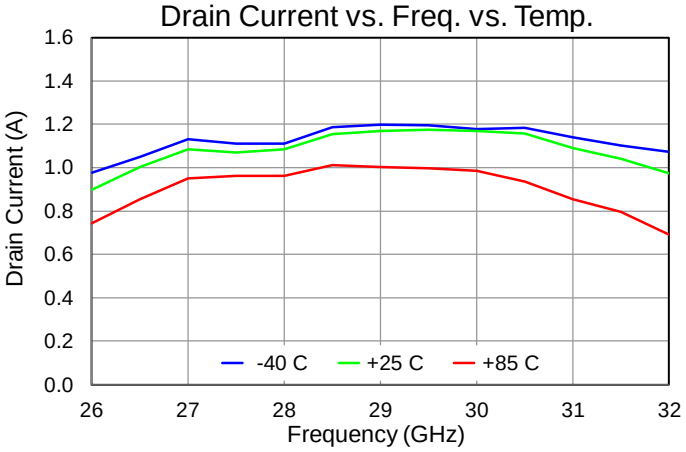




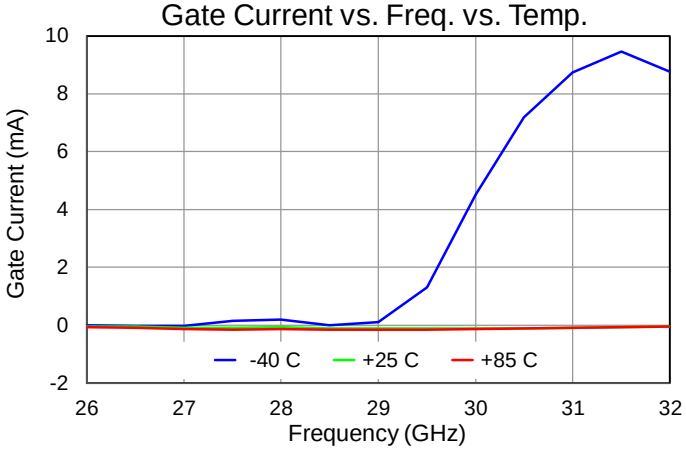
Performance Plots – Large Signal

Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 200 mA, T=+25 °C, P_{IN} = 21 dBm

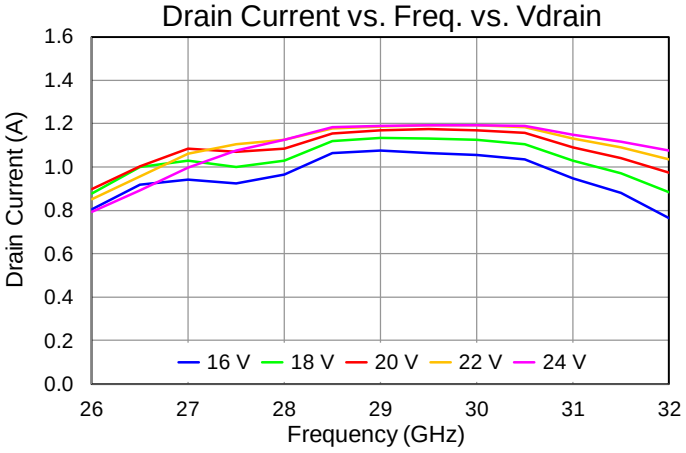
Drain Current vs. Freq. vs. Temp.



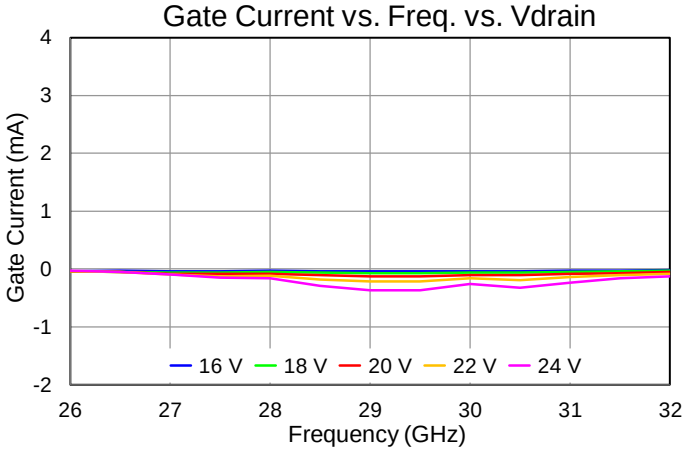
Gate Current vs. Freq. vs. Temp.



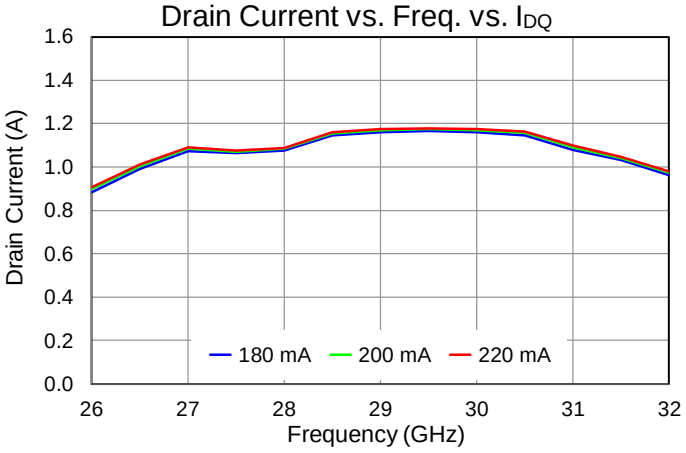
Drain Current vs. Freq. vs. Vdrain



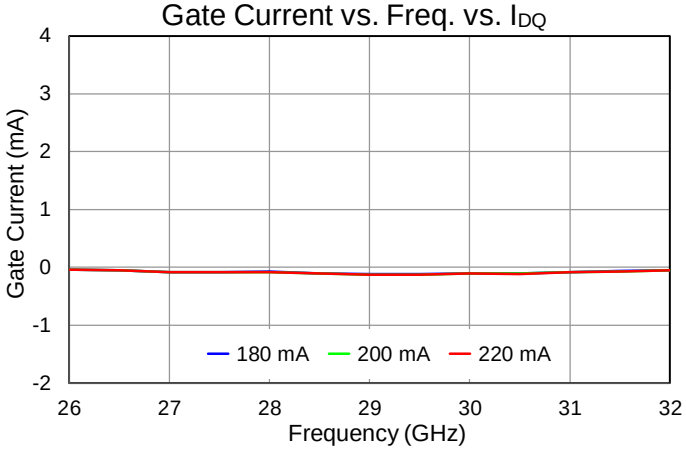
Gate Current vs. Freq. vs. Vdrain



Drain Current vs. Freq. vs. I_{DQ}



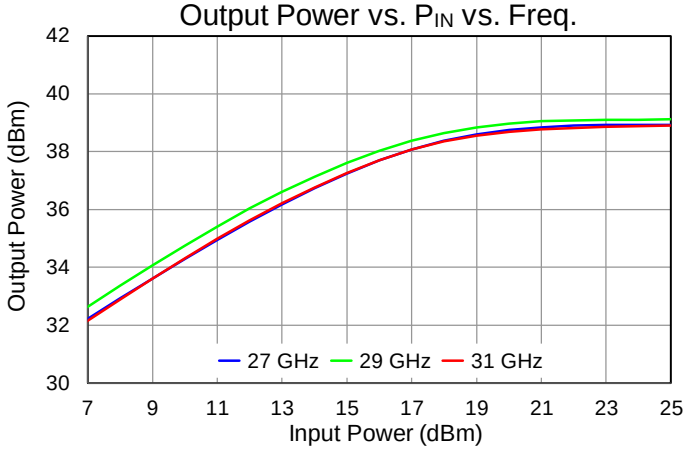
Gate Current vs. Freq. vs. I_{DQ}



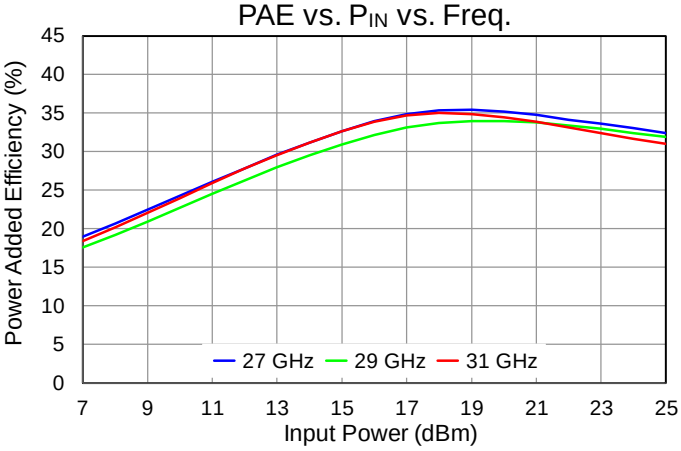
Performance Plots – Large Signal

Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 200 mA, T=+25 °C

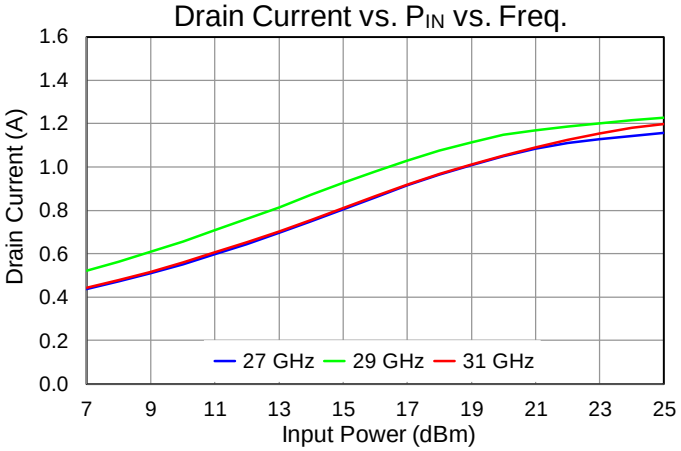
Output Power vs. P_{IN} vs. Freq.



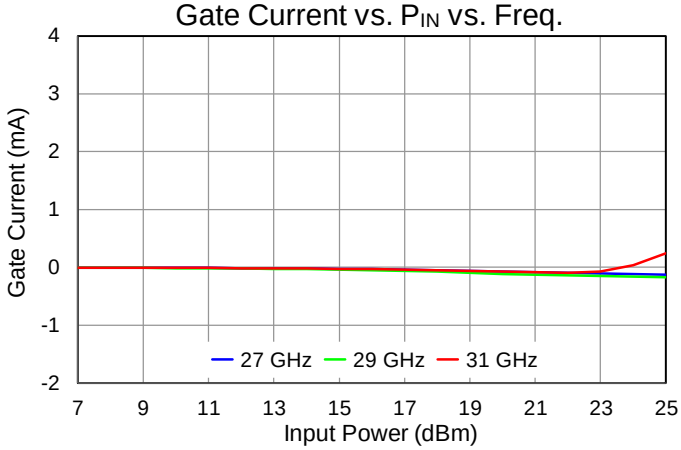
PAE vs. P_{IN} vs. Freq.



Drain Current vs. P_{IN} vs. Freq.



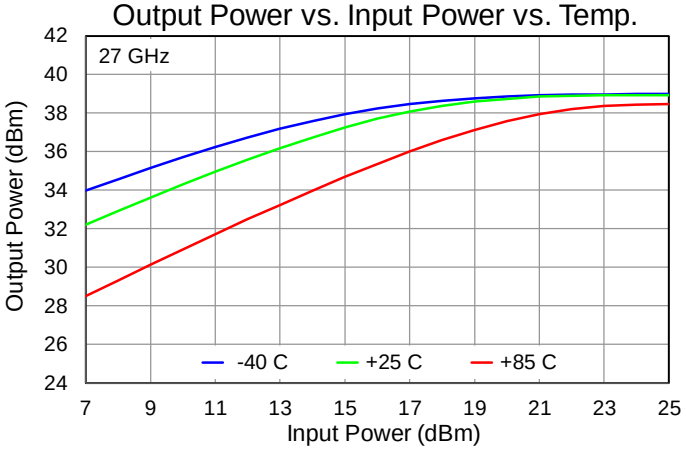
Gate Current vs. P_{IN} vs. Freq.



Performance Plots – Large Signal

Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 200 mA, T=+25 °C

Output Power vs. Input Power vs. Temp.



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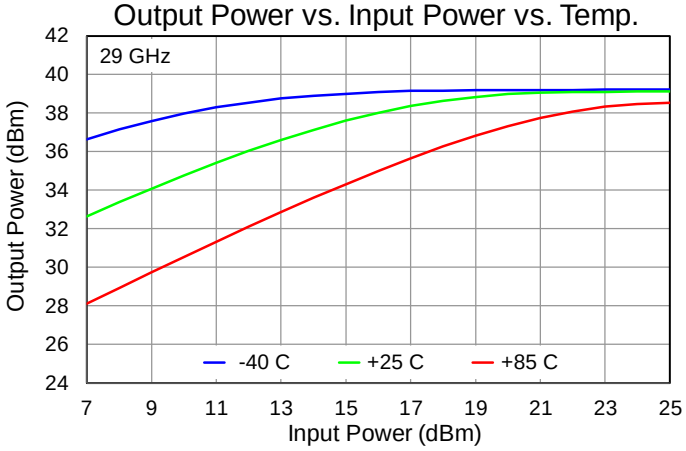
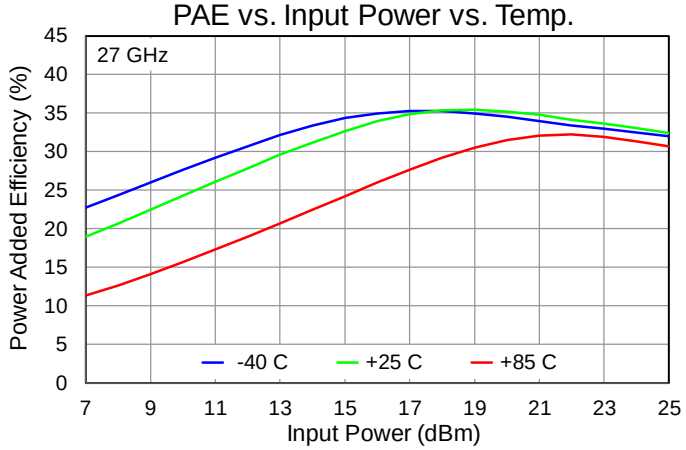
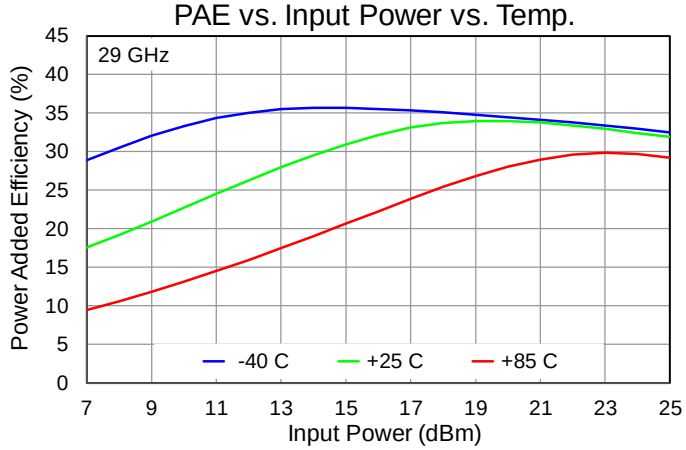


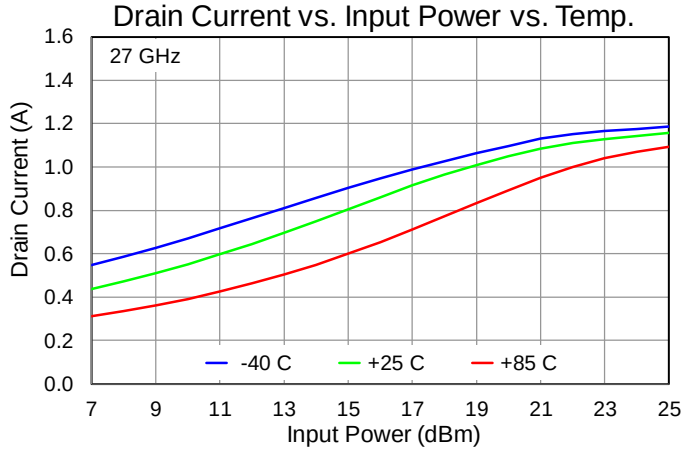
PAE vs. Input Power vs. Temp.



PAE vs. Input Power vs. Temp.



Drain Current vs. Input Power vs. Temp.



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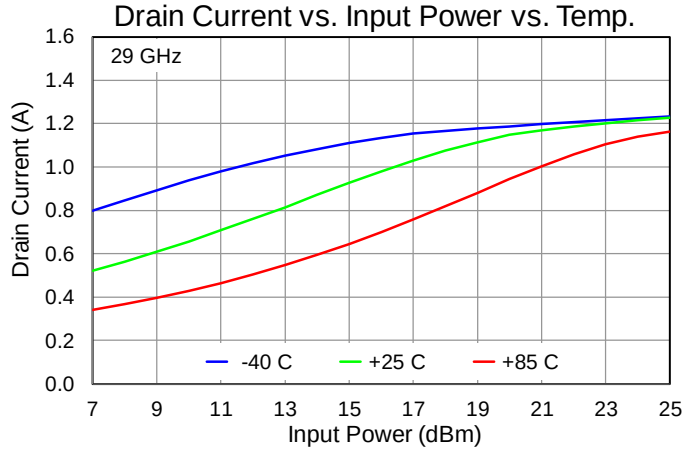

Performance Plots – Large Signal

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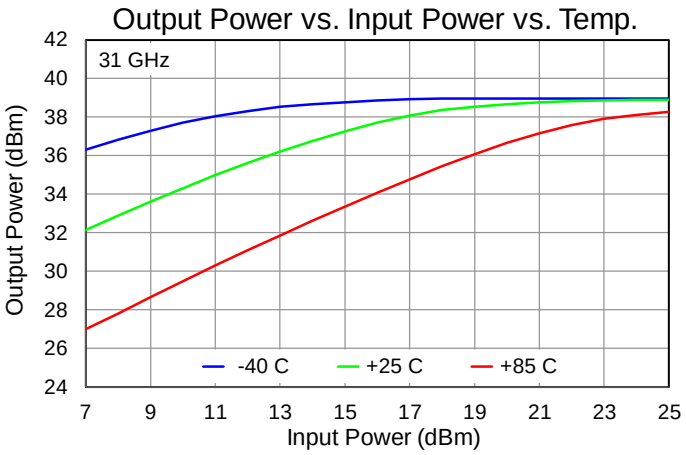

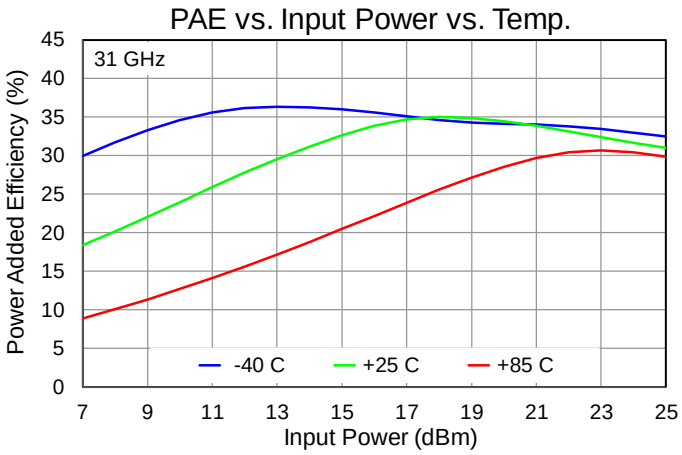

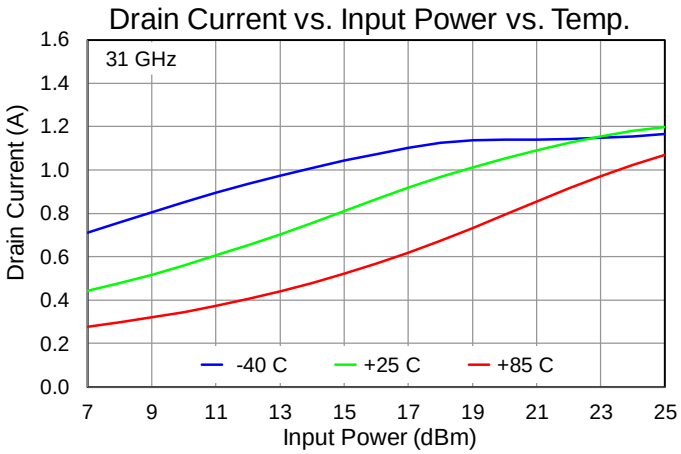

Performance Plots – Large Signal

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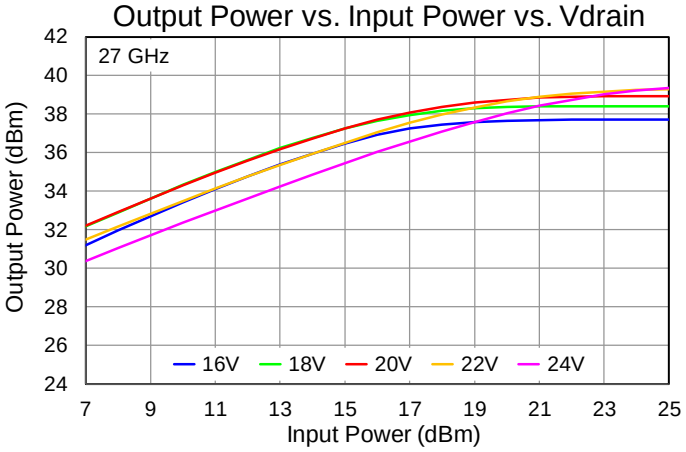
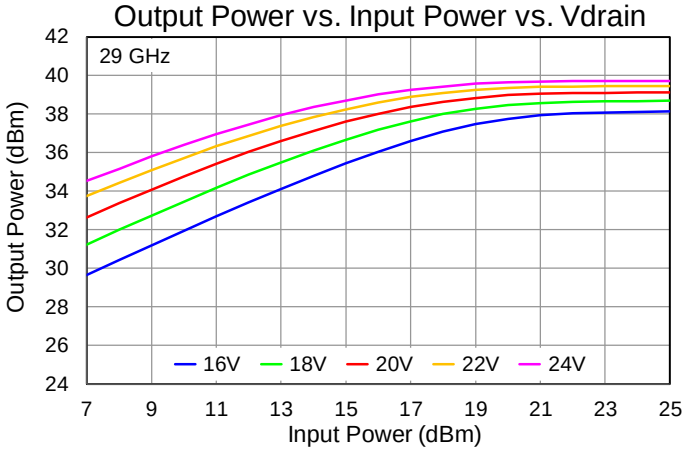
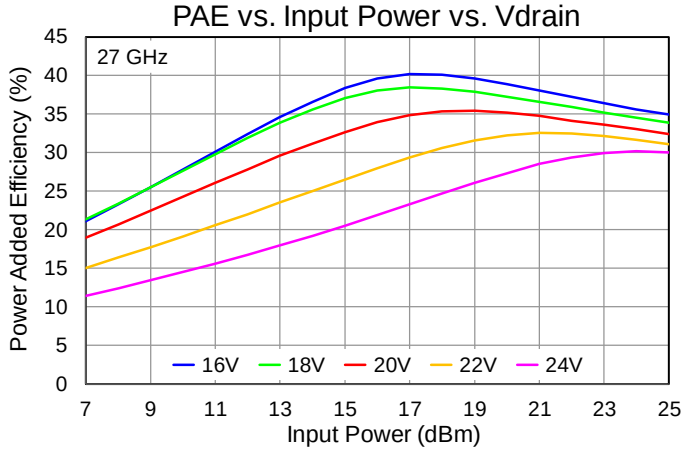
Output Power vs. Input Power vs. Vdrain



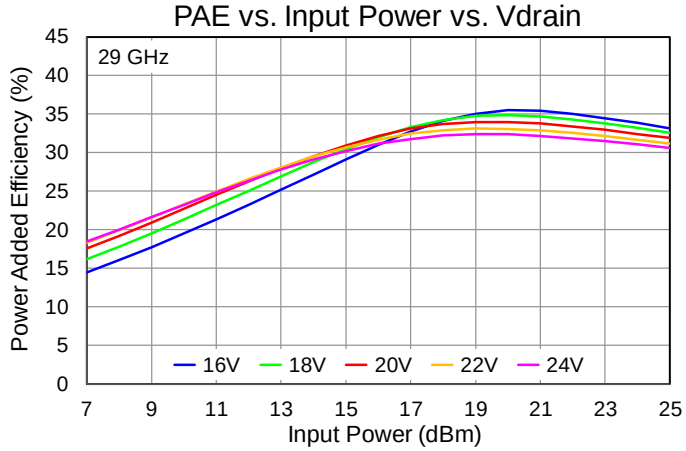
Output Power vs. Input Power vs. Vdrain



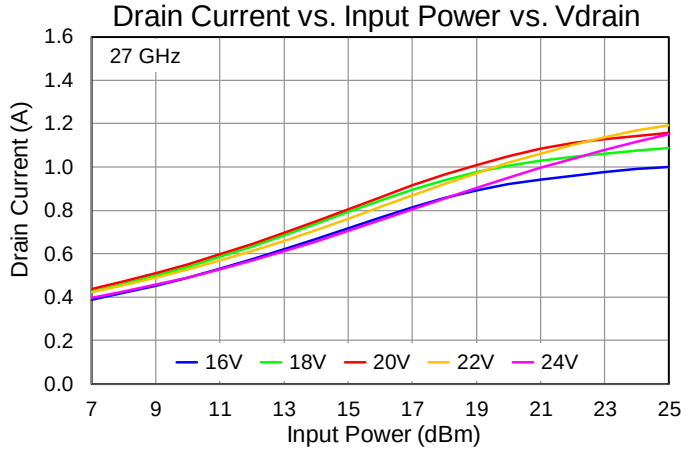
PAE vs. Input Power vs. Vdrain



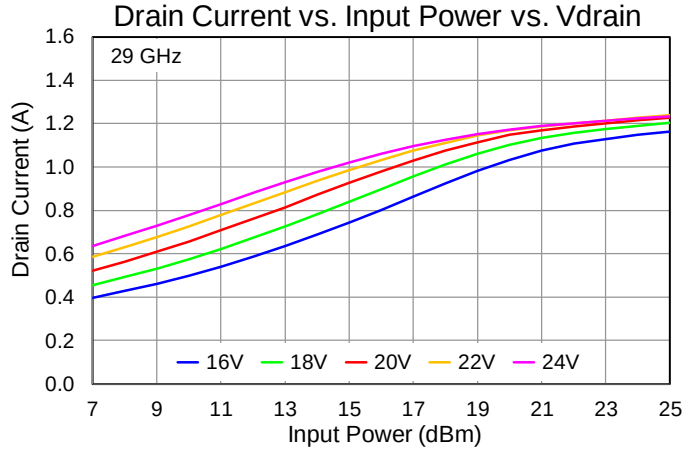
PAE vs. Input Power vs. Vdrain



Drain Current vs. Input Power vs. Vdrain

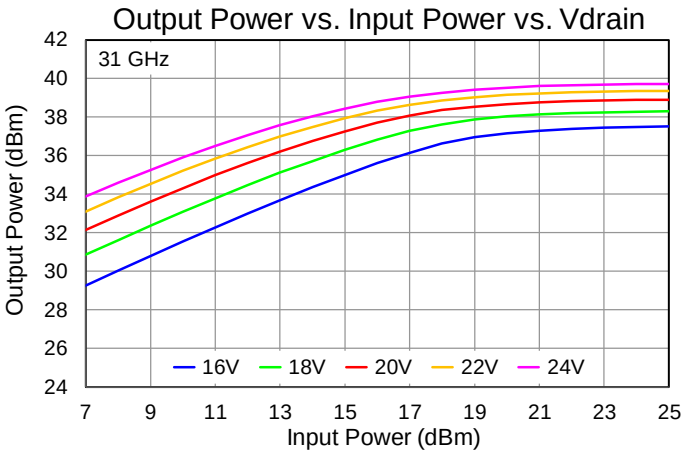


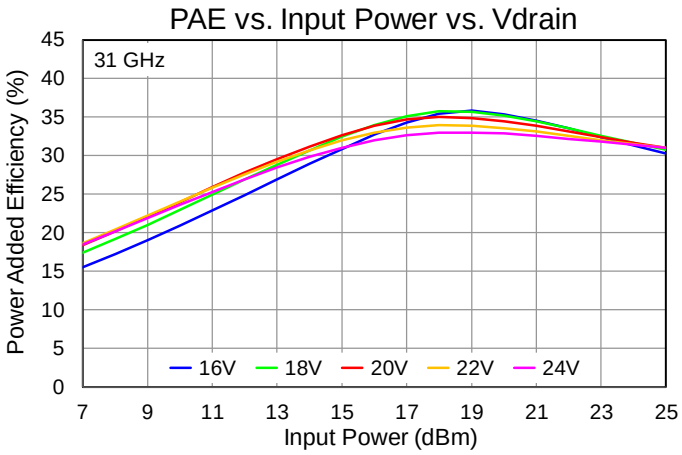
Drain Current vs. Input Power vs. Vdrain

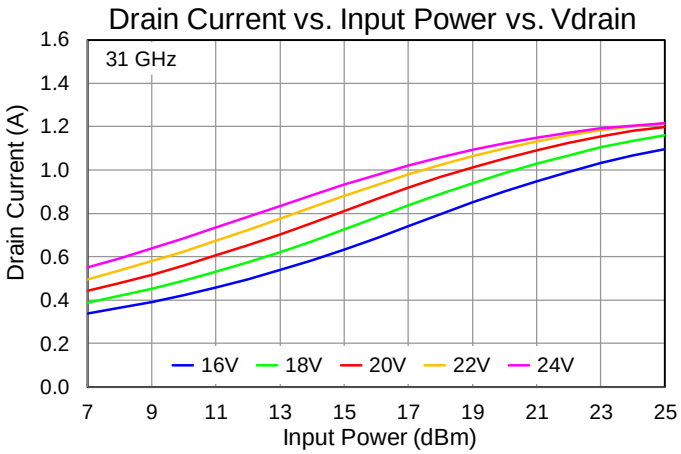


Performance Plots – Large Signal

Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 200 mA, T=+25 °C



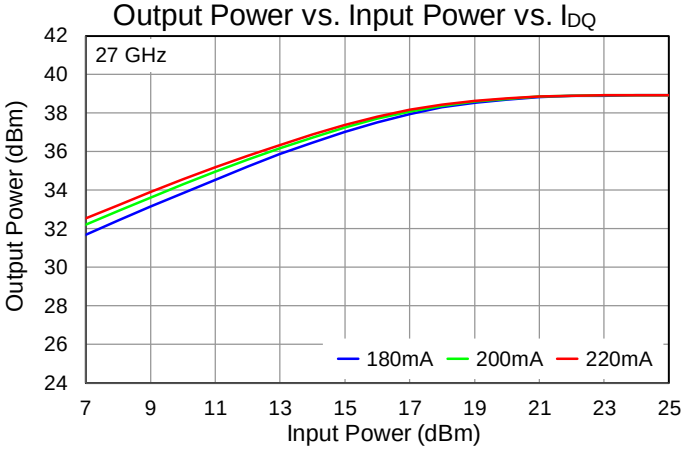




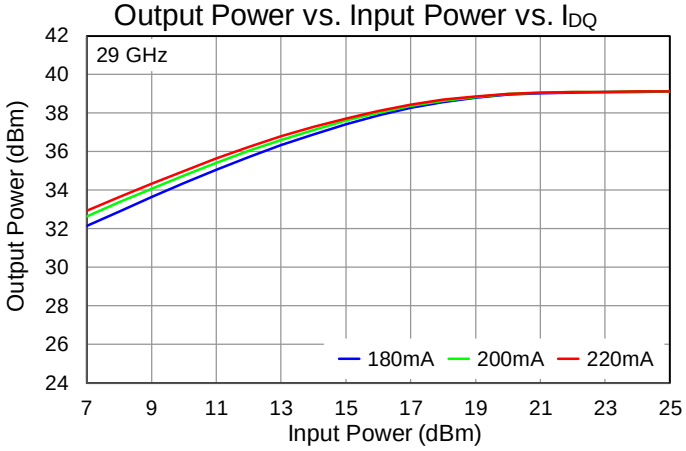
Performance Plots – Large Signal

Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 200 mA, T=+25 °C

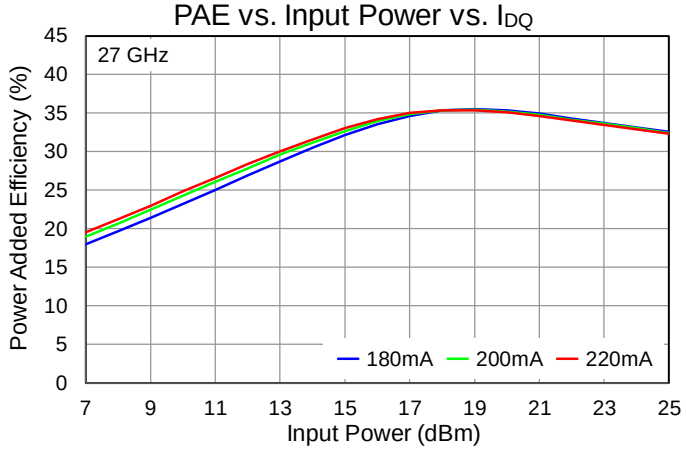
Output Power vs. Input Power vs. I_{DQ}



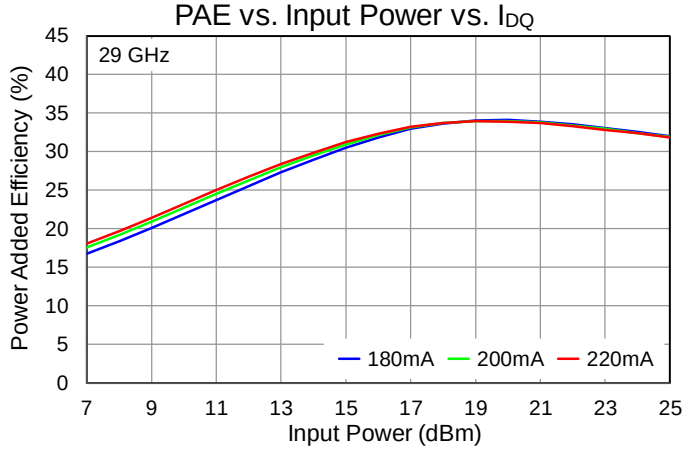
Output Power vs. Input Power vs. I_{DQ}



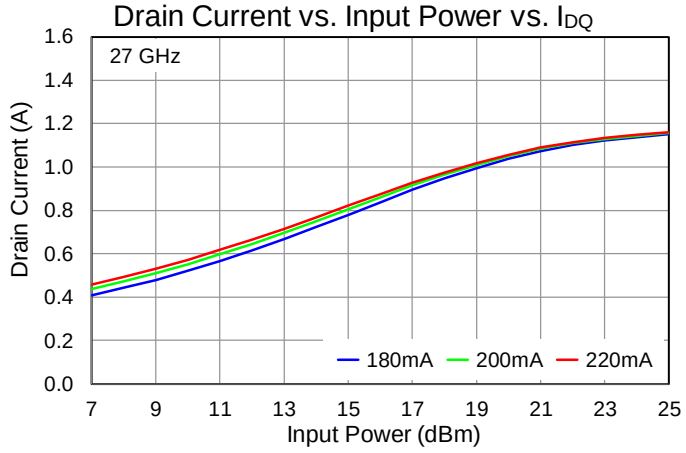
PAE vs. Input Power vs. I_{DQ}



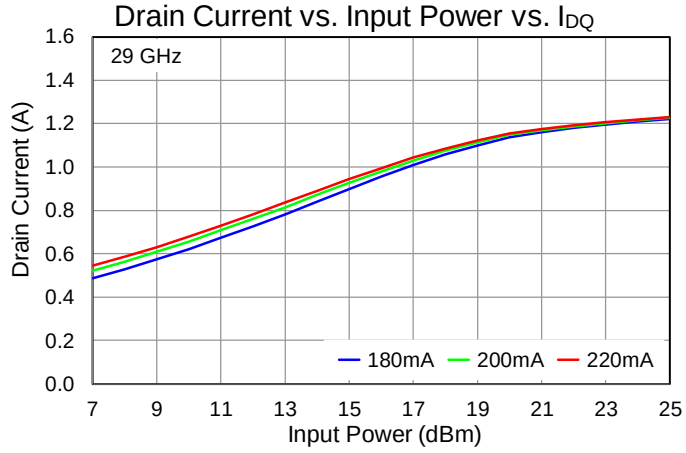
PAE vs. Input Power vs. I_{DQ}



Drain Current vs. Input Power vs. I_{DQ}

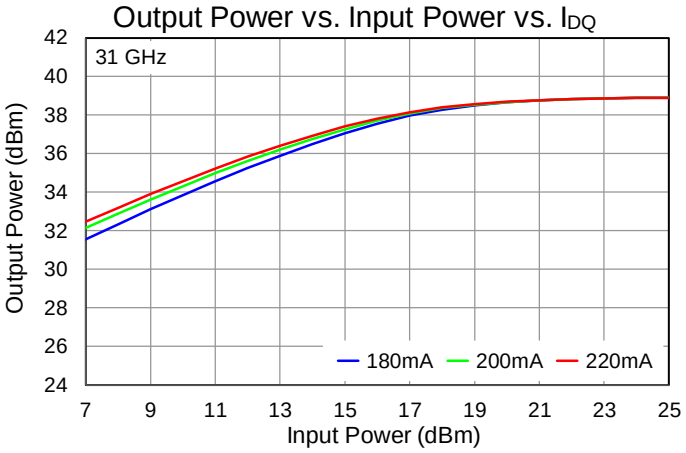


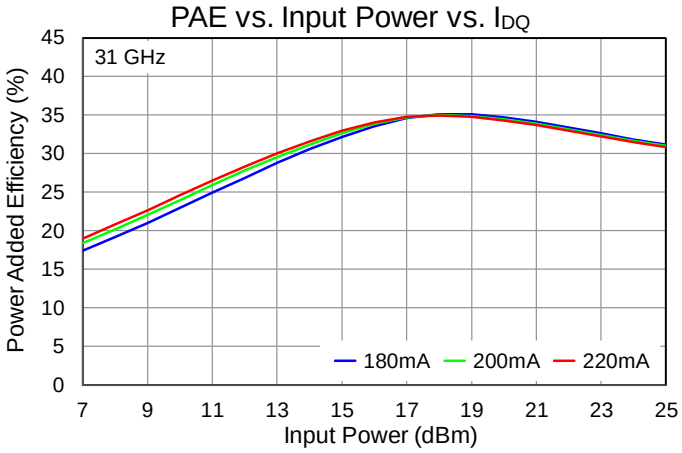
Drain Current vs. Input Power vs. I_{DQ}

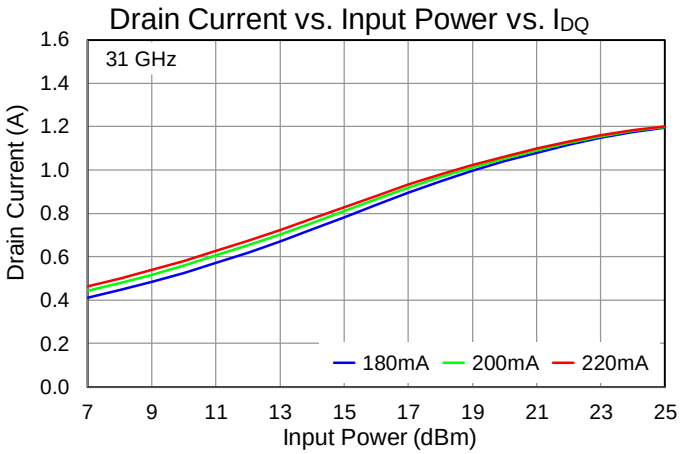


Performance Plots – Large Signal

Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 200 mA, T=+25 °C

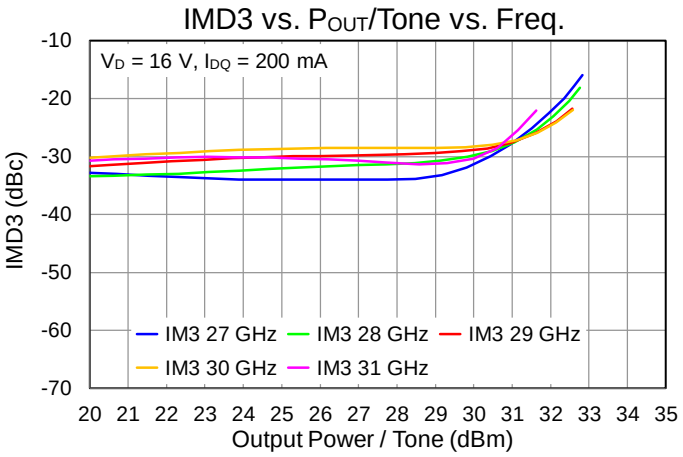


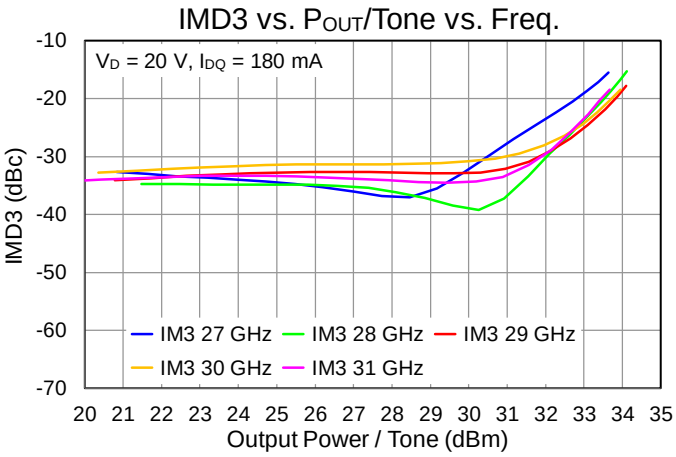


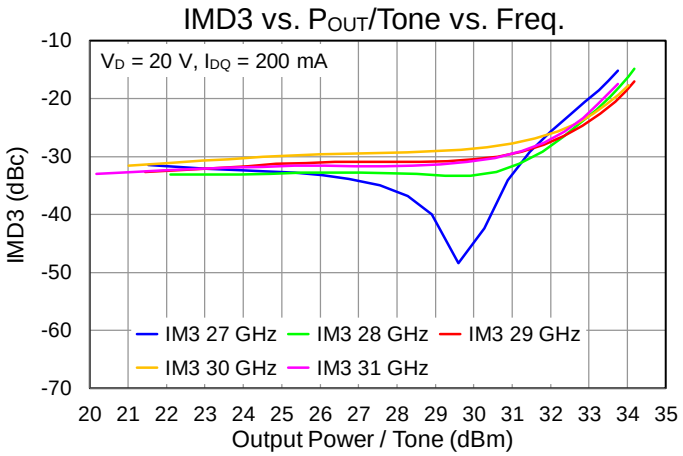


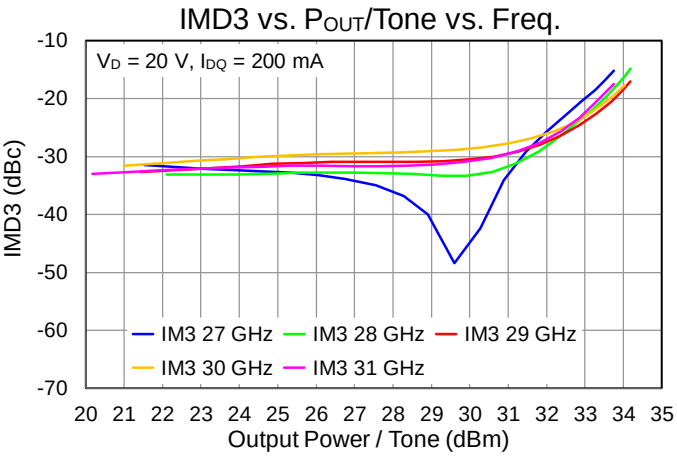
Performance Plots – Linearity

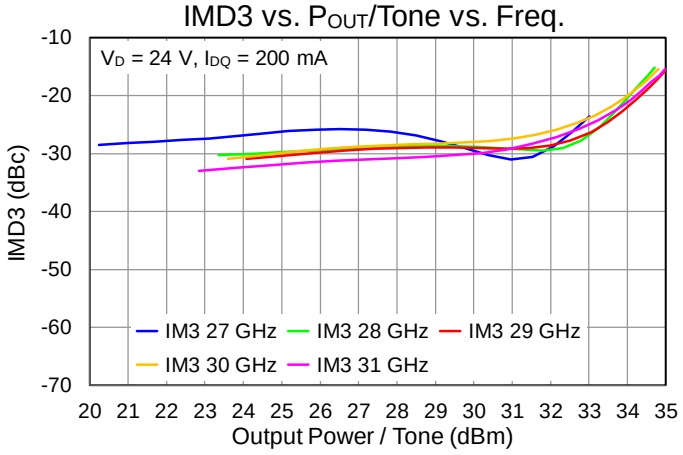
Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 200 mA, T=+25 °C, 10 MHz tone spacing

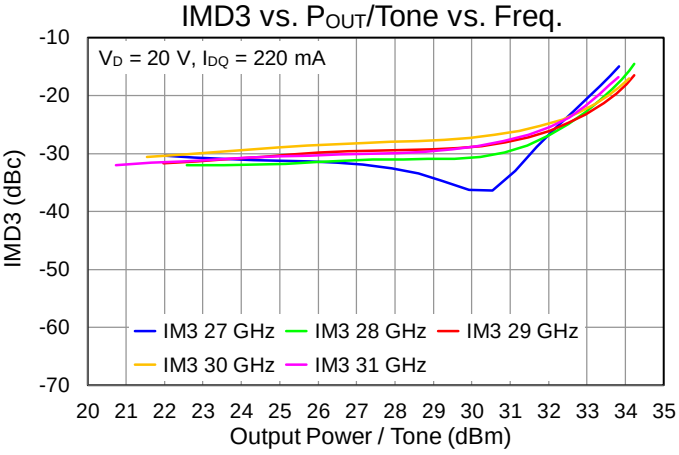






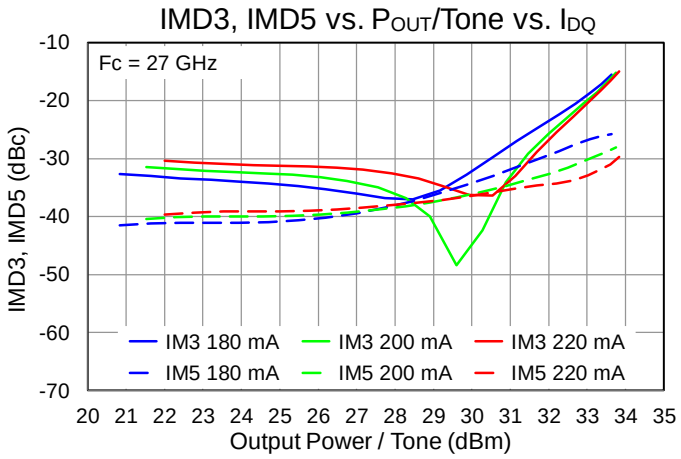


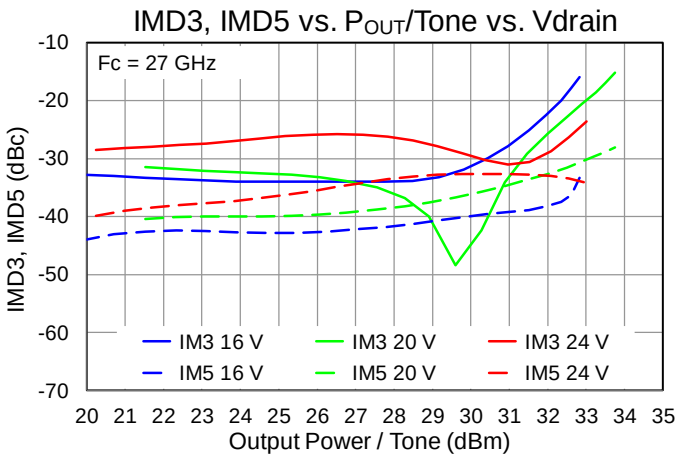


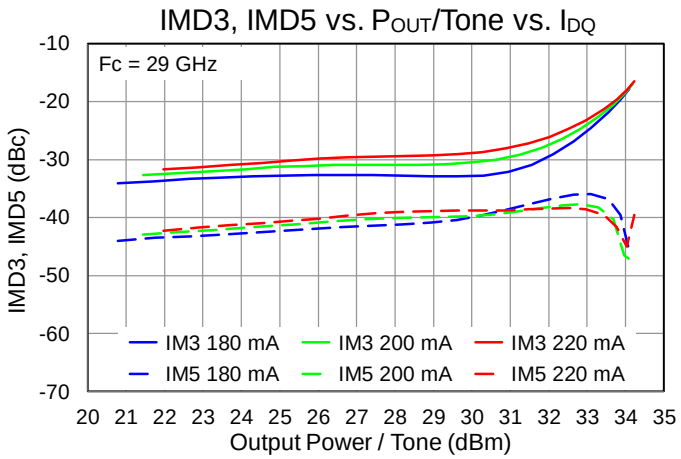


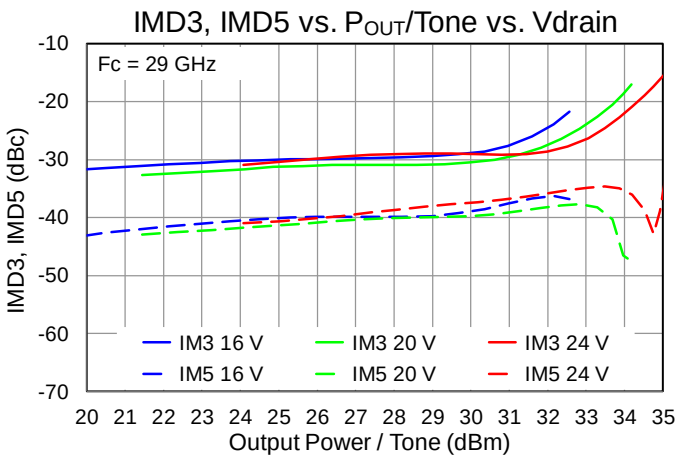
Performance Plots – Linearity

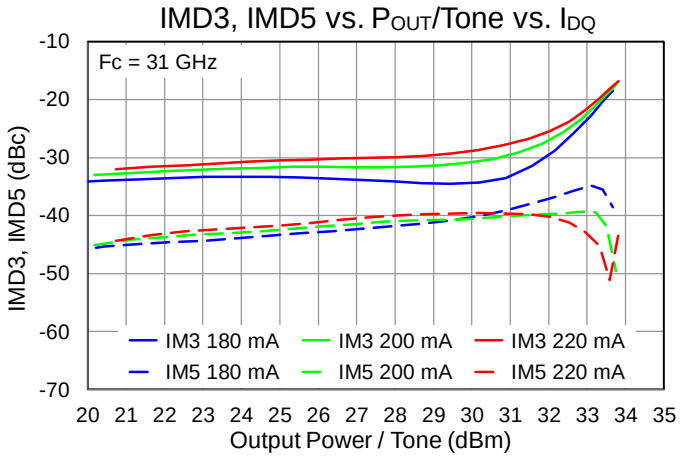
Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 200 mA, T=+25 °C, 10 MHz tone spacing

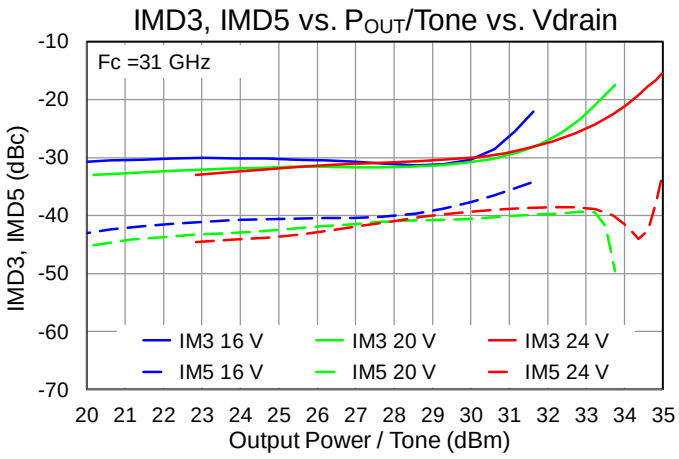






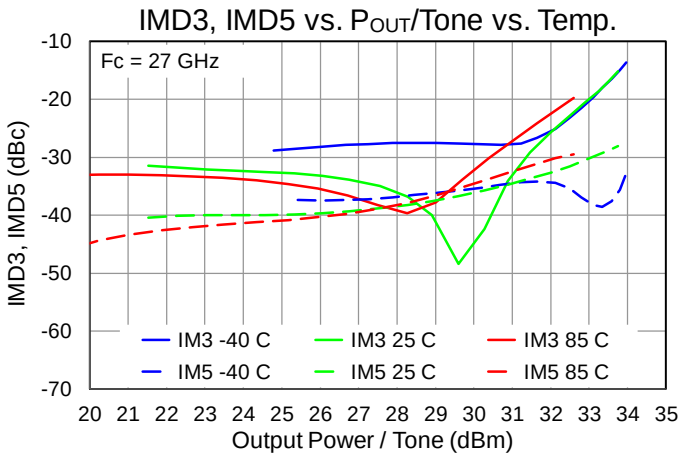


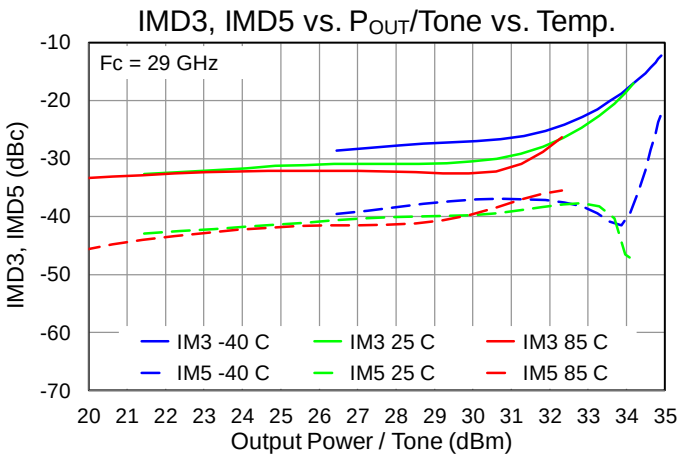


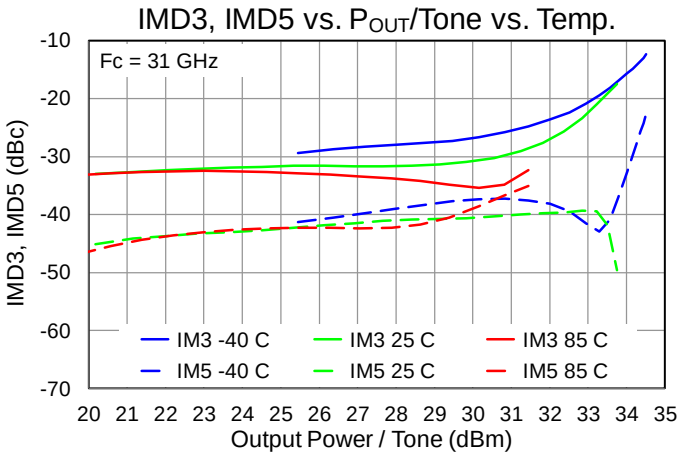


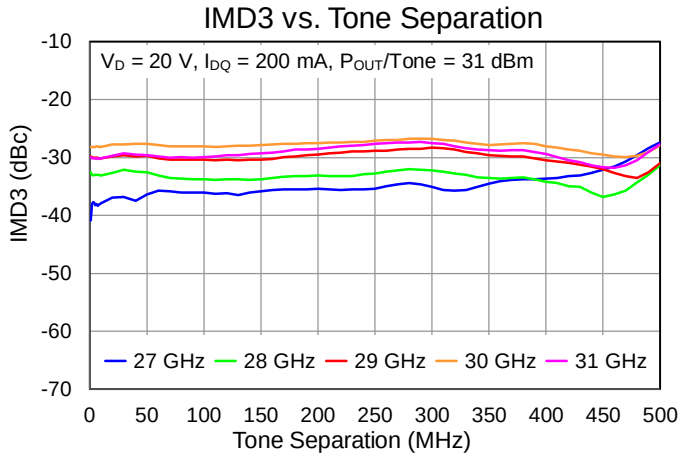
Performance Plots – Linearity

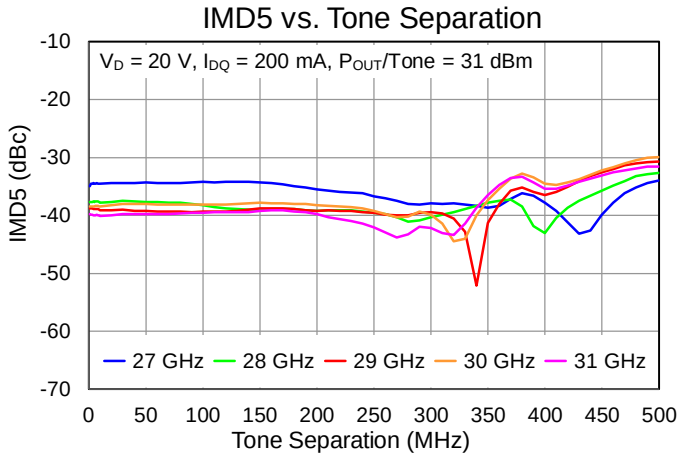
Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 200 mA, T=+25 °C, 10 MHz tone spacing







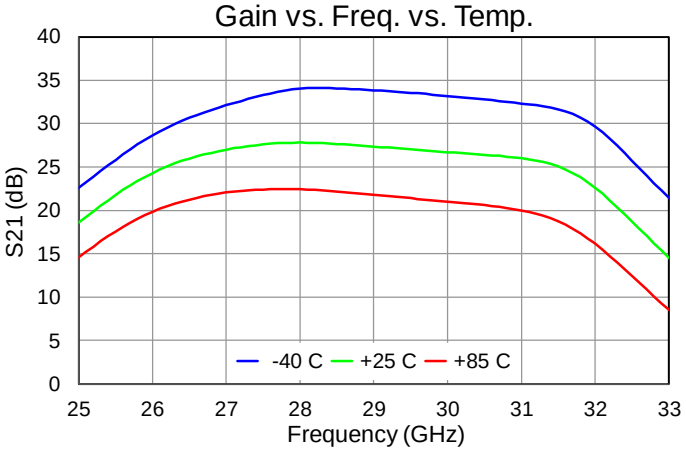




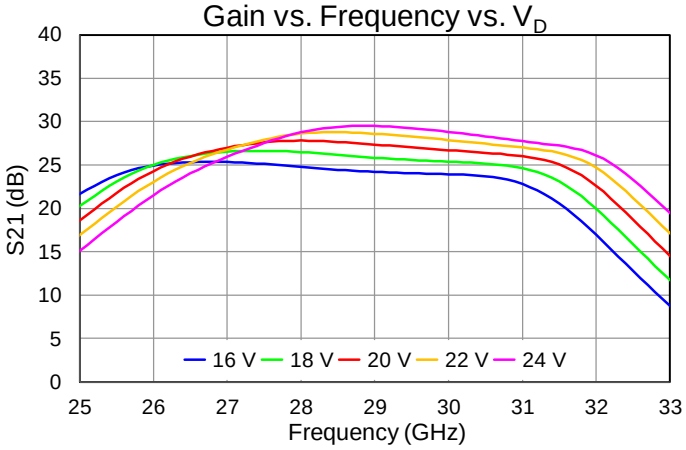
Performance Plots – Small Signal

Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 200 mA, T=+25 °C

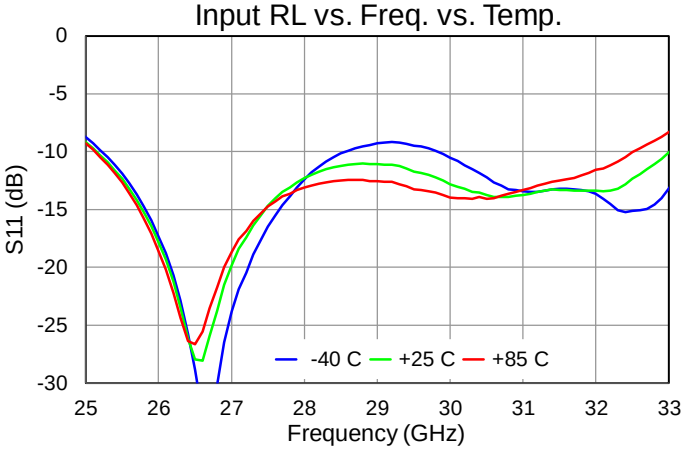
Gain vs. Freq. vs. Temp.



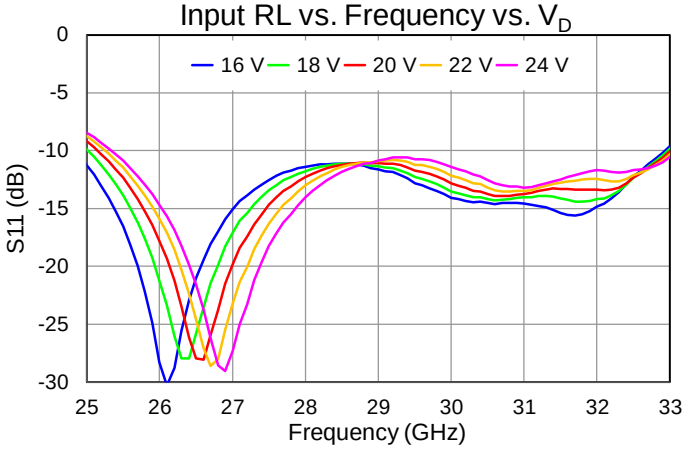
Gain vs. Frequency vs. V_D



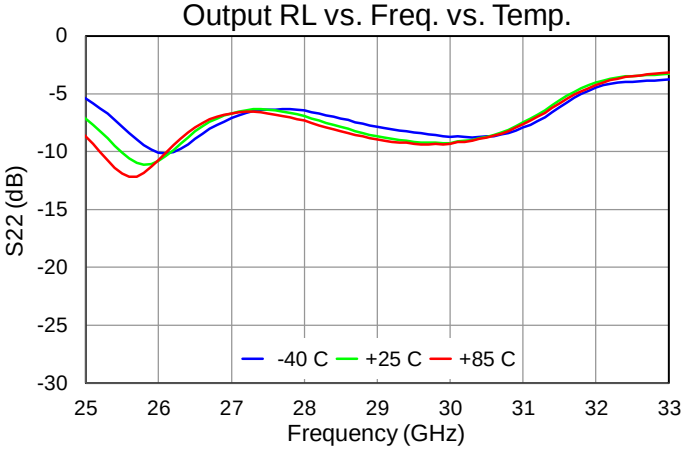
Input RL vs. Freq. vs. Temp.



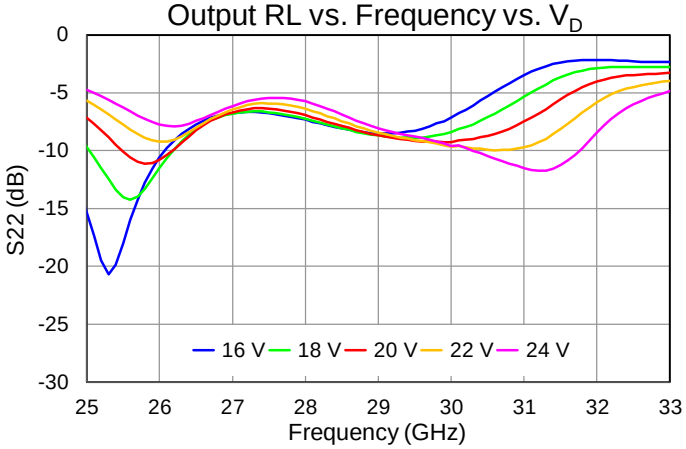
Input RL vs. Frequency vs. V_D



Output RL vs. Freq. vs. Temp.

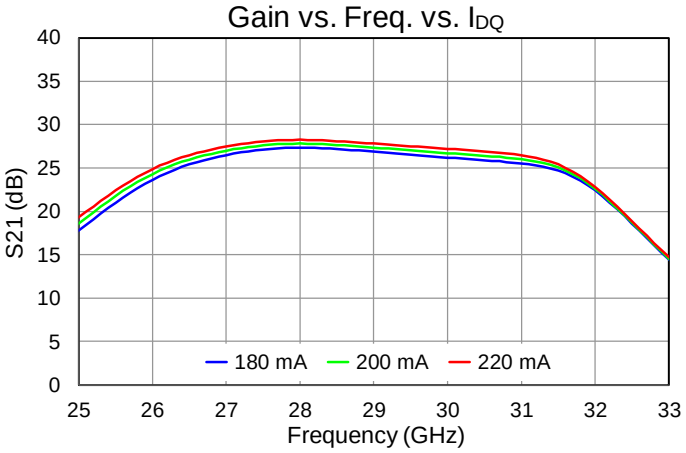


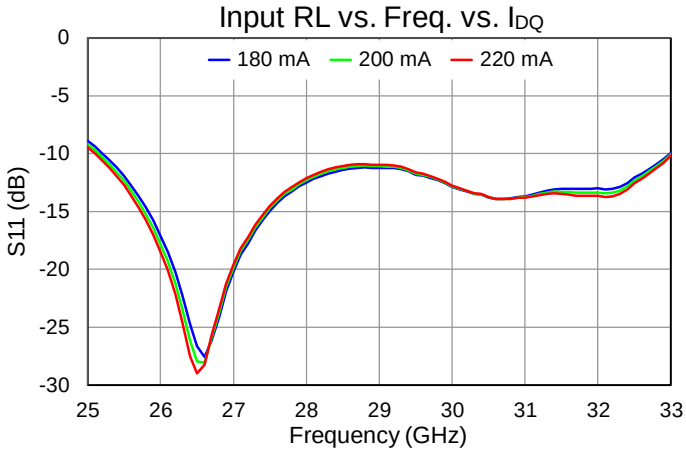
Output RL vs. Frequency vs. V_D

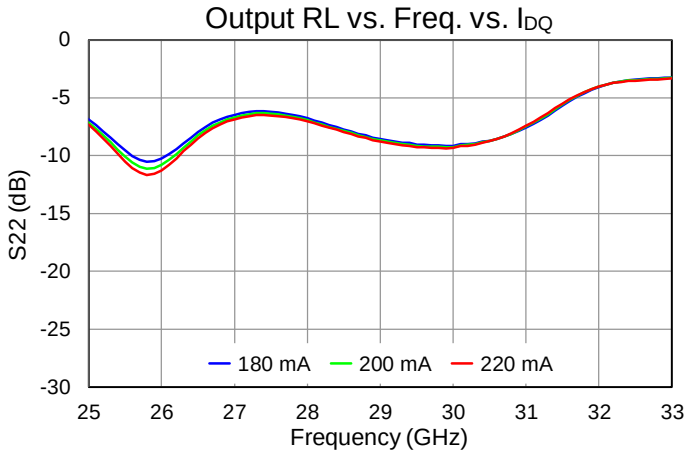


Performance Plots – Small Signal

Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 200 mA, T=+25 °C





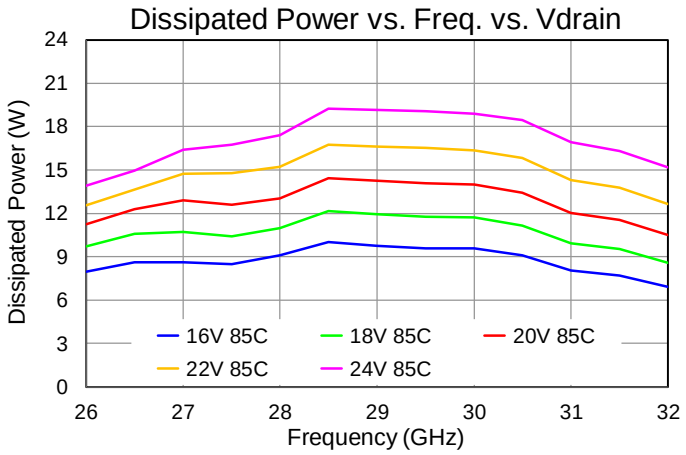


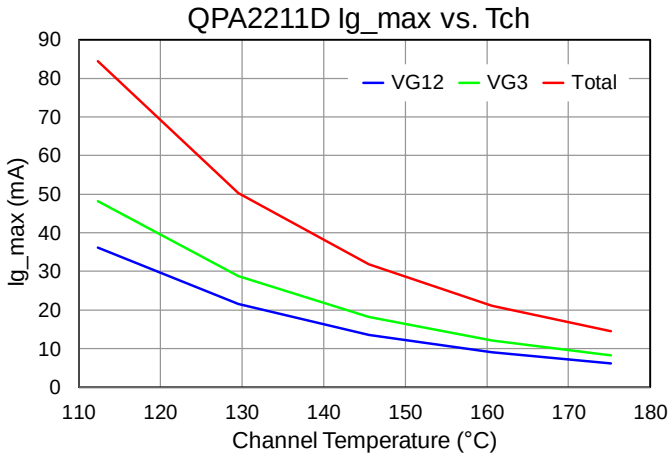
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 20 V, I_{DQ} = 200 mA, P_{DISS} = 4.00 W, No RF (quiescent DC operation)	4.75	ºC/W
Channel Temperature, T_{CH} (No RF) (2)		104	°C
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 20 V, I_{DQ} = 200 mA, Freq = 28.5 GHz, I_{D_Drive} = 1010 mA, P_{IN} = 21 dBm, P_{OUT} = 37.7 dBm, P_{DISS} = 14.40 W	5.55	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		165	°C
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 24 V, I_{DQ} = 200 mA, Freq = 28.5 GHz, I_{D_Drive} = 1105 mA, P_{IN} = 21 dBm, P_{OUT} = 38.7 dBm, P_{DISS} = 19.23 W	5.88	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		198	°C

Notes:
1. Thermal resistance determined to the back of 20 mil CuMo carrier plate (85 °C)
2. IR scan equivalent. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

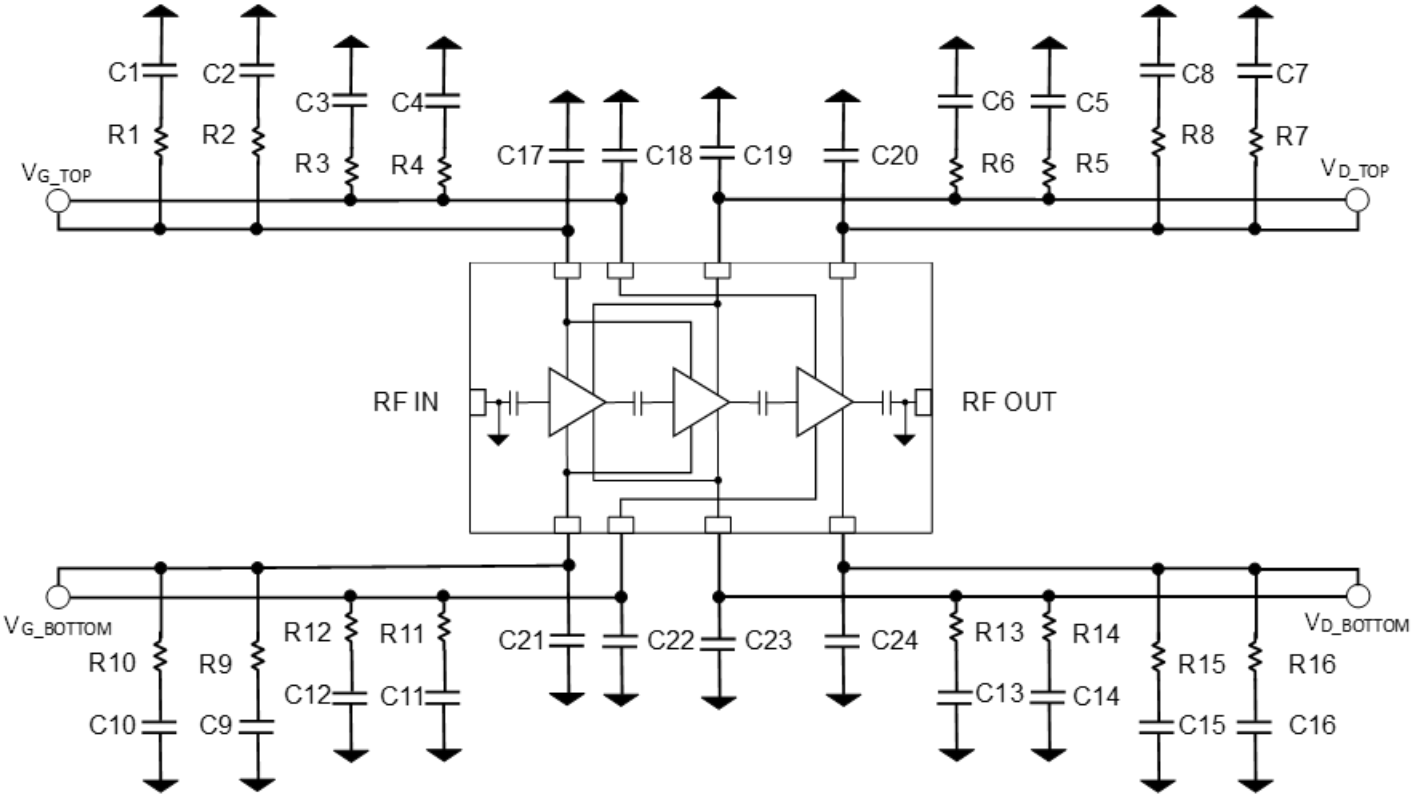
Dissipated Power and Maximum Gate Current





Test conditions, unless otherwise noted: V_D = 20 V, I_{DQ} = 200 mA, T = +25 °C, P_{IN} = 21 dBm

Applications Information

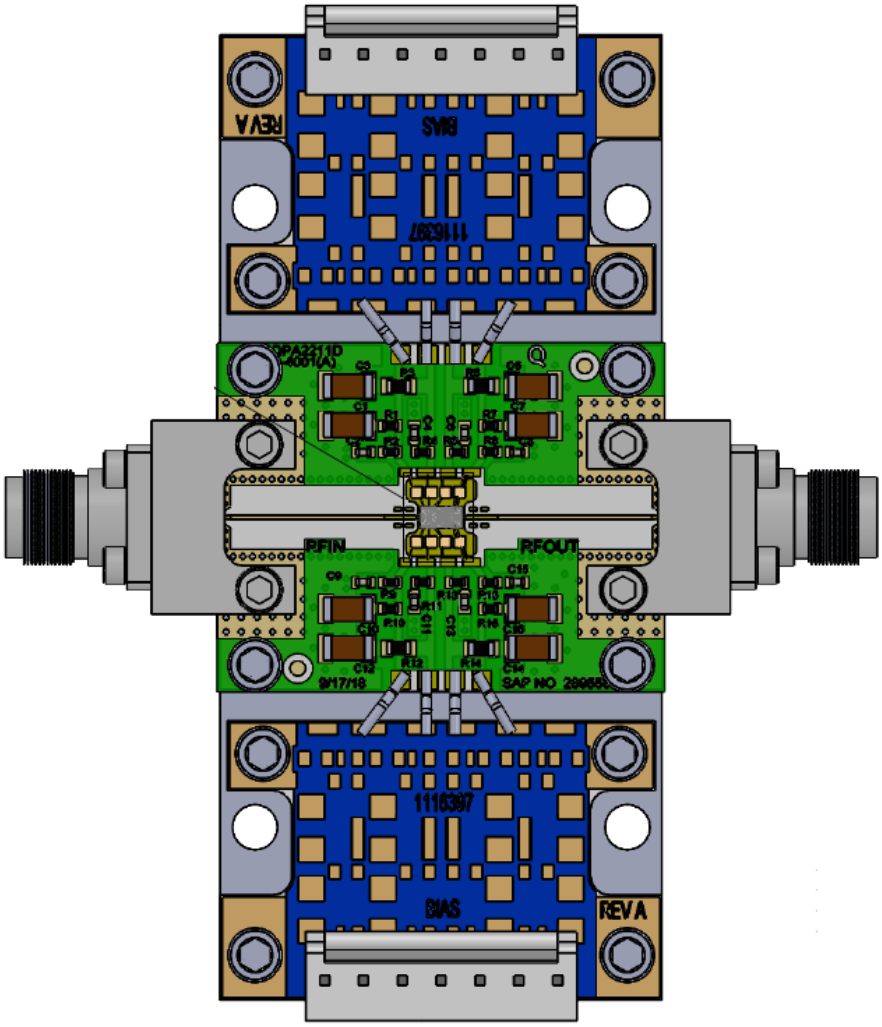


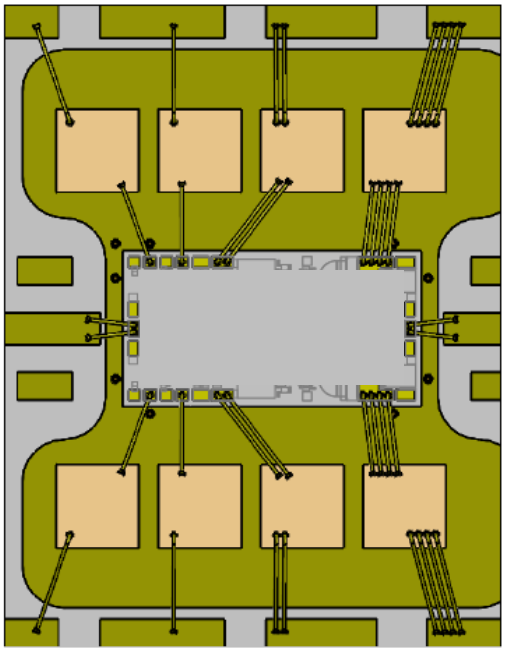
V_{G_TOP} and V_{G_BOTTOM} should be tied together
V_{D_TOP} and V_{D_BOTTOM} should be tied together
V_{G12} and V_{G3} can be separated, if desired, in an attempt to improve IMD performance.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1,C3,C5,C7,C10,C12,C14,C16	10 uF	CAP, 10uF, 20%, 50V, 20%, X5R, 1206	Various	
C2,C4,C6,C8,C9,C11,C13,C15	0.01 uF	CAP, 0.01uF, 10%, 50V, X7R, 0402	Various	
C17,C18,C19,C20,C21,C22,C23,C24	10000 pF	CAP, 10000pF, 20%, 100V, X7R, 30X30, SL	Various	
R1,R10	5.1 Ω	RES, 5.1 OHM, 5%, 50V, 0402	Various	
R2,R4,R6,R7,R8,R9,R11,R13,R15,R16	0 Ω	RES, 0 OHM, JMPR, 0402	Various	
R3,R12	5.1 Ω	RES, 5.1 ohm, 5%,0.1W, 0603	Various	
R5,R14	0 Ω	RES, 0 ohm, 1/10W, 0603	Various	
J1, J2	2.4 mm	RF Connector, 2.4 mm	SW Microwave	1492-04A-5

Evaluation Board (EVB) Layout Assembly





Die and capacitor placement and bonding detail

PCB is made from Rogers 6202 dielectric, .005 inch thick, 0.5 oz. copper both sides.

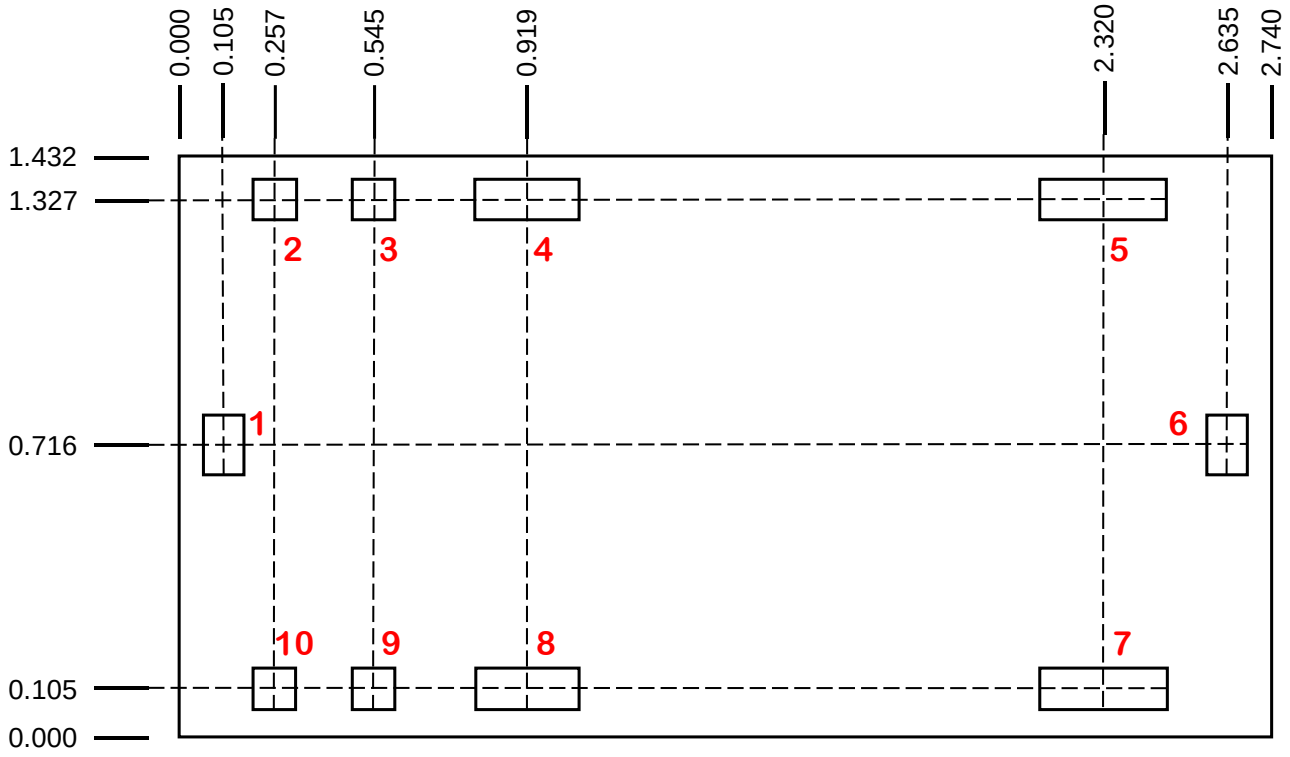
Bias-Up Procedure

1. Set I_D limit to 2000 mA, I_G limit to 20 mA
2. Set V_G to −5.0 V
3. Set V_D +20 V
4. Adjust V_G more positive until $I_{DQ} \approx 200$ mA
5. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to −5.0 V. Ensure $I_{DQ} \sim 0$ mA
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_G supply

Mechanical Information



Dimensions are in mm
Thickness: 0.050
Die x, y size tolerance: ± 0.050
Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Size (um x um)	Description
1	RF IN	90 x 140	RF input. 50 Ohms. DC blocked, DC grounded.
2, 10	V_{G12}	100 x 90	Gate voltage stages 1 & 2. Bypass network required; refer to page 18.
3, 9	V_{G3}	100 x 90	Gate voltage stage3. Bypass network required; refer to page 18.
4, 8	V_{D12}	250 x 90	Drain voltage stages 1 & 2. Bypass network required; refer to page 18.
5, 7	V_{D3}	312 x 90	Drain voltage stage 3. Bypass network required; refer to page 18.
6	RF OUT	90 x 140	RF output. 50 Ohms. DC blocked, DC grounded.

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESD/JEDEC JS-001

Caution!

ESD-Sensitive Device

Solderability

Use only AuSn (80/20) solder, and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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