

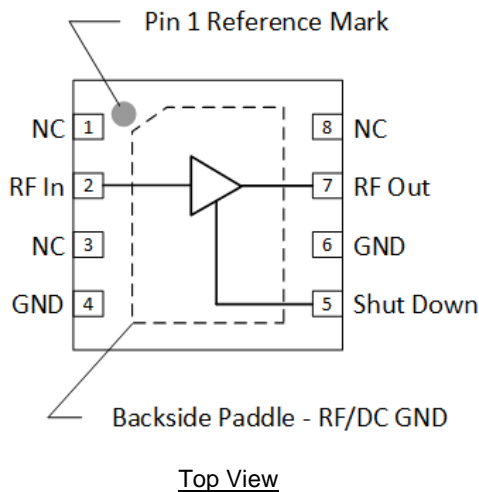
### Product Overview

The QPA9126 is a cascadable, high linearity gain block amplifier in a low-cost surface mount package. At 3.5 GHz, the amplifier provides 16 dB gain, +35.5 dBm OIP3 and 1.4 dB Noise Figure while drawing 70 mA current from a 5V supply.

The QPA9126 provides very flat gain across a broad range of frequencies with the integration of a shut-down biasing capability to allow for operation for TDD applications. The low noise figure and high linearity performance allows the device to be used in both receiver and transmitter chains for high performance systems. The internal active bias circuit also enables stable operation over bias and temperature variations and can be biased from a single positive supply ranging from +3.3 to +5 volts. The amplifier is internally matched using a high-performance E-pHEMT process and is housed in a small 2 x 2 mm surface-mount package.

The QPA9126 covers the 1 – 6 GHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.

### Functional Block Diagram



8 Pad 2 x 2 mm DFN Package

### Key Features

- 1.0 – 6.0 GHz Operational
- 50Ω Matched RF Input and Output
- 0.3dB Gain Flatness over 400 MHz Bandwidth
- 16 dB Gain
- +35 dBm Output IP3
- +20 dBm P1dB
- 1.4dB Noise Figure
- 1.8V Logic Compatible Shutdown Control

### Applications

- 5G m-MIMO
- Mobile Infrastructure
- Repeater / DAS
- General Purpose Wireless
- TDD / FDD System
- Defense Communication

### Ordering Information

Part No.	Description
QPA9126TR7	2,500 pieces on a 7" reel (standard)
QPA9126 EVB-01	Evaluation Board

## Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 °C to +150 °C
RF Input Power, CW, 50 Ω, T=25 °C	22 dBm
Device Voltage (V <sub>DD</sub> )	+7 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

## Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V <sub>DD</sub> )	+3.3	+5.0	+5.25	V
T <sub>CASE</sub>	-40		+105	°C
T <sub>j</sub> for >10 <sup>6</sup> hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

Parameter	Conditions <sup>(1)</sup>	Min	Typ	Max	Units
Operational Frequency Range		1000		6000	MHz
Test Frequency			3500		MHz
Gain			16		dB
Gain Flatness	Over 400 MHz		0.3		dB
Input Return Loss			9		dB
Output Return Loss			12		dB
Output P1dB			20		dBm
Output IP3	P <sub>out</sub> = +1 dBm/tone, Δf = 1 MHz		35.5		dBm
Noise Figure	EVB trace loss excluded		1.4		dB
Device Current, ON	V <sub>PD</sub> = 0 V		68		mA
Device Current, OFF			4.5		mA
V <sub>PD</sub> , Logic Low		0		0.63	V
V <sub>PD</sub> , Logic High		1.17		V <sub>DD</sub>	V
I <sub>PD</sub> , Control Pin Current			30		μA
Device ON or OFF Timing	50% of V <sub>PD</sub> to 90% or 10% RF Output		0.07		μS
Thermal Resistance, θ <sub>JC</sub>	Junction to case			50.0	°C/W

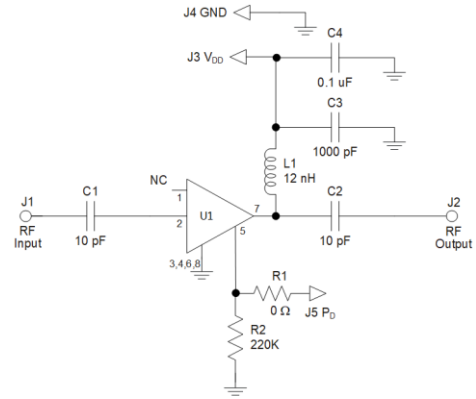
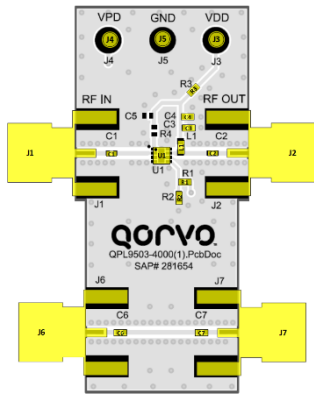
Notes:

1. Test conditions unless otherwise noted: V<sub>DD</sub> on EVB = +5.0V, V<sub>PD</sub> = 0V, Temp = +25 °C, 50 Ω system.

## Logic Table

Parameter, V <sub>PD</sub>	High	Low
Device State	OFF	ON

## Evaluation Board - QPA9126EV-01



**Notes:**

1. See Evaluation Board PCB Information for material and stack-up
2. R3, 0 Ω jumper, is not shown on the schematic. It could be replaced with cooper trace in target layout

## Bill of Material

Ref. Des.	Value	Description	Manuf.	Part Number
n/a	-	Printed Circuit Board	Qorvo	281654
U1	-	High Gain High Linearity Amplifier	Qorvo	QPA9126
R1, R3	0 Ω	Res, 0 Ω, 0402, 1/10W	various	
R2	220 KΩ	Res, 220 KΩ, 0402, 5%, 1/16W	various	
C1, C2	10 pF	Cap, 10 pF, 0402, 5%, 50V C0G	various	
C3	1000 pF	Cap, 1000 pF, 0402, 10%, 50V X7R	various	
C4	0.1 μF	Cap, 0.1 μF, 0402, 10%, 50V, X5R	various	
L1	12 nH	Ind, 12 nH, 0603, 5%, W/W	Coilcraft	0603HP-12NXGLW
J1, J2	-	Conn, SMA F STRT .062"	Cinch Connectivity	142-0701-851

## Typical Performance on EVB

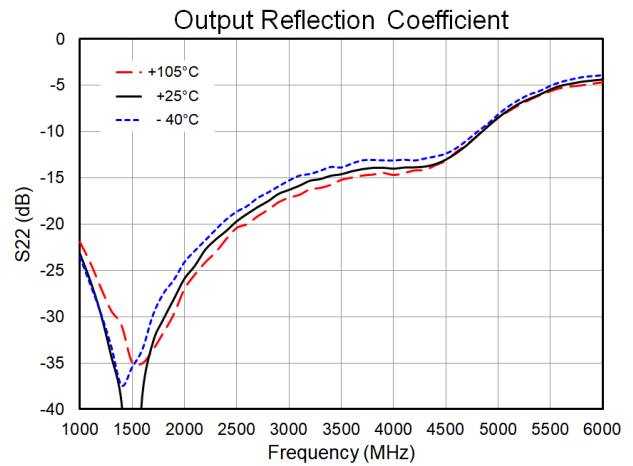
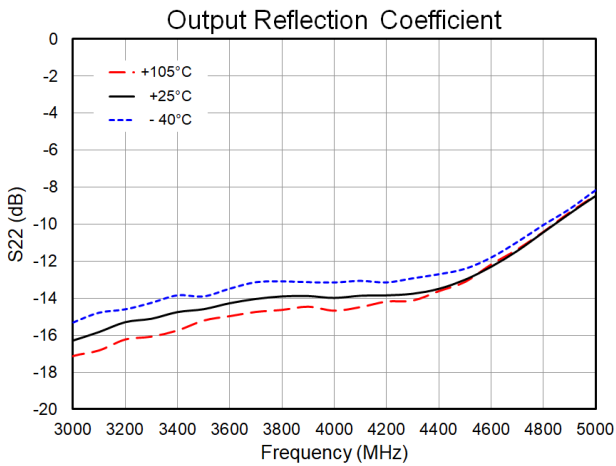
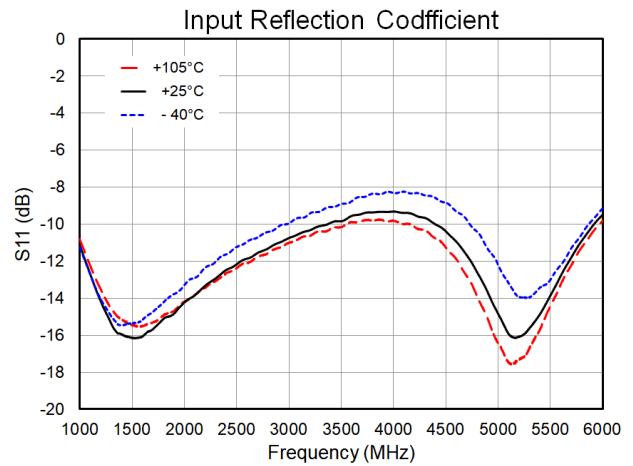
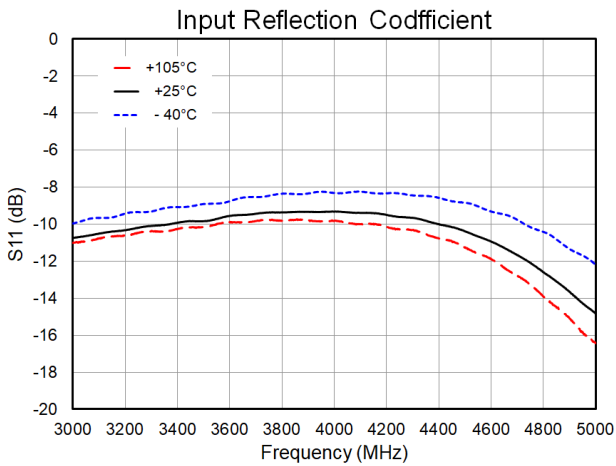
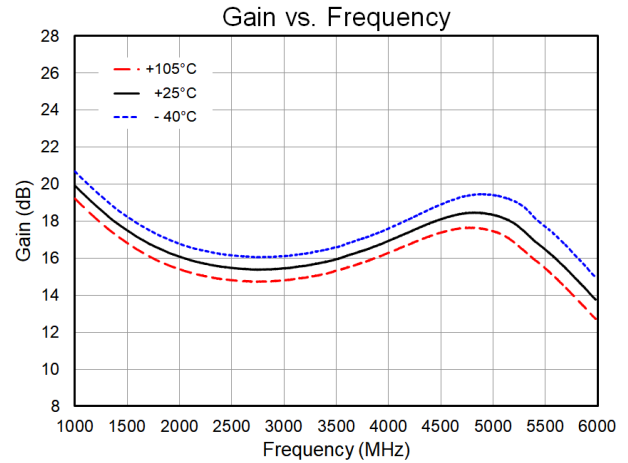
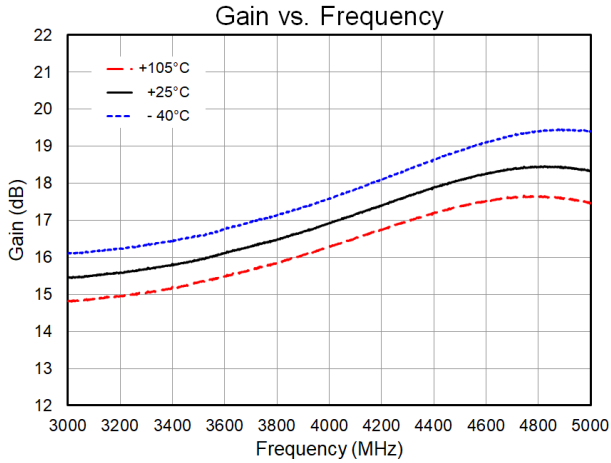
Parameter	Conditions	Typical Value					Units
		3000	3500	4000	4500	5000	
Frequency		3000	3500	4000	4500	5000	MHz
Gain	Small Signal	15.4	15.9	16.9	18.1	18.3	dB
Input Return Loss		10.7	9.8	9.3	10.4	14.8	dB
Output Return Loss		16.3	14.6	14.0	13.0	8.5	dB
Noise Figure	Including EVB trace loss	1.57	1.56	1.67	1.70	1.78	dB
Output P1dB		20.9	20.1	19.2	18.0	18.2	dBm
Output IP3	Pout = +1 dBm/tone, Δf = 1 MHz	37.1	36.5	37.4	36.8	35.4	dBm
Device Current	I <sub>DD</sub>	68					mA

**Notes:**

1. Test Conditions unless otherwise noted: V<sub>DD</sub> on EVB = +5.0V, V<sub>PD</sub> = 0 V, Temp.=+25 °C

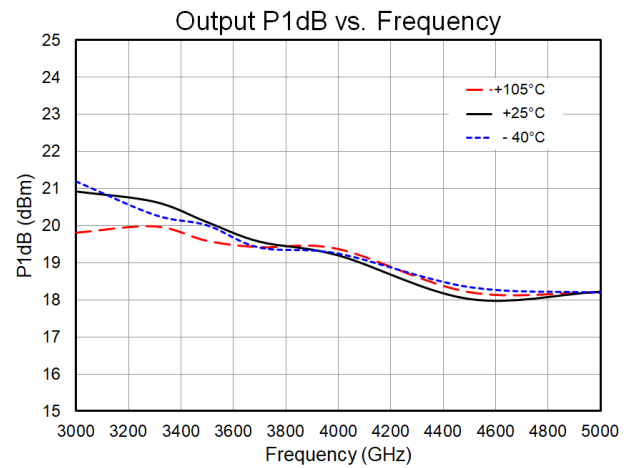
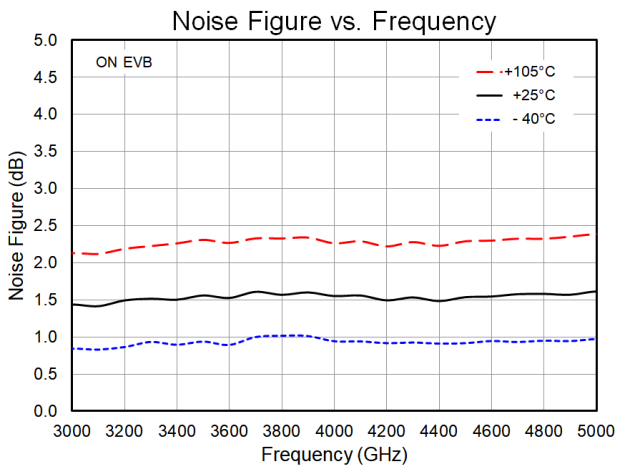
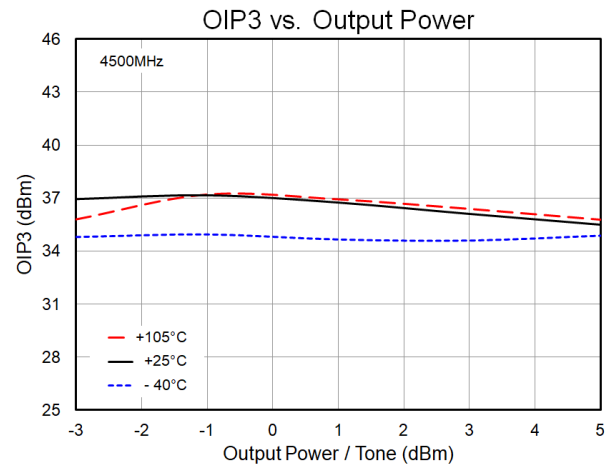
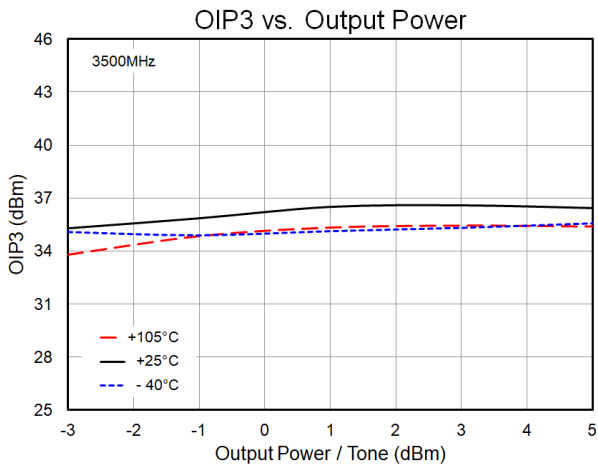
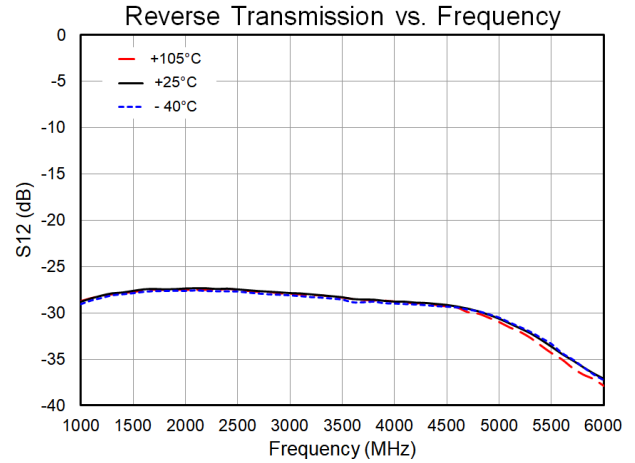
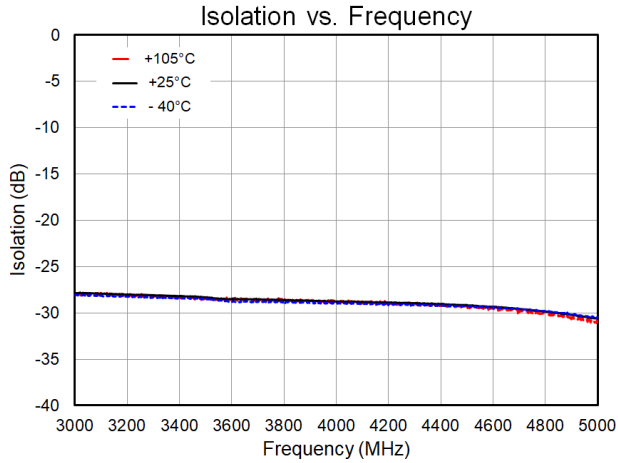
**Performance Plots – QPA9126EVB-01**

Test conditions unless otherwise noted:  $V_{DD}$  on EVB = +5.0 V,  $I_{DD}$  = 70 mA,  $V_{PD}$  = 0 V, Temp. = +25 °C



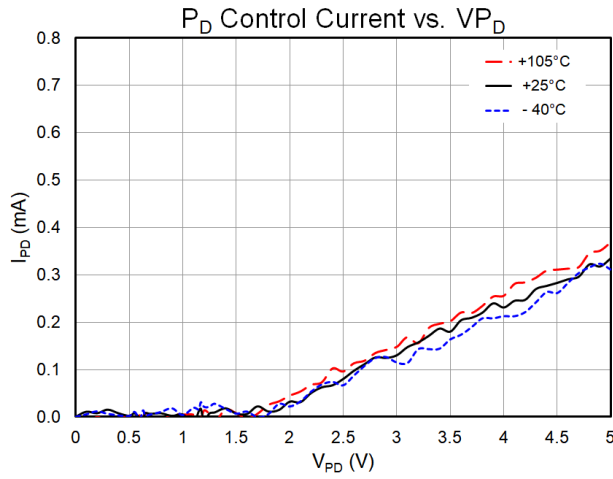
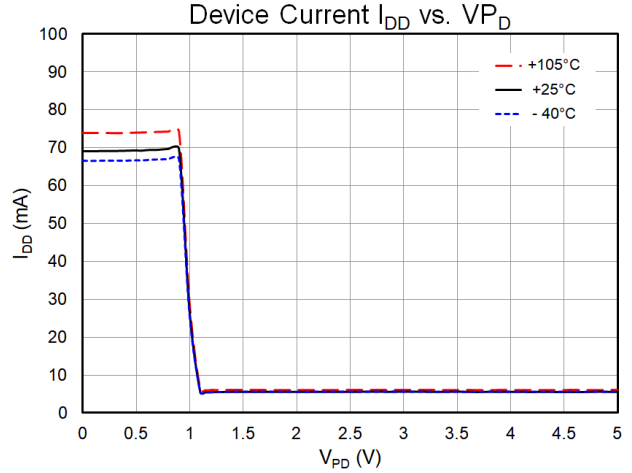
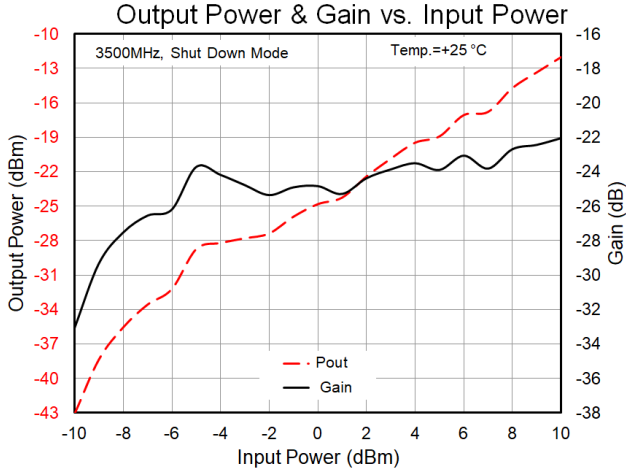
## Performance Plots – QPA9126EVB-01 (Continue)

Test conditions unless otherwise noted:  $V_{DD} = +5.0\text{ V}$ ,  $I_{DD} = 70\text{ mA}$ ,  $V_{PD} = 0\text{ V}$ , Temp. =  $+25\text{ }^{\circ}\text{C}$



Performance Plots – QPA9126EVB-01 (Continue)

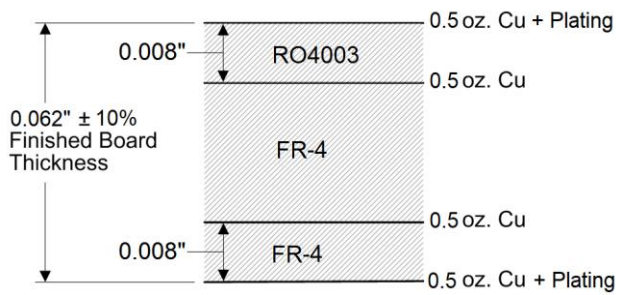
Test conditions unless otherwise noted:  $V_{DD}$  on EVB = +5V,  $I_{DD}$  = 70 mA,  $V_{PD}$  = 0 V, Temp.=+25 °C, on QPA9126EVB01



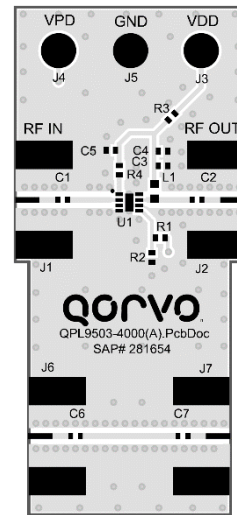
**Evaluation Board PCB Information**

**PC Board Layout**

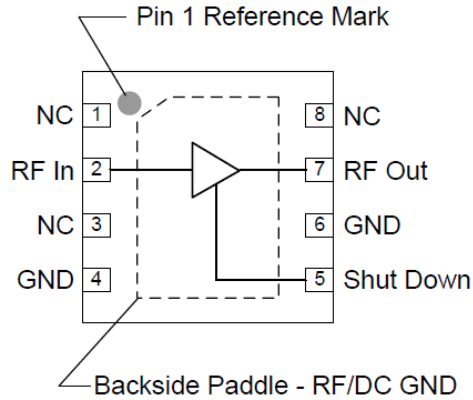
PCB Material Stackup



50 Ω line dimensions: width = 0.0182", spacing = 0.020"



## Pad Configuration and Description



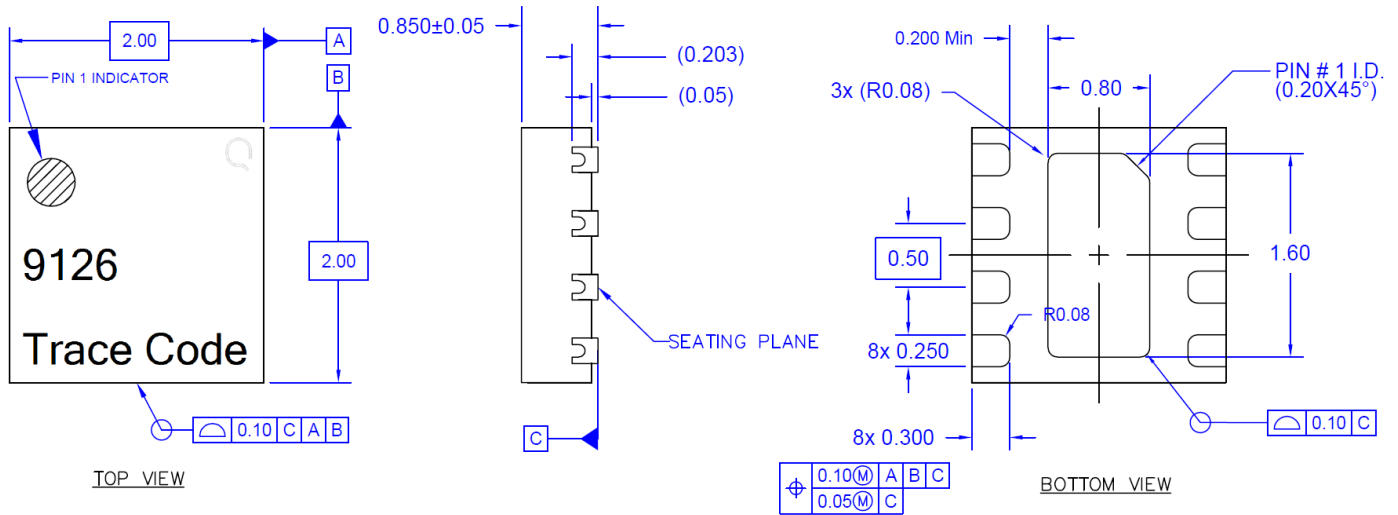
Top View

Pad No.	Label	Description
1, 3, 4, 6, 8	NC or GND	No electrical connection internally. It may be left floating or connected to ground. Land pads should be provided for PCB mounting integrity.
2	RF IN	RF input. Internally matched to 50Ω. External DC Block required
5	Shut Down	Amplifier ON/OFF Logic control input, controls internal bias voltage regulator
7	RF OUT	RF output and the amplifier DC supply $V_{DD}$ input. Internally matched to 50Ω. External chock and DC Block capacitor required.
Backside Paddle	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.



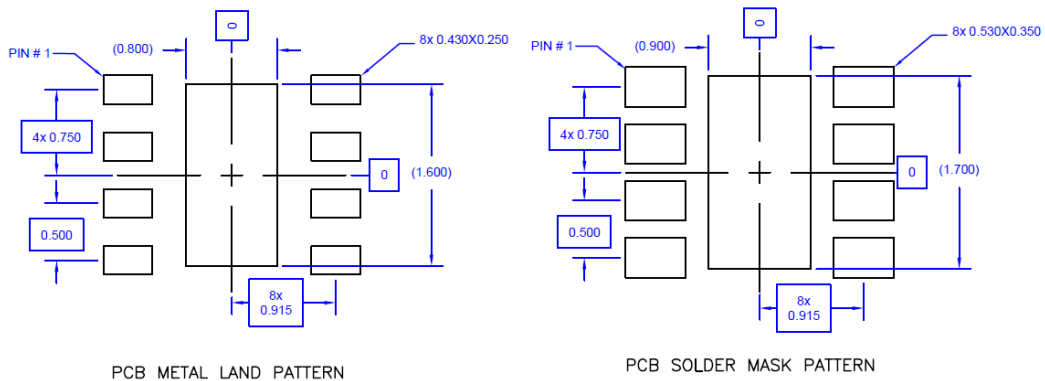
## Package Marking and Dimensions

Marking: Pin 1 marker – Dot and Logo – Q  
 Part Number – 9126  
 Trace Code – XXXX up to 4 Characters assigned by sub-contractor



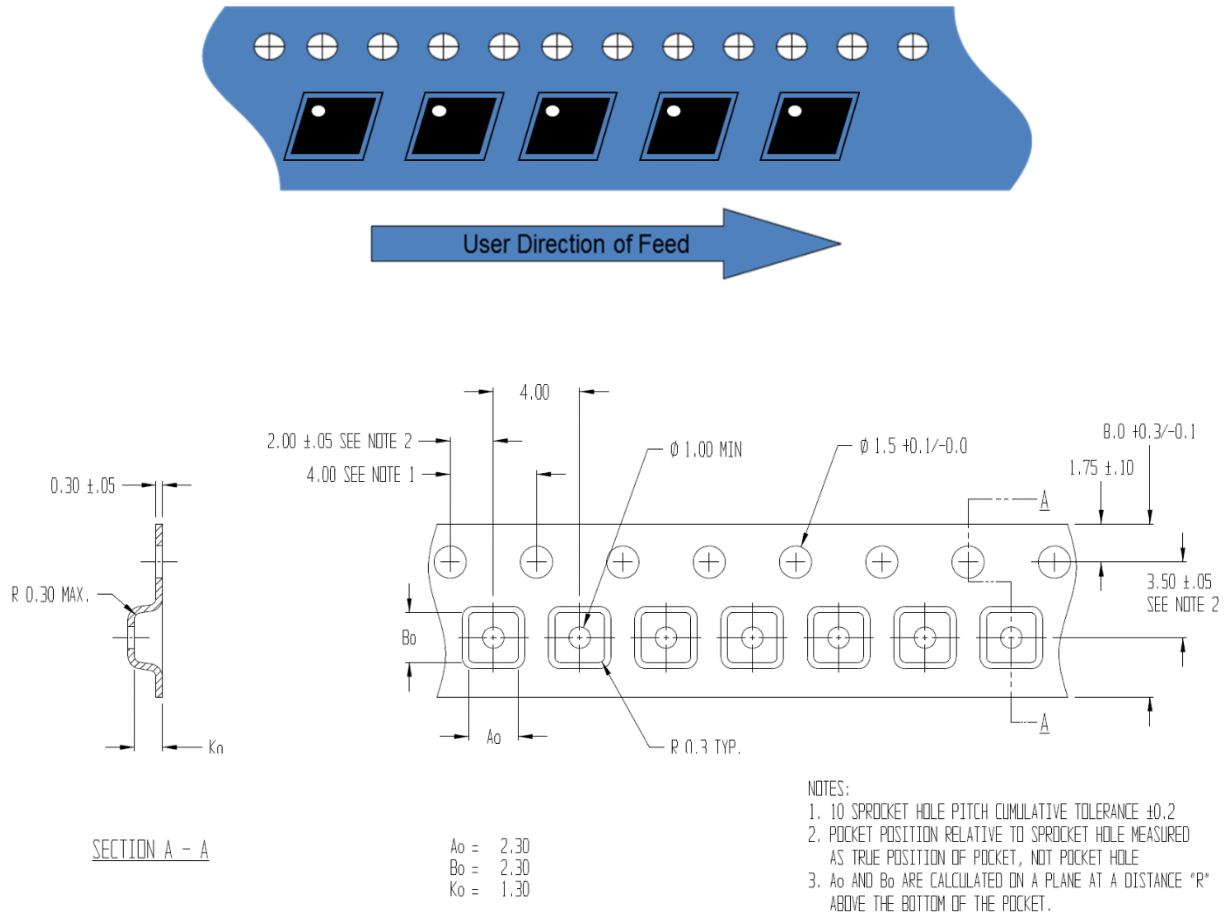
- Notes:
1. All dimensions are in millimeters. Angles are in degrees.
  2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
  3. Contact plating: NiPdAu

## Recommended PCB Layout Pattern



- Notes:
1. All dimensions are in millimeters. Angles are in degrees.
  2. Use 1 oz. copper minimum for top and bottom layer metal.
  3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01").
  4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

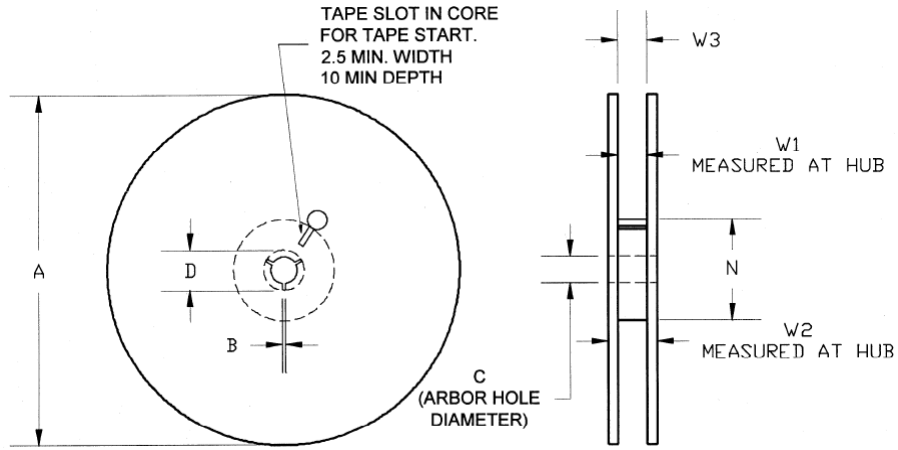
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.091	2.30
	Width	B0	0.091	2.30
	Depth	K0	0.051	1.30
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.138	3.50
Cover Tape	Width	C	0.213	5.40
Carrier Tape	Width	W	0.315	8.00

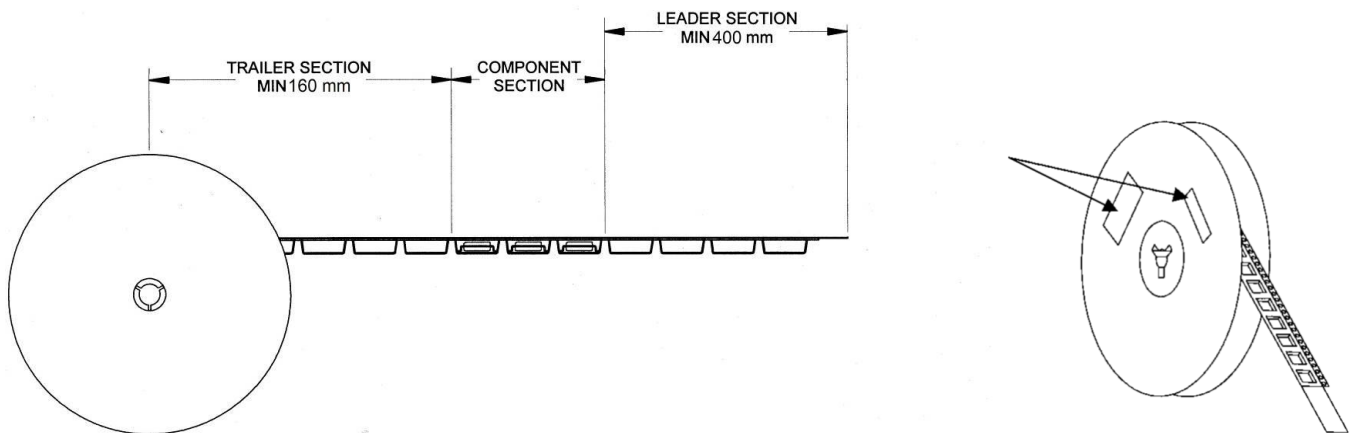
**Tape and Reel Information – Reel Dimensions**

Standard T/R size = 2,500 pieces on a 7" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.559	14.2
	Space Between Flange	W1	0.346	8.8
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

**Tape and Reel Information – Tape Length and Label Placement**



- Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
  2. Labels are placed on the flange opposite the sprockets in the carrier tape.

## Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020



Caution!  
 ESD-Sensitive Device

## Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes. Solder profiles available upon request.

Contact plating: NiPdAu

## RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free



## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Web:** [www.qorvo.com](http://www.qorvo.com)

**Tel:** 1-844-890-8163

**Email:** [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

For technical questions and application information

**Email:** [appsupport@qorvo.com](mailto:appsupport@qorvo.com)

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