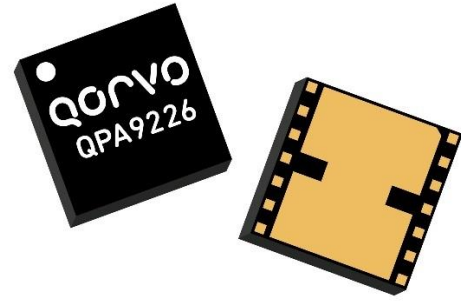


General Description

The QPA9226 is a high-linearity three-stage power amplifier in a low-cost surface-mount package with on-chip bias control and temperature control circuits, suitable for small cell or enterprise Femtocell base station applications.

The QPA9226 provides 34 dB high gain and -50 dBc ACLR at +24 dBm linear power using a 20 MHz LTE signal over the 2.5–2.7 GHz frequency range covering 3GPP Bands 7, 38, 41.

The QPA9226 integrates three high performance amplifier stages to allow for a compact system design and requires very few external components for operation. The amplifier is bias adjustable allowing the amplifier's power consumption to be optimized for specific performance requirements. The QPA9226 is available in a RoHS-compliant 7 x 7 mm surface mount package.

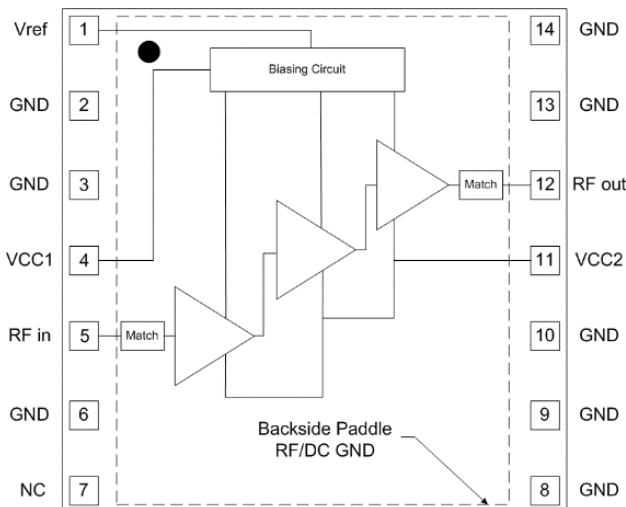


14 Pin 7 x 7 mm Leadless SMT Package

Product Features

- 2.5 – 2.7 GHz Frequency Range
- Fully integrated, 3-Stage Power Amplifier
- Internally Matched 50 Ω Input & Output
- -50 dBc ACLR at $P_{avg} = +24$ dBm
- 34 dB Gain
- 14% PAE at +24 dBm
- 198 mA Quiescent Current
- On-chip Control Bias and Temp. Comp Circuit
- RoHS compliant
- Covers Bands 7, 38, 41

Functional Block Diagram



Top View

Applications

- Small Cell / Picocell
- Enterprise Femtocell
- Customer Premises Equipment (CPE)
- Data Cards and Terminals
- Distributed Antenna Systems (DAS)
- Booster Amps, Repeaters

Ordering Information

Part No.	Description
QPA9226TR13	2,500 pieces on a 13" reel (standard)
QPA9226PCB401	QPA9226 Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to +150 °C
RF Input Power, CW, 50Ω, T=+25 °C	+9 dBm
Supply Voltage (V _{CC})	6 V
V _{REF}	+3.5 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V _{CC1} , V _{CC2}	+3.6	+4.5	+5.25	V
V _{ref}	+2.75	+2.85	+2.95	V
T _{CASE}	-40		+85	°C
T _j at T _{CASE} max			+218	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

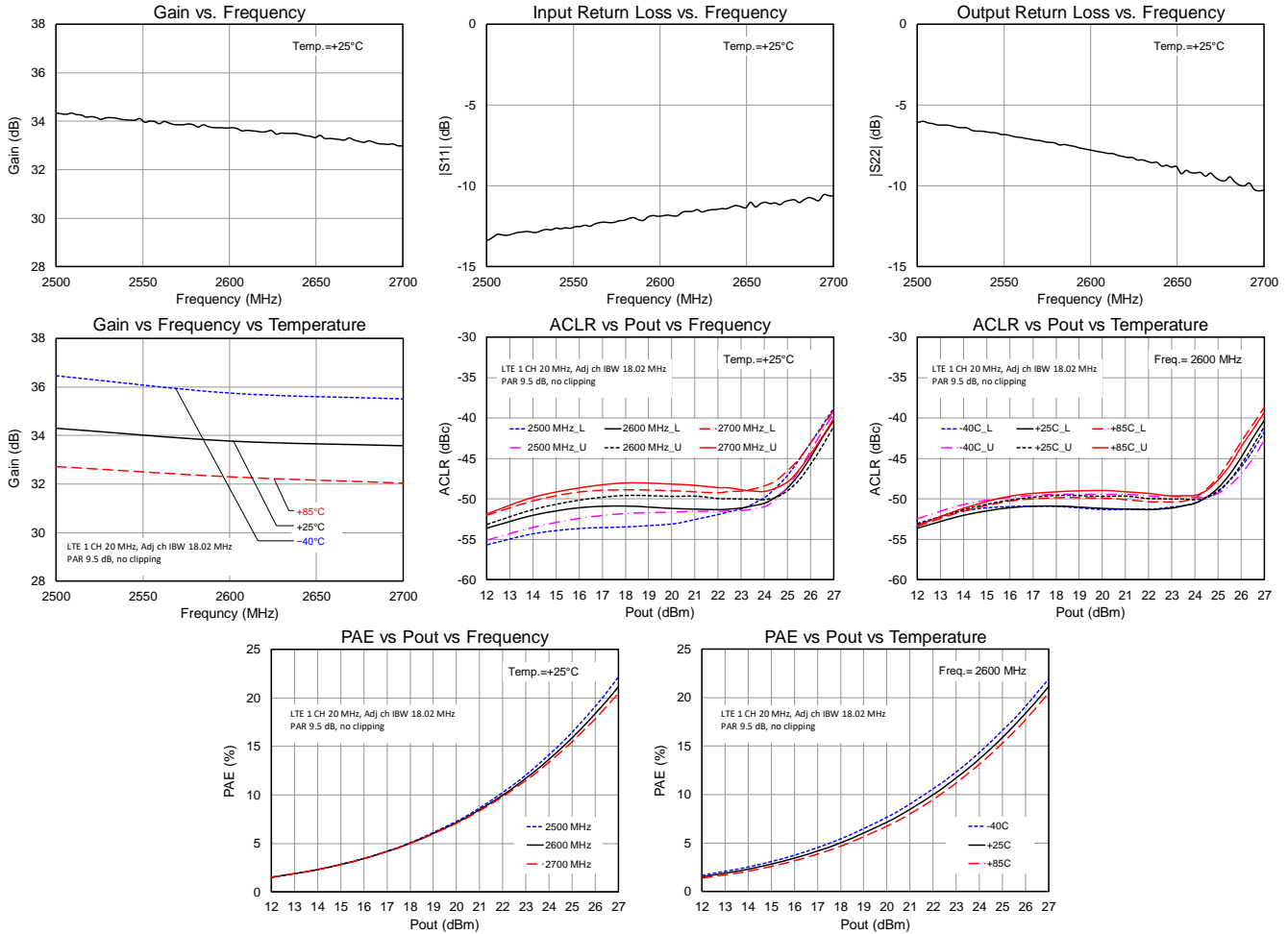
Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Units
Frequency Range		2500		2700	MHz
Test Frequency			2600		MHz
Gain		31	34		dB
Input Return Loss			12		dB
Output Return Loss			7.0		dB
Output P1dB			33.5		dBm
ACLR	P _{OUT} = +24 dBm, 20 MHz LTE E-TM1.1, 9.5 dB PAR		-50	-47	dBc
Power Added Efficiency	P _{OUT} = +24 dBm, 20 MHz LTE E-TM1.1, 9.5 dB PAR	12.5	14		%
Spurious Output Level	P _{OUT} = +24 dBm, 10:1 VSWR		58		dBc
VSWR survivability	No permanent degradation or failure	10:1			-
Quiescent Current, I _{CQ}	V _{CC1} + V _{CC2}	180	198	250	mA
Reference Current, I _{ref}	Temp = -40°C to +85°C, V _{REF} = +2.85V		6	8	mA
Leakage Current	V _{CC} = +4.5 V, V _{REF} = 0 V		1.5	5	μA
Operational Current, I _{CC}	P _{OUT} = +24 dBm		398	450	mA
Switching Time	0% V _{ref} to 90% RF Rise time		1.7	2.5	μs
	100% V _{ref} to 10% RF Fall time		0.87	1	μs
Harmonics	2F ₀ at +24dBm, CW signal		-32	-28	dBc
	3F ₀ at +24dBm, CW signal		-38	-33	dBc
	4F ₀ at +24dBm, CW signal		-66	-61	dBc
Thermal Resistance, θ _{Jc}	Module (junction to case)			34.8	°C/W

Notes:

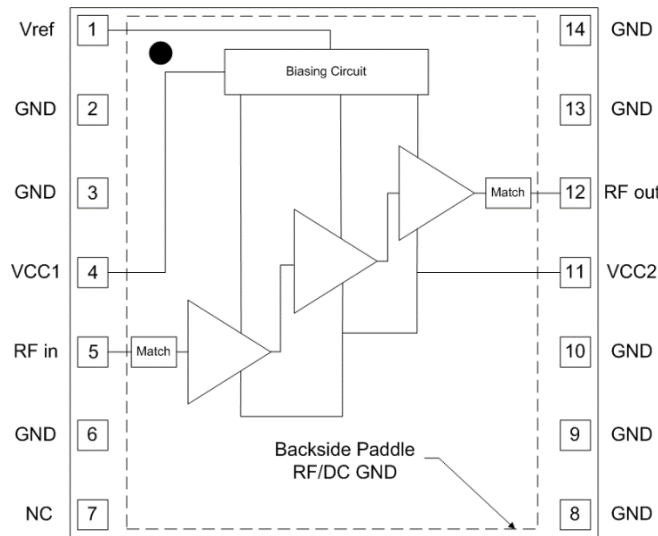
1. Test conditions unless otherwise noted: V_{CC1} = V_{CC2} = +4.5 V, V_{REF} = +2.85V, Temp = +25 °C, 50 Ω system.

Performance Plots

Test conditions unless otherwise noted: $V_{CC1} = V_{CC2} = +4.5V$, $V_{REF} = +2.85V$, $I_{CQ} = 198mA$, $Temp. = +25^{\circ}C$



Pin Configuration and Description

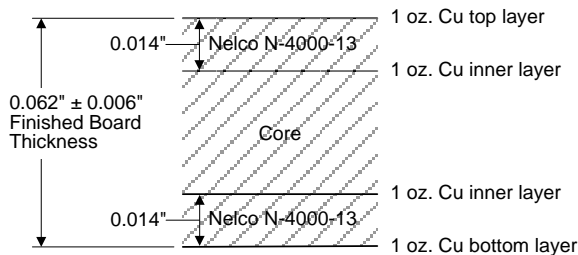


Top View

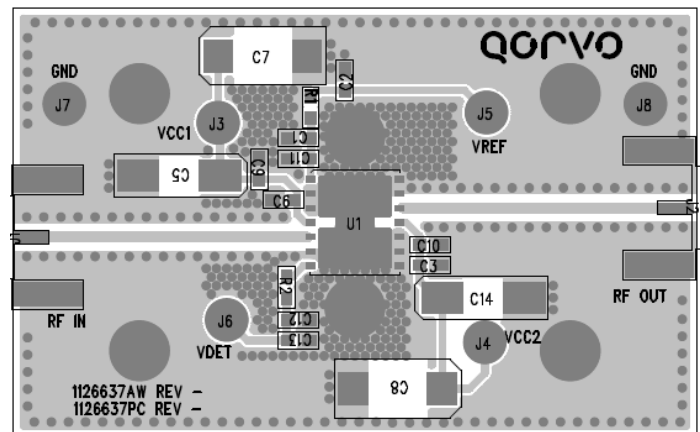
Pad No.	Label	Description
1	V _{REF}	Sets the bias current for the amplifiers. It can also be used to power down the device.
2, 3, 6, 8, 9, 10, 13, 14	GND	RF and DC ground.
4	VCC1	Voltage supply for the active bias circuitry.
5	RF in	RF input pin. The DC is internally blocked at this pin.
7	NC	No internal connection.
11	VCC2	DC voltage supply connection for AMP1, 2, 3.
12	RF out	RF output pin. The DC is internally blocked at this pin.
Backside Paddle	RF/DC GND	RF/DC ground. See PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

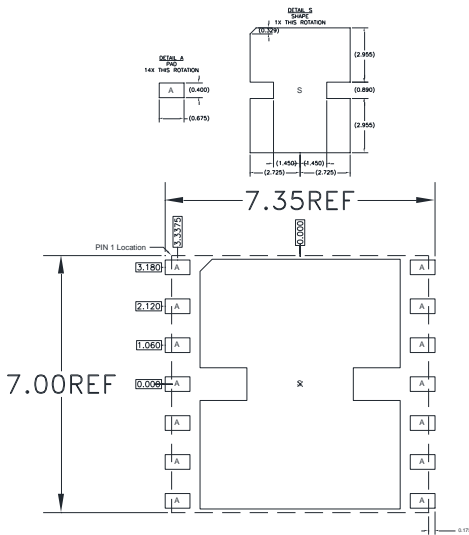
Qorvo PCB 1126637 Material and Stack-up



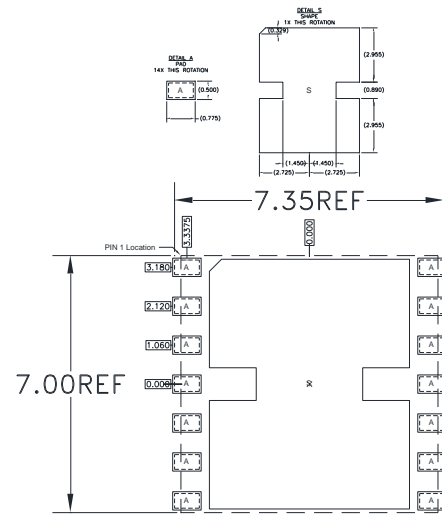
50 Ω line dimensions: width = .028"
spacing = .028".



PCB Mounting Pattern



RECOMMENDED
LAND PATTERN

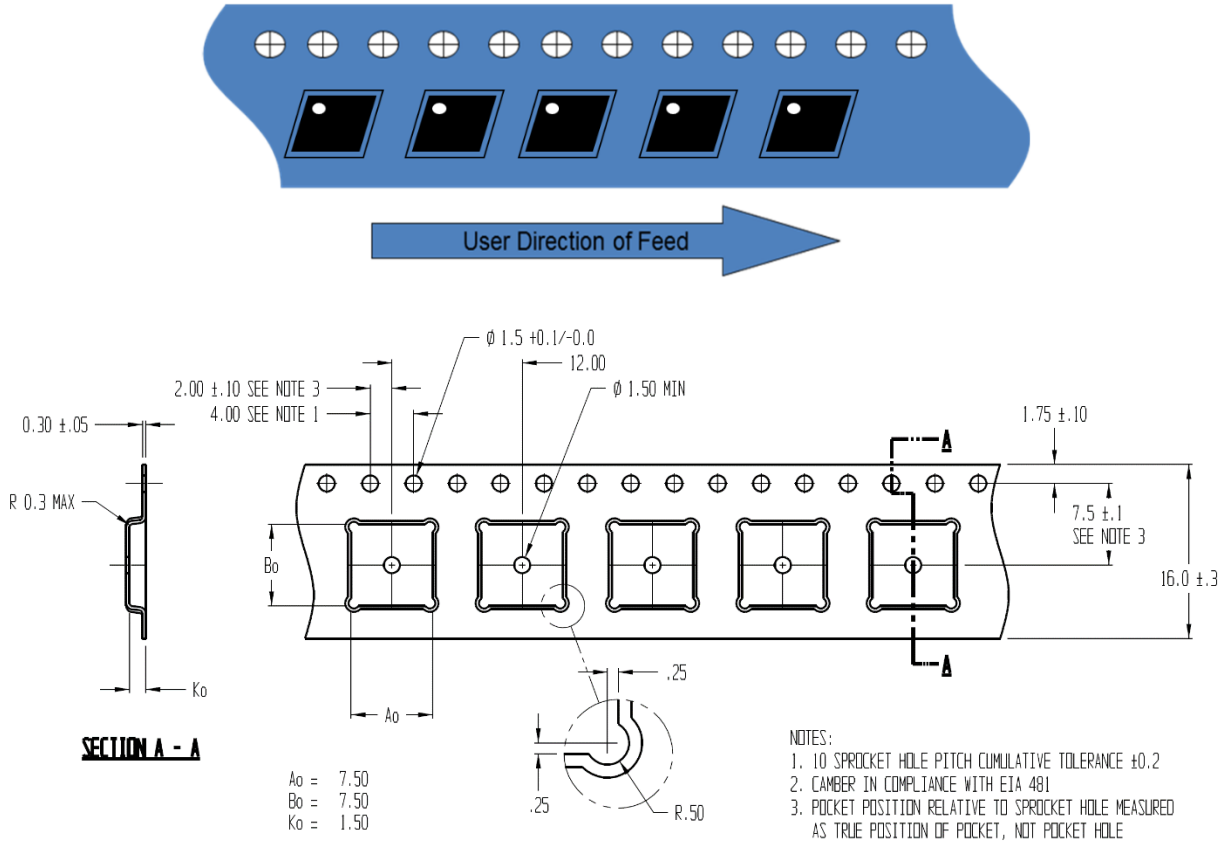


RECOMMENDED
LAND PATTERN MASK

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.010").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

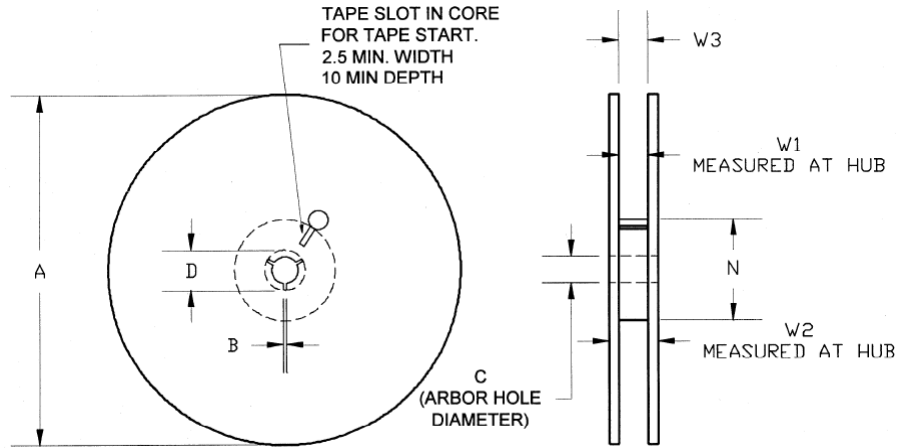
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.295	7.50
	Width	B0	0.295	7.50
	Depth	K0	0.059	1.50
	Pitch	P1	0.472	12.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.295	7.50
Cover Tape	Width	C	0.524	13.30
Carrier Tape	Width	W	0.630	16.0

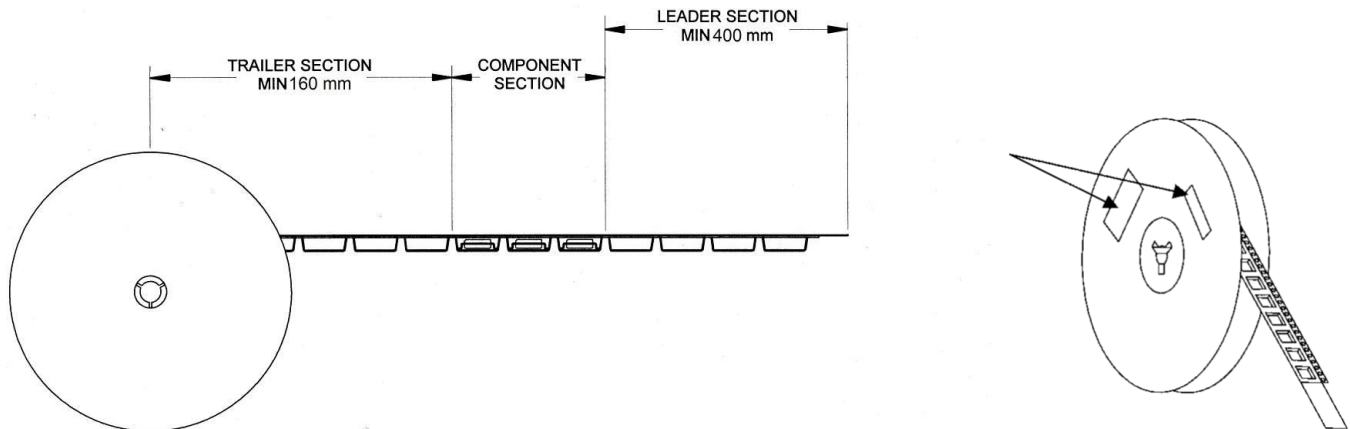
Tape and Reel Information – Reel Dimensions (13")

Standard T/R size = 2,500 pieces on a 13" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.874	22.2
	Space Between Flange	W1	0.661	16.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 2	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.

Solder profiles available upon request.

Contact plating: Electrolytic plated Au over Ni (*Ni 5.0±3.0 µm; Au 0.10 µm min.*)

RoHS Compliance

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: **1-844-890-8163**

Web: www.qorvo.com

Email: customer.support@qorvo.com

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