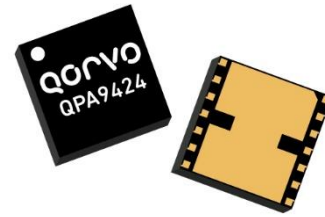


Product Overview

The QPA9424 is a high-linearity three-stage power amplifier in a low-cost surface-mount package with on-chip bias control and temperature control circuits, suitable for small cell base station applications.

The QPA9424 provides 35.8 dB gain and +27 dBm linear power over the 2300 – 2400 MHz frequency range covering band 30 and band 40. This amplifier is able to achieve -48.5 dBc ACLR at +27 dBm output power with 20 MHz LTE signal.

The QPA9424 integrates three high performance amplifier stages onto a module to allow for a compact system design and requires very few external components for operation. The amplifier is bias adjustable allowing the amplifier's power consumption to be optimized. The QPA9424 is available in a 7 x 7 mm surface mount package.

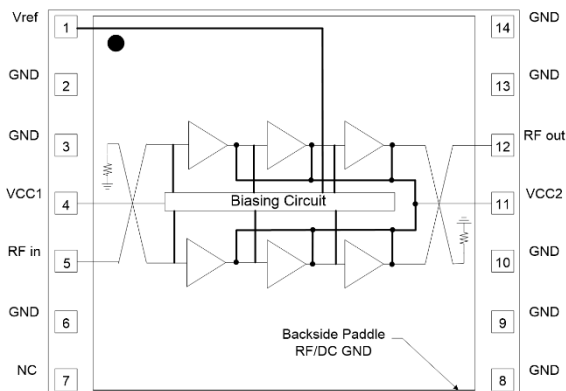


7 mm x 7 mm Leadless SMT Package

Key Features

- 2.300 – 2.400 GHz Frequency Range
- Fully integrated, 3 Stage Power Amplifier
- Internally Matched 50 Ω Input/Output
- -48.5 dBc ACLR at Pavg = +27 dBm
- 35.8 dB Gain
- 14.6% PAE at +27 dBm
- 455 mA Quiescent Current
- On-chip Control Bias and Temp. Comp Circuit

Functional Block Diagram



Top View

Applications

- Small Cell / Picocell
- Band 30 & Band 40
- Enterprise Femtocell
- Customer Premises Equipment (CPE)
- Data Cards and Terminals
- Distributed Antenna Systems (DAS)
- Booster Amps, Repeaters

Ordering Information

Part No.	Description
QPA9424TR13	2500 pieces on a 13" reel
QPA9424EVB-01	2300 – 2400 MHz Evaluation board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to +150 °C
Supply Voltage (V _{CC})	+6 V
V _{ref}	+3.5 V
RF Input Power, CW, 50Ω, T=25°C	+13 dBm
T _j at T _{CASE} = 125°C	+196°C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V _{CC1} , V _{CC2}	+3.6	+4.5	+5.25	V
V _{ref}	+2.75	+2.85	+2.95	V
T _{CASE}	-40		+85	°C
T _j at T _{CASE} max			+156	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

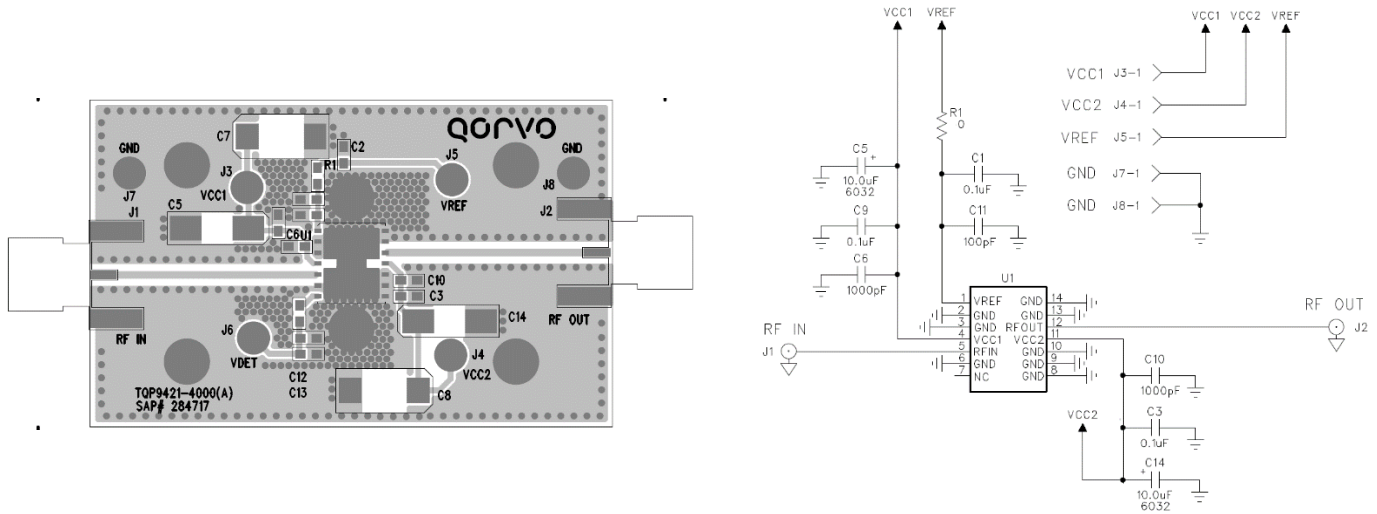
Test conditions unless otherwise noted: V_{CC1} = V_{CC2} = +4.5 V, V_{ref} = +2.85 V, Temp = +25 °C

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		2300		2400	MHz
Test Frequency			2350		MHz
Gain	P _{OUT} +27 dBm, CW	32	35.8	38	dB
Input Return Loss ⁽³⁾	CW, small signal	15	20		dB
Output Return Loss ⁽³⁾		15	21.5		dB
P1dB	CW		35.4		dBm
ACLR	P _{OUT} +27 dBm, 20 MHz LTE E-TM1.1, 9.5 dB PAR		-48.5	-45	dBc
	P _{OUT} +27 dBm, 20x2 MHz LTE E-TM1.1, 9.5 dB PAR		-44.8		dBc
Power Added Efficiency	P _{OUT} +27 dBm, 20 MHz LTE E-TM1.1, 9.5 dB PAR	13	14.6		%
Quiescent Current, I _{CQ} ⁽¹⁾	V _{CC1} + V _{CC2}	330	455	520	mA
Leakage Current on V _{CC}	V _{CC} +4.5V, V _{ref} 0V		1.3	10	μA
Reference Current, I _{ref} ⁽³⁾	Temp -40°C to +85°C, V _{ref} = +2.85V		15	19.5	mA
Operational Current, I _{CC}	P _{OUT} +27 dBm, 20 MHz LTE E-TM1.1, 9.5 dB PAR		763	870	mA
Wake Up Time ⁽²⁾	50% of control signal to 90% of the RF output		1290		ns
Power Down Time ⁽²⁾	50% of control signal to 10% of the RF output		670		ns
Spurious Output Level	P _{OUT} ≤ +27dBm, In & Out of band load VSWR ≤ 10:1		-60		dBc
VSWR survivability	No permanent degradation or failure		≥10:1		-
Harmonics ⁽³⁾	2F ₀ (P _{OUT} +27 dBm), CW signal		-45	-35	dBc
	3F ₀ (P _{OUT} +27 dBm), CW signal		-56	-43	dBc
	4F ₀ (P _{OUT} +27 dBm), CW signal		-65		dBc
Thermal Resistance, θ _{jc}	Module (junction to case)		17.4		°C/W

Notes:

- V_{CC1} draws very little current and provides the bias voltage to the current mirror circuit along with V_{ref} to set the bias point for the whole amplifier.
- Control signal applied to V_{ref} Pin, 0 to 2.85V
- Guaranteed by design, not tested in production

QPA9424 Application Circuit Schematic and Layout



Bill of Material - QPA9424EVB01

Ref Designation	Value	Description	Manufacture	Part Number
-	-	Printed Circuit Board	Qorvo	
U1	-	Amplifier, High Linearity 0.5 W Power	Qorvo	QPA9424
R1	0 Ω	Resistor, Chip, 0603, 5%	various	
C1	0.01 µF	Capacitor, Chip, 0603, 5%	various	
C11	100 pF	Capacitor, Chip, 0603, 5%	various	
C3, C9	0.1 µF	Capacitor, Chip, 0603, 5%	various	
C5, C14	10 µF	Capacitor, Chip, 6032, 10%, Tantalum	various	
C6, C10	1000 pF	Capacitor, Chip, 0603, 5%, NPO/C0G	various	

QPA9424EVB01 Typical Performances

Test conditions unless otherwise noted: $V_{CC1} = V_{CC2} = +4.5V$, $V_{ref} = +2.85V$, $P_{out} 27dBm$, 2350MHz, Signal PAR 9.5dB, Temp= +25 °C

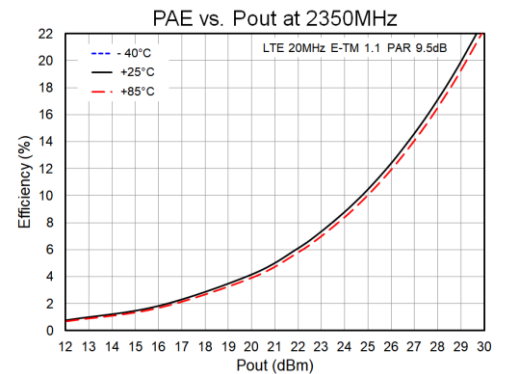
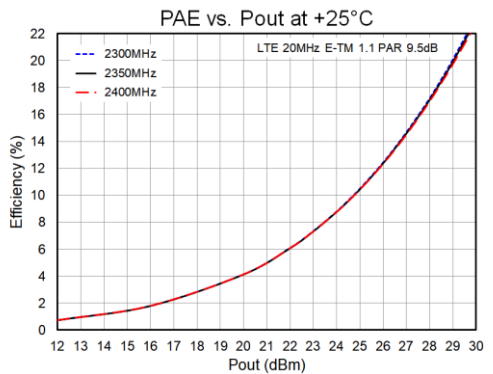
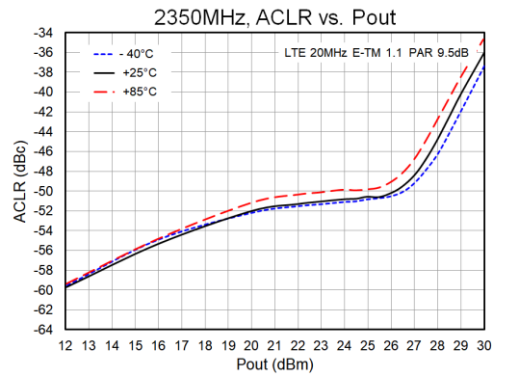
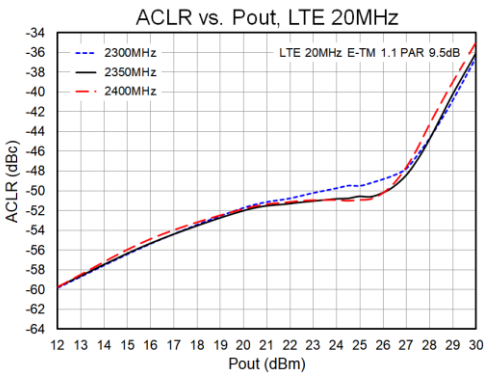
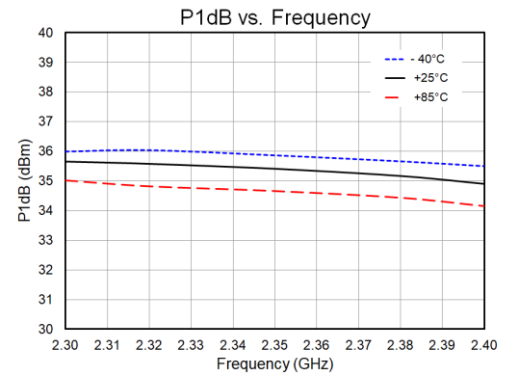
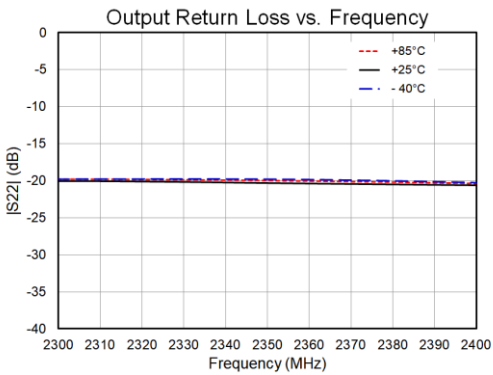
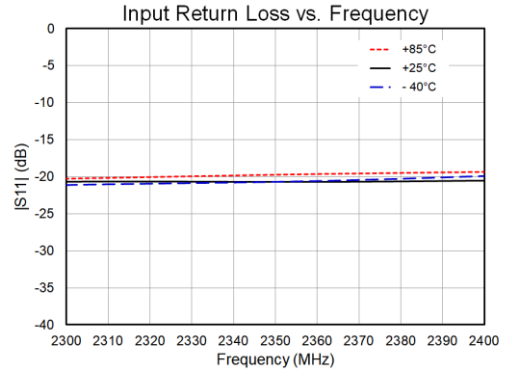
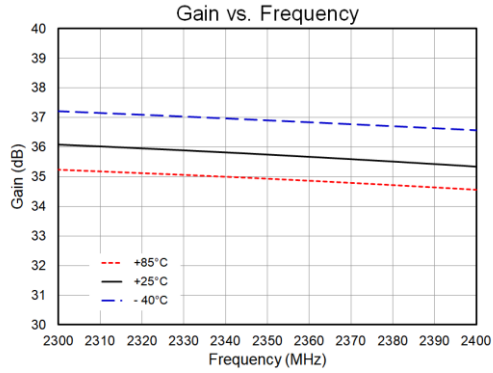
LTE Signal BW	20MHz	20MHz x 2	Units
ACLR1-Low	- 48.4	- 44.8	dBc
ACLR1-high	- 49.8	- 45.0	dBc

Parameter	Conditions	-40°C	+25°C	+85°C	Units
Gain		37.2	35.8	34.1	dB
ACLR	$P_{OUT} = +27 dBm$, 20 MHz LTE E-TM1.1, 9.5dB PAR	-49.2	-48.4	-46.8	dBc
PAE		15.2	14.6	14.0	%
P1dB	CW	+35.8	+35.4	+34.7	dBm

Test Frequency = 2350MHz

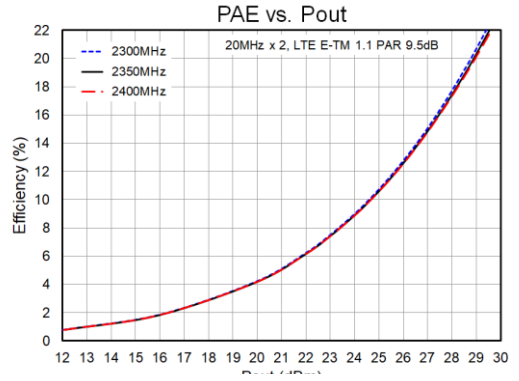
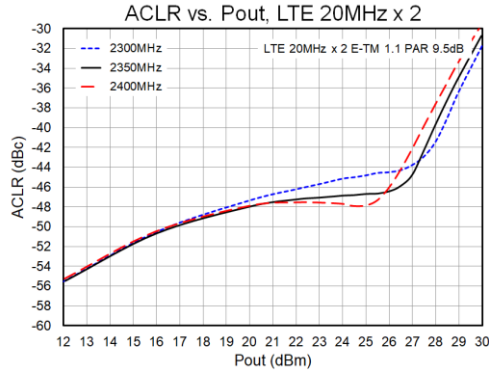
Performance Plots

Test conditions unless otherwise noted: $V_{CC1} = V_{CC2} = +4.5V$, $V_{ref} = +2.85V$, LTE signal PAR = 9.5dB, Temp. = +25 °C

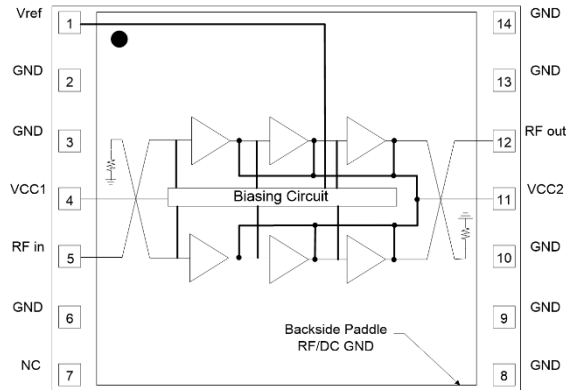


Performance Plots (continued)

Test conditions unless otherwise noted: $V_{CC1} = V_{CC2} = +4.5V$, $V_{ref} = +2.85V$, LTE signal PAR = 9.5dB, Temp. = +25 °C



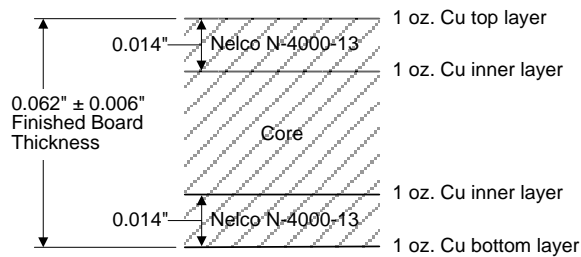
Pin Configuration and Description



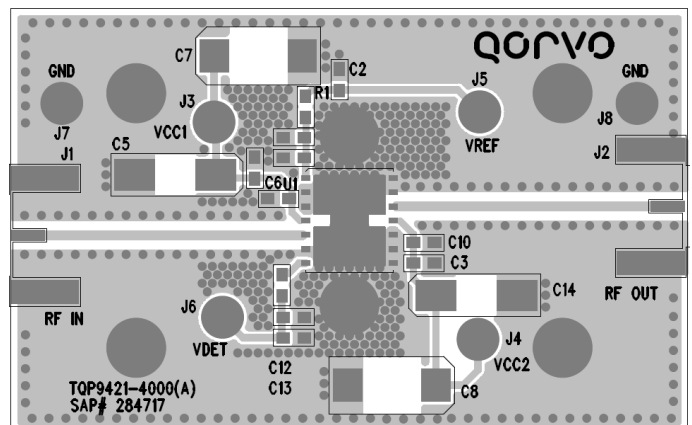
Pin No.	Label	Description
1	Vref	Provides reference voltage for internal active biasing circuit
2, 3, 6, 8, 9, 10, 13, 14	GND	RF and DC ground.
4	VCC1	Bias voltage for current mirror in combination with Vref to set the bias point.
5	RFin	RF input pin. The DC is internally blocked at this pin.
7	NC	No internal connection. Can be left open or grounded for mounting integrity.
11	VCC2	Supply to all stages.
12	RFout	RF output pin. The DC is internally blocked at this pin.
Backside Paddle	RF/DC GND	RF/DC ground. See PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

Qorvo PCB 284717 Material and Stack-up



50 Ω line dimensions: width = .028"
spacing = .028".

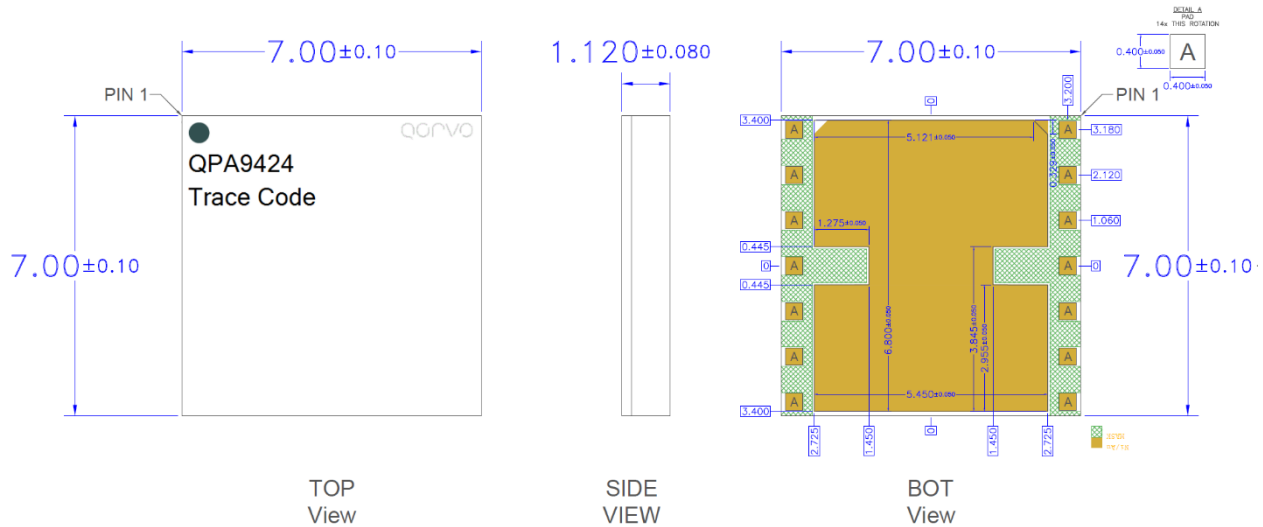


Mechanical Information

Package Marking and Dimensions

Marking: Part number – QPA9424

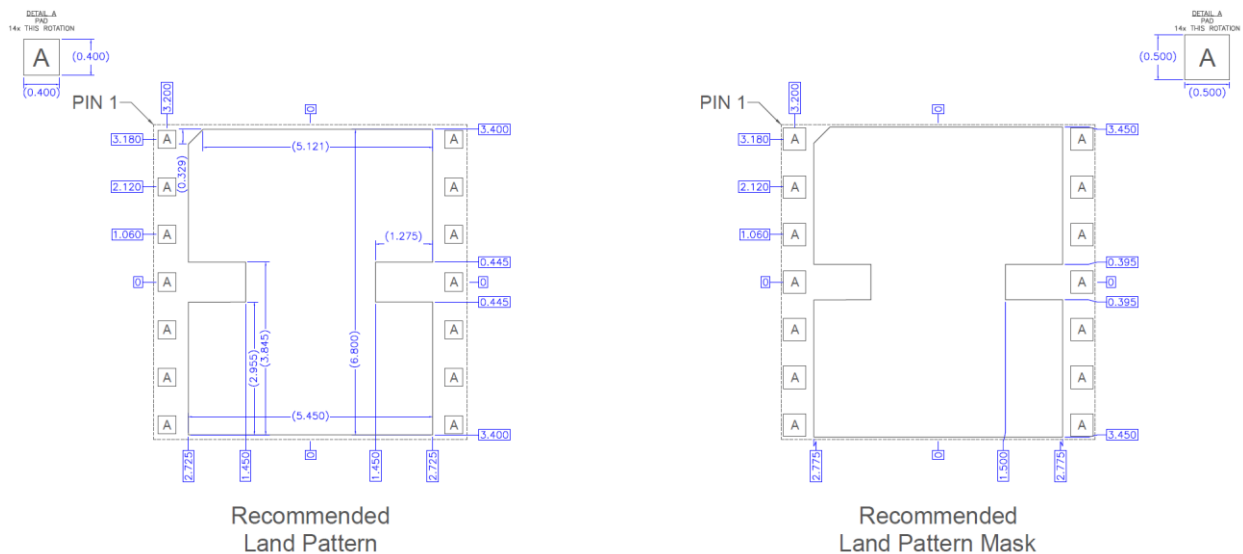
Trace code – Assigned by sub-contractor



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

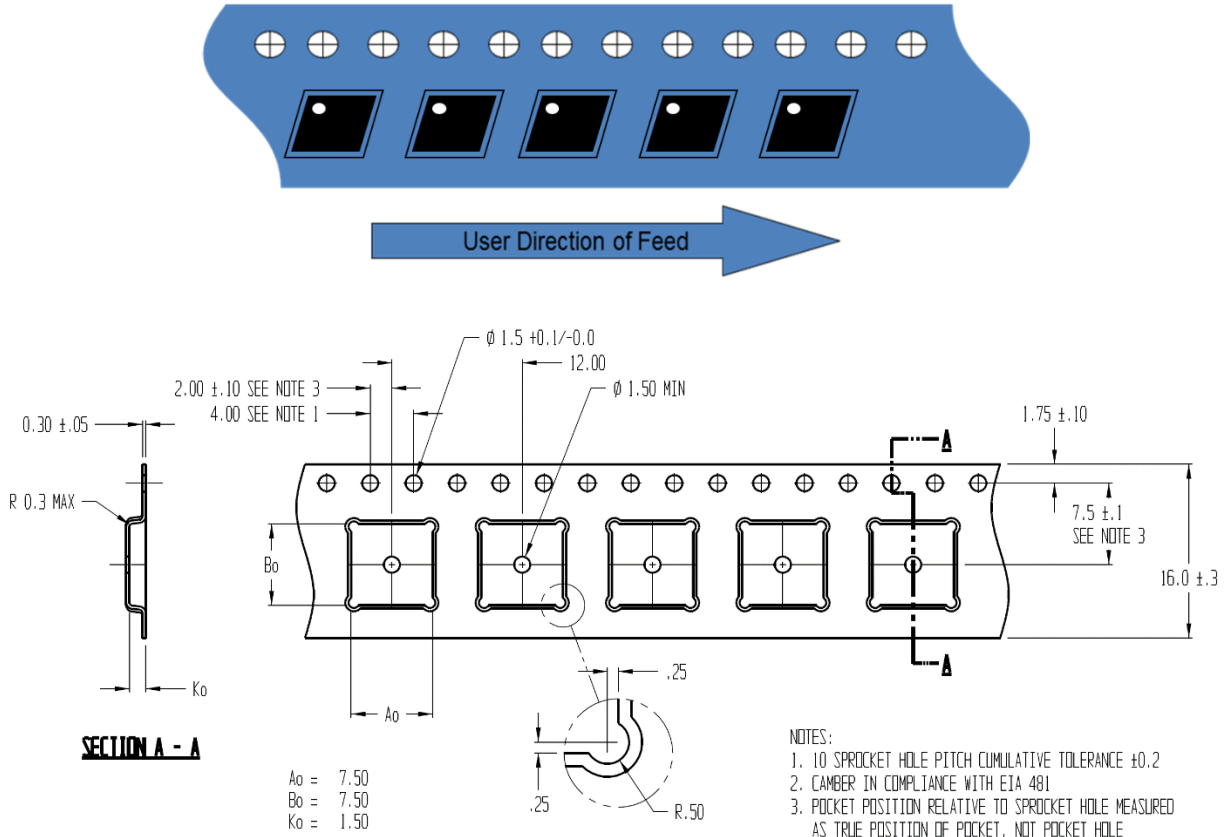
PCB Mounting Pattern



Notes:

1. A heat sink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal via holes are critical for the proper performance of this device. Via holes should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

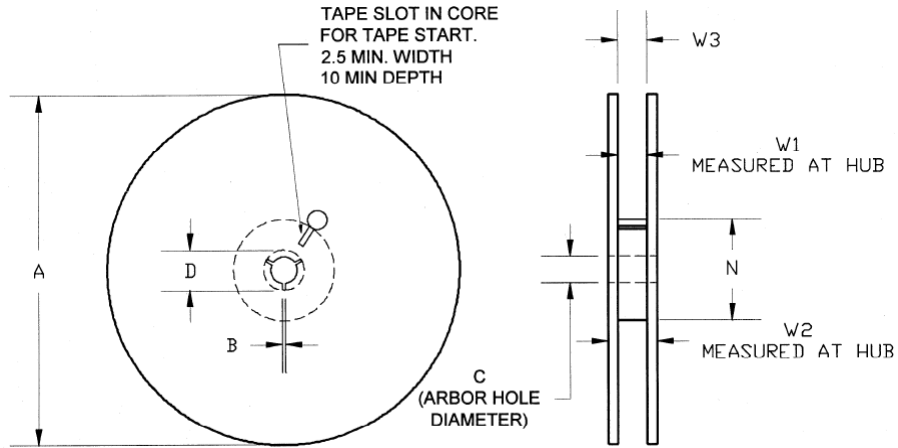
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.295	7.50
	Width	B0	0.295	7.50
	Depth	K0	0.059	1.50
	Pitch	P1	0.472	12.0
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.295	7.50
Cover Tape	Width	C	0.524	13.3
Carrier Tape	Width	W	0.630	16.0

Tape and Reel Information – Reel Dimensions (13")

Standard T/R size = 2,500 pieces on a 13" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.874	22.2
	Space Between Flange	W1	0.661	16.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



- Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
 2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
 ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: Electrolytic plated Au over Ni (*Plating thickness: Ni 5.0±30µm, Au 0.10µm minimum*)

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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