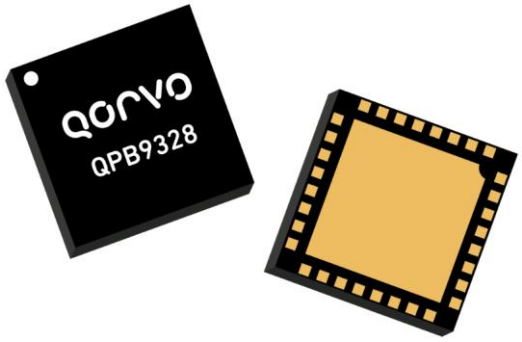
QPB9328

Dual-Channel Switch LNA Module



32 Pad 6 mm x 6 mm leadless SMT Package

Product Overview

The QPB9328 is a highly integrated front-end module targeted for TDD base stations. The LNA switch module integrates a two-stage LNA and a high-power switch in a dual channel configuration. Power down capability for the LNAs can be controlled with shut-down pins for the module.

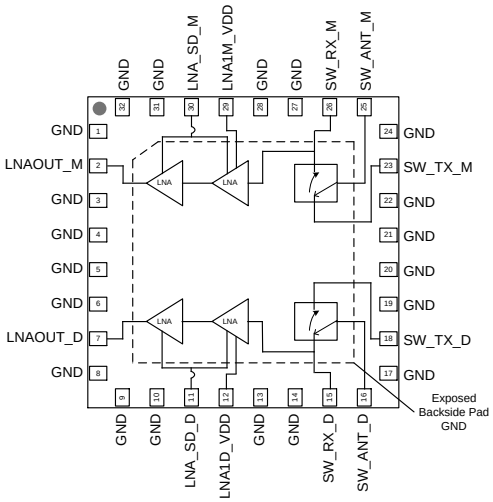
The QPB9328 can be utilized across the 4.4 – 5.0 GHz range to provide 1.8 dB noise figure for operation in the receive mode and 0.65 dB insertion loss in the transmit mode. The LNAs utilize Qorvo's high performance E-pHEMT process while the pin-diode based switch supports input RF power signals of up to 10W average power assuming 8 dB PAR.

The QPB9328 is packaged in a RoHS-compliant, compact 6 mm x 6 mm surface-mount leadless package. The switch LNA module is targeted for wireless infrastructure applications configured for TDD-based MIMO architectures. The module can be used for next generation 5G or pre-5G solutions or small cell base station applications.

Key Features

- 4.4-5.0 GHz Frequency Range
- Integrates dual channels of a two-stage LNA with high power switches
- Max RF Input power: 10W Pavg (8 dB PAR)
- 1.8 dB Noise Figure (Rx mode)
- 32 dB Gain (Rx mode)
- +34 dBm OIP3 (Rx mode)
- 0.65 dB Insertion Loss (Tx mode)
- Compact package size, 6x6 mm

Functional Block Diagram



Top View

Applications

- Wireless Infrastructure
- Small cell BTS
- Pre-5G / 5G Massive MIMO systems
- TDD-based architectures

Ordering Information

Part No.	Description
QPB9328SR	100 pcs on a 7" reel
QPB9328TR13	2500 pcs on a 13" reel
QPB9328EVB-01	Evaluation board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
LNA Supply Voltage (Pins 2, 7, 9, 11, 30, 32)	+7 V
LNA Input Power (Pavg, 8 dB PAR)	+24 dBm
Switch Input Power (Pavg, 8 dB PAR)	+40 dBm
Switch Input Power (Peak)	+48 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
LNA Voltage	+3	+5	+5.25	V
V_{MODE}		+28		V
T_{CASE}	−40		+105	°C
$T_{JUNCTION}$, (RX mode) >10^6 hours MTTF			+190	°C

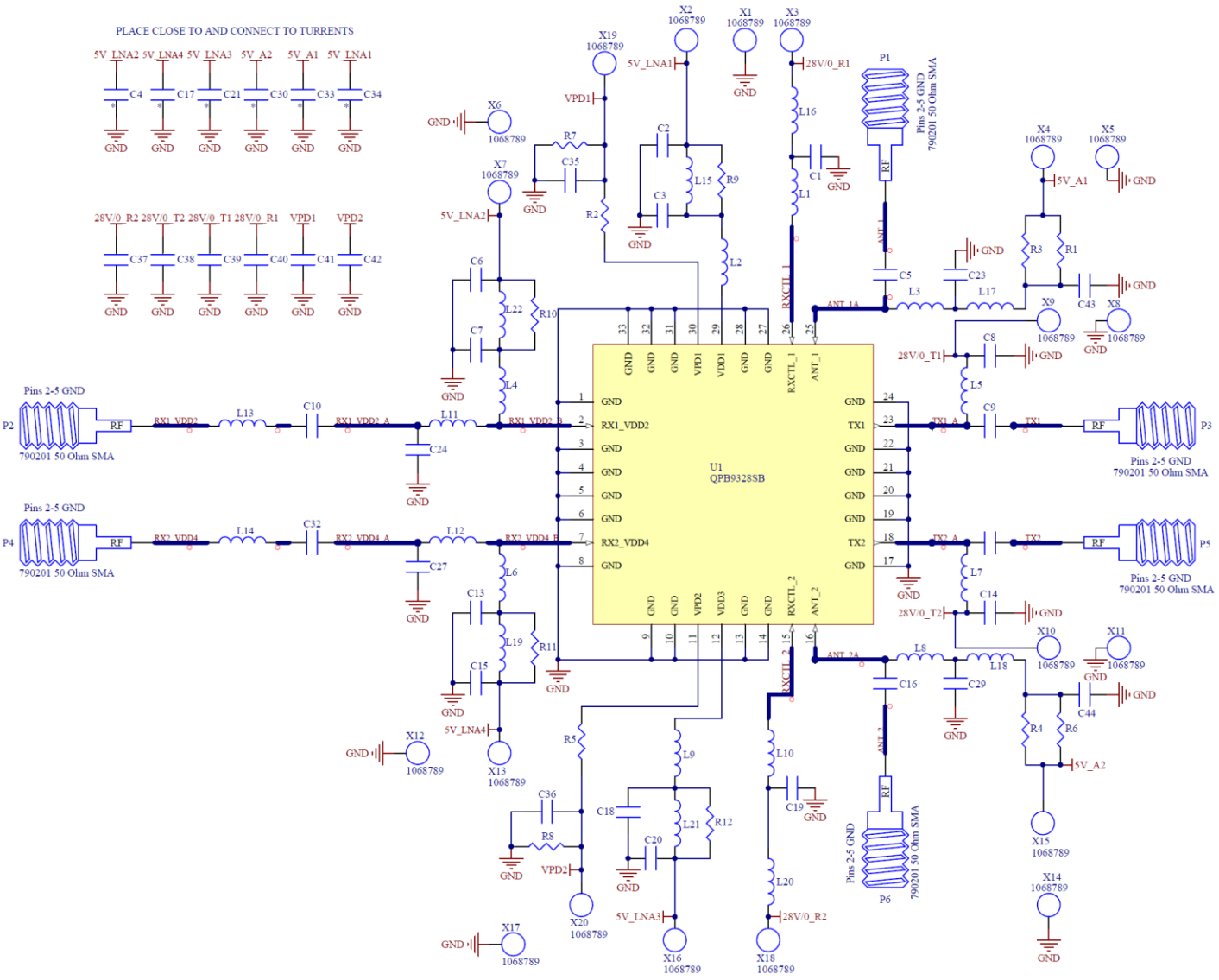
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions (1)	Min	Typ	Max	Units
Operational Frequency Range		4400		5000	MHz
Test Frequency			4700		MHz
Gain	Rx mode	30	32	36	dB
Gain Flatness	Rx mode, Any 200 MHz BW within band		0.6		dB
Noise Figure	Rx mode, De-embedded		1.8	2.1	dB
Output IP3	Rx mode, Pout/tone = +5dBm, Δf = 1MHz	32.0	34.6		dBm
OP1dB	Rx mode		19		dBm
Insertion Loss	Tx mode, De-embedded		0.65	1.0	dB
Input Return Loss	Rx mode, with external matching		13		dB
Output Return Loss	Rx mode, with external matching		17.5		dB
Channel Isolation	Rx mode, cross channel response		40		dB
Switch Isolation (2)	Tx mode		10		dB
LNA1, LNA2 Supply Voltage			5		V
LNA1, LNA2 Supply Current	Per channel	100	139	170	mA
LNA Shutdown Current	Per channel		3		mA
LNA Shutdown Control Voltage (Pin 11 and 30)	On state	0		+0.5	V
	Off state (Power down)	+1.4	+3.3	V_{DD}	V
Switch Voltage (Pin 15, 18, 26 and 26)	with +5V and 250 Ω resistor on SW_Ant Port	0		+28	V
Switch Current	Off path, per channel, +28V to SW_Tx/Rx port		1.7	5	mA
	Through path, per channel, +5V to Ant port	27	30.7	33	mA
Switch switching time	50% CTL to 10% or 90% of RF Output		490		nS
Thermal Resistance, Module	Rx mode			20.6	°C/W
	Tx mode, Pin on ANT ports			16.4	°C/W

Notes:
1. Test conditions unless otherwise noted: Temp = +25 °C, 50 Ω system, on Qorvo Evaluation Board
2. Switch Isolation is the insertion loss of the switch in the receive path while in Tx mode.
3. For proper voltage setting in each mode refer to notes on page 3, 5, 6 or 7 of application circuit and typical performance tables.

Application Circuit Schematic

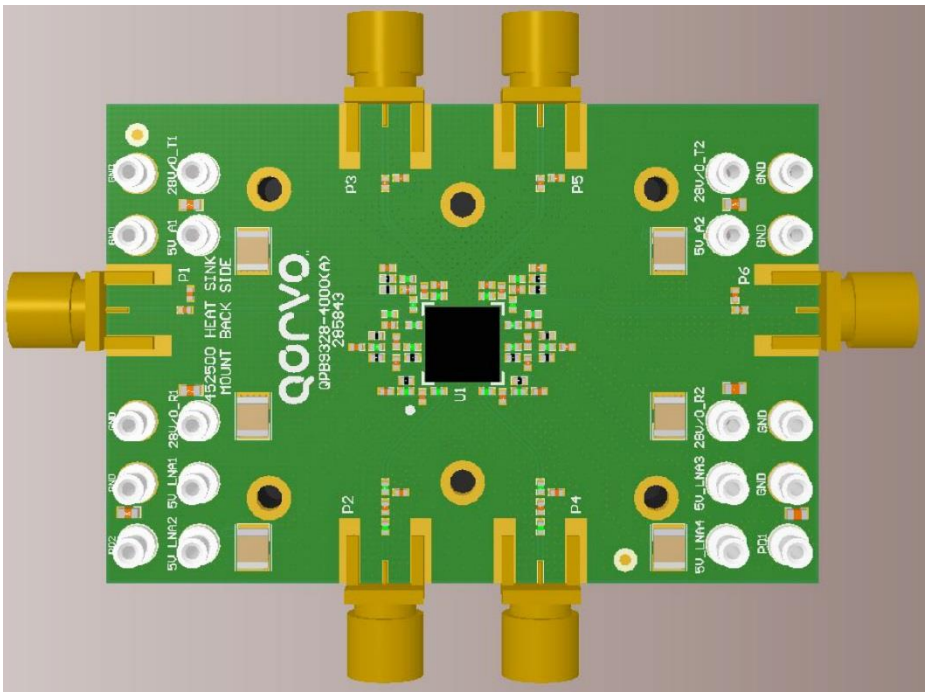


Notes:

For CH1 operation X4 (5V A1) always on +5Vdc and X7 (5V LNA2), X2 (5V LNA1) powered up to +5Vdc.
For CH2 operation X15 (5V A2) always on +5Vdc and X13 (5V LNA4), X16 (5V LNA3) powered up to +5Vdc.

- For CH1 RX operation (similar sequence for CH2):
  1. Set X9 (28V/0 T1) V_{MODE} to high (+28Vdc).
  2. Set X3 (28V/0 R1) V_{MODE} to low (0Vdc).
  3. Enable LNA's X19 (PD1) to 0Vdc.
- For CH1 TX operation (similar sequence for CH2):
  1. Disable LNA's X19 (PD1) to +5Vdc.
  2. Set X3 (28V/0 R1) V_{MODE} to high (+28Vdc).
  3. Set X9 (28V/0 T1) V_{MODE} to low (0Vdc).
- R2, R5, R7 & R8 need to be placed to improve the stability in the first stage LNA. It is recommended that they be placed as close to the pin as possible.

Application Circuit Layout



Bill of Material

Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board		
U1	n/a	Dual Channel Switch LNA Module	Qorvo	QPB9328
C23, C29	33 pF	CAP, 5%, 50V, C0G, 0402	muRata	GRM1555C1H330JA01D
C1, C5, C8, C9, C12, C14, C16, C19, C35, C36, L11, L12	33 pF	CAP, 5%, 100V, C0G, 0402	muRata	GRM1555C2A330JA01D
C2, C6, C15, C20	1 uF	CAP, 20%, 6.3V, X5R, 0402	various	
C3, C7, C13, C18, C43, C44	100 pF	CAP, 5%, 50V, C0G, 0402	muRata	GRM1555C1H101JA01D
C24, C27	3.6 nH	IND, 5%, M/L, 0402	muRata	LQG15HS5N3S02D
C10, C32	1.0 nH	IND, +/- 0.3nH, M/L, 0402	muRata	LQG15HN1N0S02D
C37, C38, C39, C40, C41, C42	100 pF	CAP, 5%, 50V, C0G, 0603	muRata	GRM1885C1H101JA01D
C4, C17, C21, C30, C33, C34	2.2 uF	CAP, 10%, 100V, X7R, 1210	various	
L13, L14	22 pF	CAP, 5%, 50V, C0G, 0402	muRata	GRM1555C1H220JA01D
L16, L20	0 Ω	RES, 0402, jumper	various	
L1, L2, L3, L5, L7, L8, L9, L10, L15, L17, L18, L21	5.1 nH	IND, +/- 0.3nH, 300mA, M/L, 0402	muRata	LQG15HN5N1S02D
L19, L22	18 nH	IND, 5%, M/L, 0402	muRata	LQG15HN18NJ02D
L4, L6	7.5 nH	IND, 5%, M/L, 0402	muRata	LQG15HN7N5J02D
R9, R10, R11, R12	470 Ω	RES, 5%, 1/16W, 0402	various	
R1, R3, R4, R6	249 Ω	RES, 1%, 1/16W, 0402	various	
R2, R5	1K Ω	RES, 1%, 1/16W, 0402	various	
R7, R8	20 K	RES, 1%, 1/16W, 0402	various	

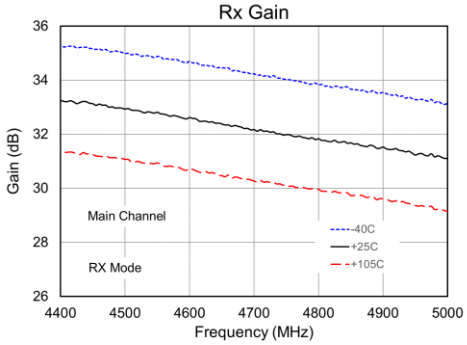
Typical Application Circuit Performance – Rx Mode

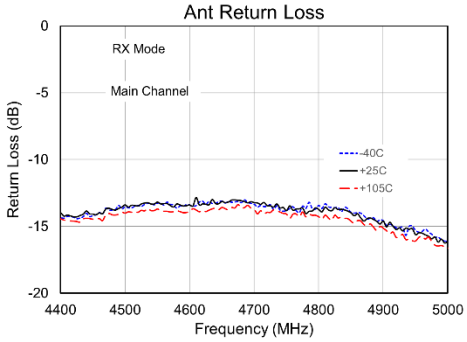
Parameter	Conditions (1)	Typical Value			Units
Frequency		4400	4700	5000	MHz
Gain		33.2	32.0	31.2	dB
Input Return Loss	ANT port, main channel	14.5	13.1	16.0	dB
Output Return Loss	RX port, main channel	15.0	17.5	16.2	dB
Output P1dB		+18.9	+19.0	+20.2	dBm
OIP3	Pout= +3 dBm/tone, Δf=1 MHz	+33.9	+34.4	+35.4	dBm
Noise Figure (2)	De-embedded	1.8	1.8	2.0	dB

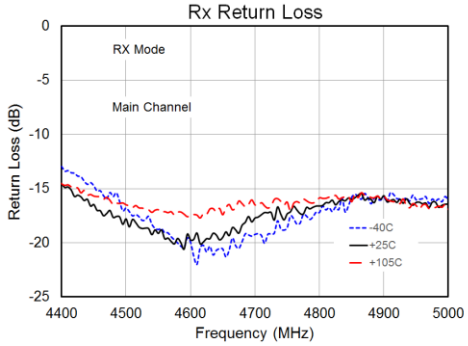
Notes:
1. Test conditions unless otherwise noted: LNA1, 2, 3, 4, A1, A2 = +5V; 28V/0 T1, 2 = +28V; 28V/0 R1, 2, PD1, 2 = 0V; Temp. = +25 °C

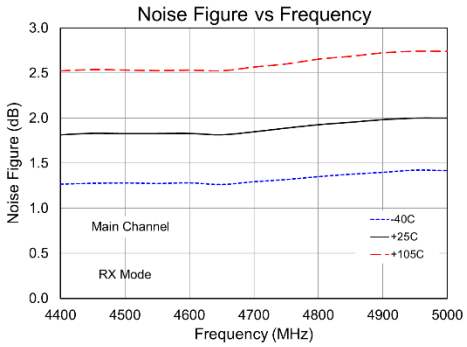
Application Circuit Performance Plots – Rx Mode (Main Channel)

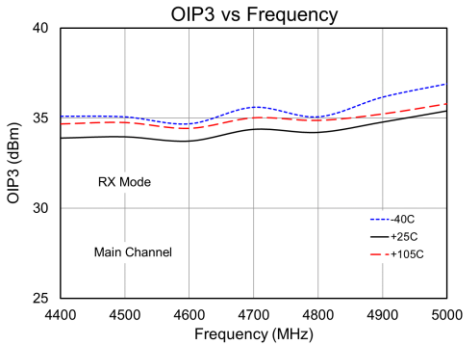
Test conditions unless otherwise noted: LNA1, 2, 3, 4, A1, A2 = +5V; 28V/0 T1, 2 = +28V; 28V/0 R1, 2, PD1, 2 = 0V; Temp.= +25 °C

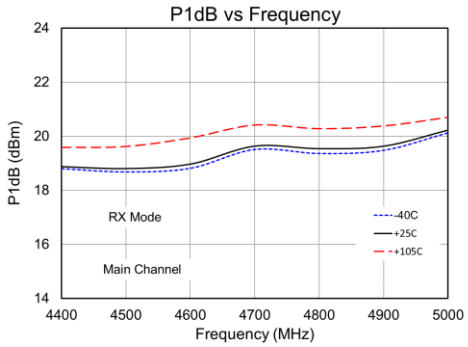


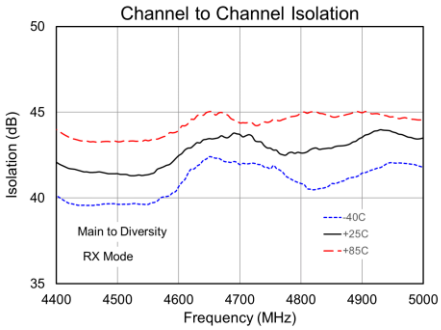






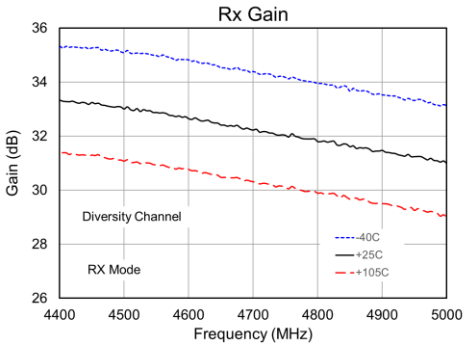


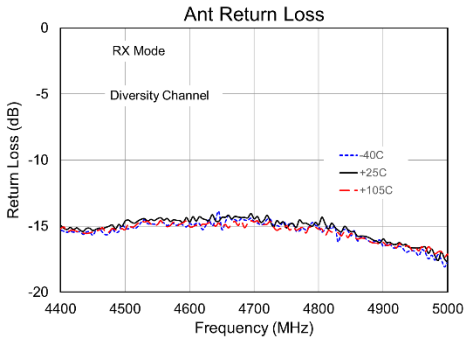


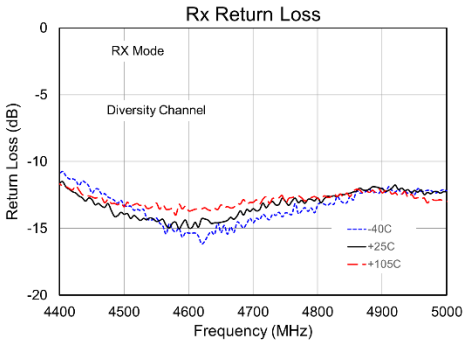


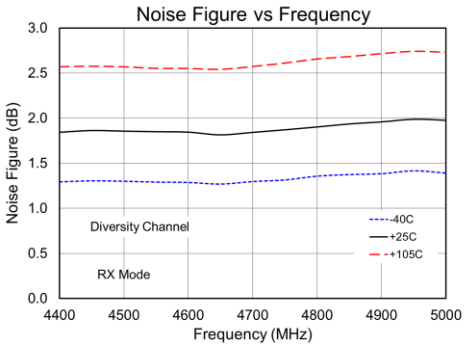
Application Circuit Performance Plots – Rx Mode (Diversity Channel)

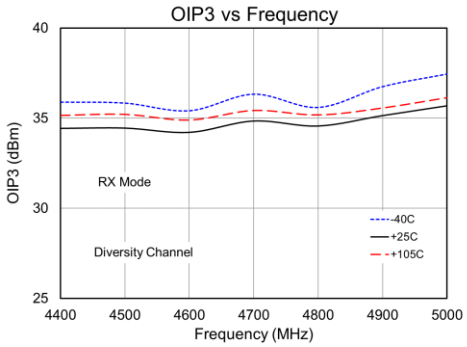
Test conditions unless otherwise noted: LNA1, 2, 3, 4, A1, A2 = +5V; 28V/0 T1, 2 = +28V; 28V/0 R1, 2, PD1, 2 = 0V; Temp.= +25 °C

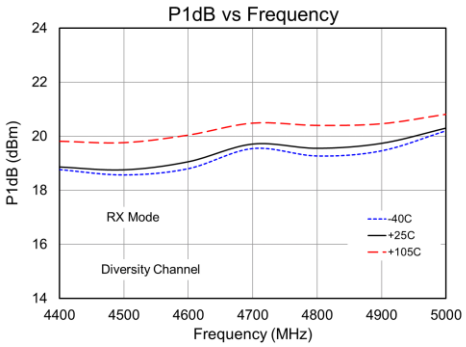


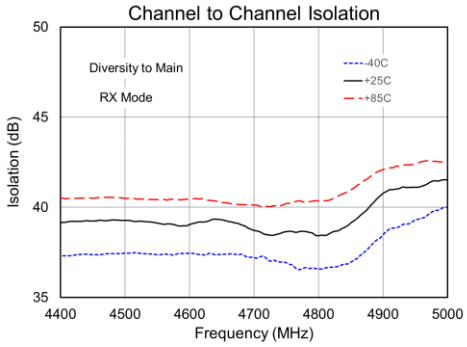












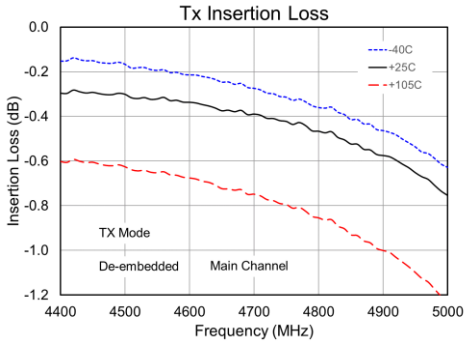
Typical Application Circuit Performance – Tx Mode

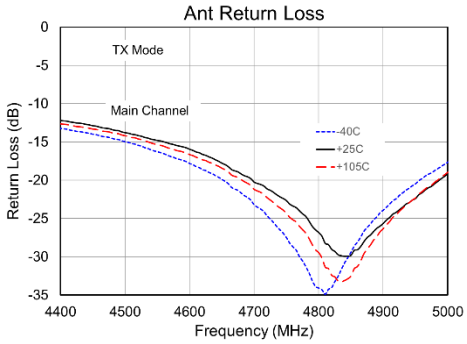
Parameter	Conditions[1]	Typical Value			Units
Frequency		4400	4700	5000	MHz
Insertion Loss	De-embedded, main channel	0.30	0.39	0.76	dB
Input Return Loss	ANT port, main channel	12.6	20.7	18.9	dB
Output Return Loss	TX port, main channel	12.0	16.5	17.6	dB

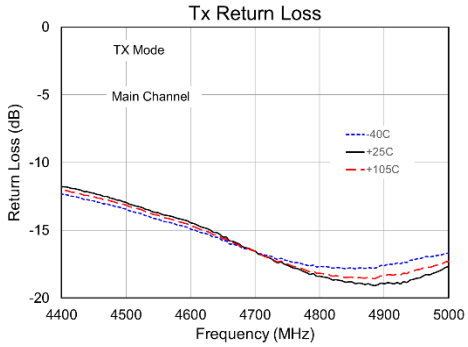
Notes:
1. Test conditions unless otherwise noted: LNA1, 2, 3, 4, A1, A2, PD1, 2 = +5V; 28V/0 R1, 2 = +28V; 28V/0 T1, 2 = 0V; Temp. = +25 °C

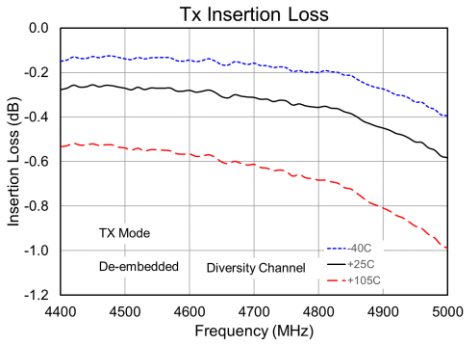
Application Circuit Performance Plots – Tx Mode

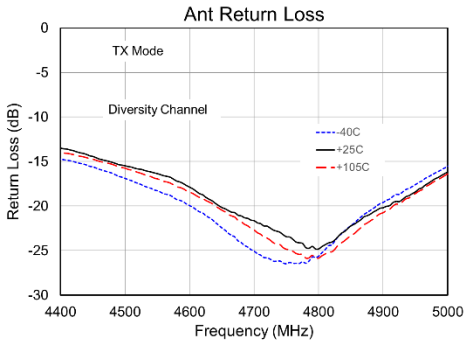
Test conditions unless otherwise noted: LNA1, 2, 3, 4, A1, A2, PD1, 2 = +5V; 28V/0 R1, 2 = +28V; 28V/0 T1, 2 = 0V; Temp.= +25 °C

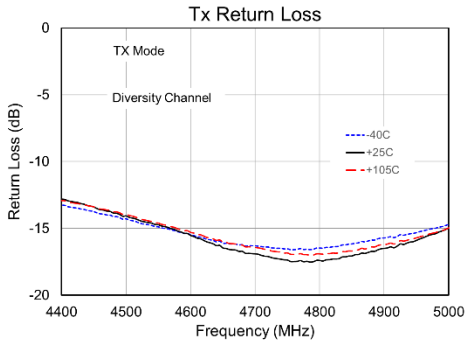




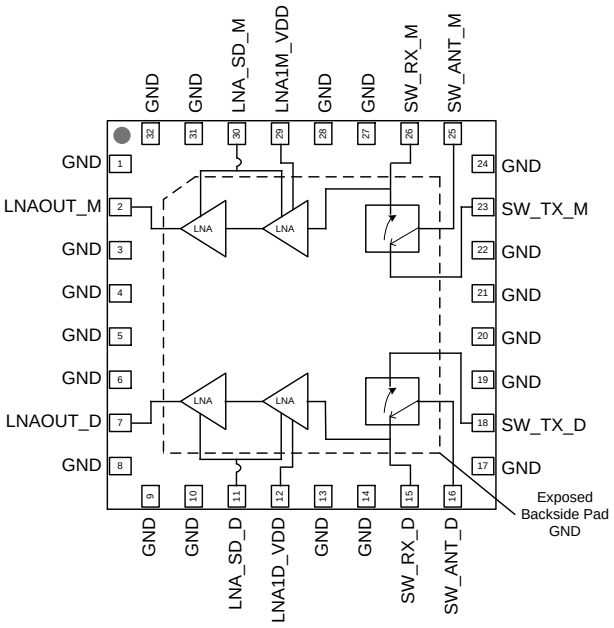








Pin Configuration and Description



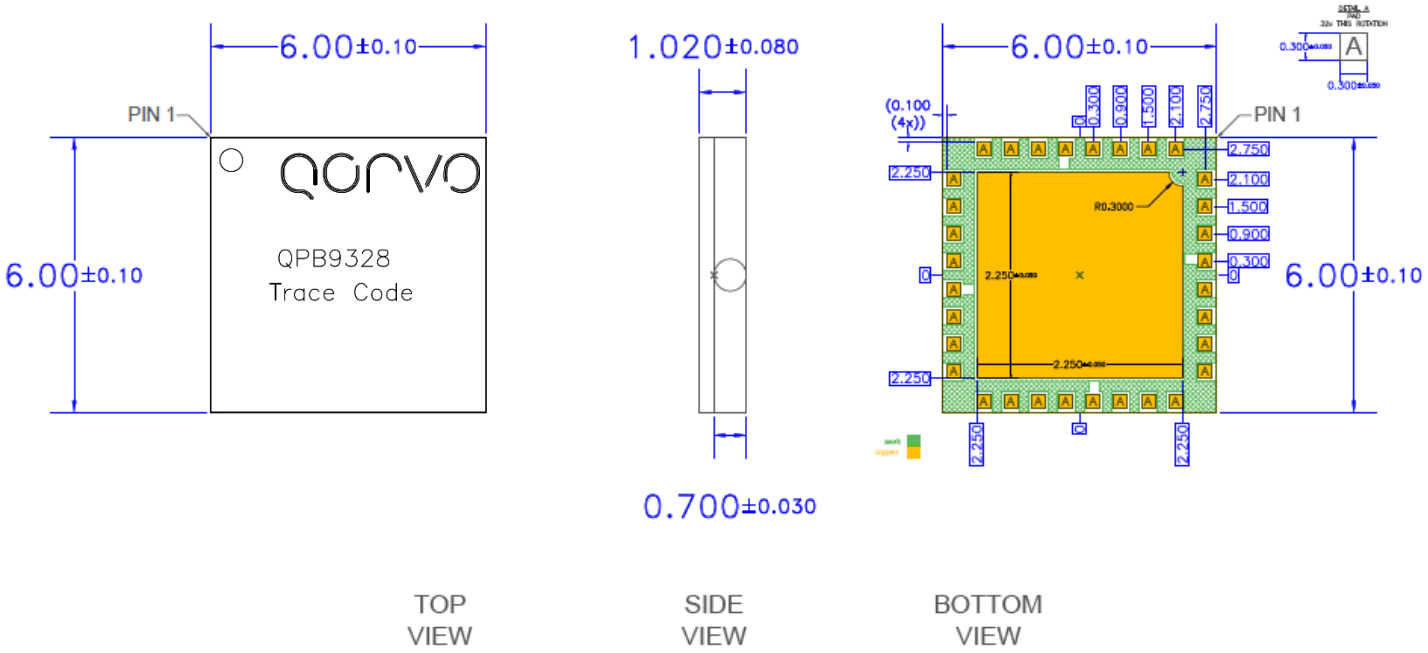
Top View

Pin No.	Label	Description
1, 3, 4, 5, 6, 8, 9, 10, 13, 14, 17, 19, 20, 21, 22, 24, 27, 28, 31, 32	GND	Ground connection. This pin is connected internally and can be left floating or connected to ground.
2	LNAOUT_M	Main channel RX output port. Bias port for LNA2. Needs external DC block.
7	LNAOUT_D	Diversity channel RX output port. Bias port for LNA2. Needs external DC block.
11	LNA_SD_D	Common shutdown pin for both LNA1 & 2 on diversity channel.
12	LNA1D_VDD	Diversity channel LNA1 bias voltage supply pin. External choke and bypass caps needed.
15	SW_RX_D	RX port of switch on diversity channel.
16	SW_ANT_D	Diversity channel antenna port on switch.
18	SW_TX_D	TX port of switch on diversity channel.
23	SW_TX_M	TX port of switch on main channel.
25	SW_ANT_M	Main channel antenna port on switch.
26	SW_RX_M	RX port of switch on diversity channel.
29	LNA1M_VDD	Main channel LNA1 bias voltage supply pin. External choke and bypass caps needed.
30	LNA_SD_M	Common shutdown pin for both LNA1 & 2 on main channel.
Backside Pad	GND	Ground connection. The back side of the package should be connected to the ground plan though as short of a connection as possible. PCB via holes under the device are required.

Package Marking and Dimensions

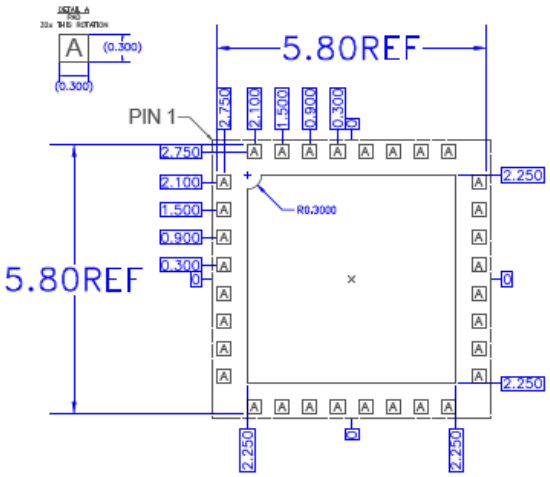
Marking

Part Number: QPB9328
Long Trace Code: XXXXXXXX
Up to 8 Characters to be assigned by sub-contractor

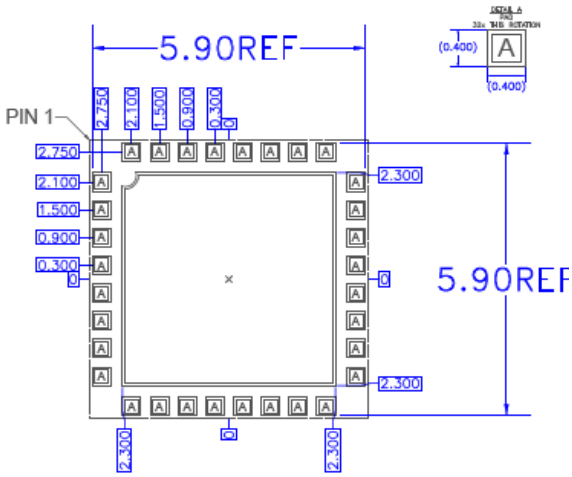


Notes:
1. All dimensions are in microns. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



RECOMMENDED
LAND PATTERN



RECOMMENDED
LAND PATTERN MASK

Notes:

1. A heat sink underneath the area of the PCB for the mounted device is recommended for proper thermal operation.
2. Ground / thermal via holes are critical for the proper performance of this device. Via holes should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment). This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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