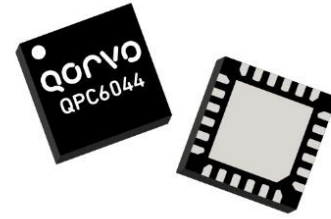


Product Overview

The QPC6044 is a Silicon on Insulator (SOI) Single-Pole 4-Throw (SP4T) switch designed for uses in cellular, 3G, LTE and other high-performance communication systems. It offers a high isolation, symmetric throw ports with excellent linearity and power handling capability. No DC blocking capacitors are necessary on the RF ports. The design is non-reflective as such the RF1, RF2, RF3 and RF4 ports are terminated with 50 Ω load(s) in the non-throw or OFF state. The QPC6044 is 1.8V positive control logic compatible. It incorporates a single pin control to disable the internal Negative Voltage Generator (NVG). And the required negative voltage can be supplied by an off-chip external source to the same pin.

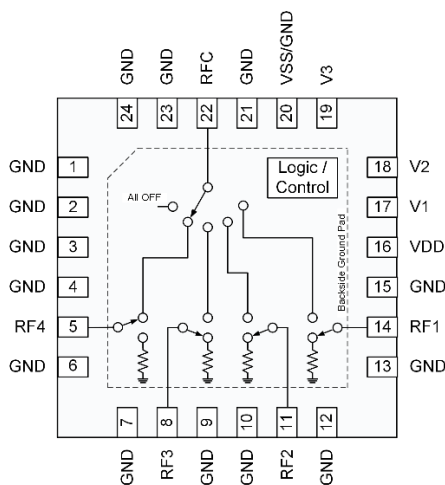


24-Pin, 4 x 4 mm QFN Package

Key Features

- 5 – 6000 MHz Operation
- Symmetrical SP4T
- Non-Reflective RF1, RF2, RF3 & RF4 Ports, Terminated in ALL-OFF State
- No Blocking Capacitors Necessary Unless DC Voltage on RF line
- High Isolation: 54 dB at 2 GHz
- High Input IP3: +61 dBm
- 1.8 V Logic Compatible

Functional Block Diagram



Top View

Applications

- Cellular, 3G, 4G, 5G Infrastructure
- WiBro, WiMax, LTE
- High Performance Communication Systems
- Test Equipment

Ordering Information

Part No.	Description
QPC6044TR13	2,500 pieces on a 13" reel (standard)
QPC6044 PCK410	5 MHz – 6GHz Evaluation Board with 5-piece samples

Absolute Maximum Ratings

Parameter		Rating
Storage Temperature		-40 to +150 °C
RF Input Power, non-internally terminated		+37.5 dBm
RF Input Power, RFX terminated		+29 dBm
Device Voltage	(VDD)	+6 V
	(VSS)	-6 V
Control Voltage	(V1, V2, V3) Low / High	-0.2 V / +6 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (VDD)	+2.7	+5.0	+5.5	V
Device Voltage (VSS), External Negative Voltage Supply	-5.5	-5.0	-2.7	V
Device Voltage (VSS), Internal Negative Voltage Generator		0		V
T _{CASE}	-40		+105	°C
T _j for >10 ⁶ hours MTTF			+125	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Units
Operational Frequency Range		5		6000	MHz
Insertion Loss ⁽²⁾ (RFC to RF1/RF2/RF3/RF4)	450 MHz		0.87		dB
	900 MHz		0.91		dB
	2100 MHz		0.98	1.25	dB
	2600 MHz		1.00		dB
	4000 MHz		1.05		dB
	6000 MHz		1.20		dB
Isolation (RFC to RF1/RF2/RF3/RF4)	450 MHz		66		dB
	900 MHz		61		dB
	2100 MHz	50	54		dB
	2600 MHz		52		dB
	4000 MHz		48.5		dB
	6000 MHz		45.5		dB
Isolation (RF1/2/3/4 to RF1/2/3/4)	450 MHz		62		dB
	900 MHz		57		dB
	2100 MHz		50		dB
	2600 MHz		48		dB
	4000 MHz		45		dB
	6000 MHz		42		dB
Return Loss (RF1/RF2/RF3/RF4 ON-State)	450 MHz		26		dB
	900 MHz		25		dB
	2100 MHz		26		dB
	2600 MHz		27		dB
	4000 MHz		30		dB
	6000 MHz		20		dB
Return Loss (RF1/RF2/RF3/RF4 OFF-State)	450 MHz		32		dB
	900 MHz		28		dB
	2100 MHz		23		dB
	2600 MHz		22		dB
	4000 MHz		20		dB
	6000 MHz		15		dB

Electrical Specifications (Continued)

Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Units
Operational Frequency Range		5		6000	MHz
Input IP3	1.0 GHz, +17 dBm input power per-tone, 1 MHz tone spacing	55	61		dBm
Input 1 dB Compression Power	1.0 GHz		37		dBm
NVG Spur	Internal NVG ON		-104		dBm
Setting Time	50% V1/V2/V3 to optimum functionality		1	4	μs
Start-up Time	90% VDD to full functionality		5	25	μs
Switching Time	50% control to 10/90% RF		150	240	ns
Supply Current (I _{VDD})	VDD 5.0V		100		μA
Control Current, (I _{V1} , I _{V2} , I _{V3})	V1, V2, V3 each at 5.0V		2		μA
VSS Current (I _{VSS})	VSS -5.0V, Internal NVG disabled		100		μA
Low Control Voltage (V1, V2, V3)	1.8 V Logic compatible	0		0.63	V
High Control Voltage (V1, V2, V3)		1.1		VDD	V

Notes:

1. Test conditions unless otherwise noted: VDD = +3V to +5V, V1/V2/V3 = 0/+5.0V, Temp = +25 °C, 50 Ω system, RF ports DC Voltage 0V
2. PCB trace loss deducted

Maximum Operating Power at High Temperature, ≥50 MHz CW

Input Port	State	Power at each port		Thermal Resistance, θ _{jc}
		T _c +85°C	T _c +105°C	
RFC, RF1, RF2, RF3, or RF4	ON, Active Throw	35.4 dBm	32.2 dBm ⁽¹⁾	56 °C/W
RF1, RF2, RF3, or RF4	OFF, 1 port	27.8 dBm	24.8 dBm ⁽³⁾	66 °C/W
RF1, RF2, RF3, RF4	OFF, 2 ports adjacent	26.7 dBm	23.7 dBm ⁽²⁾⁽³⁾	85 °C/W
RF1, RF2, RF3 and RF4	OFF, All 4 ports	26.6 dBm	23.6 dBm ⁽³⁾	86 °C/W

Notes:

1. For frequency <50 MHz, the maximum operating power at all temperatures should be at least 2 dB below P1dB refer to performance plot
2. Two ports adjacent being driven simultaneously
3. Internally terminated OFF state

Truth Table – 3 Pin Control

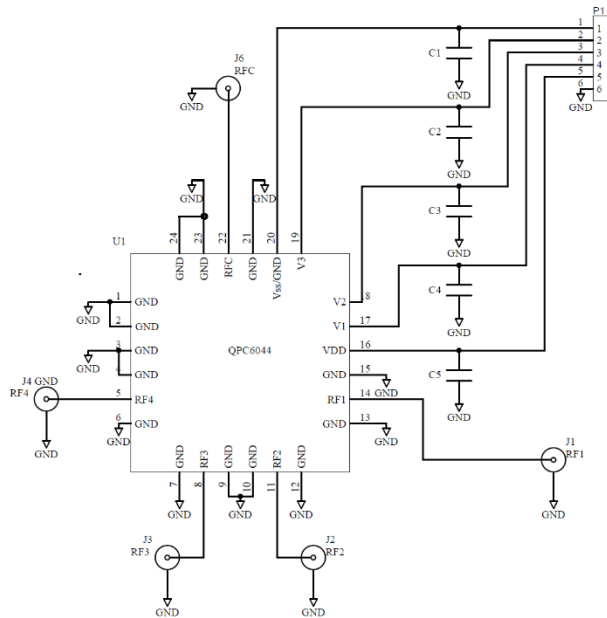
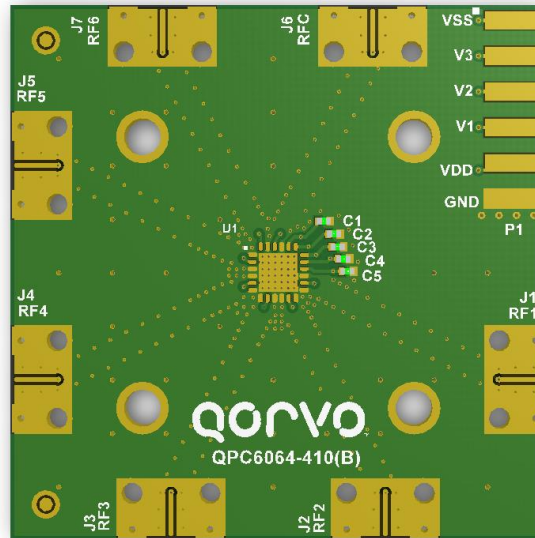
Control Input			Mode of Signal Path
V1	V2	V3	
0	0	0	RFC ↔ RF4, Active ON
1	0	0	RFC ↔ RF1, Active ON
0	1	0	RFC ↔ RF2, Active ON
1	1	0	RFC ↔ RF3, Active ON
0	0	1	RFC ↔ RF4, Active ON
1	0	1	All OFF, RFC Reflective
0	1	1	
1	1	1	

Truth Table – 2 Pin Control ⁽¹⁾

Control Input		Mode of Signal Path	
V1	V2		
1	0	RFC ↔ RF1	Active ON
0	1	RFC ↔ RF2	Active ON
1	1	RFC ↔ RF3	Active ON
0	0	RFC ↔ RF4	Active ON

Note: 1. V3 must be grounded

5 MHz to 6 GHz Evaluation Board – QPC6044PCK-410

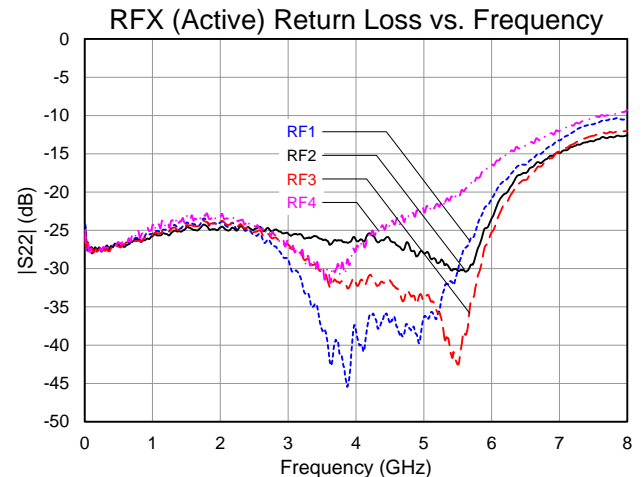
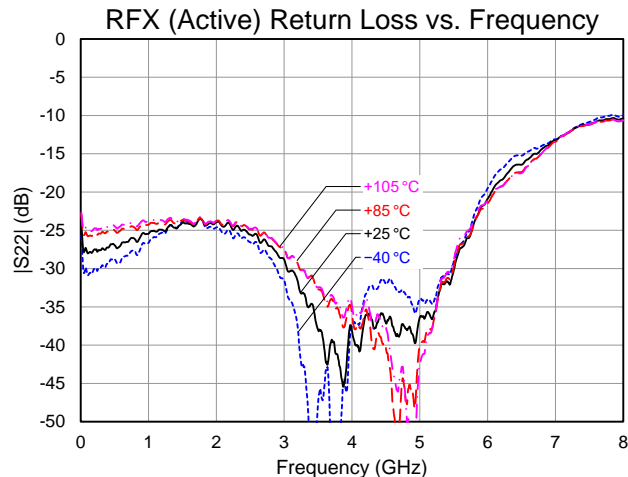
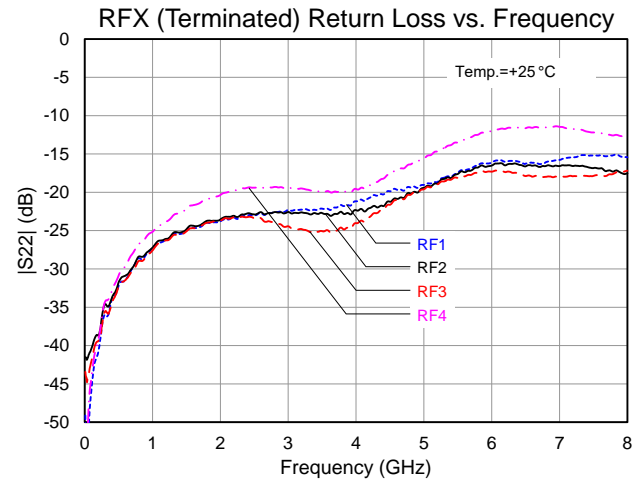
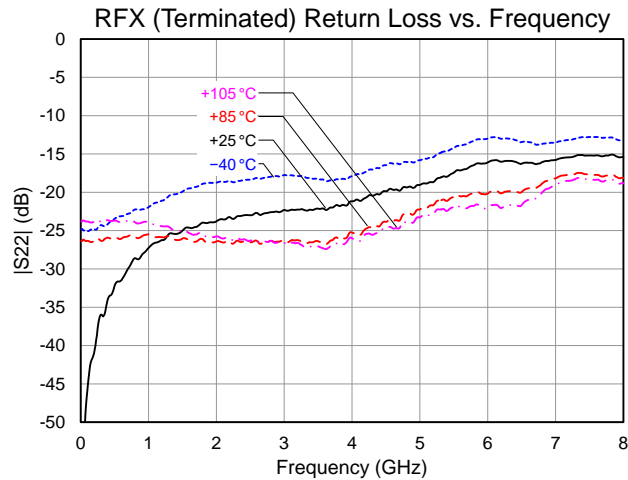
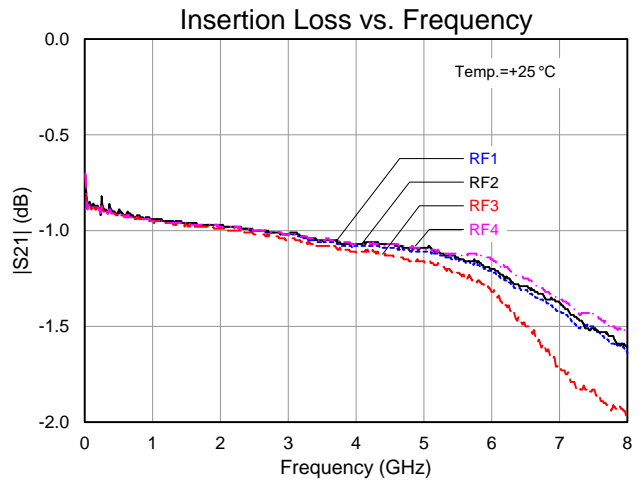
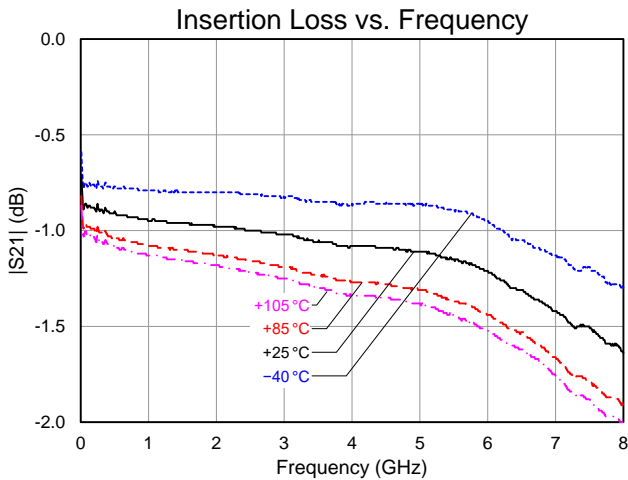


Bill of Material – QPC6044PCK-410

Reference Des.	Value	Description	Manuf.	Part Number
-	-	Printed Circuit Board	Qorvo	QpC6064-410(B)
U1	-	SOI, High Isolation SP4T RF switch	Qorvo	QPC6044
C1, C2, C3, C4, C5	100 pF	CAP, 100 pF, 5%, 50V, COG, 0402	Taiyo Yuden	RM UMK105 CG101JV-F
J1, J2, J3, J4, J6	SMA	CONN, SMA, EL, FLT VIPER, MAT-21-1038	Amphenol	901-10425
P1	-	CONN, HDR, ST, PLRZD, 6-Pin, 0.100"	AMP	640454-6

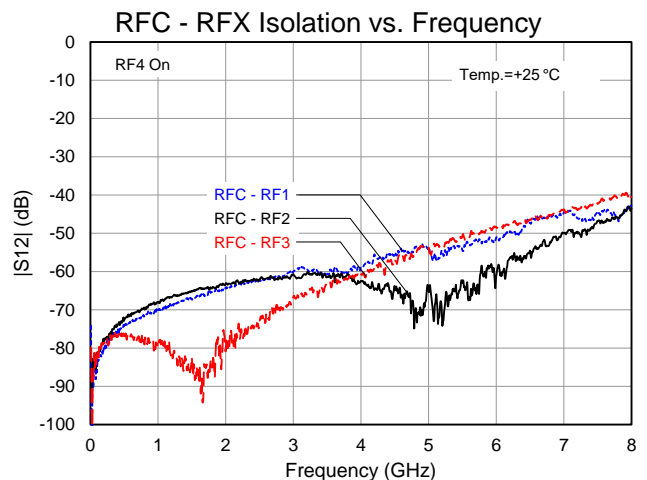
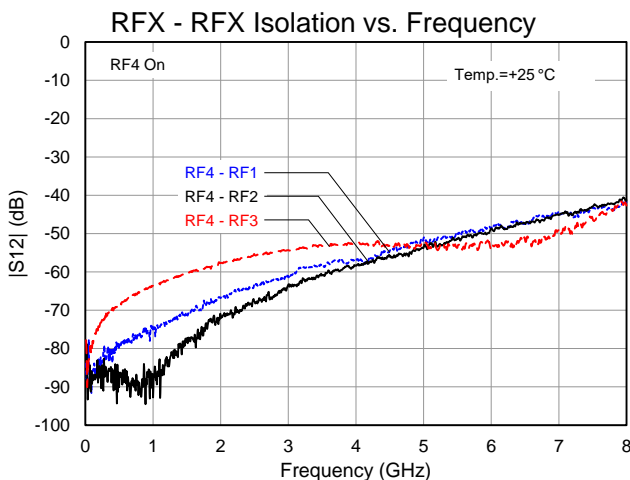
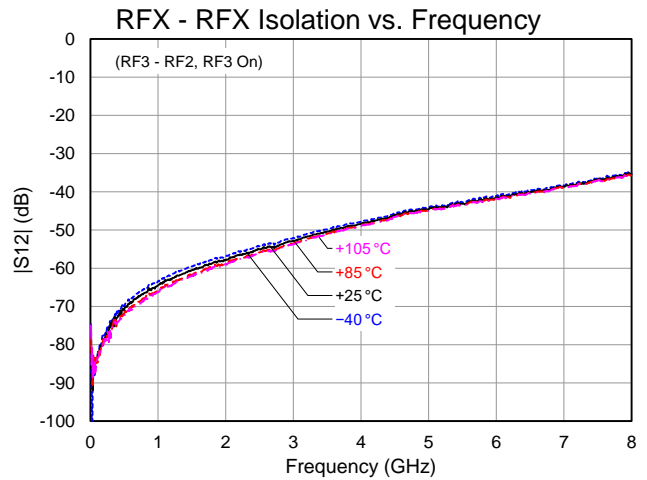
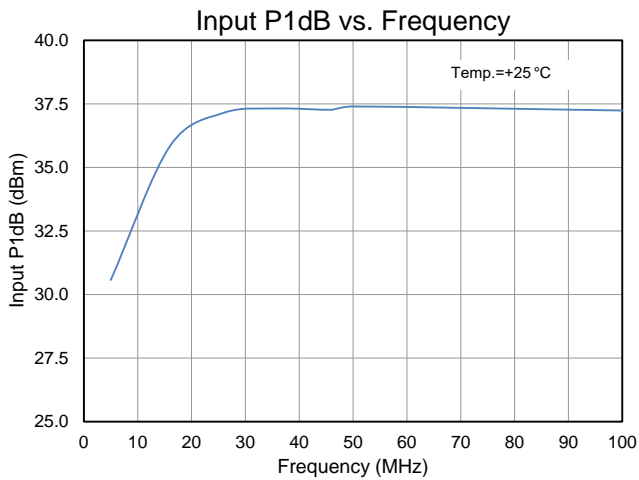
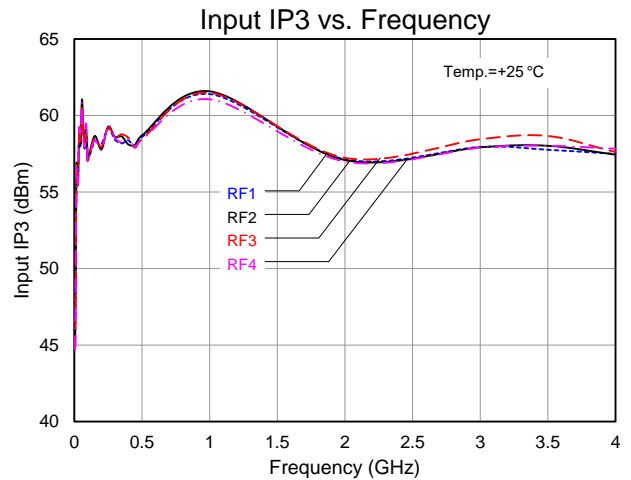
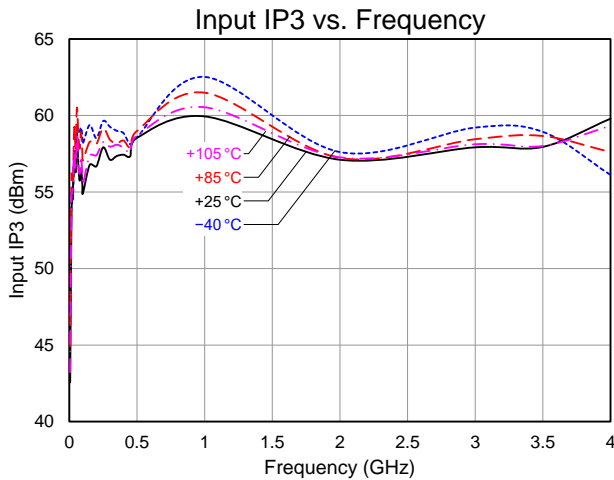
Performance Plots – QPC6044PCK-410

Test conditions unless otherwise noted: VDD = +3.0 V, Temp.=+25 °C



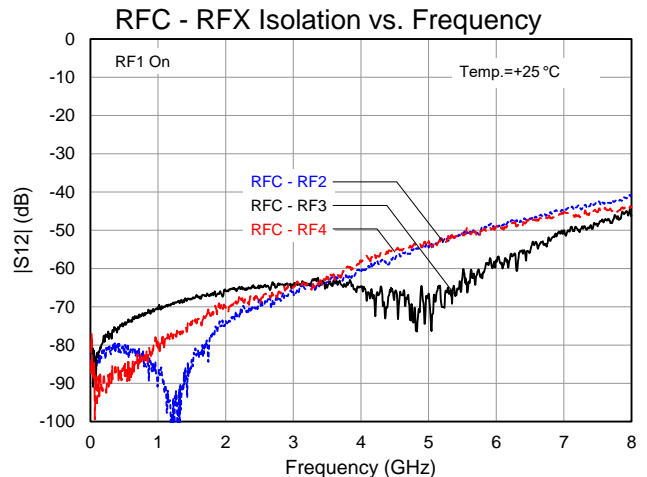
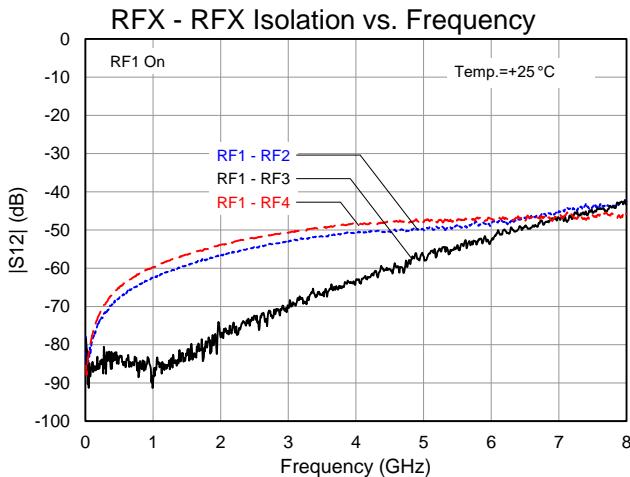
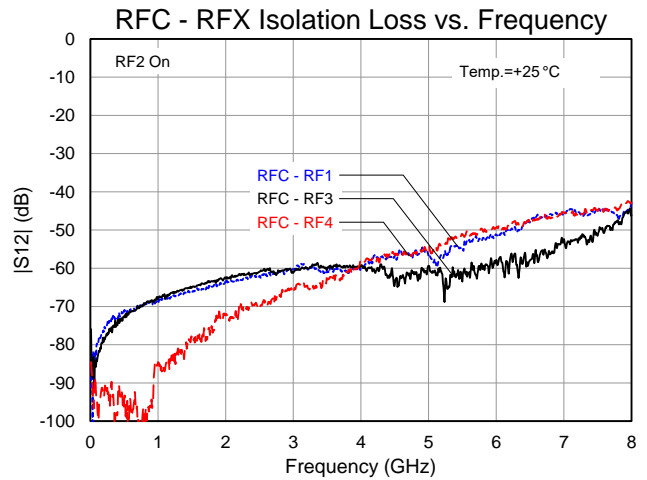
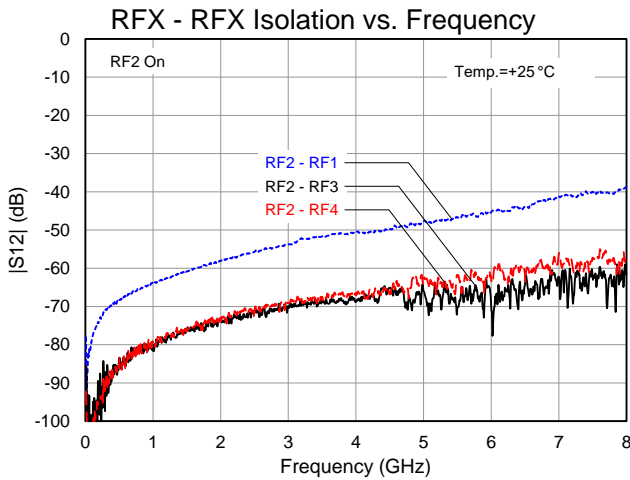
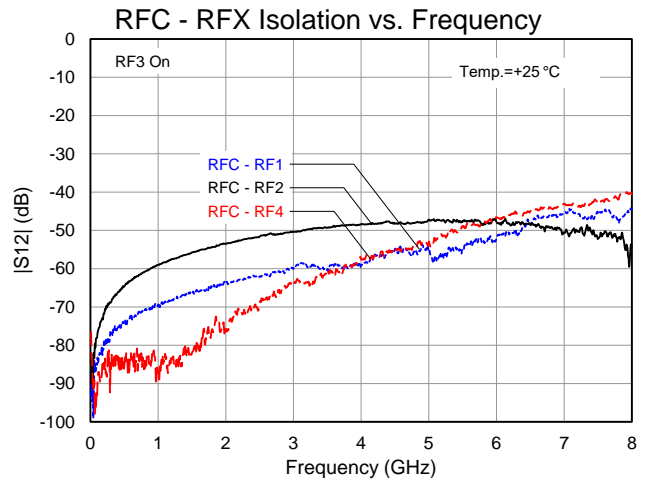
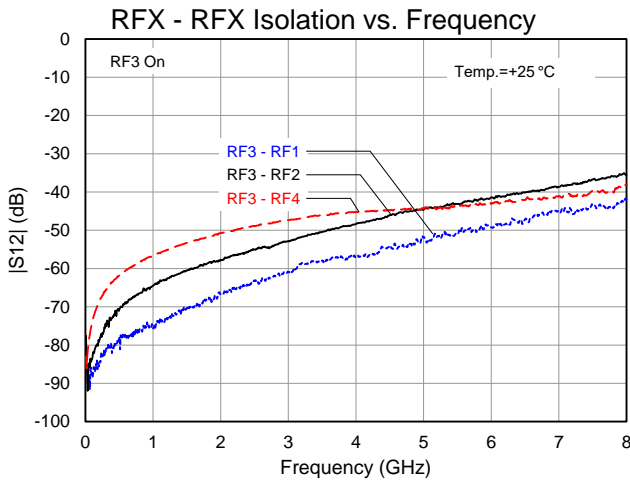
Performance Plots – QPC6044PCK-410 (Continued 1)

Test conditions unless otherwise noted: VDD = +3.0 V, Temp.=+25 °C

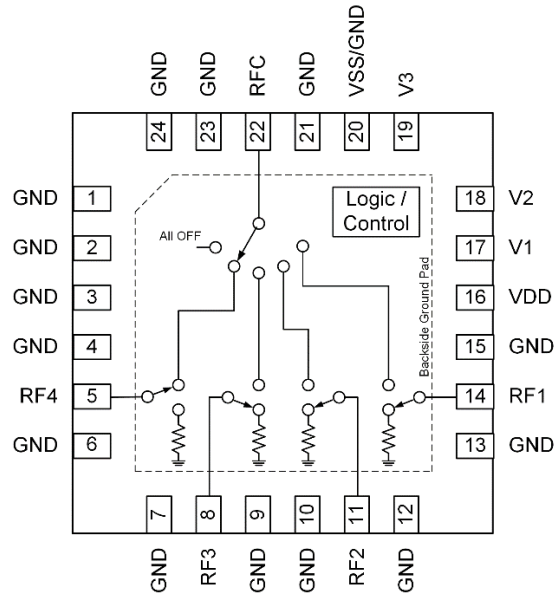


Performance Plots – QPC6044PCK-410 (Continued 2)

Test conditions unless otherwise noted: VDD = +3.0 V, Temp.=+25 °C



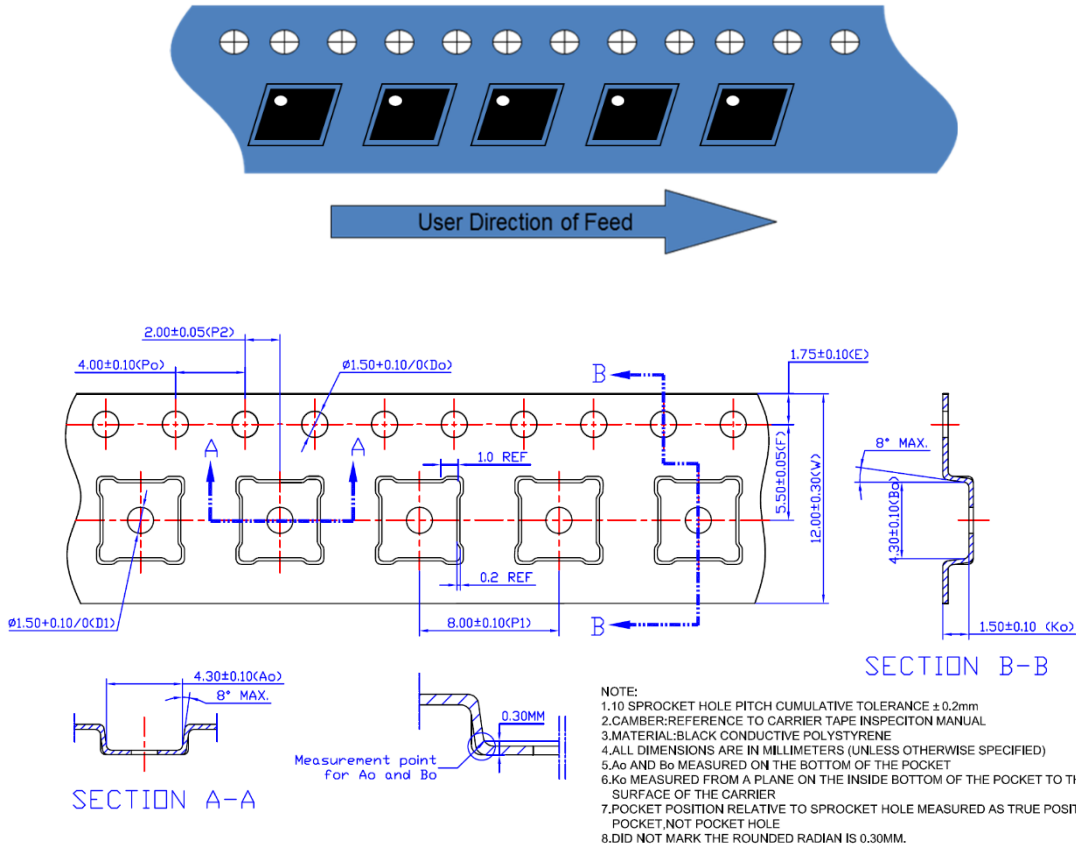
Pad Configuration and Description



Top View

Pad No.	Label	Description
1-4, 6, 7, 9, 10, 12, 13, 15, 21, 23, 24	GND	DC and RF ground, connect to low inductive path to PCB ground
5	RF4	RF Port 4
8	RF3	RF Port 3
11	RF2	RF Port 2
14	RF1	RF Port 1
16	VDD	DC Supply Voltage Input
17	V1	Control Input 1
18	V2	Control Input 2
19	V3	Control Input 3
20	VSS/GND	Negative DC Supply Voltage and Internal Negative Voltage Generator (NVG) control input. Provide low inductive ground connection on this pin to enable internal NVG or directly connect -2.7V to -5V external voltage supply to disable the internal NVG. Re-enable internal NVG, VDD cycling required
22	RFC	RF Common Port
Backside Paddle	GND	RF and DC ground. Must be soldered on PCB ground plane over a bed of via holes to minimize inductance and thermal resistance

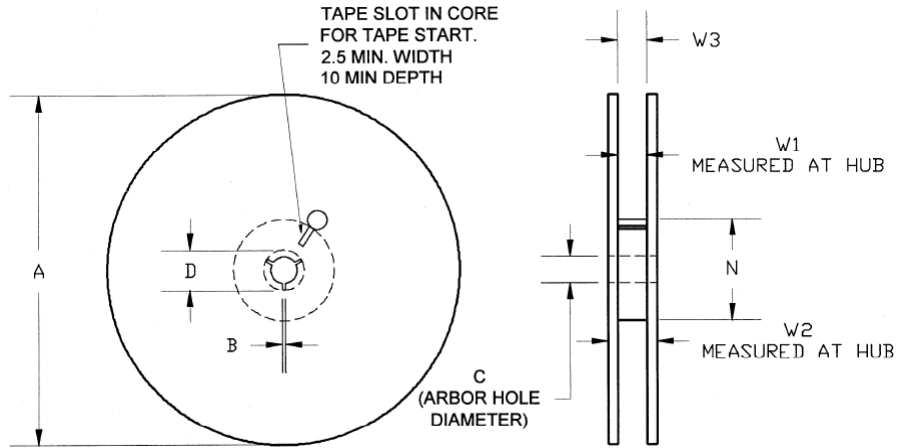
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.169	4.30
	Width	B0	0.169	4.30
	Depth	K0	0.059	1.50
	Pitch	P1	0.314	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

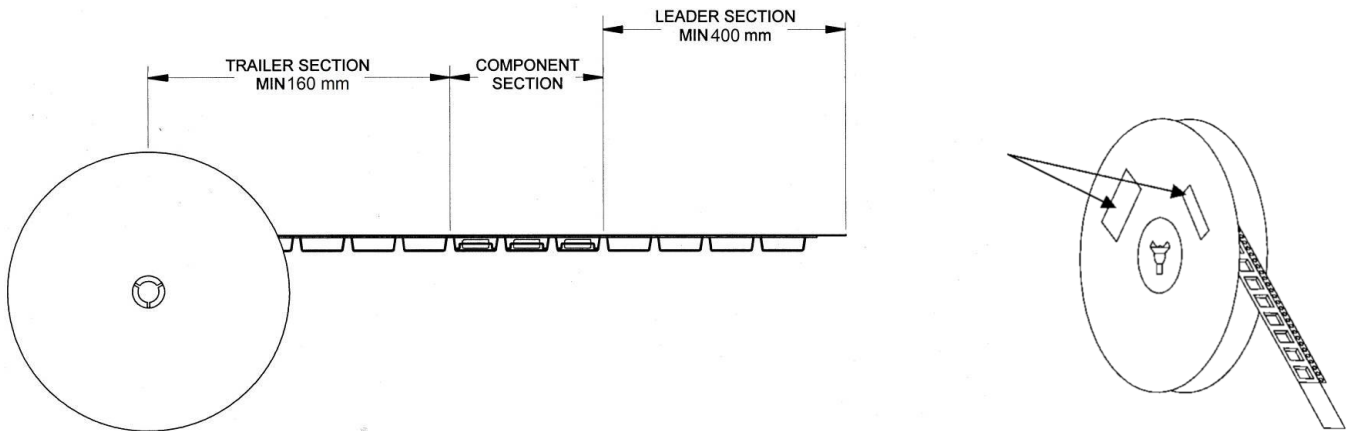
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 13" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



- Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
 2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 2	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 2	IPC/JEDEC J-STD-020



Caution!
 ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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