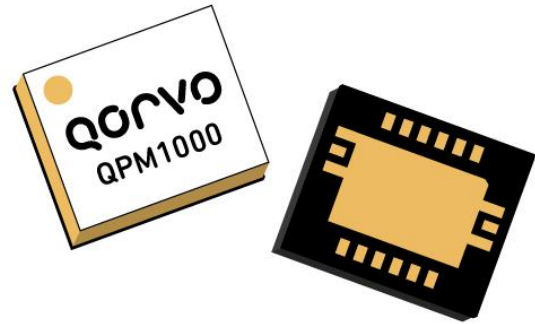


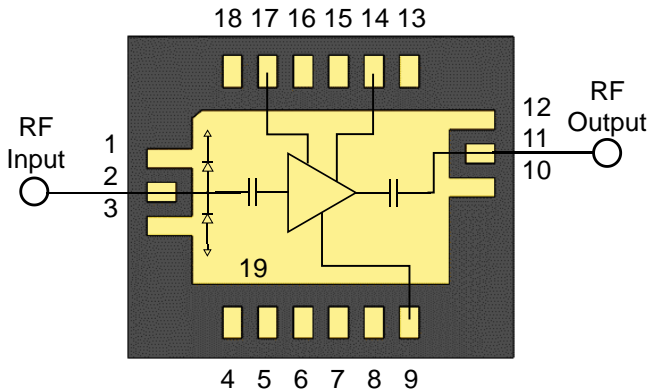
Product Description

The Qorvo QPM1000 is an integrated limiter/LNA providing robust, high performance over the 2–20GHz frequency range. The QPM1000 delivers 17 dB small signal gain with gain control and > 18 dBm P1dB with a range of noise figure of 1.5 – 4 dB across frequency. In addition, the integrated limiter provides a robustness level of up to 4 W of incident power without performance degradation.

The QPM1000 is packaged in an air cavity, laminate-based 6 x 5 mm QFN for easy handling. With a small form factor coupled with both ports matched to 50 ohms, the QPM1000 is ideally suited to support both commercial and defense related applications where robust receiver front ends are required.



Functional Block Diagram



Applications

- Receiver Front End Building Block

Product Features

- Frequency Range: 2 – 20 GHz
- Input Power CW Survivability: 4 W
- Gain: > 17 dB
- Adjustable gain (> 30 dB using V_{G2})
- Noise Figure: < 2.0 dB (3-12 GHz)
- Noise Figure: < 4.0 dB (outer frequencies)
- IM3: < -21 dBc ($P_{IN} \leq 0$ dBm)
- Bias: $V_D = 5$ V, $I_D = 100$ mA, $V_{G1} = -0.6$ V typical, $V_{G2} = +1.3$ V
- Package dimensions: 6.00 x 5.00 x 1.72 mm

Ordering Information

Part No.	Description
QPM1000	2 – 20 GHz Limiter/LNA, Waffle Pack, Qty 25
QPM1000TR7	Tape and Reel 7", Qty 750
QPM1000EVB01	QPM1000 Evaluation Board, Qty 1

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	7 V
Gate Voltage Range (V_{G1})	-2 to 0 V
Gate Voltage Range (V_{G2})	-2 to +3 V
Drain Current (I_D)	144 mA
Gate Current Range (I_{G1})	-24 to +24 mA
Gate Current Range (I_{G2})	-24 to +24 mA
RF Input Power, CW, 50 Ω , 25 °C	36 dBm
RF Input Power, CW, 50 Ω , 85 °C	33 dBm
Incident Power, Pulsed ¹ , 50 Ω , 85 °C	40 dBm
Channel Temperature (T_{CH})	200 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-55 to 150 °C

Note:

¹ Pulse conditions: PW = 100 us, Duty Cycle = 10%

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating

Parameter	Value / Range
Drain Voltage (V_D)	5 V
Drain Current (I_{DQ})	100 mA
Gate Voltage (V_{G1}) ¹ , typical	-0.6 V
Gate Voltage (V_{G2})	+1.3 V
Operating Temperature Range (T_{BASE})	-40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Note:

¹ Adjust V_{G1} to achieve the required I_{DQ} .

Electrical Specifications

Parameter	Min	Typ	Max	Units
Operational Frequency Range	2	–	20	GHz
Small Signal Gain	–	> 17	–	dB
Input Return Loss	–	> 9.7	–	dB
Output Return Loss	–	> 7.6	–	dB
Noise Figure: 2 GHz	–	2.8	–	dB
Noise Figure: 8 GHz	–	1.7	–	dB
Noise Figure: 14 GHz	–	2.3	–	dB
Noise Figure: 20 GHz	–	4.0	–	dB
Third-Order Intermodulation Distortion ($P_{IN} \leq 0$ dBm / Tone, 10 MHz Tone Spacing)	–	< -21	–	dBc
Output Power (Saturation; $P_{IN} = 10$ dBm)	–	> 21	–	dBm
Output Power (1 dB Compression)	–	> 17	–	dBm
Small Signal Gain Temperature Coefficient	–	-0.010	–	dB/°C
Noise Figure Temperature Coefficient	–	0.010	–	dB/°C
Output Power Temperature Coefficient	–	-0.004	–	dBm/°C

Test conditions unless otherwise noted: 25 °C, $V_D = +5$ V, $I_{DQ} = 100$ mA, $V_{G1} = -0.6$ V Typical, $V_{G2} = 1.3$ V

Thermal and Reliability Information

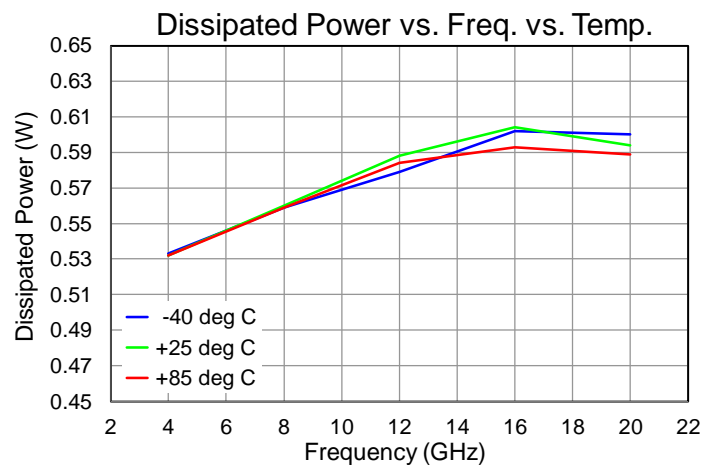
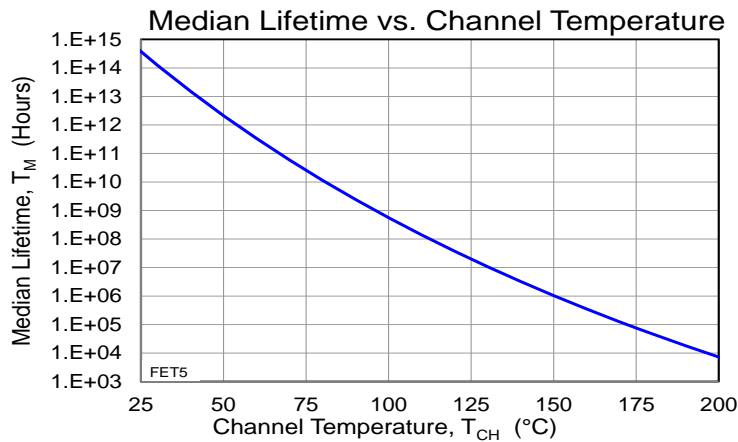
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) ⁽¹⁾	$T_{BASE} = 85\text{ }^\circ\text{C}$, $V_D = 5\text{ V}$	30.2	$^\circ\text{C/W}$
Channel Temperature (T_{CH}) (Under RF drive)	At Freq = 16 GHz, $P_{IN} = 10\text{ dBm}$: $I_{DQ} = 100\text{ mA}$, $I_{D_Drive} = 144\text{ mA}$	102	$^\circ\text{C}$
Median Lifetime (T_M)	$P_{OUT} = 20.3\text{ dBm}$, $P_{DISS} = 0.562\text{ W}$	4.77E+8	Hrs

Notes:

1. Thermal resistance measured to back of package.

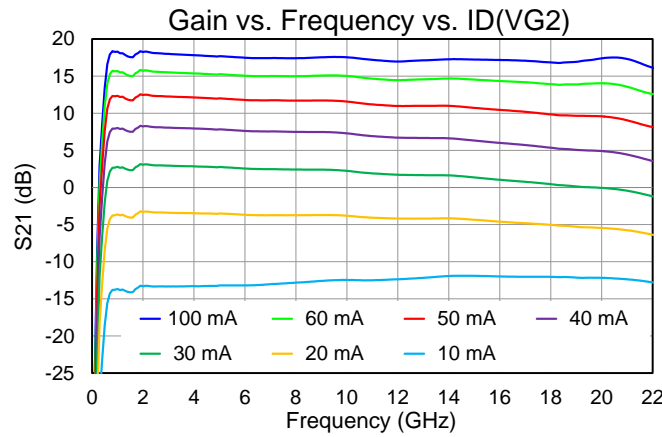
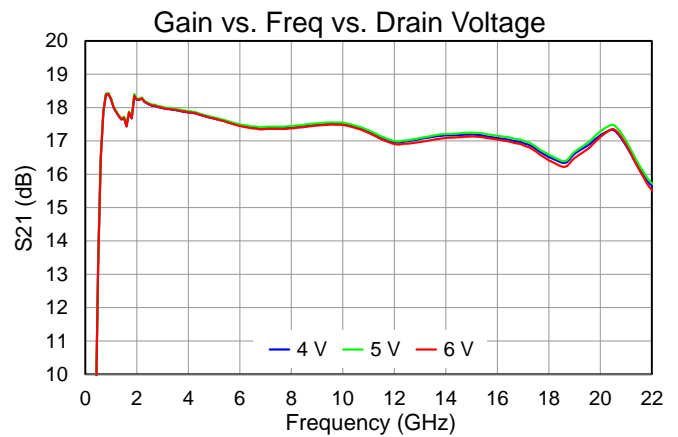
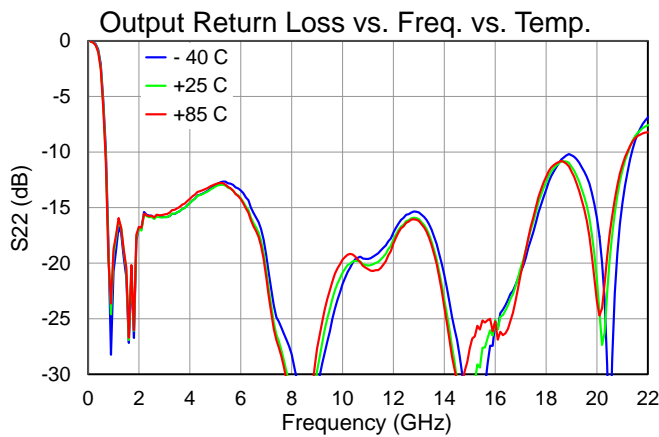
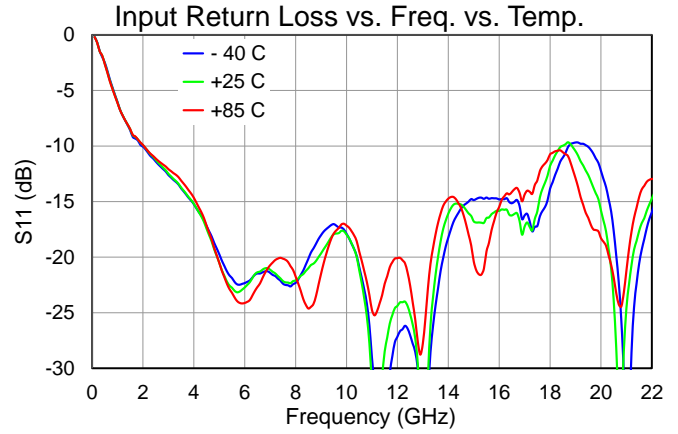
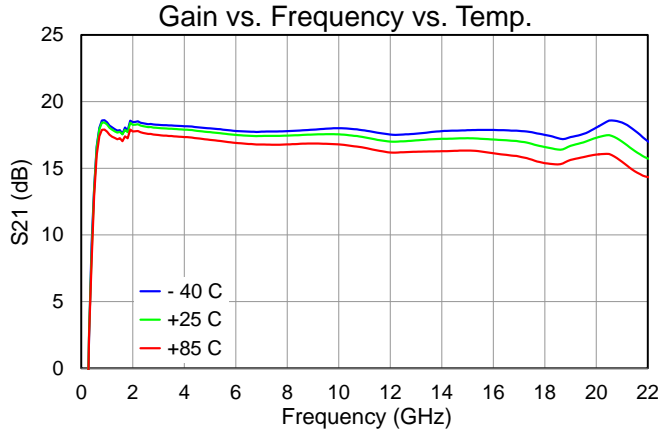
Median Lifetime

Test Conditions: $V_D = 6\text{ V}$; Failure Criteria = 10% reduction in I_{D_MAX} during DC Testing



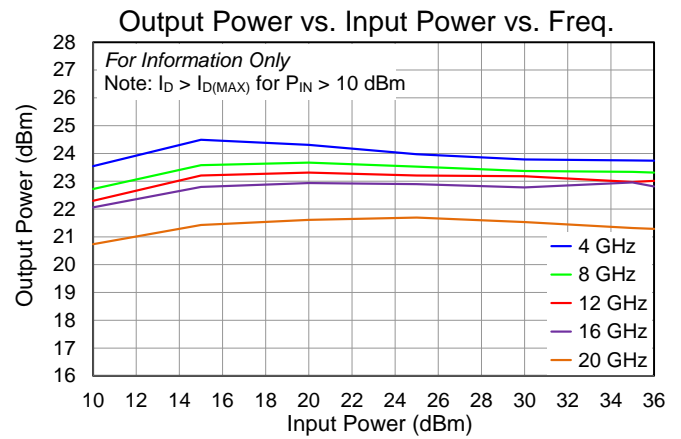
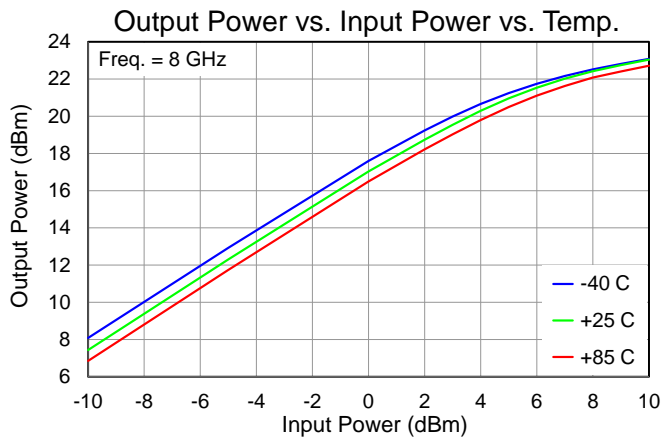
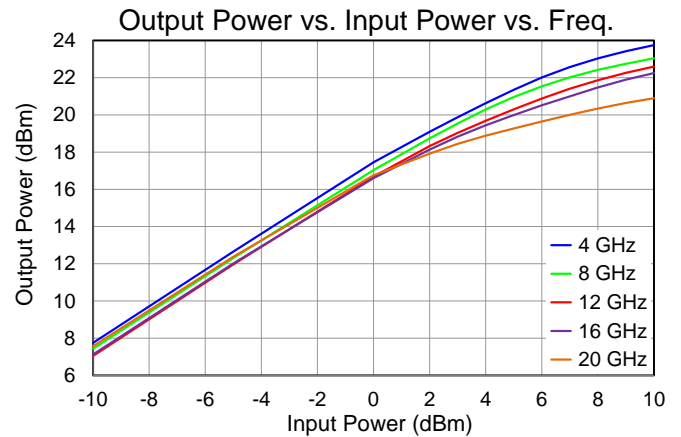
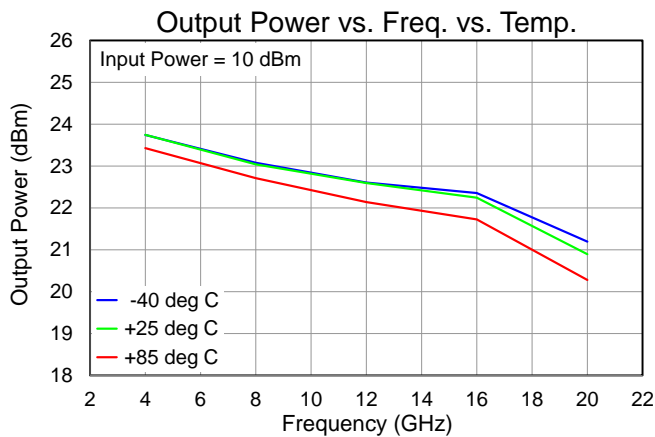
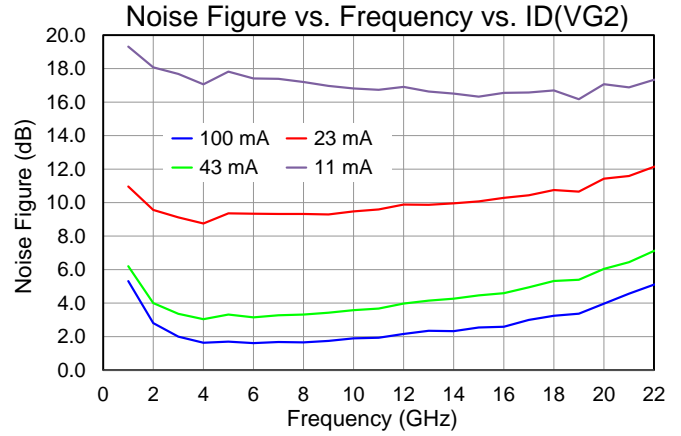
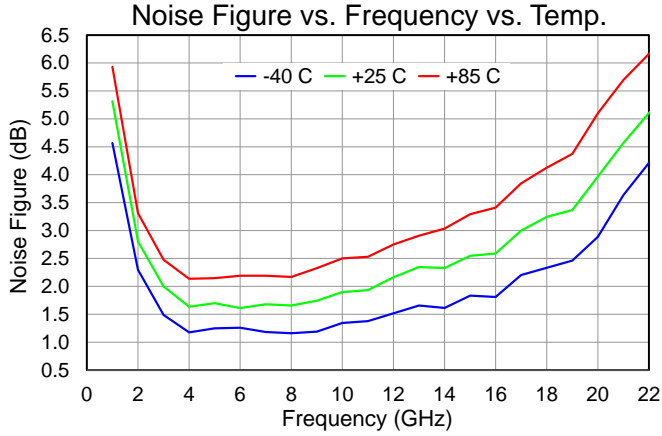
Performance Plots – Small Signal

Conditions unless otherwise specified: $V_D = 5\text{ V}$, $I_{DQ} = 100\text{ mA}$, $V_{G2} = 1.3\text{ V}$



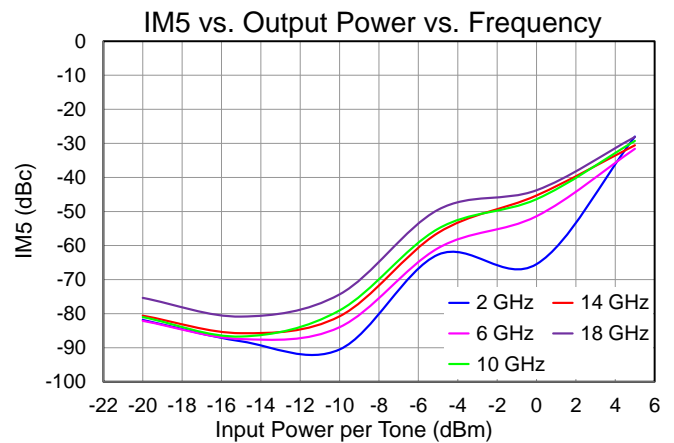
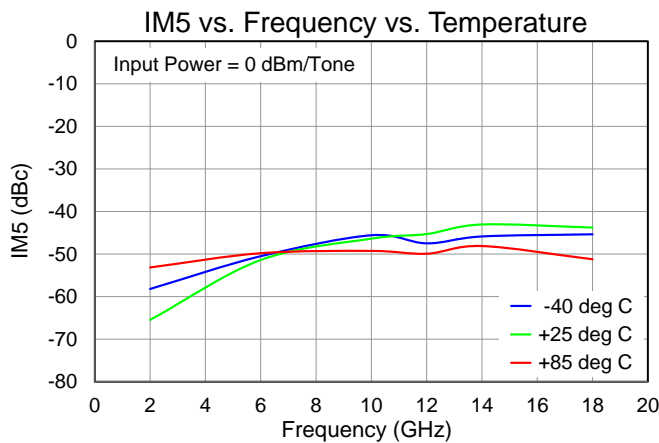
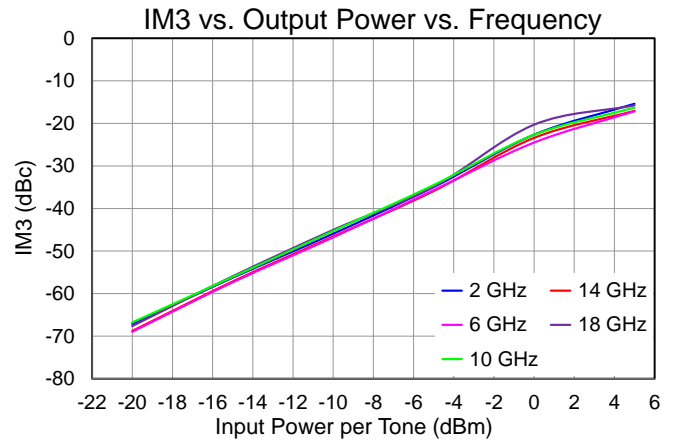
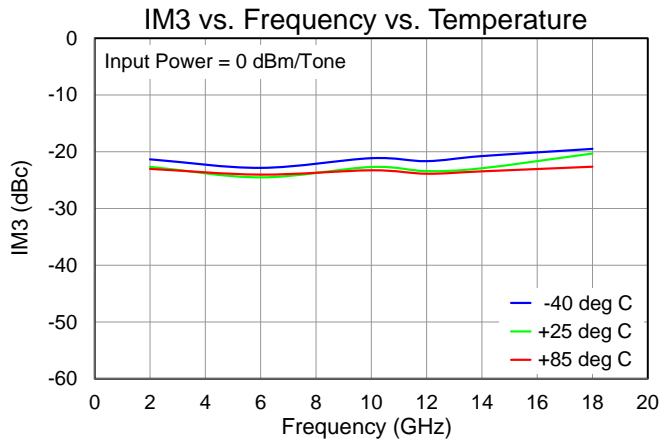
Performance Plots – Noise Figure & Large Signal

Conditions unless otherwise specified: $V_D = 5\text{ V}$, $I_{DQ} = 100\text{ mA}$, $V_{G2} = 1.3\text{ V}$

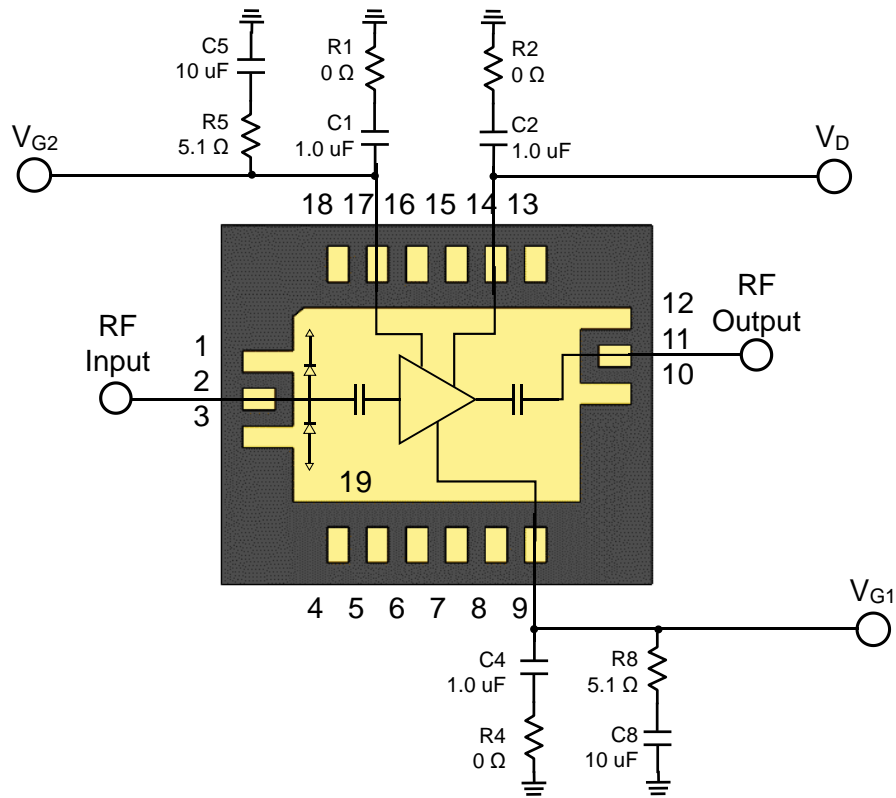


Performance Plots – Linearity

Conditions unless otherwise specified: $V_D = 5\text{ V}$, $I_{DQ} = 100\text{ mA}$, $V_{G2} = 1.3\text{ V}$



Applications Information and Pin Layout



Bias Up Procedure

1. Set I_D limit to 145 mA, I_G limit to 24 mA
2. Apply -1.5 V to V_{G1}
3. Apply $+5$ V to V_D ; ensure I_{DQ} is approx. 0 mA
4. Apply $+1.3$ V to V_{G2}
5. Adjust V_{G1} until $I_{DQ} = 100$ mA ($V_{G1} \sim -0.6$ V Typ.)
6. Turn on RF supply

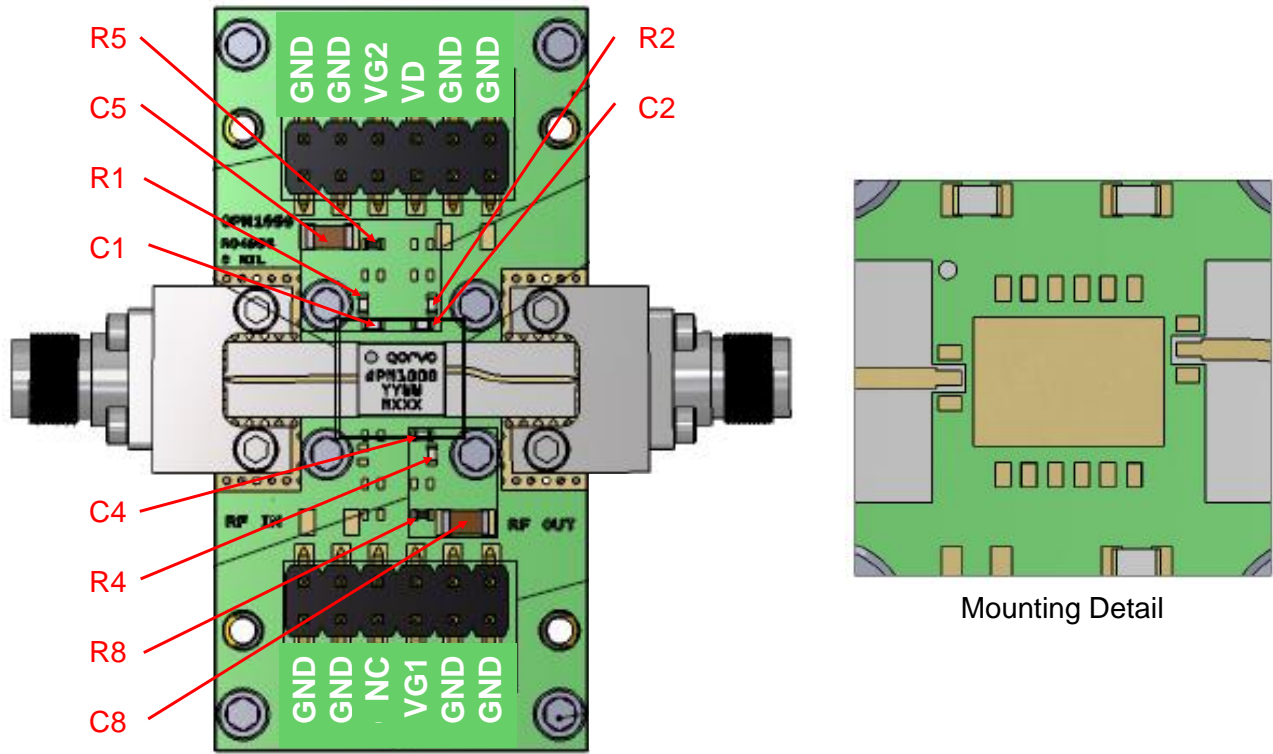
Bias Down Procedure

1. Turn off RF supply
2. Reduce V_{G1} to -1.5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_{G2} to 0 V
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_{G1} and V_{G2} supplies

Pad Description

Pin No.	Label	Description
1, 3, 10, 12, 19	GND	RF Ground
2	RF Input	RF Input; matched to 50 Ω
4 – 8, 13, 15, 16, 18	NC	No connection in package. Can be grounded on the PCB if desired.
9	V_{G1}	Gate Voltage 1; Bias network is required; see Application Information above.
11	RF Output	RF Output; matched to 50 Ω ; DC blocked
14	V_D	Drain voltage; Bias network is required; see Application Information above.
17	V_{G2}	Gate Voltage 2; Bias network is required; see Application Information above.

Evaluation Board and Mounting Detail

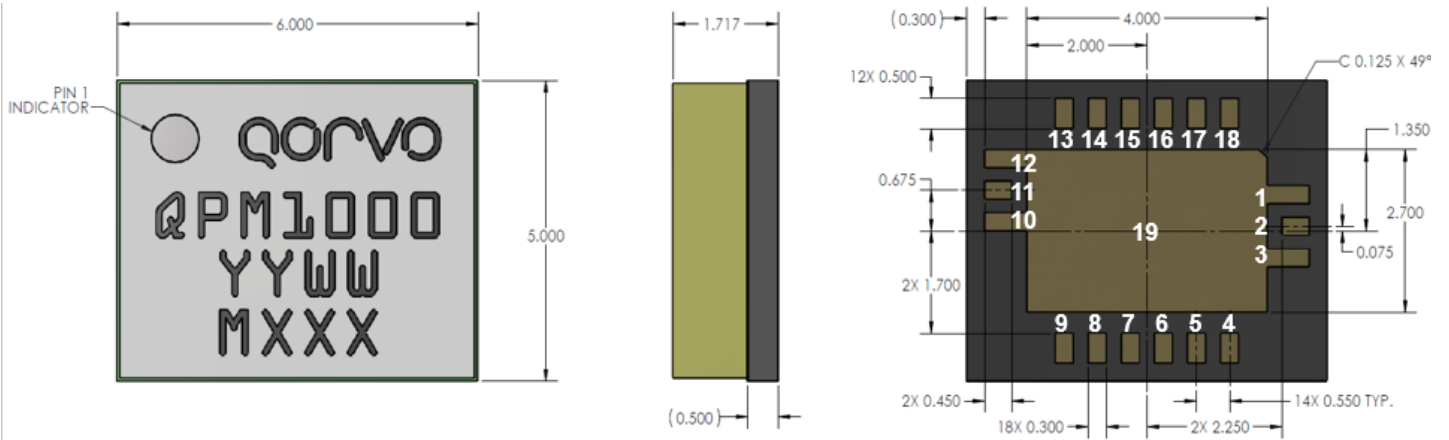


RF Layer is 0.008" thick Rogers Corp. RO40003C ($\epsilon_r = 3.35$). Metal layers are 1.0 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-5.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1, C2, C4	1.0 μ F	Cap, 402, +50 V, ± 10 %, X7R	Various	–
C5, C8	10.0 μ F	Cap, 1206, +50 V, ± 20 %, X5R	Various	–
R1, R2, R4	0 Ω	Res, 0402, SMT	Various	–
R5, R8	5.1 Ω	Res, 0402, SMT	Various	–

Mechanical Drawing



NOTES:
PACKAGE METAL BASE AND LEADS
ARE GOLD PLATED.

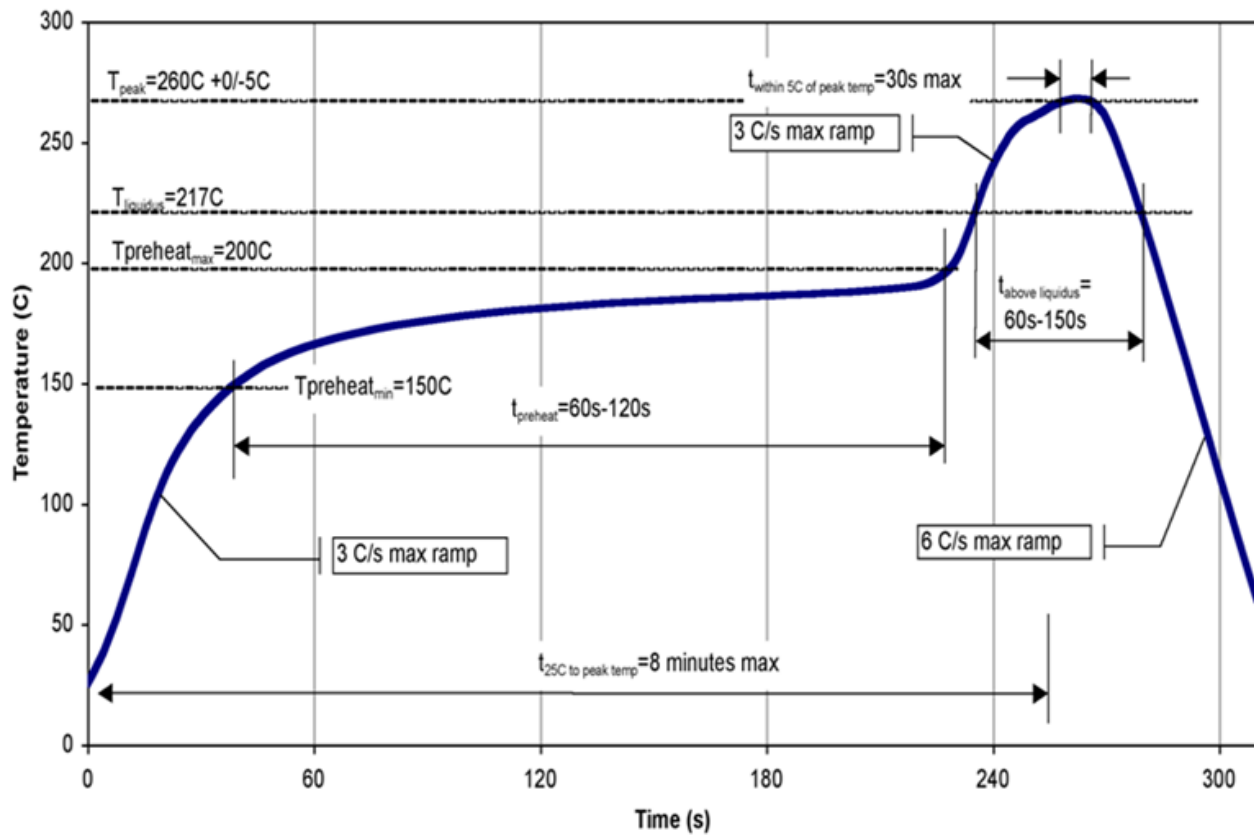
PART MARKING:
QPM1000: PART NUMBER
YY: PART ASSY YEAR
WW: PART ASSY WEEK
MXXX: LOT NUMBER

DIMENSIONS IN MM

Solderability

1. Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C.
2. This package is non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing is highly recommended.

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ANSI/ESD/JEDEC JS-001
ESD – Charge Device Model (CDM)	Class C3	ANSI/ESD/JEDEC JS-002
MSL – 260 °C Convection Reflow	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: 1-844-890-8163

Web: www.qorvo.com

Email: customer.support@qorvo.com

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