RF2312

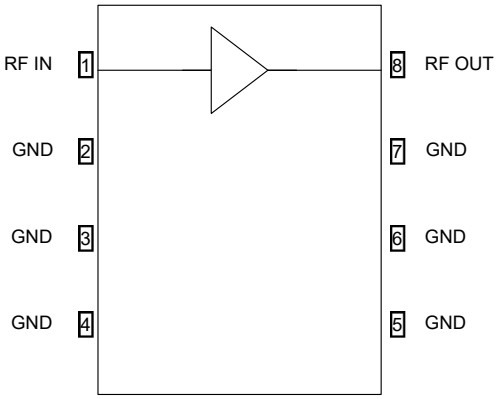
Linear General Purpose Amplifier

General Description

The RF2312 is a general purpose, low cost, high linearity RF amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process and has been designed for use as an easily cascadable 75Ω gain block. In addition to the high linearity, the gain flatness of better than 0.5 dB from 5 – 725 MHz, makes this part ideal for cable TV Return Path FDX applications. The device is self-contained with 75Ω input and output impedances and requires only two external DC biasing elements to operate as specified.

SOIC-8 Package

Functional Block Diagram



Key Features

- 5 – 725 MHz Operation
- 75Ω Internally Matched Input and Output
- 15 dB Small Signal Gain
- 3.8 dB Noise Figure
- +20 dBm Output Power
- Single 5 – 12 V Positive Power Supply

Applications

- DOCSIS 3.1 & 4.0 Return Path Amplifier
- Laser Diode Driver
- FDX Return Path Amplifier

Ordering Information

Part Number	Description
RF2312SQ	Sample Bag with 25 pieces
RF2312SR	7” Reel with 100 pieces
RF2312TR13	13” Reel with 2500 pieces
RF2312PCK	5 – 725 MHz PCBA w 5-pc Sample Bag

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40 to +150 °C
Maximum Device Voltage (V_{DD})	6.3 V
Input RF Power	+18 dBm
Output Load VSWR	20 :1

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Device Voltage (V_{DD})		+5.5	+5.7	V
Ambient Operating Temperature	−40		+85	°C
Operating Current Range	40	100	120	mA
(Icc = 120mA, Pdiss=0.702W, Ta=85C) θ_{JC}		114.9		°C/W
(Icc = 100mA, Pdiss=0.555W, Ta=85C) θ_{JC}		114.1		°C/W
MTTF Ta=85°C, Pdiss=.702W		2170		years

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions		Min	Typ	Max	Units
Operational Frequency Range			5		725	MHz
Gain	At 300 MHz		14.5	15.5		dB
Noise Figure	From 10 –700 MHz, −45 to +85 °C			3.8	4.1	dB
Input Return Loss	Appropriate values for the DC blocking capacitors and bias inductor are required to maintain this Return Loss at the intended operating frequency range.	5MHz		18		dB
		300MHz		21		dB
		700MHz		22		dB
Output Return Loss	Appropriate values for the DC blocking capacitors and bias inductor are required to maintain this Return Loss at the intended operating frequency range.	5MHz		15		dB
		300MHz		27		dB
		700MHz		17		dB
Reverse Isolation				19		dB
Output IP3	At 7 MHz (2 Tone 5 dBm / Tone 1 MHz Spacing)			+45		dBm
Output IP3	At 300 MHz (2 Tone 5 dBm / Tone 6 MHz Spacing)			+42		dBm
Output IP3	At 700 MHz (2 Tone 5 dBm / Tone 6 MHz Spacing)			+36		dBm
Output IP2	At 5 MHz (2 Tone 3 dBm / Tone 6 MHz Spacing)			+61		dBm
Output IP2	At 300 MHz (2 Tone 3 dBm / Tone 6 MHz Spacing)			+59		dBm
Output IP2	At 700 MHz (2 Tone 3 dBm / Tone 6 MHz Spacing)			+50		dBm
Output P1dB	At 5 MHz			+22.8		dBm
Output P1dB	At 300 MHz			+22		dBm
Output P1dB	At 700 MHz			+20		dBm

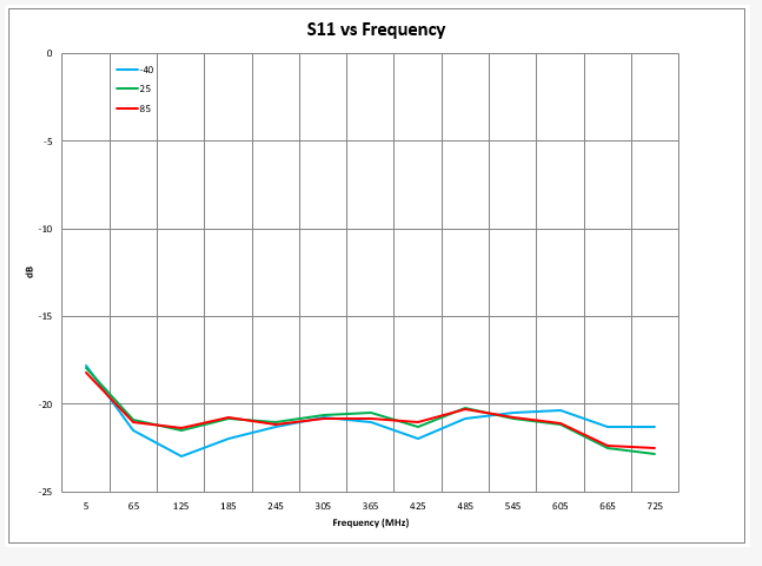
Notes:
Test conditions unless otherwise noted: V_{DD} = +9.0 V, Temp = +25°C in a 75Ω system.

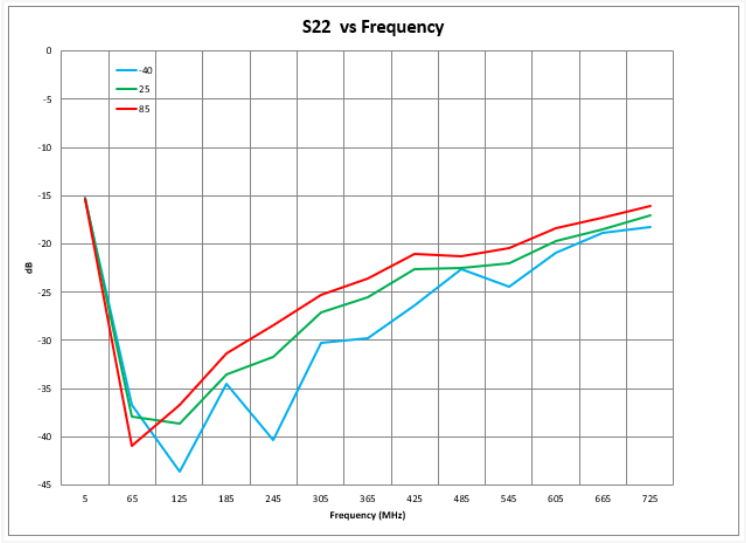
77 Channels

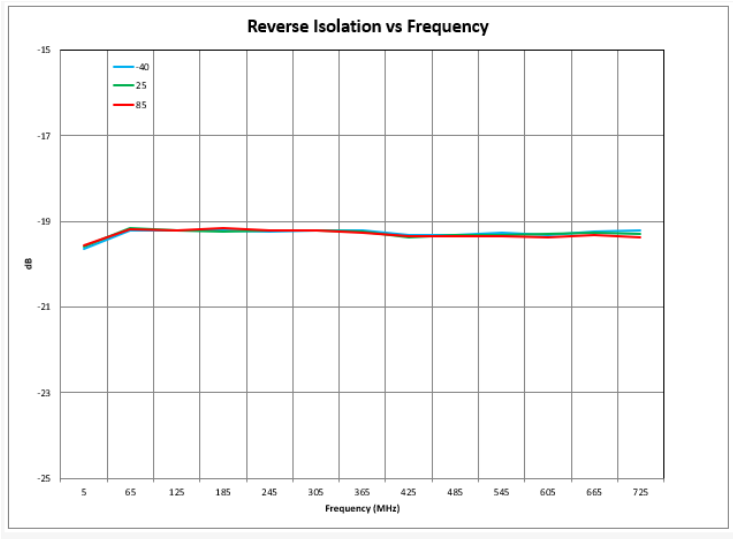
Parameter	Conditions	Min	Typical	Max	Units
	77 Channels to 550 MHz at 10 dBmV,				
CSO	61.25 MHz		>86		dBc
	83.25 MHz		>86		dBc
	193.25 MHz		76		dBc
	313.2625 MHz		72		dBc
	547.25 MHz		64		dBc
CTB	61.25 MHz		>86		dBc
	83.25 MHz		>86		dBc
	193.25 MHz		86		dBc
	313.2625 MHz		84		dBc
	547.25 MHz		83		dBc
CNR		65	66		dB

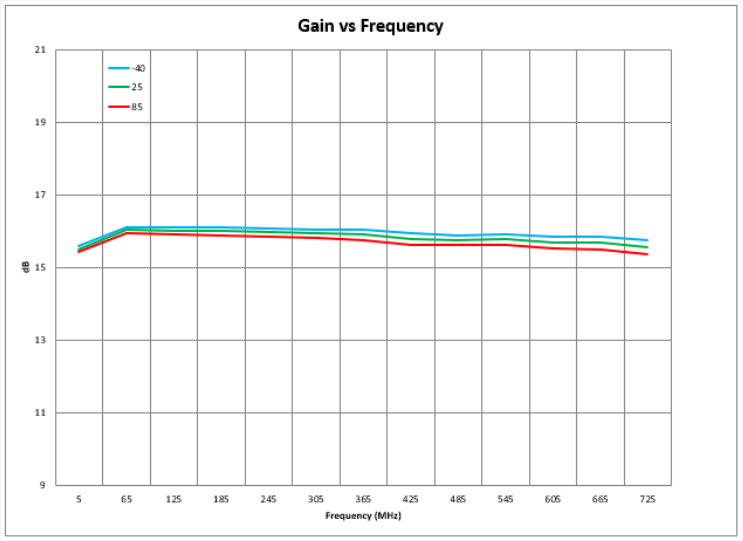
Performance Plots

Unless otherwise specified: V_{DD} = 9.0V in a 75Ω system.



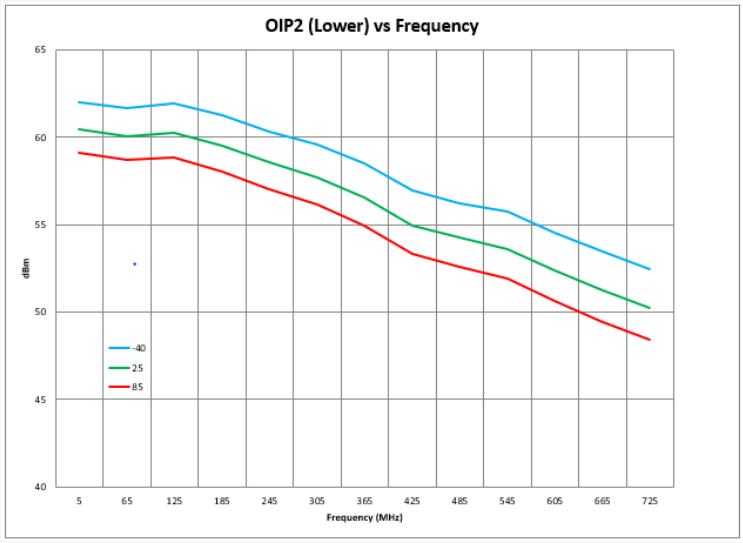


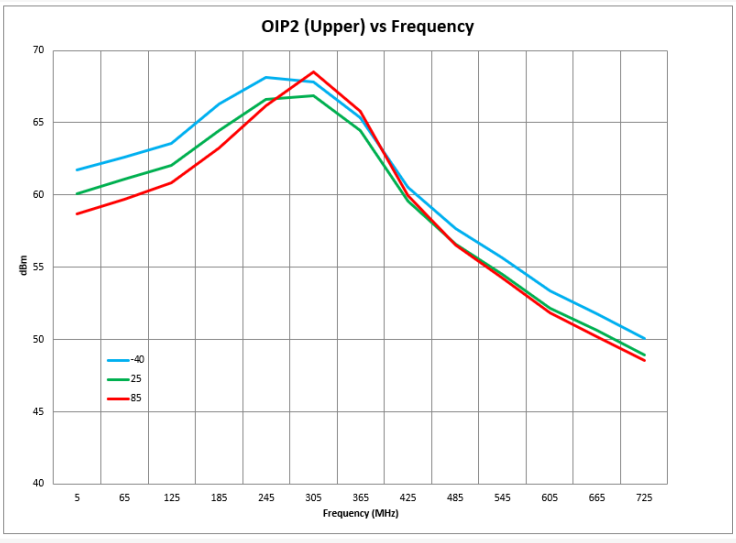


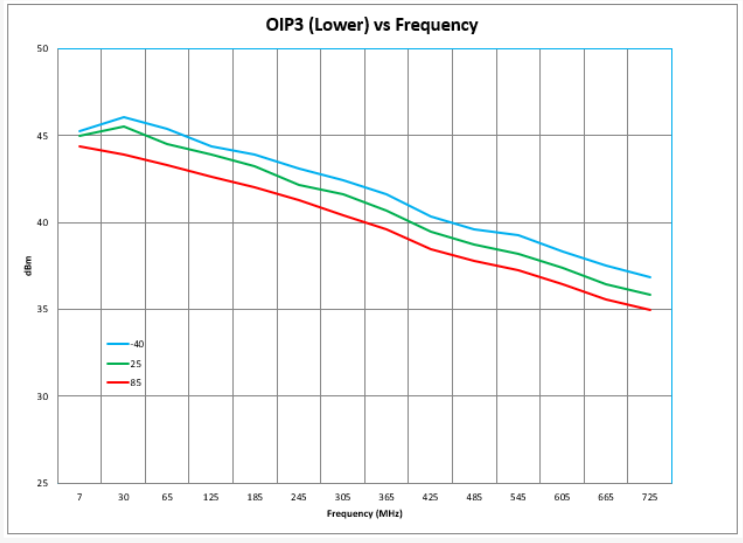


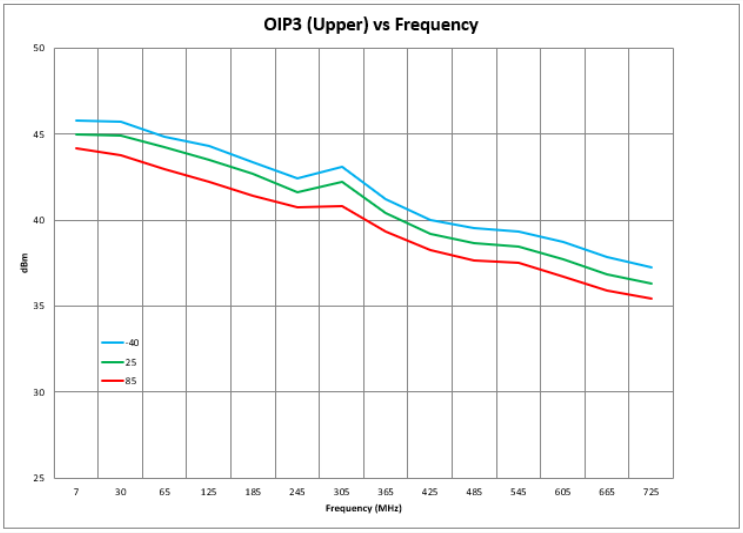
Performance Plots (Cont'd)

Unless otherwise specified: V_{DD} = 9.0V in a 75Ω system.



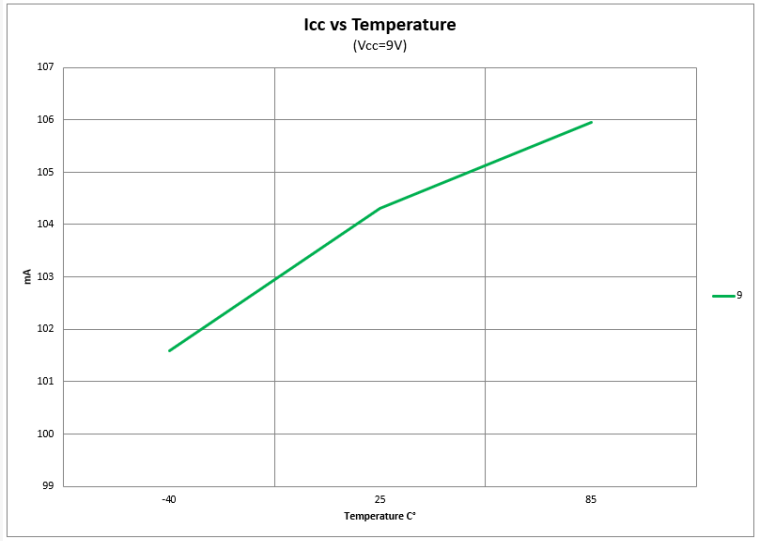


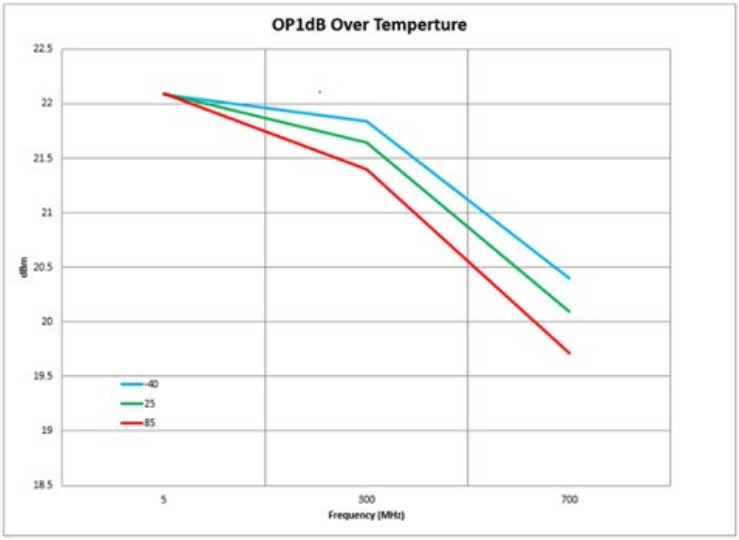


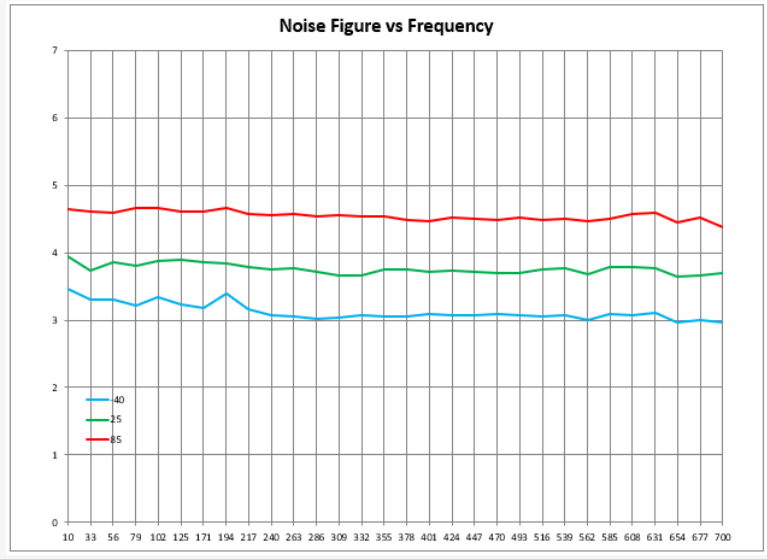


Performance Plots (Cont'd)

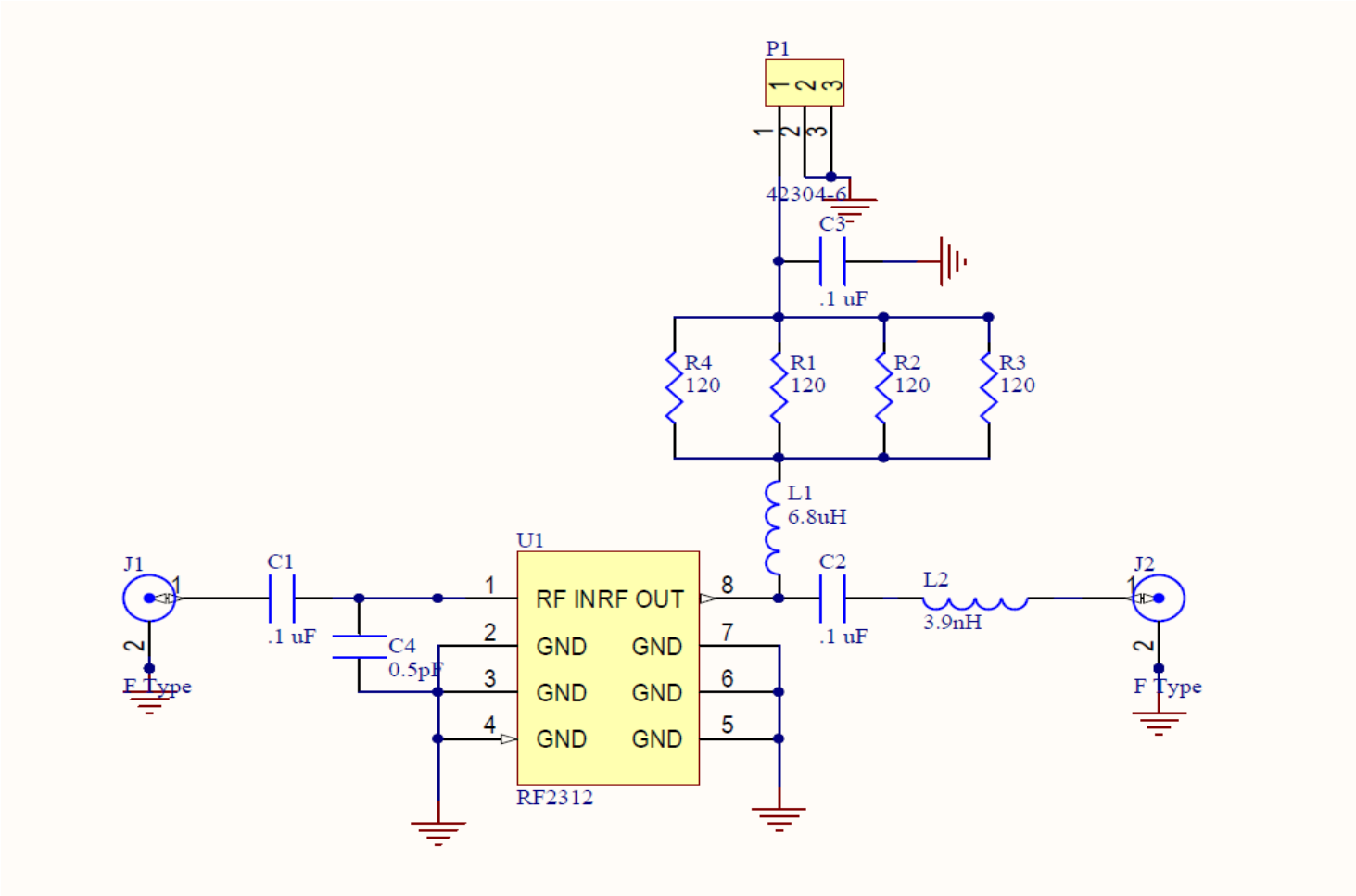
Unless otherwise specified: V_{DD} = 9.0V in a 75Ω system.







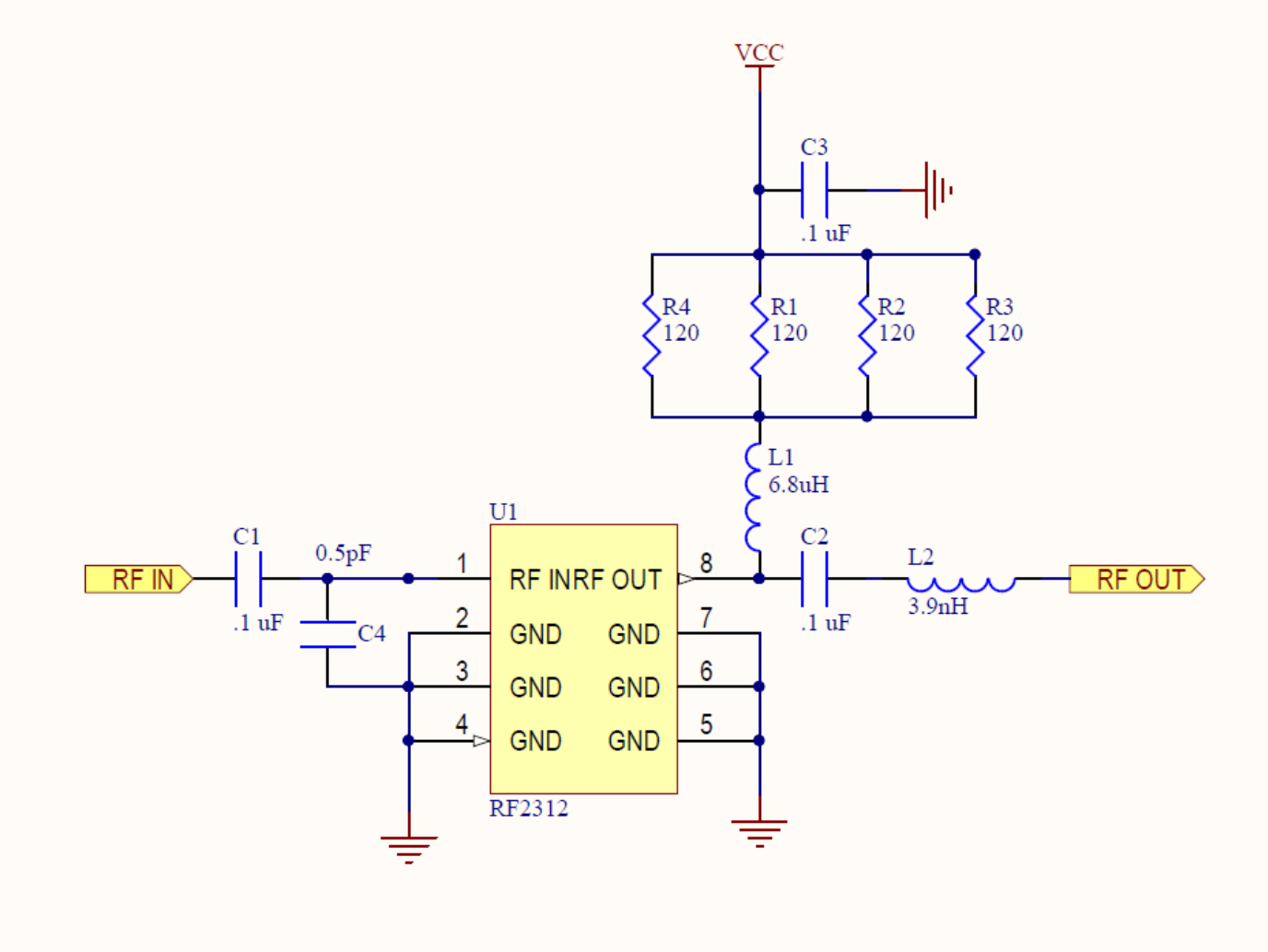
Evaluation Board Schematic



Bill of Material – RF2312

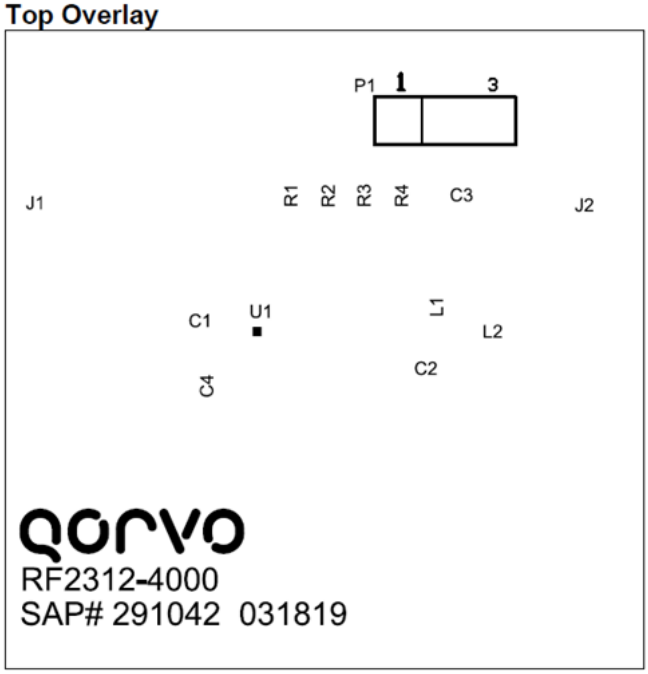
Reference Designator	Description	Manufacturer	Manufacturer PN
PCB	75Ω PCB, SW1012-410	Qorvo	
U1	15 dB 5 – 700 MHz Linear RF Amplifier	Qorvo	RF2312
C1, C2	CAP, 0.1 uF, X7R, 0603	Johanson Technology	250R14W104KV4T
C3	CAP, 0.1 uF, 5%, 25V, C0G, 1206	Murata Electronics	GRM31C5C1E104JA01L
C4	CAP, 0.5 pF, 25V, LF, 0402	AVX Asia Limited	04023J0R5ABSTR
L1	IND, 6.8 uH, 5%, W/W, 1008	Coilcraft, Inc.	1008LS-682XJLC
L2	IND, 3.9 nH, 130 mA, 0402	Murata Electronics	LQP15MN3N9B02D
R1, R2, R3, R4	RES, 121 Ω, 5%, 1/10W, 0805	Kamaya, Inc	RMC1/10-121JTP

Application Circuit Schematic

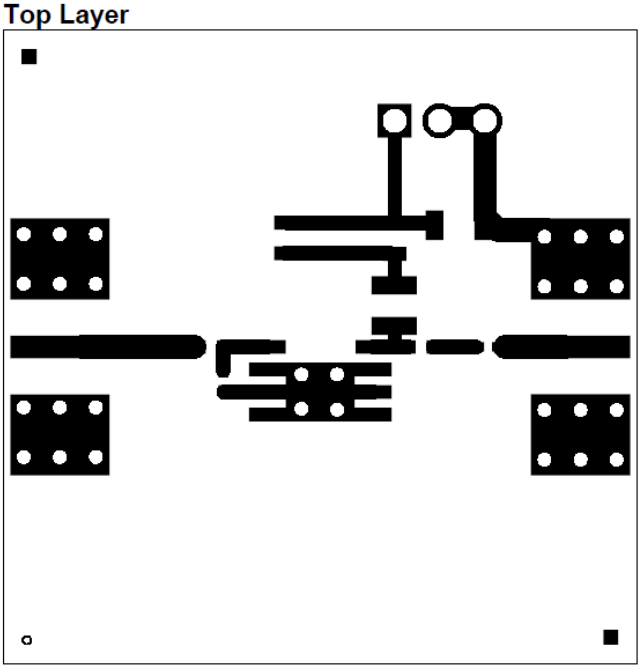


Evaluation Board Layout

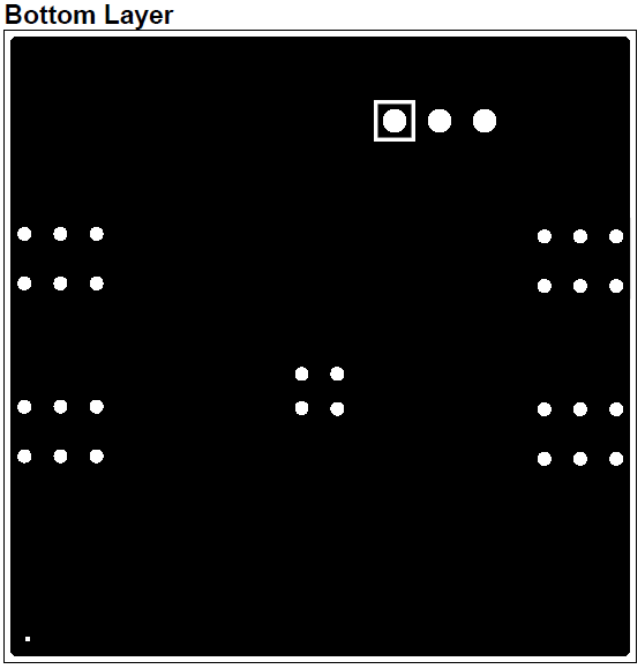
Top Overlay

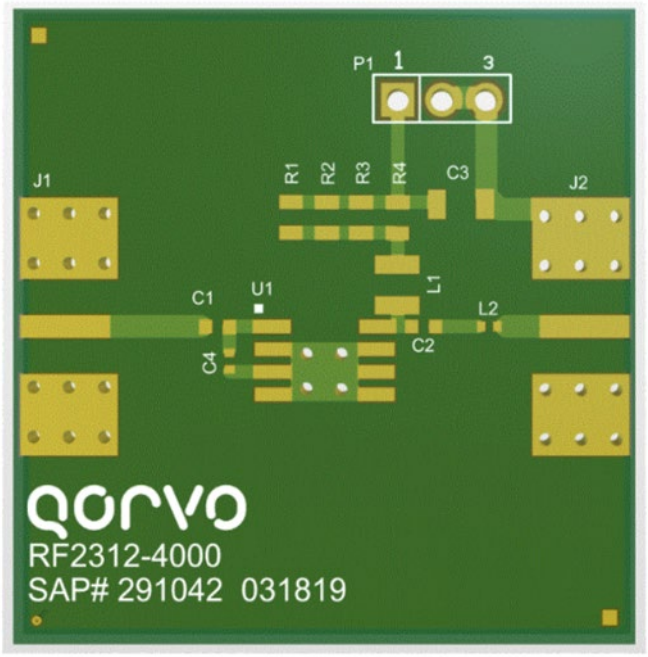


Top Layer

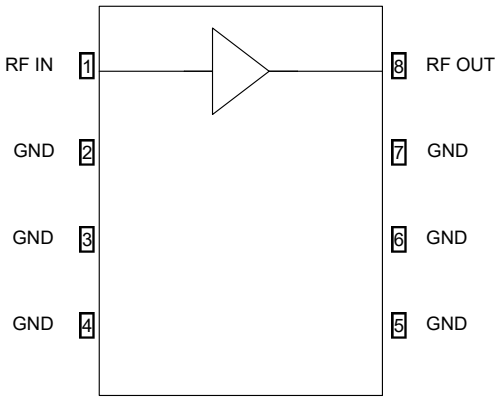


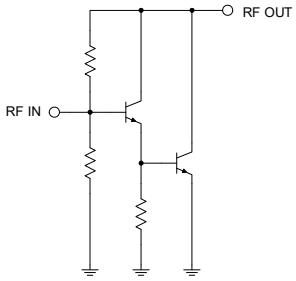
Bottom Layer





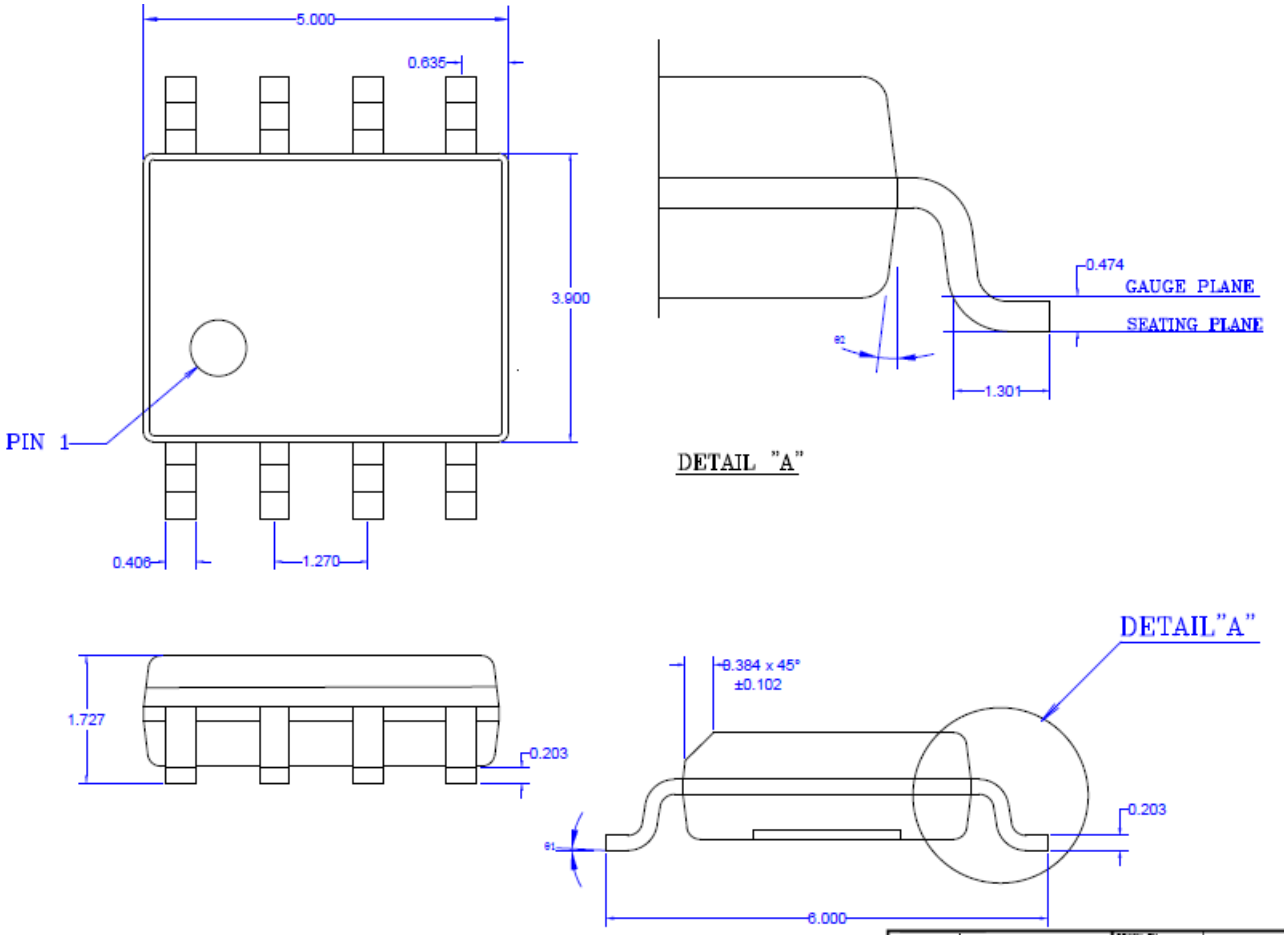
Pin Configuration and Description





Pin Number	Label	Description
1	RF IN	RF input pin. This pin is NOT internally DC-blocked. A DC-blocking capacitor, suitable for the frequency of operation, should be used in all applications. The device has internal feedback, and not using a DC blocking capacitor will disable the temperature compensation. The bias of the device can be controlled by this pin. Adding an optional 1kΩ resistor to ground on this pin reduces the bias level, which may be compensated for by a higher supply voltage to maintain the appropriate bias level. The net effect of this is an increased output power capability, as well as higher linearity for signals with high crest factors. DC-coupling of the input is not allowed, because this will override the internal feedback loop and cause temperature instability.
2	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane. Each ground pin should have a via to the ground plane.
3	GND	Same as pin 2
4	GND	Same as pin 2
5	GND	Same as pin 2
6	GND	Same as pin 2
7	GND	Same as pin 2
8	RF OUT	RF output and bias pin. Because DC is present on this pin, a DC-blocking capacitor, suitable for the frequency of operation, should be used in most applications. For biasing, an RF choke in series with a resistor is needed. The value for the resistor R_C is 30 Ω (0.5 W) for V_{CC}=9 V and 21 Ω for V_{CC} = 8 V. The DC voltage on this pin is typically 6.0 V with a current of 100 mA. In lower power applications the value of R_C can be increased to lower the current and V_D on this pin.

Package Marking and Dimensions



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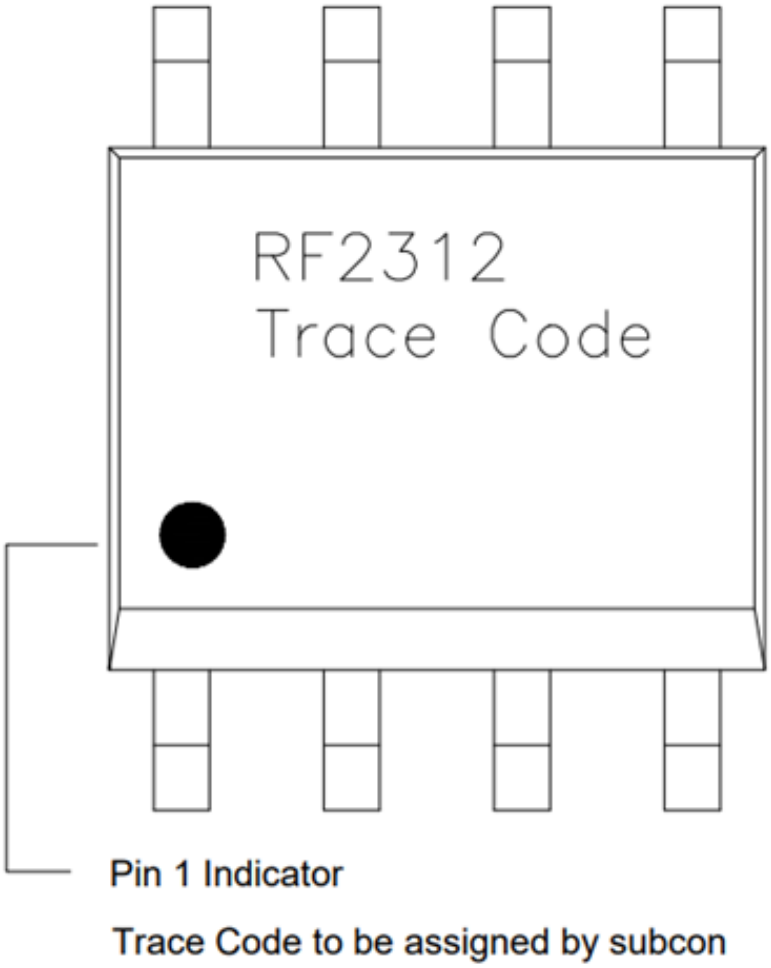
Notes:

1. All dimensions are in mm. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Branding Diagram



Trace Code to be assigned by subcon

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260 °C max. reflow temp.) soldering process.
Solder profiles available upon request.

Contact plating: Matte Sn

RoHS Compliance

This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free
- Qorvo Green

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: **1-844-890-8163**

Web: www.qorvo.com

Email: customer.support@qorvo.com

For technical questions and application information: **Email:** sjcapplications.engineering@qorvo.com

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