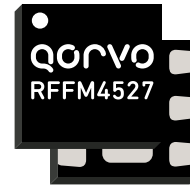


## Product Description

The RFFM4527 is a low noise amplifier (LNA) designed for Wi-Fi 802.11a/n/ac systems. The integrated input and output 50Ω match minimizes layout area in the customer's application, reduces the bill of materials and manufacturability cost. Performance is focused on a balance of low noise and gain that increases the receive sensitivity. The RFFM4527 integrates a bypass path that enables a defined gain step. The device is provided in a 1.6mm x 1.6mm x 0.5mm, 6-pin DFN package.



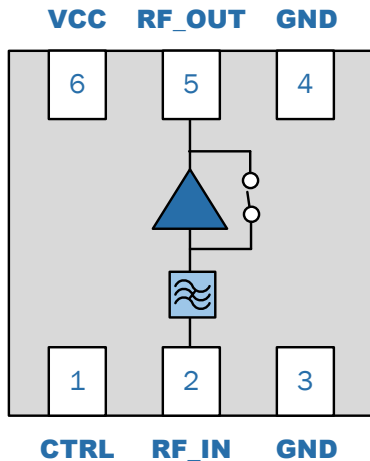
Package: DFN, 6-pin,  
1.6mm x 1.6mm x 0.5mm max

## Features

- Noise Figure = 1.6dB
- LNA Gain = 16dB
- Bypass Loss = 6dB
- Input and Output Matched to 50Ω
- Integrated 2.4GHz Rejection Filter

## Applications

- Wireless Routers
- Access Points
- Residential Gateways
- Consumer Premise Equipment
- Small Cell
- Internet of Things



Functional Block Diagram

## Ordering Information

PART NUMBER	DESCRIPTION
RFFM4527SB	Sample bag with 5 pieces
RFFM4527SQ	Sample bag with 25 pieces
RFFM4527SR	7" Reel with 100 pieces
RFFM4527TR7	7" Reel with 2500 pieces
RFFM4527PCK-410	Assembled Evaluation Board + 5 pieces

## Absolute Maximum Ratings

PARAMETER	RATING	UNIT
DC Supply Voltage (No RF Applied)	-0.3 to +6	V <sub>DC</sub>
Control Voltage	-0.5 to 6	V <sub>DC</sub>
DC Supply Current	50	mA
Storage Temperature	-40 to +150	°C
Maximum RX Input Power into 50Ω Load for 11a,n,ac (No Damage)	+10	dBm
Moisture Sensitivity	MSL2	

## Nominal Operating Parameters

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
<b>COMPLIANCE</b>					<b>802.11A, 802.11N, 802.11AC, 802.11P</b>
Operating Frequency	4.9		5.925	GHz	
Operating Temperature	-40		+85	°C	
Power Supply V <sub>DD</sub>	3	3.3	6	V	
Control Voltage-High	2.5	3	V <sub>DD</sub>	V	CTRL
Control Voltage-Low	0		0.5	V	CTRL

<b>LNA Mode</b>					<b>V<sub>DD</sub>=3.3V, T=+25°C; Unless otherwise noted</b>
Noise Figure		1.6	2.0	dB	
Small Signal Gain	14	17		dB	<i>f</i> = 5100MHz
	13	16		dB	<i>f</i> = 5900MHz
Gain Flatness	-0.2		+0.2	dB	Across any 80MHz Channel
Gain Variation	-1.6		+1.6	dB	T = -40 to 85°C
Out of Band Gain		-28		dB	<i>f</i> = 2400-2500MHz
Input Return Loss		8		dB	
Output Return loss		15		dB	
Output P <sup>1dB</sup>		+8		dBm	
Output IP3		+22		dBm	Two tone 5MHz spacing; P <sub>IN</sub> = -20dBm
RF_OUT to RF_IN (S12)		-28		dB	
RX Operating Current( I <sub>DD</sub> )		15	20	mA	

<b>Bypass Mode</b>					<b>V<sub>DD</sub>=3.3V, T=+25°C; Unless otherwise noted</b>
Small Signal Gain		-6		dB	
Gain Flatness Across any 80MHz Channel	-0.2		0.2	dB	
Out of Band Gain		-28		dB	<i>f</i> = 2400-2500MHz
Input Return Loss		12		dB	
Output Return loss		12		dB	
Input P <sup>1dB</sup>		+20		dBm	
Input IP3		+28		dBm	Two tone 5MHz spacing; P <sub>IN</sub> = +2dBm
RX Operating Current		20		µA	

## Nominal Operating Parameters (cont.)

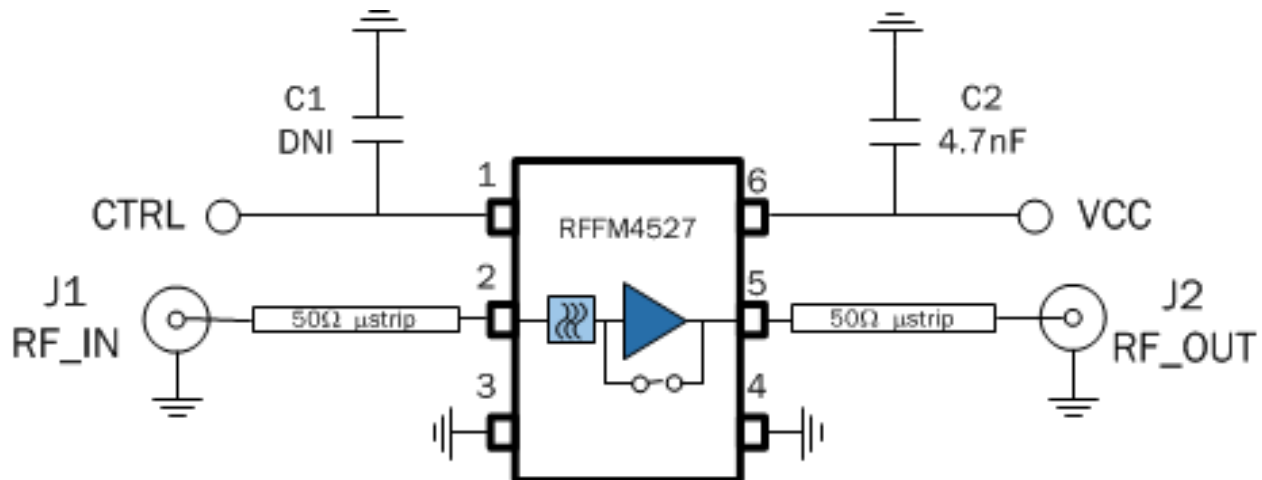
PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
<b>General Specifications</b>					
I <sub>CONTROL</sub> Current		150	200	μA	CTRL = High
		5		μA	CTRL = Low
Gain Switch Time - 50 to 90% RF Output		200		ns	Switching from Bypass to LNA mode
Gain Switch Time - 50 to 10% RF Output		200		ns	Switching from LNA Mode to Bypass

## Switch Control Logic Truth Table

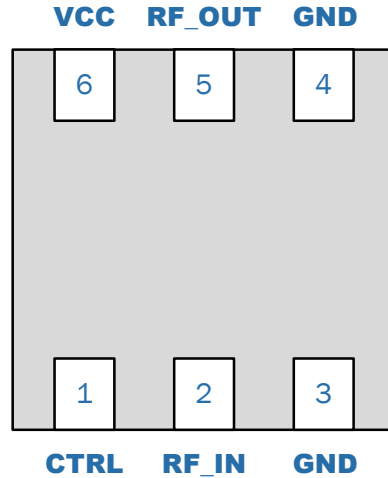
OPERATING MODE	CTRL
LNA Mode	High
Bypass Mode	Low

Note: High = 2.5 to V<sub>DD</sub>. Low = 0V to 0.5V.

## Evaluation Board Schematic



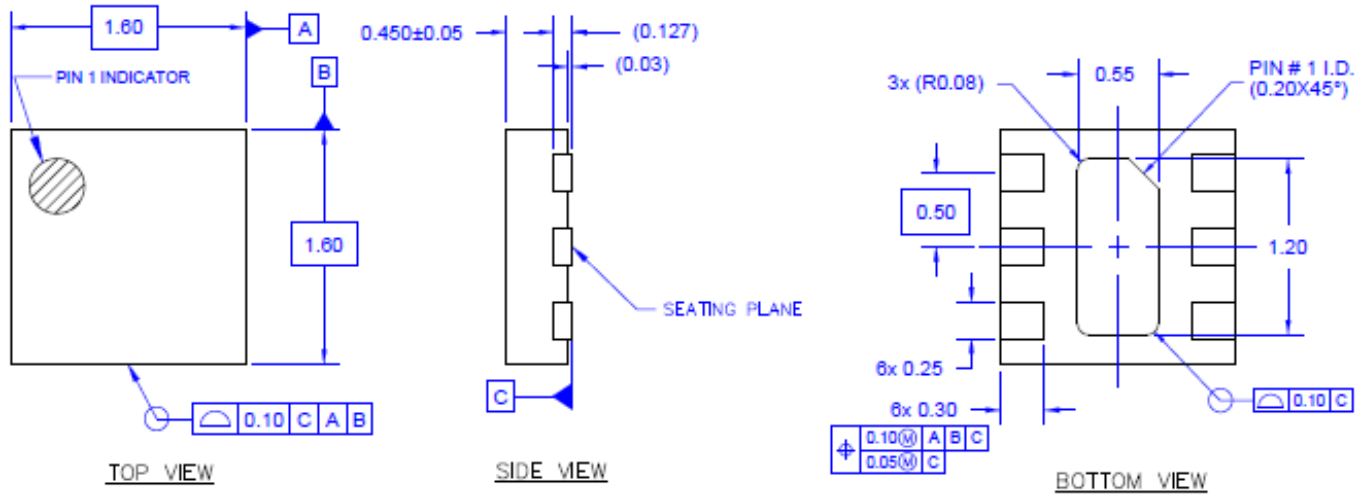
## Pin Out



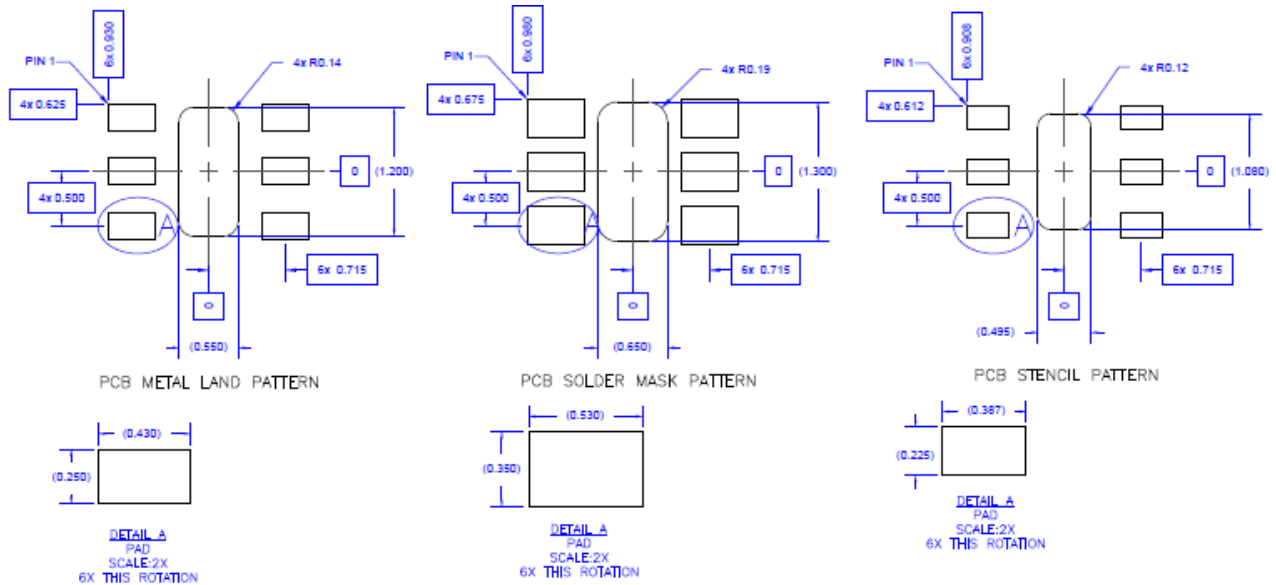
## Pin Names and Descriptions

PIN	NAME	DESCRIPTION
1	CTRL	Control voltage for switch to toggle LNA or Bypass modes.
2	RF_IN	RF input port. This port is matched to 50Ω and DC blocked.
3	GND	Not connected internally and can be left floating or connected to ground. Connecting this pin to ground is recommended.
4	GND	Not connected internally and can be left floating or connected to ground. Connecting this pin to ground is recommended.
5	RF_OUT	RF output port. This port is matched to 50Ω and DC blocked.
6	VCC	Supply voltage for LNA
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., PCB vias under the device are recommended.

Package Outline (Dimensions in millimeters)



PCB Pattern



Thermal vias for center slug should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, the power dissipation, and the electrical requirements. Example of the number and size of vias can be found on the evaluation board layout.

## Product Compliance Information

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Caution! ESD-Sensitive Device

### ESD Sensitivity Ratings

ESD Rating: Class 1C

Voltage: Passes  $\geq 1000V$  to  $< 2000V$   
Test: Human Body Model (HBM)  
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class C3

Voltage: Passes  $\geq 1000V$   
Test: Charged Device Model (CDM)  
Standard: JEDEC Standard JESD22-C101

### MSL Rating

MSL Rating: Level 2

Test:  $260^{\circ}C$  convection reflow  
Standard: JEDEC Standard IPC/JEDEC J-STD-020

### Solderability

Compatible with both lead-free ( $260^{\circ}C$  max. reflow temperature) and tin/lead ( $245^{\circ}C$  max. reflow temperature) soldering processes.

Package contact plating: NiPdAu

### RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free

## Contact Information

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For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:

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