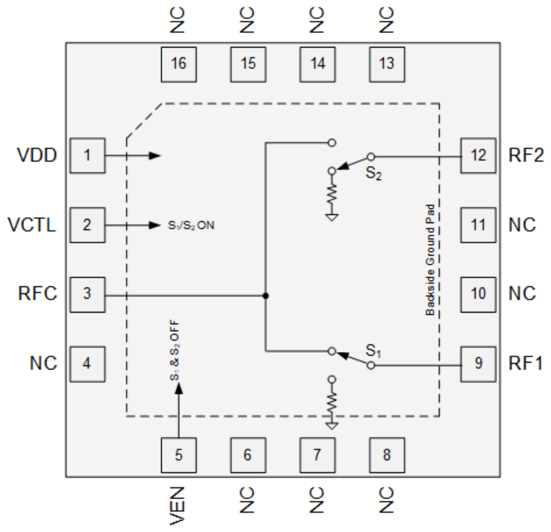
RFSW6024

5MHz to 6GHz Absorptive High Isolation SPDT Switch

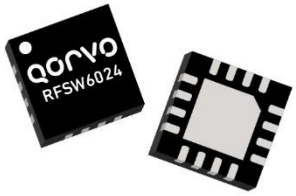
Product Overview

The RFSW6024 is a Silicon on Insulator (SOI) Single-Pole Double Throw (SPDT) switch designed for uses in cellular, 3G, LTE and other high-performance communication systems. It offers a high isolation, symmetric throw ports with excellent linearity and power handling capability. No DC blocking capacitors are necessary on the RF ports. The design is non-reflective as such the RF port 1 or RF port 2 is terminated in the non-throw state. The VEN enable pin allows the switch entering the “All OFF State”. The RFSW6024 is 1.8V positive logic compatible.

Functional Block Diagram



Top View



16 Pad 4 x 4 mm QFN Package

Key Features

- 5 – 6000 MHz Operation
- Symmetric SPDT
- Non-Reflective RF1 & RF2 Ports
- No Blocking Capacitors Necessary Unless DC Voltage on RF line
- High Isolation: 60 dB at 2 GHz
- High Input IP3: +66 dBm
- 1.8 V Logic Compatible

Applications

- Cellular, 3G, 4G, 5G Infrastructure
- WiBro, WiMax, LTE
- Wireless Backhaul
- High Performance Communication Systems
- Test Equipment

Ordering Information

Part No.	Description
RFSW6024TR13	2,500 pieces on a 13” reel (standard)
RFSW6024PCK-410	5 MHz – 6GHz Evaluation Board with 5-piece samples

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40 to +150 °C
RF Input Power, CW, 50 Ω, T=25 °C	+36 dBm
Device Voltage (VDD)	+6 V
Control Voltage (VCTL, VEN)	+6 V

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (VDD)	+2.5	+3.0	+5.5	V
T_{CASE}	−40		+105	°C
Tj for >10^6 hours MTTF			+125	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions (1)	Min	Typ	Max	Units
Operational Frequency Range		5		6000	MHz
Insertion Loss (2) (RFC to RF1/RF2)	0.3 GHz		0.55		dB
	1.0 GHz		0.60		dB
	2.0 GHz		0.75	1.00	dB
	3.0 GHz		0.90		dB
	4.0 GHz		0.90		dB
	5.0 GHz		1.10		dB
Isolation (RFC to RF1/RF2)	0.3 GHz		75		dB
	1.0 GHz		63		dB
	2.0 GHz	53	60		dB
	3.0 GHz		60		dB
	4.0 GHz		60		dB
	5.0 GHz		48		dB
Isolation (RF1 to RF2)	0.3 GHz		80		dB
	1.0 GHz		70		dB
	2.0 GHz	53	60		dB
	3.0 GHz		53		dB
	4.0 GHz		48		dB
	5.0 GHz		49		dB
Return Loss (RF1/RF2 ON-State)	0.3 GHz		28		dB
	1.0 GHz		27		dB
	2.0 GHz		20		dB
	3.0 GHz		20		dB
	4.0 GHz		22		dB
	5.0 GHz		17		dB
Return Loss (RF1/RF2 OFF-State)	0.3 GHz		37		dB
	1.0 GHz		36		dB
	2.0 GHz		30		dB
	3.0 GHz		27		dB
	4.0 GHz		23		dB
	5.0 GHz		20		dB

Electrical Specifications (Continue)

Parameter	Conditions (1)		Min	Typ	Max	Units
Operational Frequency Range			5		6000	MHz
Input IP3	1.0 GHz	+12 dBm input power per-tone, 1 MHz tone spacing	55	65		dBm
	2.0 GHz		55	65		dBm
Input 0.1 dB Compression Power	1.0 GHz			36		dBm
Input 1 dB Compression Power	1.0 GHz			36		dBm
Setting Time	50% VCTL to optimum functionality			1.5	3.0	μs
Start-up Time	90% VDD to full functionality			25	50	μs
Switching Time	50% control to 10/90% RF			250		ns
	50% control to 2/98% RF			360	600	ns
Supply Current (I_{DD})	VDD 5.0V			140	200	μA
Control Current, (I_{CTL}, I_{EN})	VCTL 5.0V			0.5	5.0	μA
Low Control Voltage (VCTL)	1.8 V Logic compatible		0		0.63	V
High Control Voltage (VCTL)			1.1		VDD	V

Notes:

1. Test conditions unless otherwise noted: VDD = +5.0 V, VCTL = 0/+5.0 V, Temp = +25 °C, 50 Ω system, RF ports DC Voltage 0V
2. PCB trace loss deducted

Maximum Operating Power at +85C, ≥300 MHz CW

Input Port	State	VEN	Power	Thermal Resistance, θ_{jc}
RFC, RF1 or RF2	ON	Low	33.0 dBm (1)	97 °C/W (2)
RFC	Both OFF & RFC Reflective	High	31.3 dBm	N/A
RF1 or RF2	OFF & Terminated (5)	Low or High	26.0 dBm	100 °C/W
RF1 and RF2	Both OFF & Terminated (5)	High	27.8 dBm (3)	65 °C/W

Notes:

1. Load VSWR ≤ 3:1; for higher load VSWR, the maximum Input power reduced to +30.5 dBm
2. Apply to resistive loss from the insertion loss not including mismatch loss
3. Total power on both RF1 and RF2 ports being driven simultaneously
4. For < 300 MHz, it is recommended to operate at least 4 dB below Input 1 dB Compression Power
5. Internally terminated

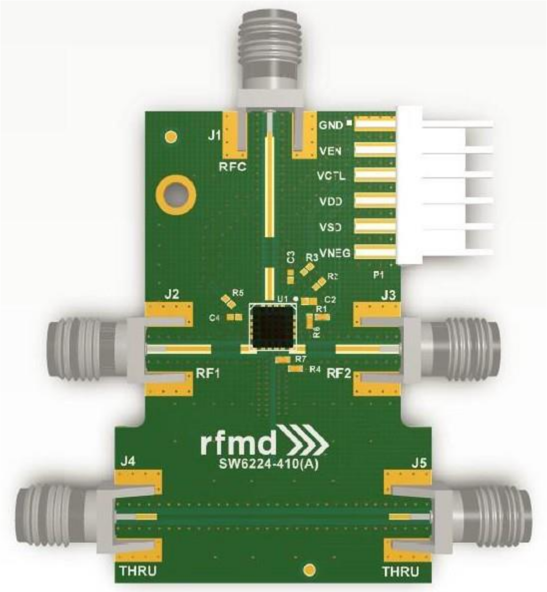
Truth Table

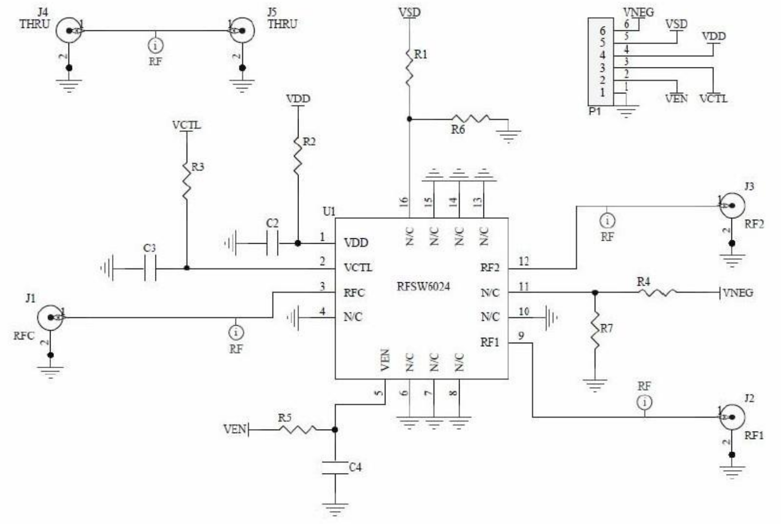
Control Input		Signal Path	
VCTL	VEN	RFC ⇆ RF1	RFC ⇆ RF2
0	0	OFF	ON
1	0	ON	OFF
0	1	OFF	OFF
1	1	OFF	OFF

Notes:

"0" = 0 V to 0.63 V; "1" = 1.1 V to VDD; VDD = 2.5 to 5.5 V must be applied for all valid states

5 MHz to 6 GHz Evaluation Board – RFSW6024PCK-410





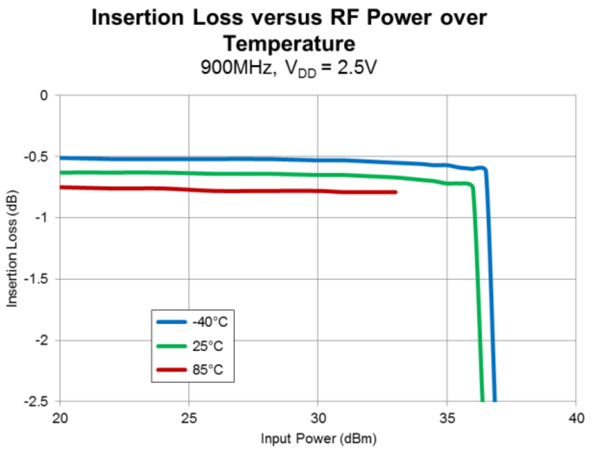
Bill of Material – RFSW6024PCK-410

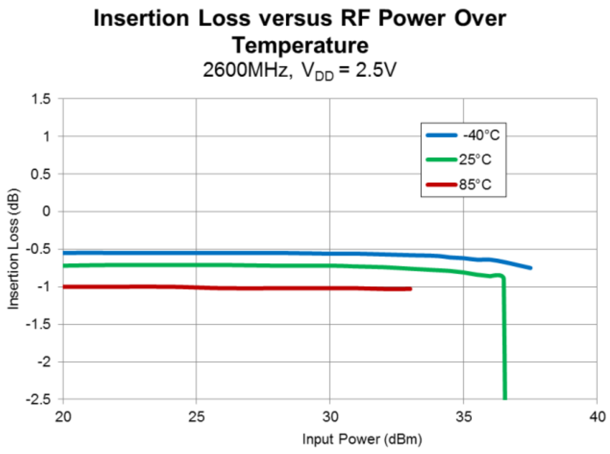
Reference Des.	Value	Description	Manuf.	Part Number
-	-	Printed Circuit Board	Qorvo	RFSW6224-410(A)
U1	-	SOI, High Isolation SPDT RF switch	Qorvo	RFSW6024
C2, C3, C4 (1)	100 pF	CAP, 100 pF, 5%, 50V, C0G, 0402	Taiyo Yuden	RM UMK105 CG101JV-F
R2, R3, R5, R6, R7	0 Ω	RES, 0 Ω, 50 Ω Max. Lead Free, 0402	KOA	RK73Z1ETTP
J1, J2, J3, J4, J5	SMA	CONN, SMA, EL, Mini FLT 0.068”, SPE-000303	Aliner	20-001CF-T
P1	-	CONN, HDR, ST, PLRZD, 6-Pin, 0.100”	AMP	640454-6

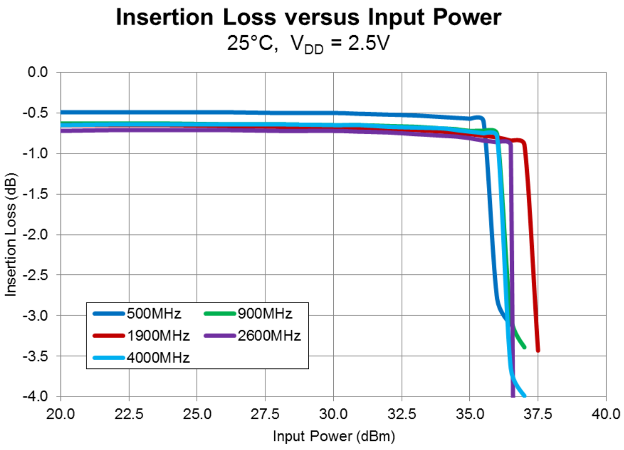
Note:
1. Optional

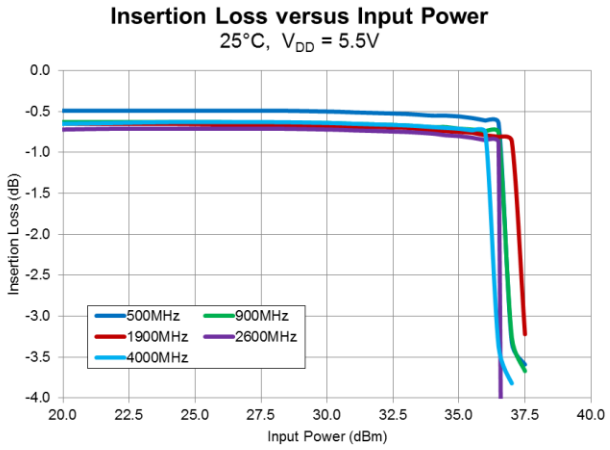
Performance Plots – RFSW6024PCK-410

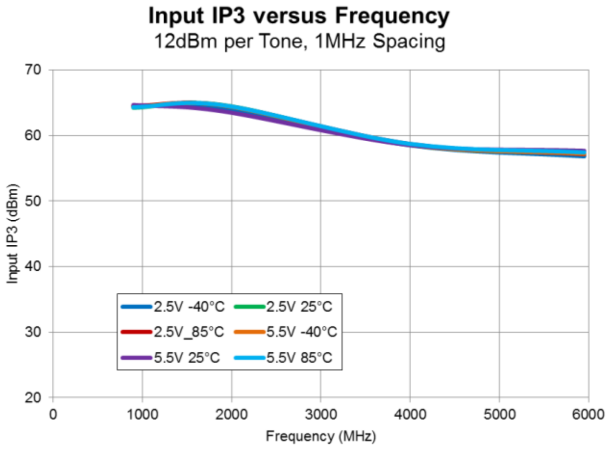
Test conditions unless otherwise noted: VDD = +3.0 V, Temp.=+25 °C

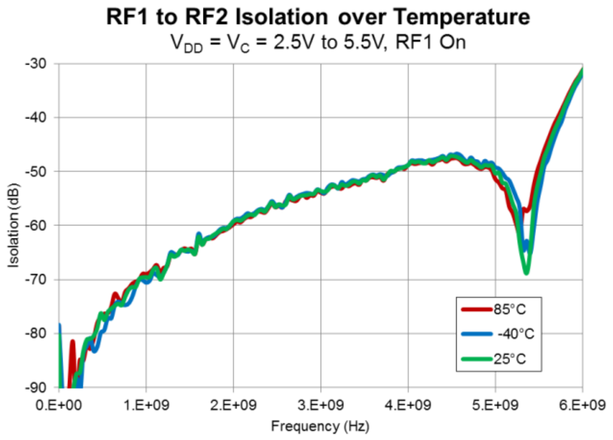

Insertion Loss versus RF Power over Temperature
900MHz, V_{DD} = 2.5V


Insertion Loss versus RF Power Over Temperature
2600MHz, V_{DD} = 2.5V


Insertion Loss versus Input Power
25°C, V_{DD} = 2.5V


Insertion Loss versus Input Power
25°C, V_{DD} = 5.5V

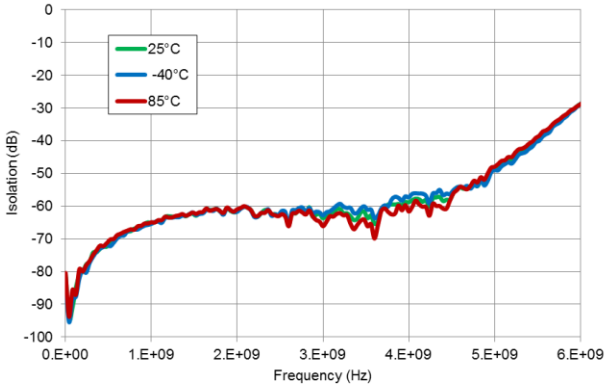

Input IP3 versus Frequency
12dBm per Tone, 1MHz Spacing


RF1 to RF2 Isolation over Temperature
V_{DD} = V_C = 2.5V to 5.5V, RF1 On

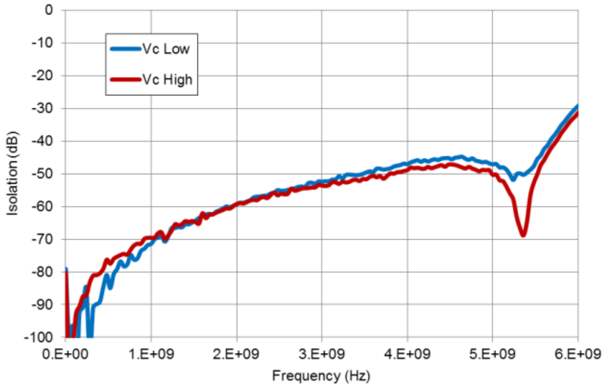
Performance Plots – RFSW6024PCK-410 (Continue 1)

Test conditions unless otherwise noted: VDD = +3.0 V, Temp.=+25 °C

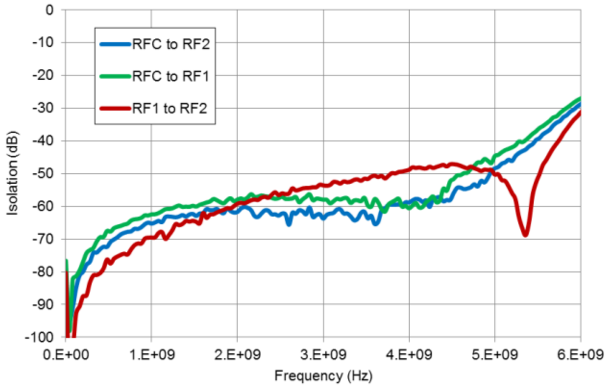
RFC to RF2 Isolation over Temperature
V_{DD} = V_C = 2.5V to 5.5V, RF1 On



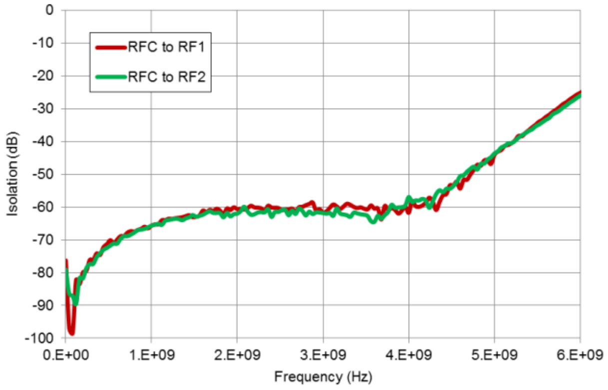
RF1 to RF2 Isolation
25°C, V_{DD} = 2.5V to 5.5V



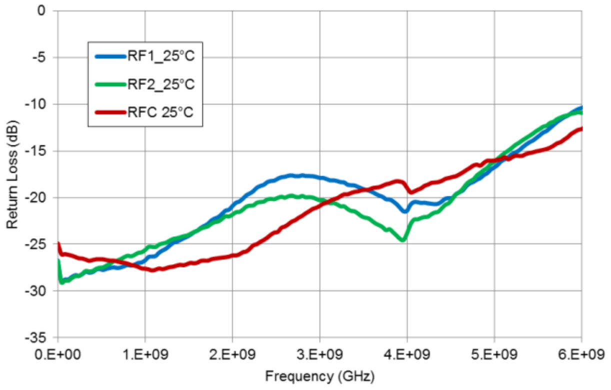
Isolation versus Frequency
25°C, V_{DD} = 2.5V to 5.5V, V_C = 0V/V_{DD}



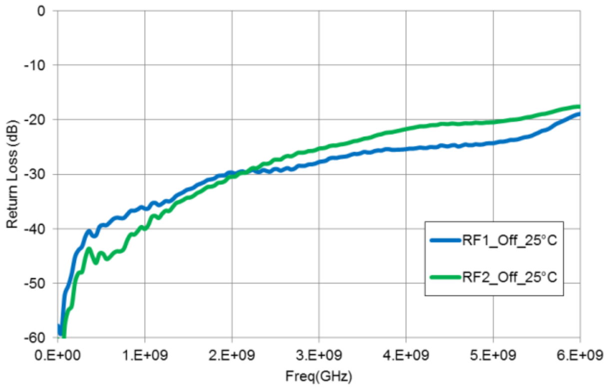
Isolation During All Off State
25°C, V_{DD} = V_{EN} = V_C = 2.5V to 5.5V



Return Loss versus Frequency
On-State, 25°C

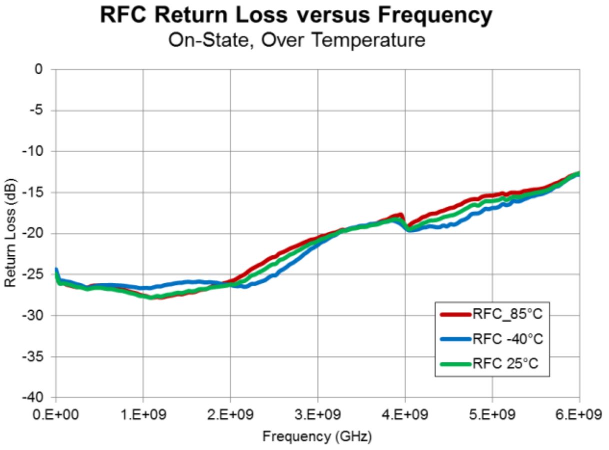


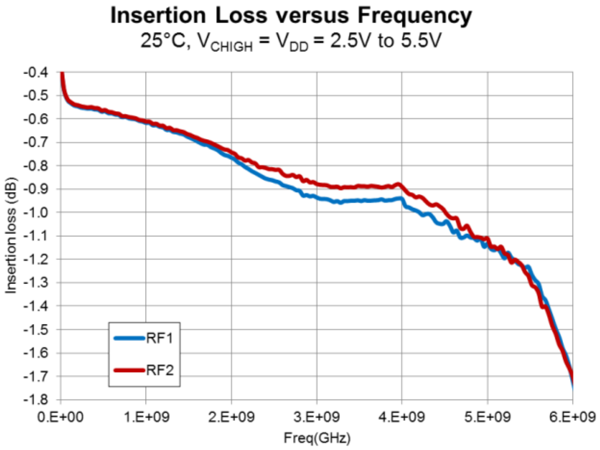
Return Loss versus Frequency
Off-State, Internal Load, 25°C

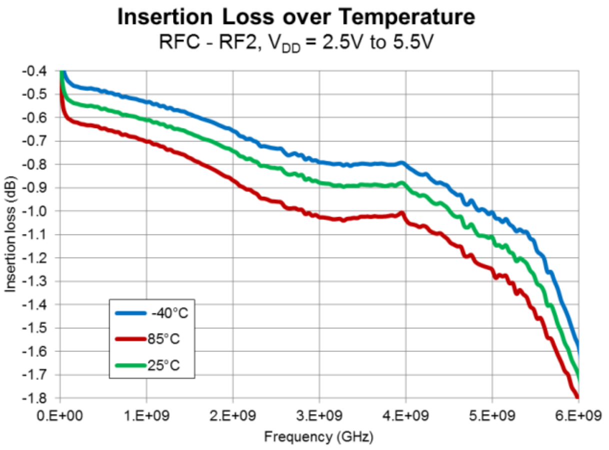


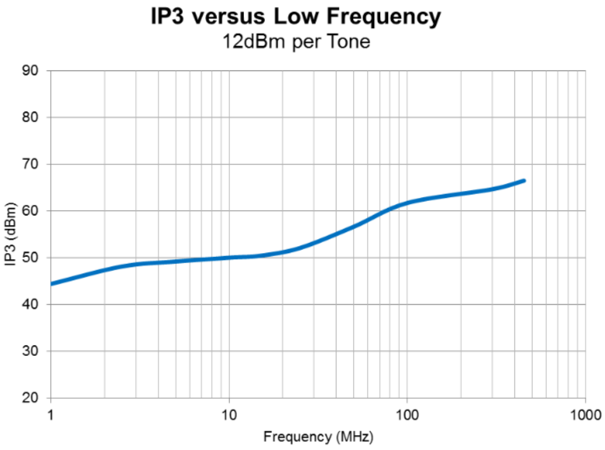
Performance Plots – RFSW6024PCK-410 (Continue 2)

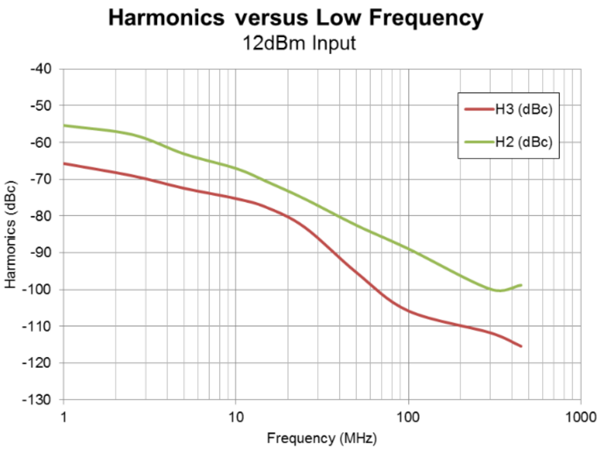
Test conditions unless otherwise noted: VDD = +3.0 V, Temp.=+25 °C

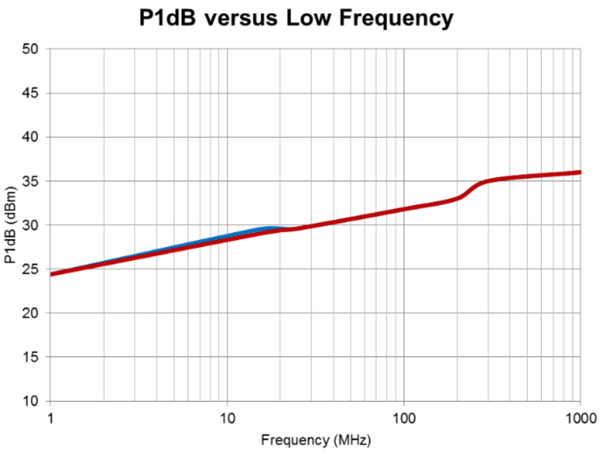

RFC Return Loss versus Frequency
On-State, Over Temperature


Insertion Loss versus Frequency
25°C, V_{CHIGH} = V_{DD} = 2.5V to 5.5V


Insertion Loss over Temperature
RFC - RF2, V_{DD} = 2.5V to 5.5V

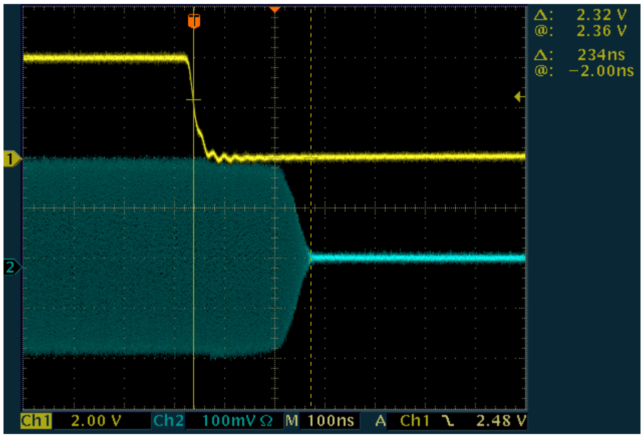

IP3 versus Low Frequency
12dBm per Tone


Harmonics versus Low Frequency
12dBm Input

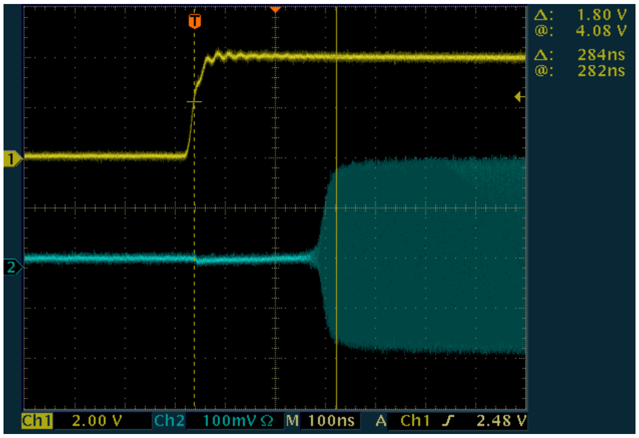

P1dB versus Low Frequency

Switching Time Plots

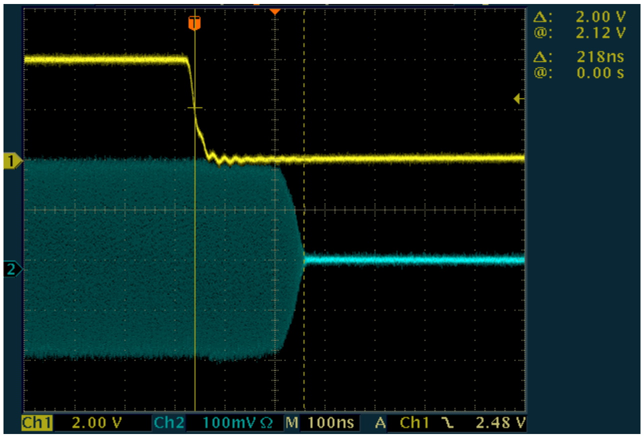
Swithing Time (t_{OFF}) = 234ns, 50% VCTL to 10% RF, +85°C



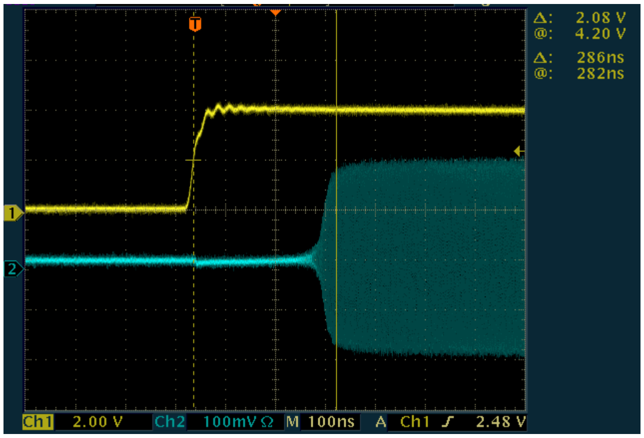
Swithing Time (t_{ON}) = 284ns, 50% VCTL to 90% RF, +85°C



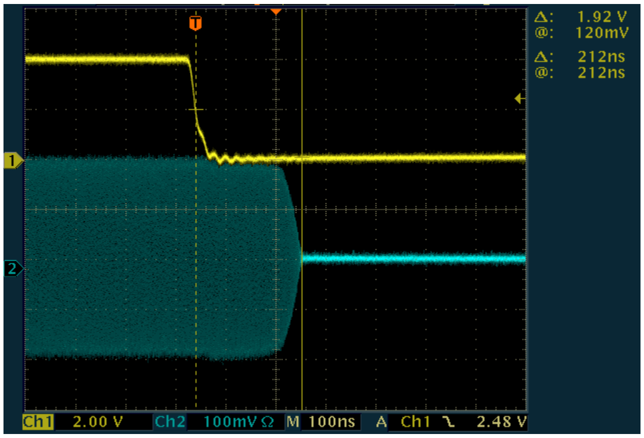
Swithing Time (t_{OFF}) = 218ns, 50% VCTL to 10% RF, +25°C



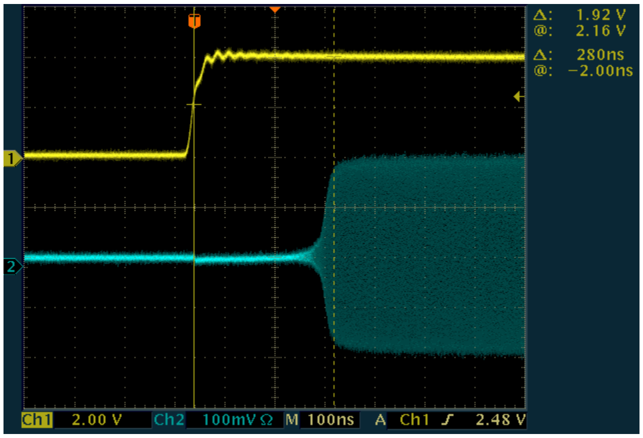
Swithing Time (t_{ON}) = 286ns, 50% VCTL to 90% RF, +25°C



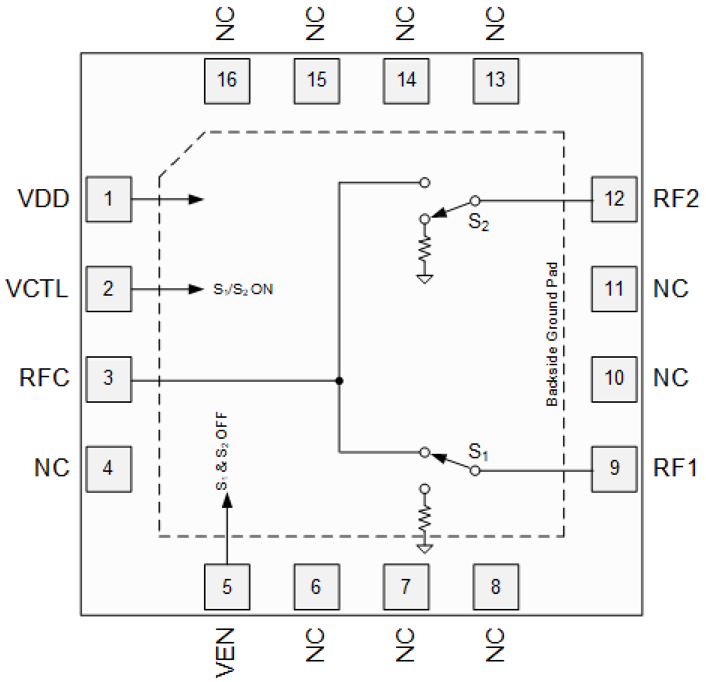
Swithing Time (t_{OFF}) = 212ns, 50% VCTL to 10% RF, -40°C



Swithing Time (t_{ON}) = 280ns, 50% VCTL to 90% RF, -40°C



Pad Configuration and Description

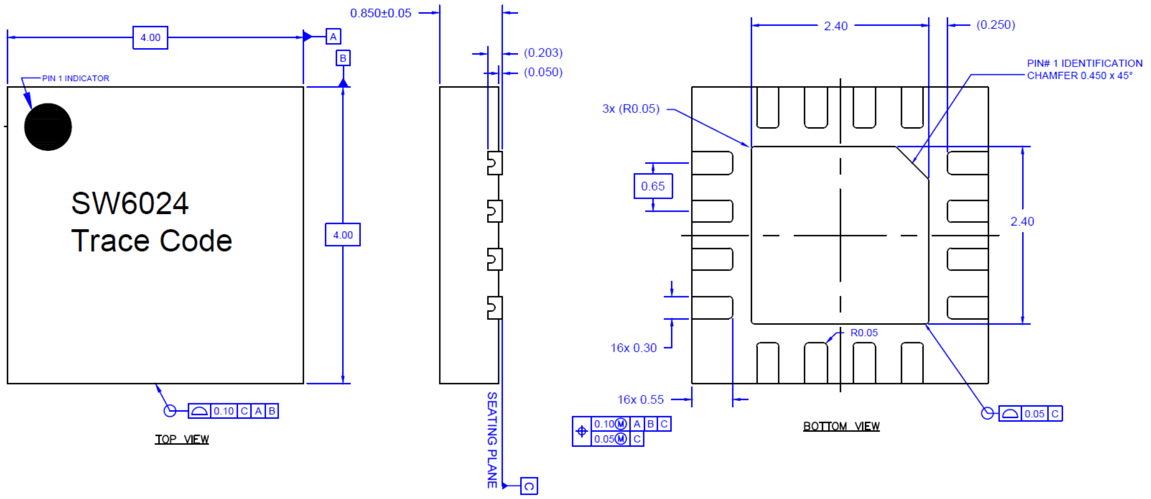


Top View

Pad No.	Label	Description
1	VDD	DC Supply Voltage Input
2	VCTL	Logic Control Input, Logic High/Low sets the switch RFC-RF1/RF2 to “ON” state
3	RFC	RF Common Port, DC blocking capacitor required if > 0.5 V external voltage is present
4, 8, 13, 16	NC	No Internal Connection, External connection to PCB Ground Recommended to maximize isolation
5	VEN	Logic Control Input, Logic High sets the switch both RF1 and RF2 to “OFF” state
6, 7, 10, 11, 14, 15	NC	Ground or No Connection, External connection to PCB Ground Recommended to maximize isolation
9	RF1	RF Port 1, DC blocking capacitor required if > 0.5 V external voltage is present
12	RF2	RF Port 2, DC blocking capacitor required if > 0.5 V external voltage is present
Backside Paddle	GND	RF and DC ground. Must be soldered on PCB ground plane over a bed of via holes to minimize inductance and thermal resistance

Package Marking and Dimensions

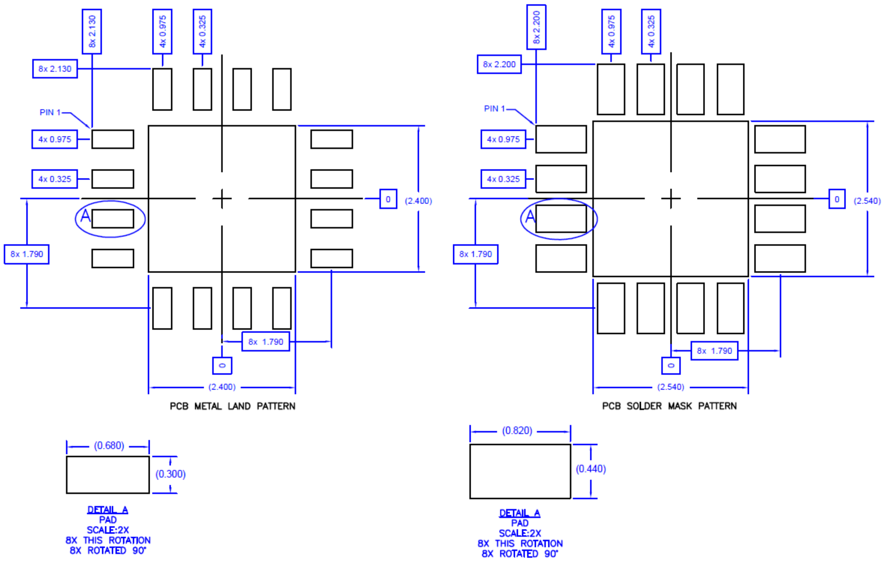
Marking: Part Number – SW6024
Trace Code – Assigned by subcontractor



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Contact plating: NiPdAu

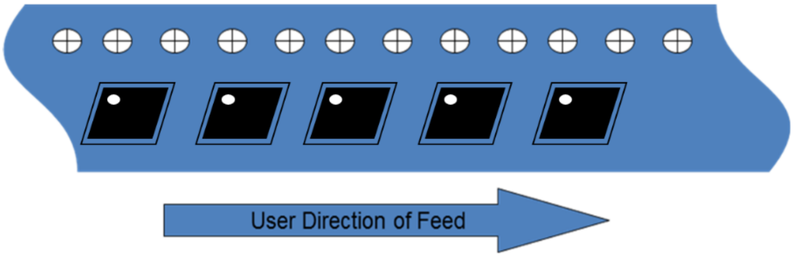
PCB Mounting Pattern

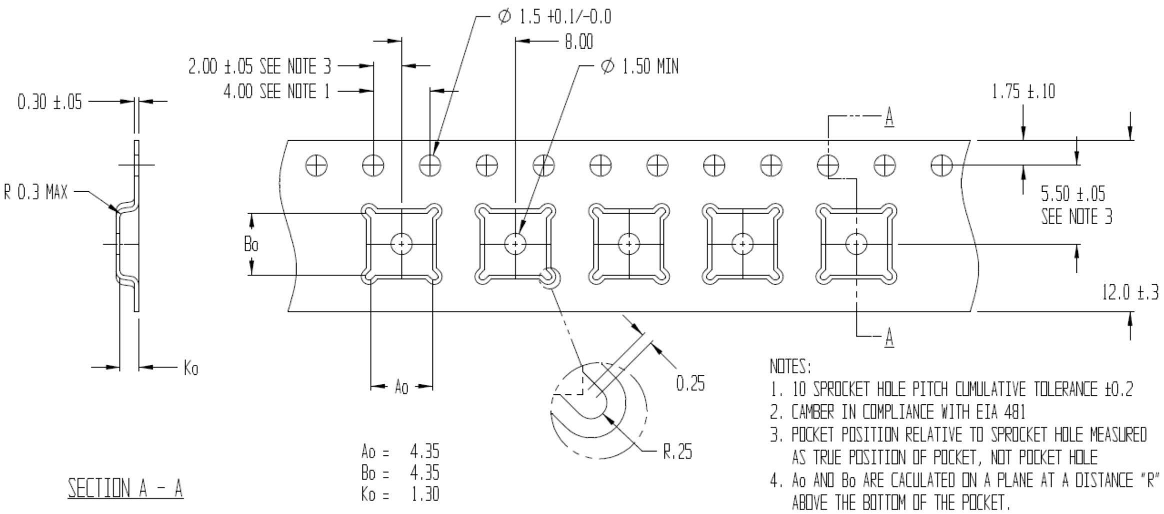


Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Tape and Reel Information – Carrier and Cover Tape Dimensions



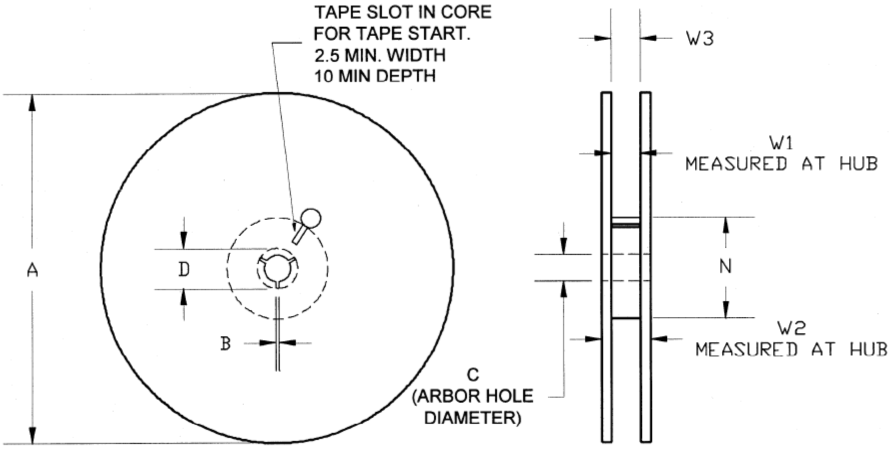


NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
4. Ao AND Bo ARE CACULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.171	4.35
	Width	B0	0.171	4.35
	Depth	K0	0.051	1.30
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.0

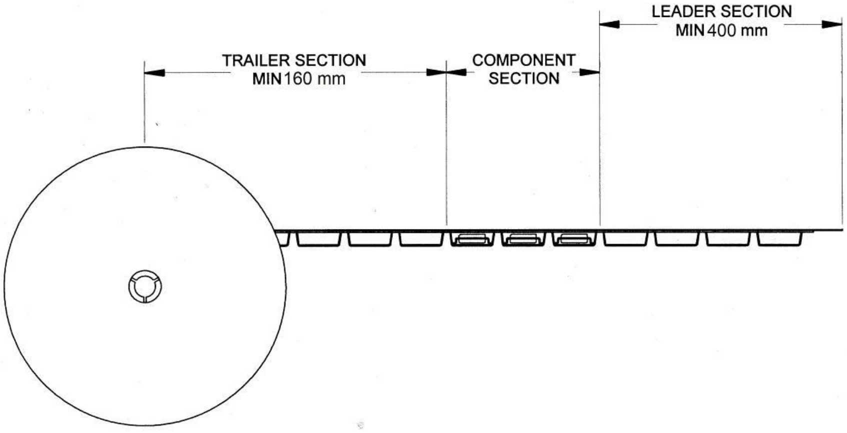
Tape and Reel Information – Reel Dimensions

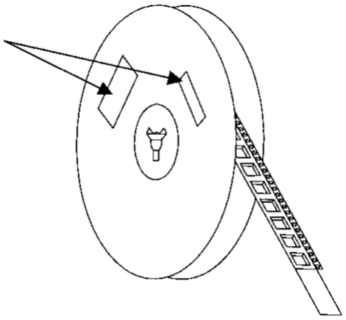
Standard T/R size = 2,500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement





Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 2	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 2	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

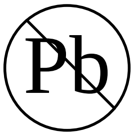
Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com
Tel: **1-844-890-8163**
Email: customer.support@qorvo.com

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