TGA2216-SM

0.1–3.0 GHz 10 W GaN Power Amplifier

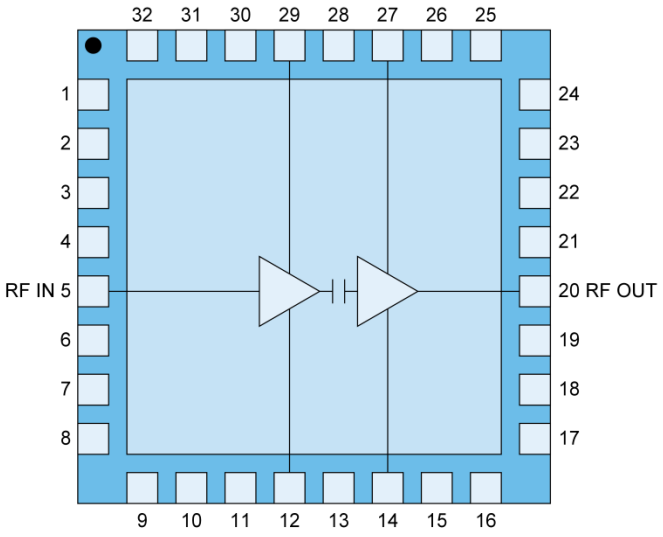
Product Overview

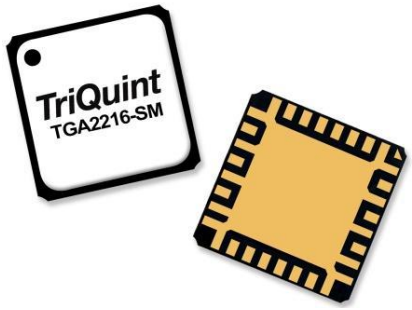
Qorvo's TGA2216-SM is a wideband cascode amplifier fabricated on Qorvo's production 0.25 um GaN on SiC process. The cascode configuration offers exceptional wideband performance as well as supporting 40 V operation. The TGA2216-SM operates from 0.1–3.0 GHz and provides greater than 10 W of saturated output power with greater than 13 dB of large signal gain and greater than 40% power-added efficiency.

The TGA2216-SM is available in a low-cost, surface mount 32 lead 5 x 5 AIN QFN. It is ideally suited to support both radar and communication applications across defense and commercial markets as well as electronic warfare. The TGA2216-SM is fully matched to 50Ω at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.

Lead-free and RoHS compliant.

Functional Block Diagram





Key Features

- Frequency Range: 0.1–3.0 GHz
- P_{SAT}: >40 dBm at PIN = 27 dBm
- P1dB: >35 dBm
- PAE: 50% @ midband
- Large Signal Gain: >13 dB
- Small Signal Gain: 21 dB
- Bias: V_D = 40 V, I_{DQ} = 360 mA, V_{G1} = -2.4 V Typical, V_{G2} = +17.7 V Typical
- Wideband Flat Gain and Power
- Package Dimensions: 5.0 x 5.0 x 1.45 mm

Applications

- Commercial and Military Radar
- Communications
- Electronic Warfare

Ordering Information

Part	Description
TGA2216-SM	0.1–3.0 GHz 10 W GaN Power Amplifier
TGA2216-SMTR13	1000 pcs. on 13 inch reel
TGA2216-SMEVBP01	Evaluation Board

Absolute Maximum Ratings

Parameter	Value/Range
Drain Voltage (V_D)	80 V
Gate Voltage Range (V_{G1})	-8 to 0 V
Gate Voltage Range (V_{G2})	0 to 40 V
Drain Current (I_D)	760 mA
Gate Current (I_{G1})	-5 to 5.6 mA
Gate Current (I_{G2})	-5 to 5.6 mA
Power Dissipation (P_{DISS}), 85 °C	28 W
Input Power (P_{IN}), CW, 50 Ω, 85 °C,	33 dBm
Input Power (P_{IN}), CW, VSWR 10:1, V_D = 40 V, 85 °C	27 dBm
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value/Range
Drain Voltage (V_D)	40 V
Drain Current (I_{DQ})	360 mA
Gate Voltage (V_{G1})	-2.4 V (Typ.)
Gate Voltage (V_{G2})	+17.7 V (Typ.)

Electrical Specifications

Test conditions unless otherwise noted: 25 °C, V_D = 40 V, I_{DQ} = 360 mA, V_{G1} = −2.4 V Typical, V_{G2} = +17.7 V Typical

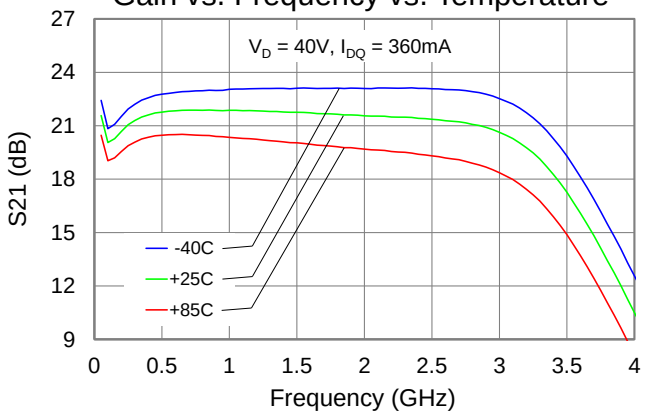
Parameter	Min	Typ	Max	Units
Operational Frequency Range	0.1		3.0	GHz
Small Signal Gain		21		dB
Input Return Loss		> 8		dB
Output Return Loss		> 11		dB
Output Power (P_{IN} = 27 dBm)		> 40		dBm
Power Added Efficiency (P_{IN} = 27 dBm)		50 (mid band)		%
Power @ 1 dB Compression (P1 dB)		> 35		dBm
IM3 @ 120 mA, P_{OUT}/tone = 30 dBm		−25		dBc
IM5 @ 120 mA, P_{OUT}/tone = 30 dBm		−33		dBc
Gate Leakage (V_D = 10 V, V_{G1} = −3.7 V, V_{G2} = 17.7 V)	−5.28			mA
Small Signal Gain Temperature Coefficient		−0.03		dB/°C
Output Power Temperature Coefficient		−0.007		dBm/°C
Recommended Operating Voltage:		40	48	V

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

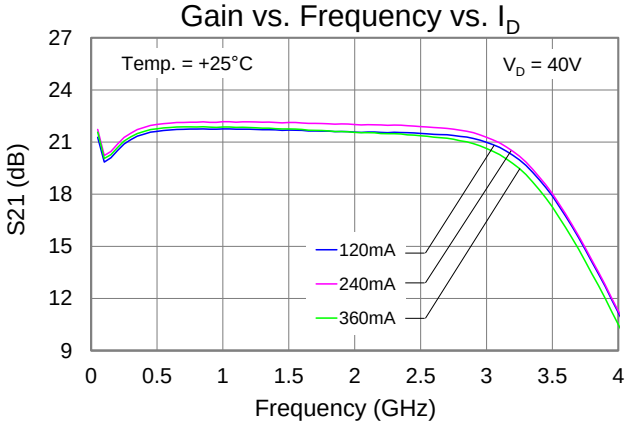
Typical Performance: Small Signal

The plots reflect performance measured with an external coaxial bias tee and DC blocks (See application circuit on page 11)

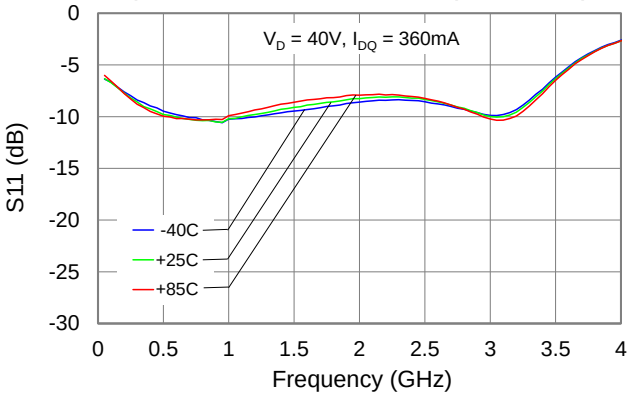
Gain vs. Frequency vs. Temperature



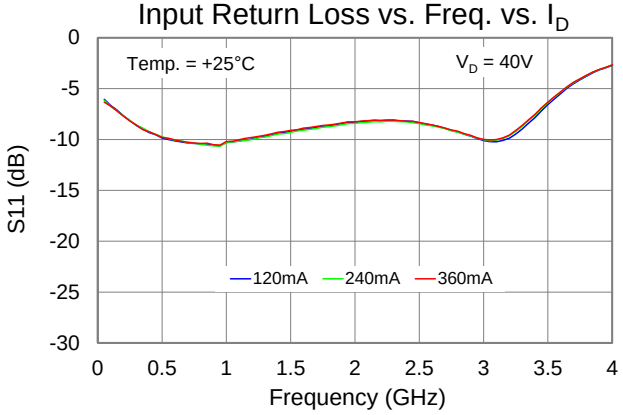
Gain vs. Frequency vs. I_D



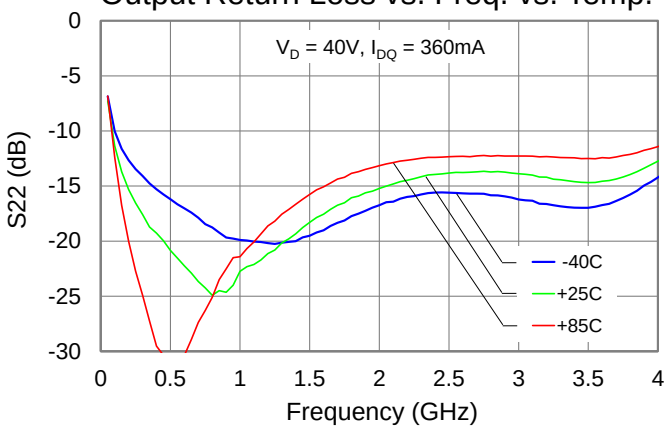
Input Return Loss vs. Freq. vs. Temp.



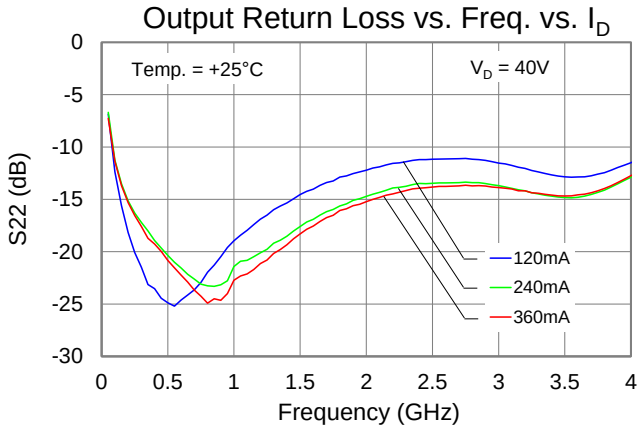
Input Return Loss vs. Freq. vs. I_D



Output Return Loss vs. Freq. vs. Temp.

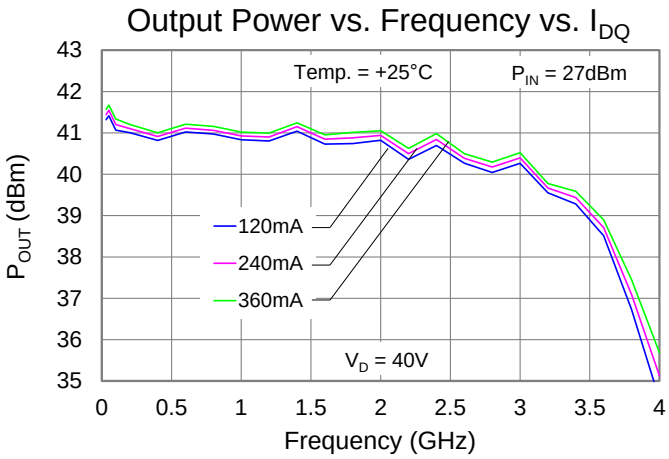


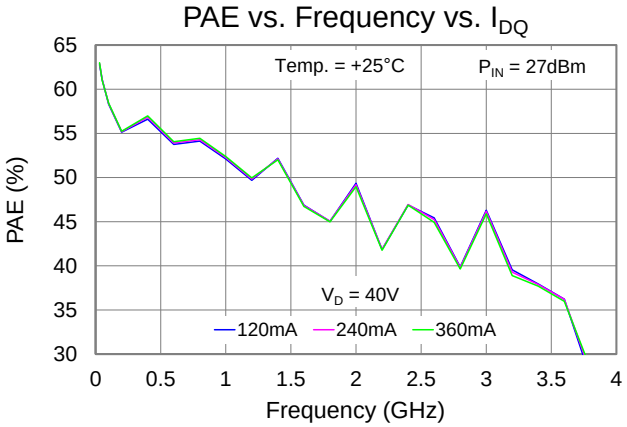
Output Return Loss vs. Freq. vs. I_D

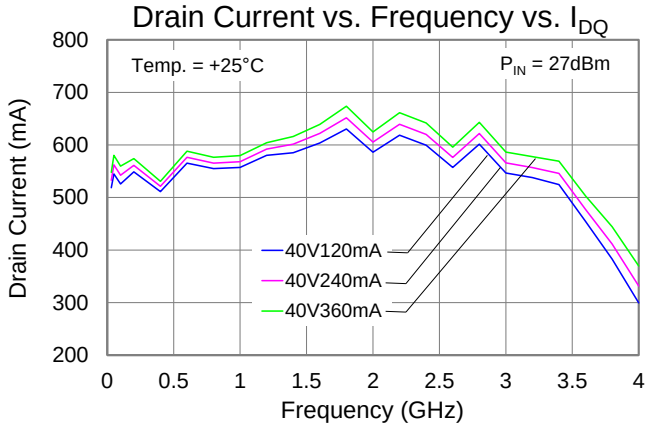


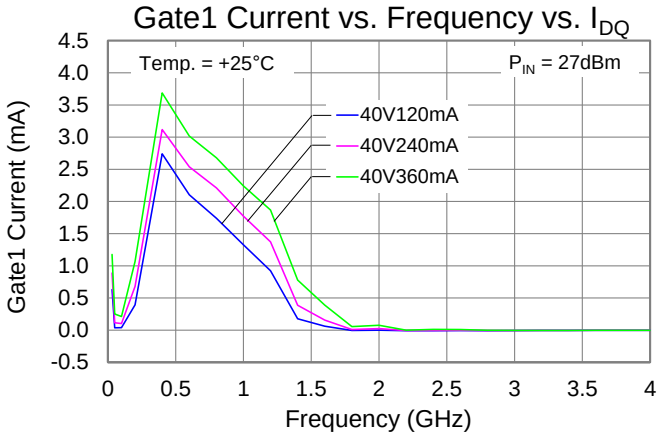
Typical Performance: Large Signal (CW)

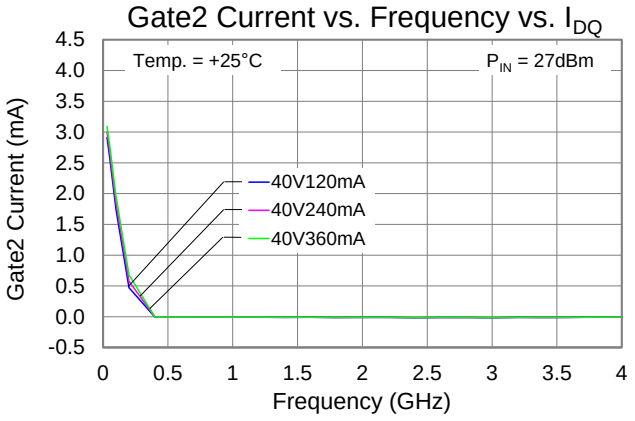
The plots reflect performance measured with an external coaxial bias tee and DC (See application circuit on page 11)





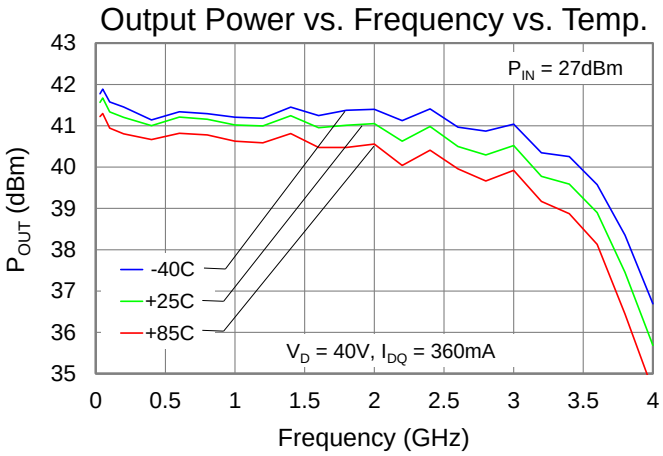


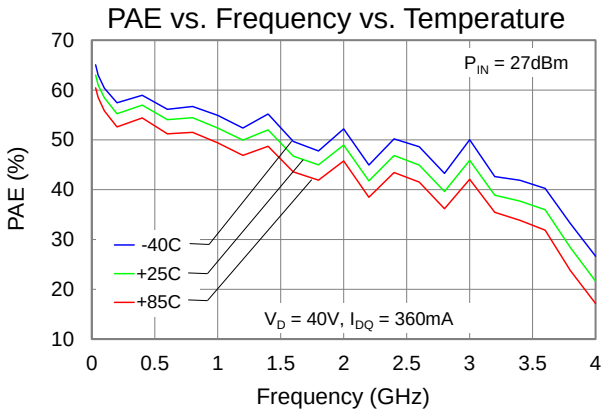


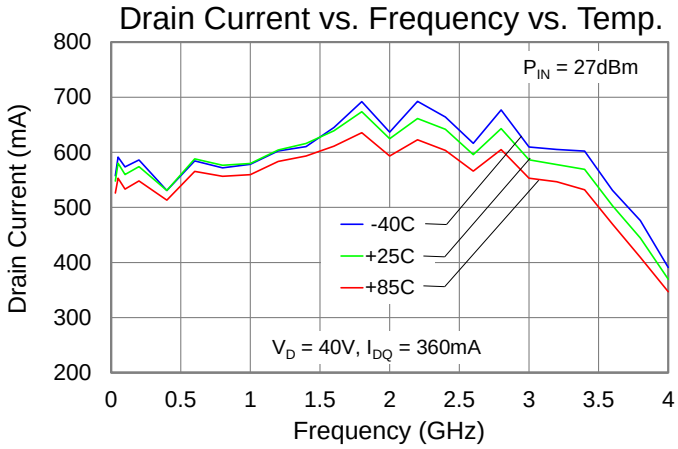


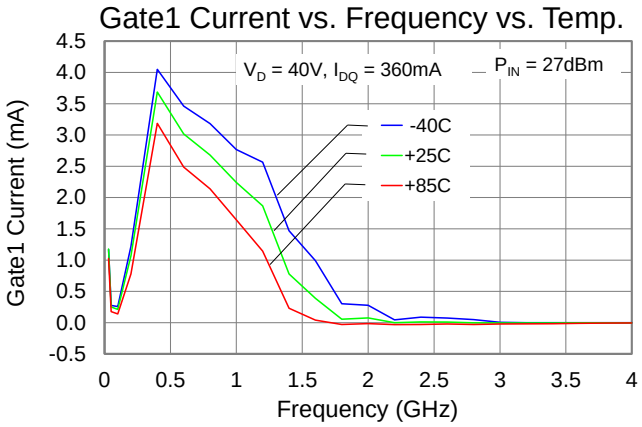
Typical Performance: Large Signal (CW)

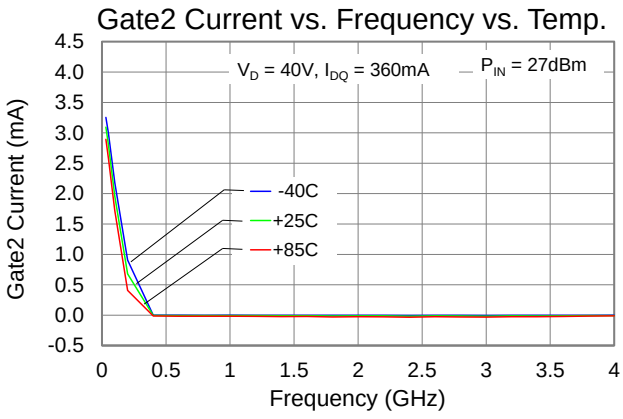
The plots reflect performance measured with an external coaxial bias tee and DC blocks (See application circuit on page 11)





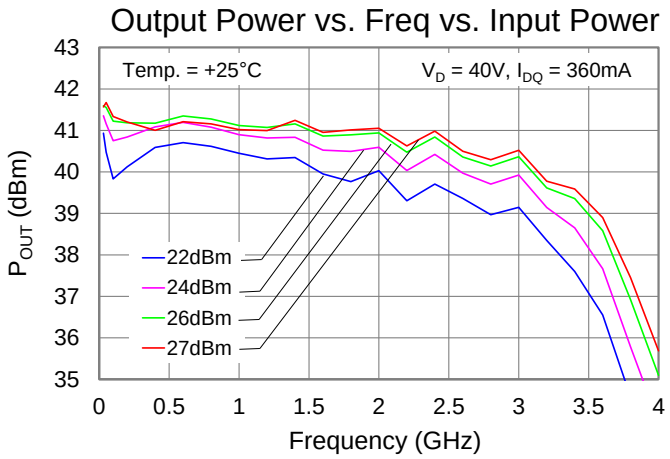


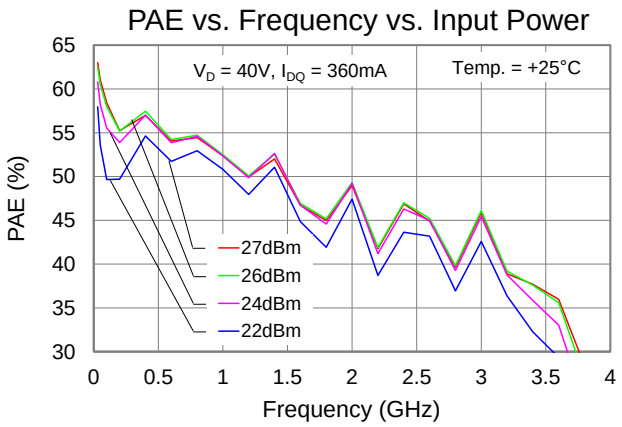


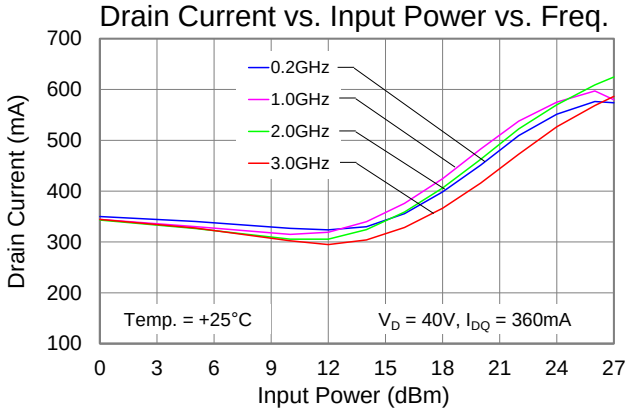


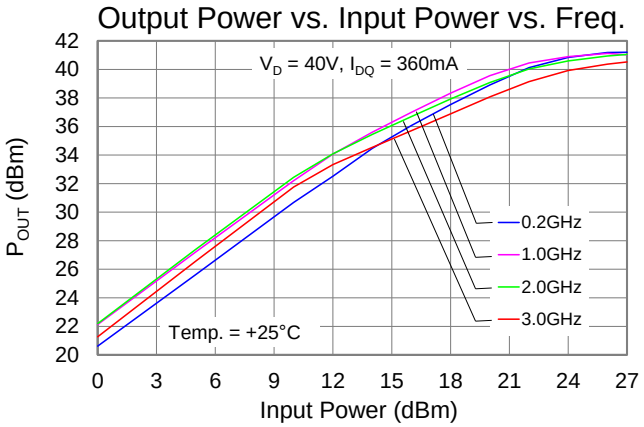
Typical Performance: Large Signal (CW)

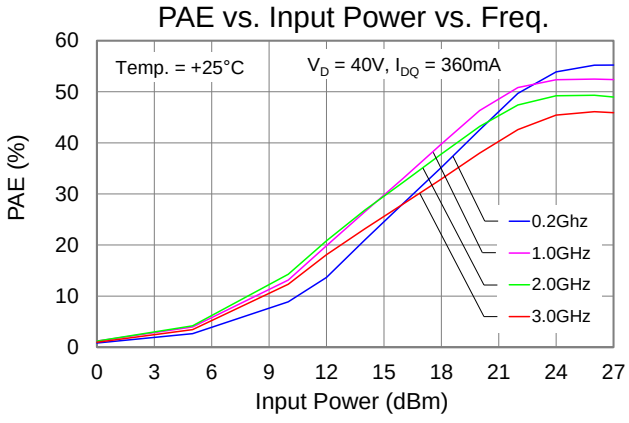
The plots reflect performance measured with an external coaxial bias tee and DC blocks (See application circuit on page 11)







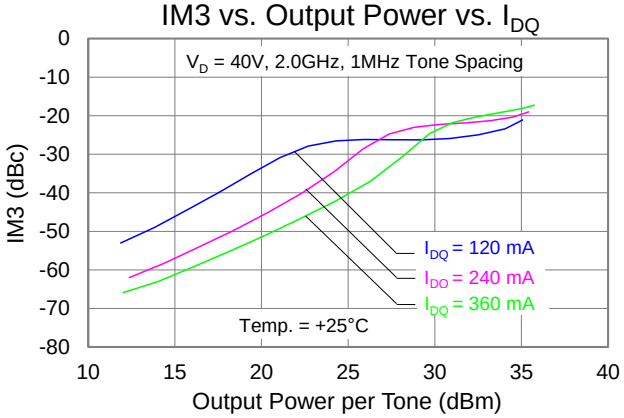




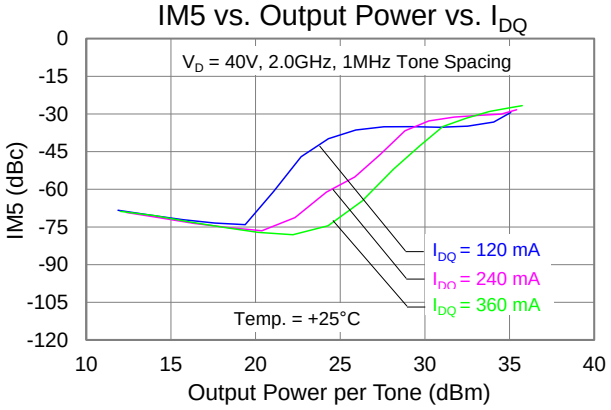
Typical Performance: Linearity

The plots reflect performance measured with an external coaxial bias tee and DC blocks (See application circuit on page 11)

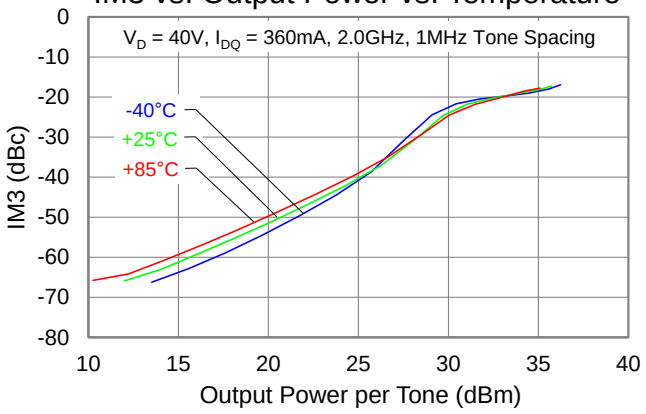
IM3 vs. Output Power vs. I_{DQ}



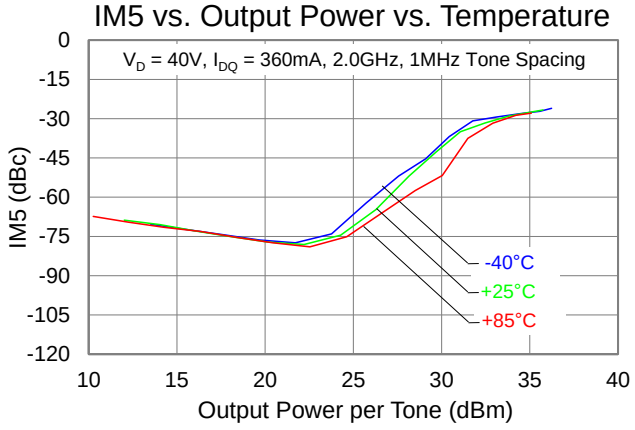
IM5 vs. Output Power vs. I_{DQ}



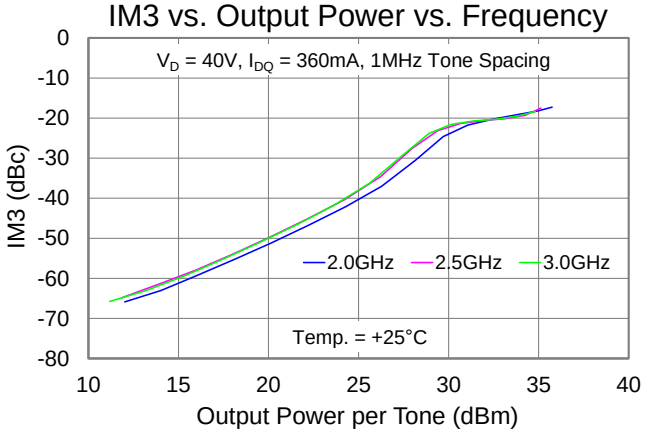
IM3 vs. Output Power vs. Temperature



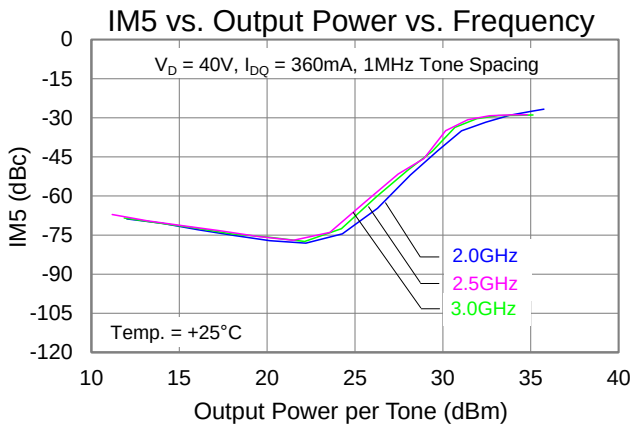
IM5 vs. Output Power vs. Temperature



IM3 vs. Output Power vs. Frequency

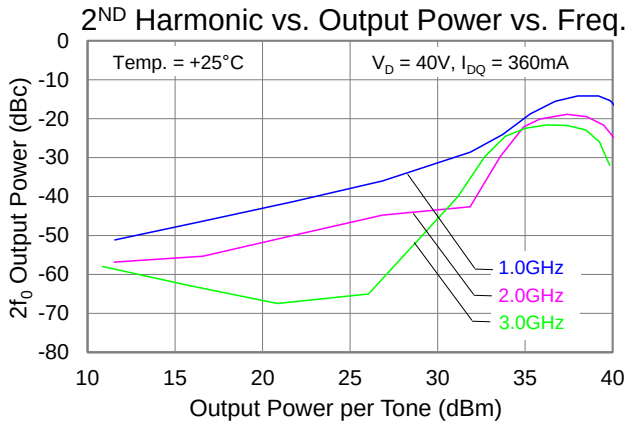


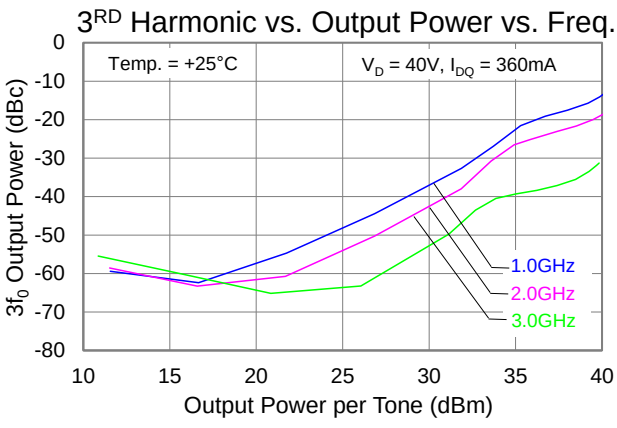
IM5 vs. Output Power vs. Frequency

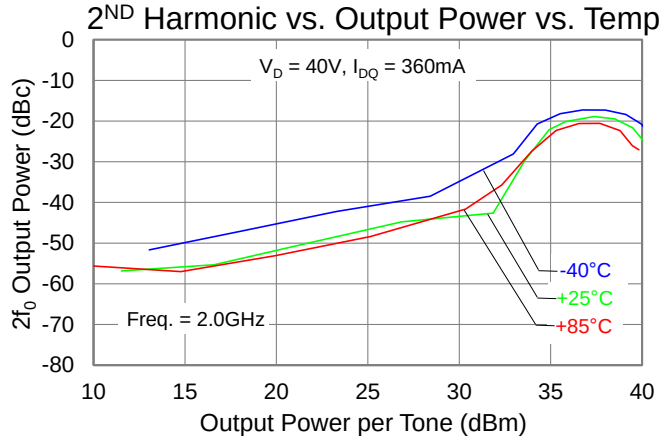


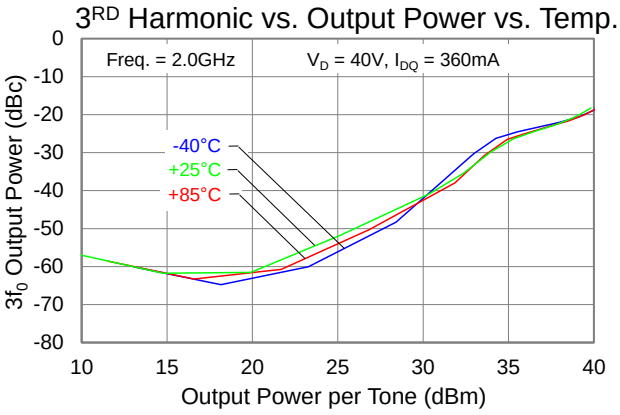
Typical Performance: Linearity

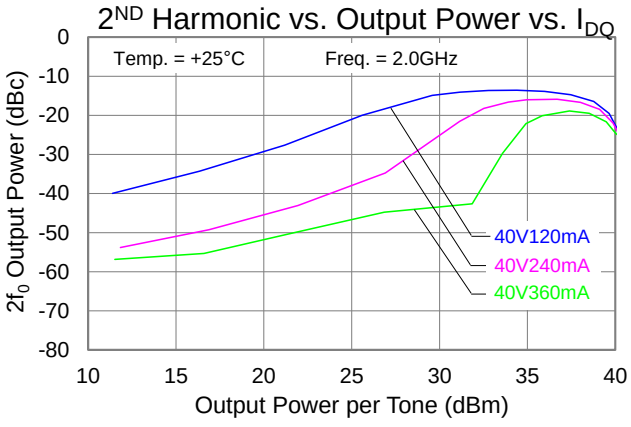
The plots reflect performance measured with an external coaxial bias tee and DC blocks (See application circuit on page 11)

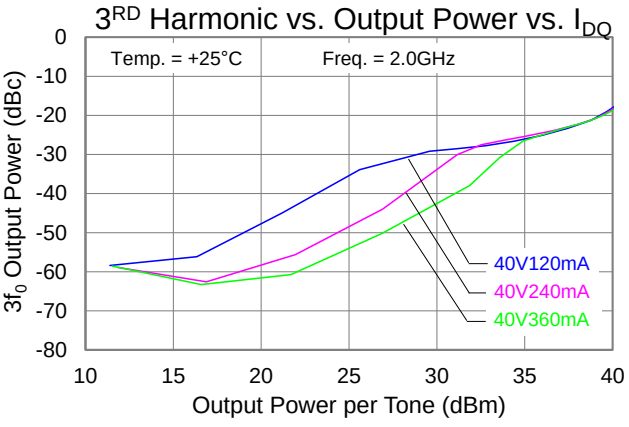






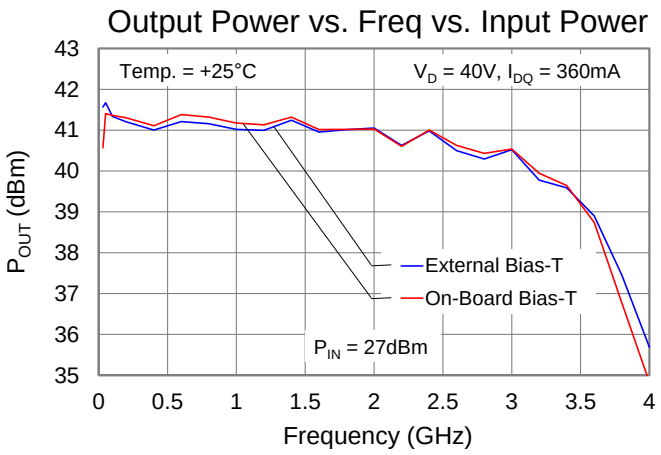


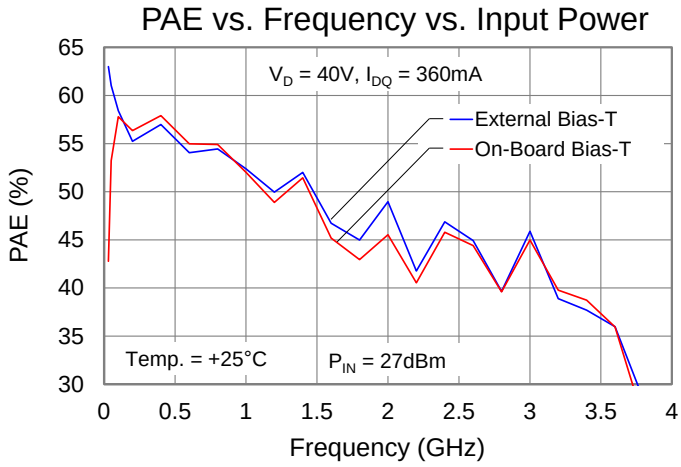




Typical Performance: Large Signal (CW), On-board vs. External Coaxial Bias-T

The plots below reflect performance measured between external bias tee and on-board bias tee
(See application circuit on pages 11 and 13)

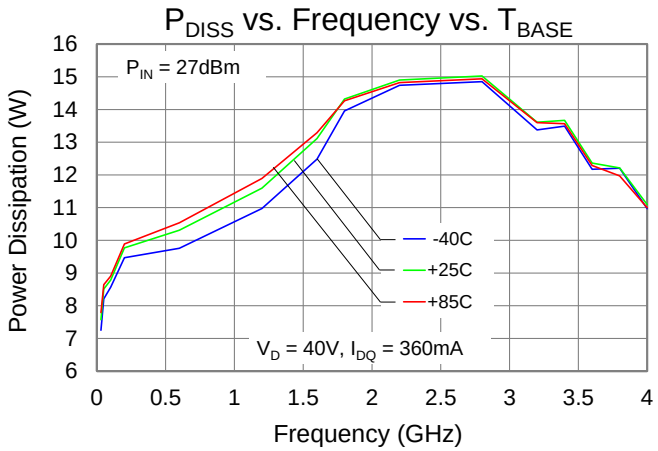




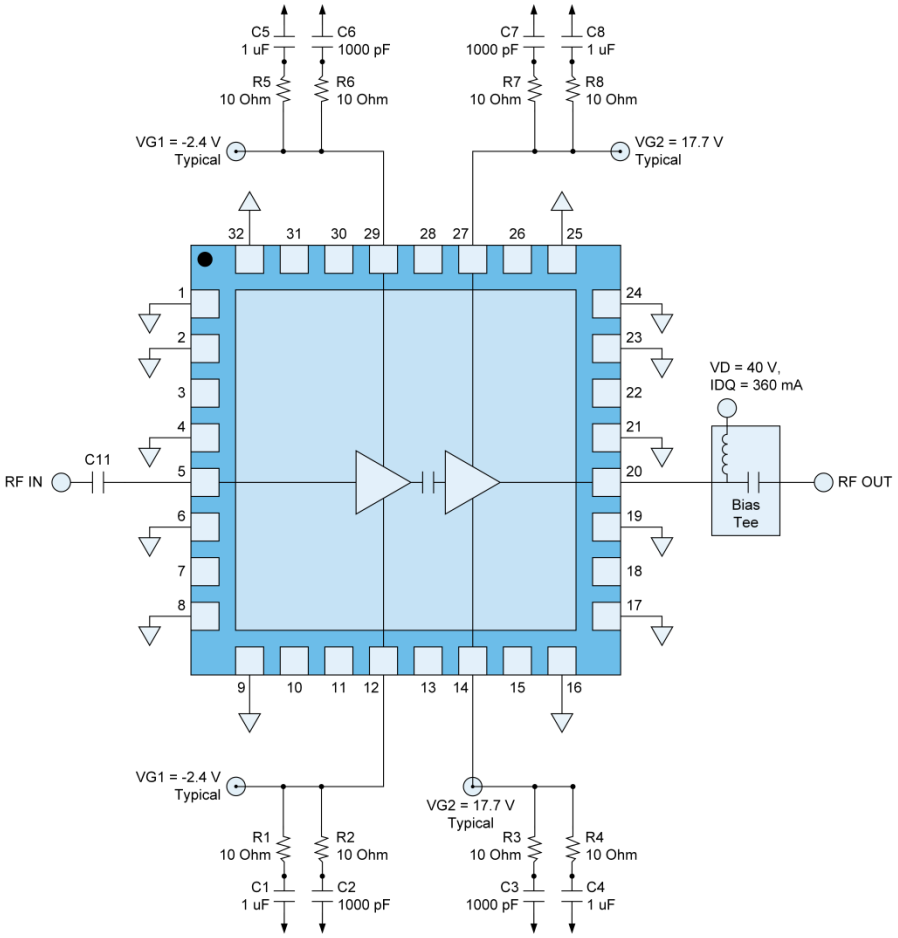
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D(3) = 40 V (CW) I_{DQ} = 360 mA, I_{D_Drive} = 610 mA P_{IN} = 27 dBm, P_{OUT} = 40 dBm, P_{DISS} = 15 W	4.20	ºC/W
Channel Temperature (T_{CH}) (Under RF drive)		148.0	°C

Notes:
1. Thermal resistance referenced to the back of the package.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates
3. The drain voltage for Cascode amplifier transistor is ½ of the V_D.



Application Circuit (Coaxial input DC block and coaxial output bias tee)



Notes:

1. VG1 & VG2 can be biased from either side (Top or Bottom.)
2. Coaxial input DC block (C11) is used for input port (RF In.)
3. External wide bandwidth Bias-Tee is used for output port (RF Out). VD is applied through the output Bias-Tee.

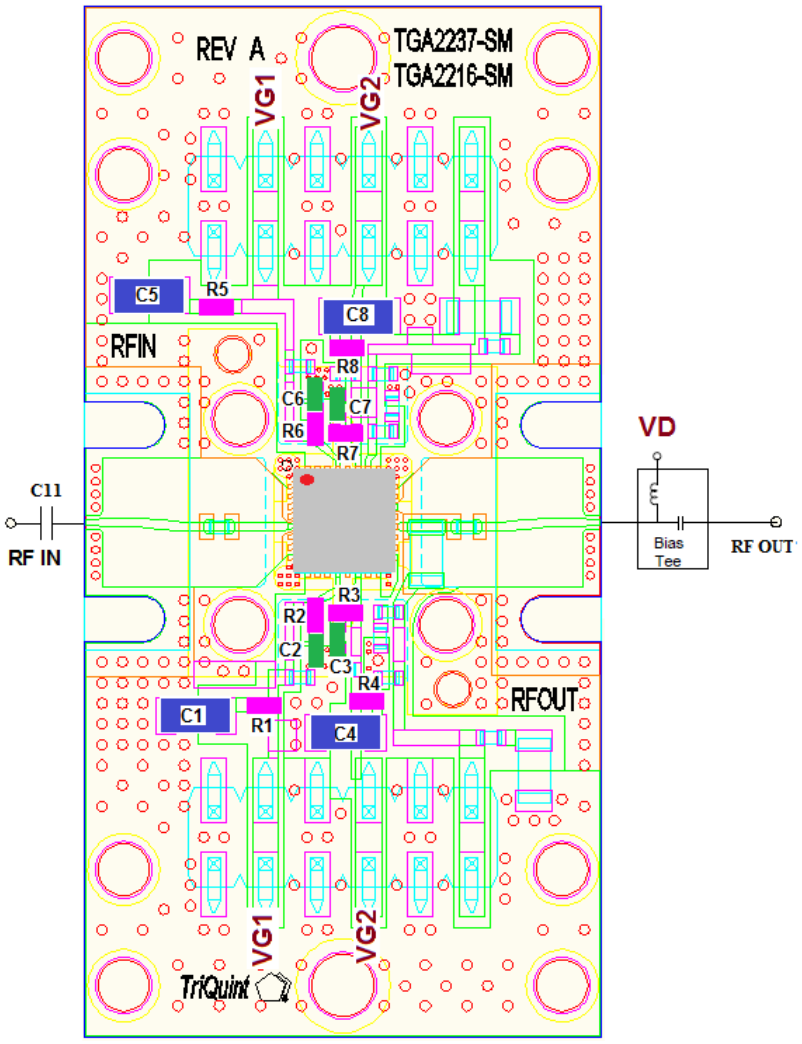
Bias-up Procedure

1. Set I_D limit to 720 mA, I_{G1} & I_{G2} limit to 5 mA
2. Set V_{G1} to -5.0 V
3. Set V_{G2} to (VD/2) - 2.7 V or 40 V/2 - 2.7 V = 17.3V
4. Set V_D +40 V
5. Adjust V_{G1} more positive until I_{DQ} = 360 mA (V_{G1} ~ -2.4 V Typical)
6. Adjust VG2 to (VD/2) + VG1; (V_{G2} ~ +17.7 V Typical)
7. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Reduce V_{G1} to -5.0 V. Ensure I_{DQ} ~ 0 mA
3. Reduce V_{G2} to 0 V.
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_{G2} supply
7. Turn off V_{G1} supply

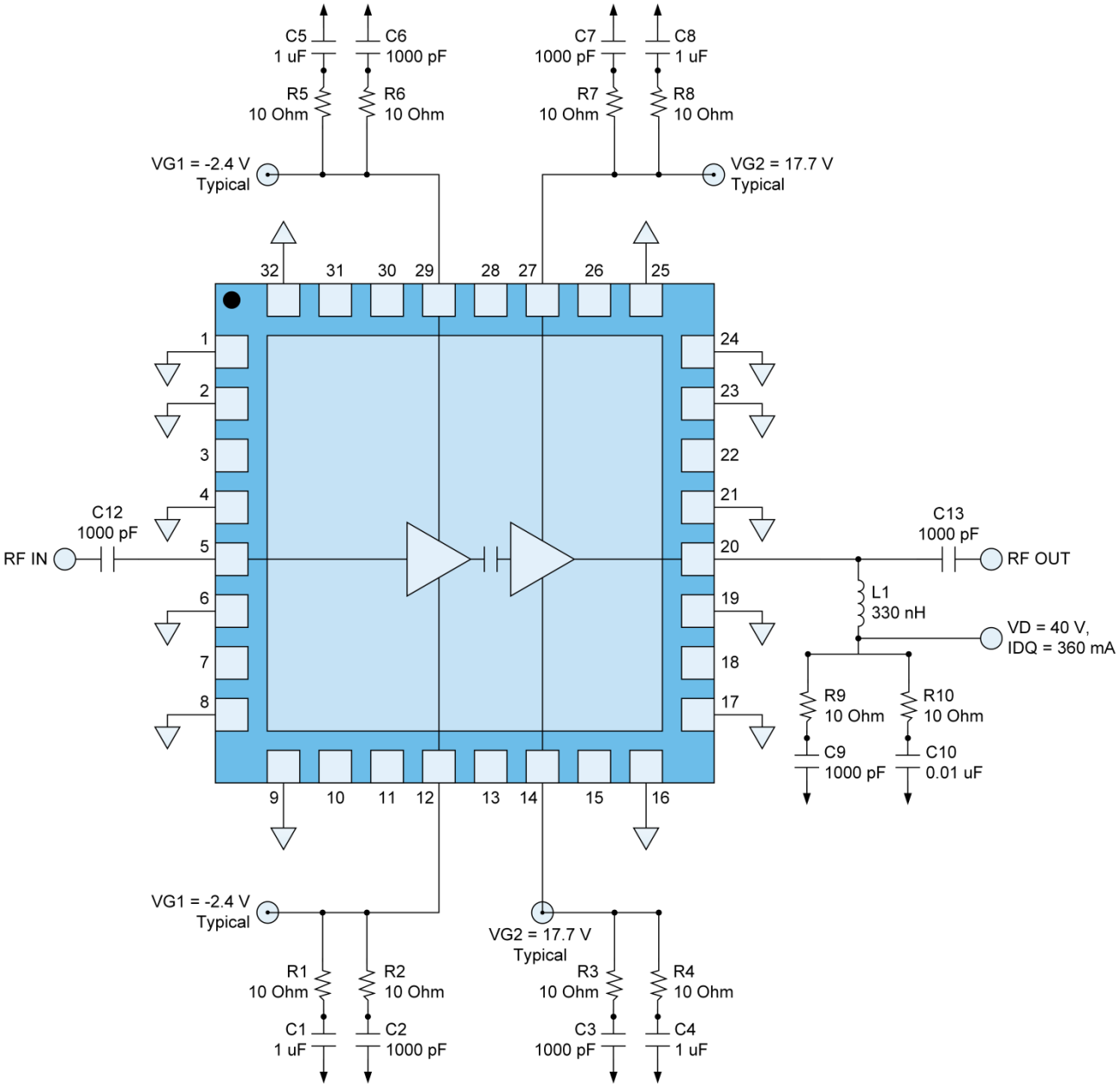
Assembly Drawing (Coaxial input DC block and coaxial output bias tee)



Bill of Materials

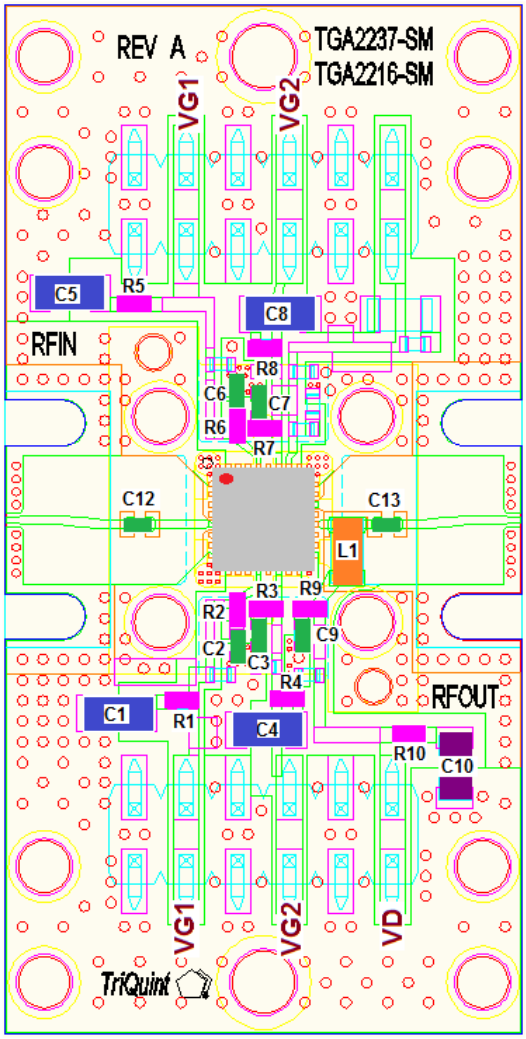
Reference Des.	Value	Description	Manuf.	Part Number
C1, C4, C5, C8	1 uF	Cap, 1206, 50 V, 10%, X7R	Various	
C2, C3, C6, C7	1000 pF	Cap, 0402, 100 V, 10%, X7R	Various	
C11	1000 pF	DC Block	Various	
R1 – R8	10 Ω	Res, 0402	Various	

Application Circuit (Option with board-level DC blocks and output bias tee)



1. Performance of the DUT with surface mount DC blocks and bias tee components may be degraded relative to the coaxial option. These components should be optimized for the desired operational bandwidth.
2. VG1 & VG2 can be biased from either side (Top or Bottom.)

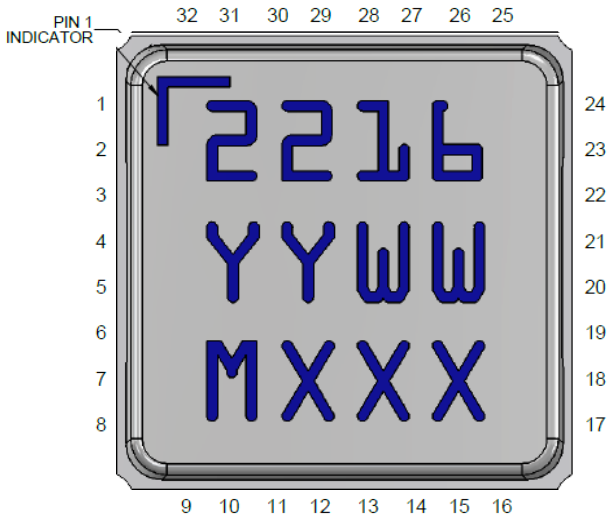
Evaluation Board Layout with On-Board DC Blocks and Output Bias-T Option

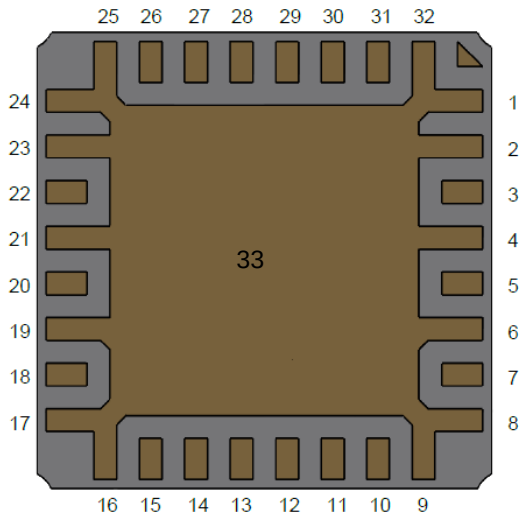


Bill of Materials For On-Board Bias-Tee

Reference Des.	Value	Description	Manuf.	Part Number
C1, C4, C5, C8	1u F	Cap, 1206, 50 V, 10%, X7R		
C2-C3, C6-C7, C9, C12, C13	1000 pF	Cap, 0402, 100 V, 10%, X7R	Various	
C10	0.01 uF	Cap, 1206, 100 V, 10%, X7R	Various	
L1	330 nH	Ind, 1206, 100 V, 10%, X7R	Various	
R1 – R10	10 Ω	Res, 0402	Various	

Pin Layout

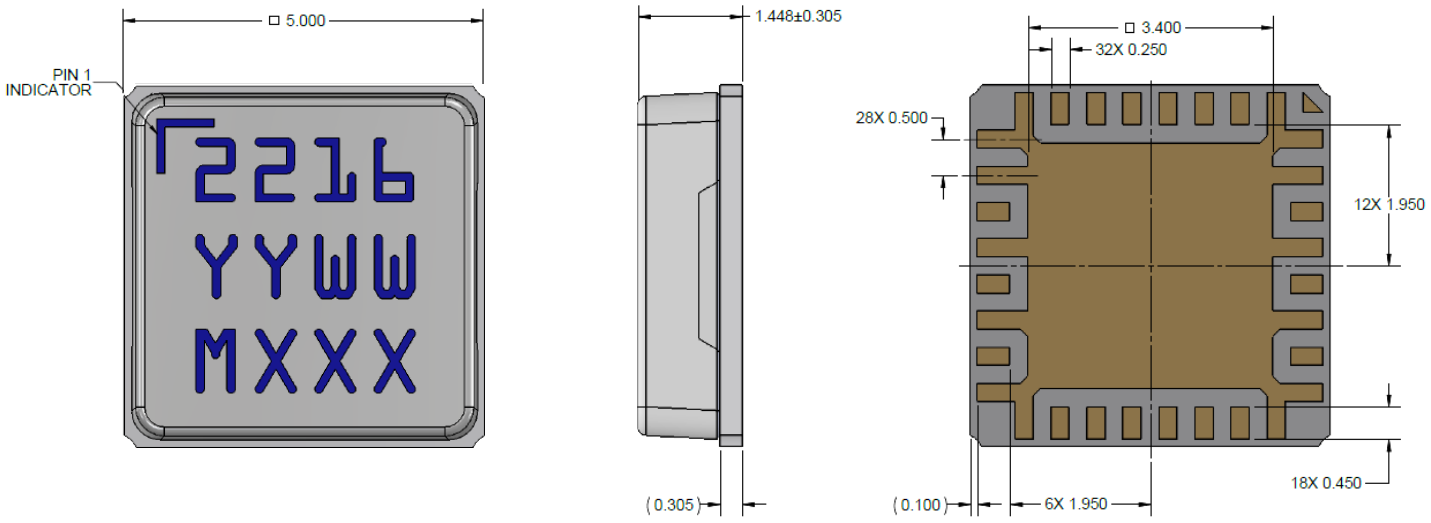




Pin Description

Pad Number	Symbol	Description
1-2, 4, 6, 8-9, 16-17, 19, 21, 23-25, 32	GND	Connected to ground paddle (pin 33); must be grounded on PCB
3, 7, 10-11, 13, 15, 18, 22, 26, 28, 30-31	NC	No internal connection. Recommended to connect to PCB ground
5	RF IN	Input; matched to 50 Ω. VG1 gate voltage is present; external DC block is required.
12, 29	VG1	Gate voltage1. Bias network is required; see recommended Application Information on page 12 or 14
14, 27	VG2	Gate voltage2. Bias network is required; see recommended Application Information on page 12 or 14
20	RF OUT/ DRAIN	Output; matched to 50 Ω. Bias network is required; see recommended Application Information on page 12 or 14.
33	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance

Mechanical Information



Units: millimeters
Tolerances: unless specified
x.xx = ± 0.25
x.xxx = ± 0.125
Materials:
Base: Ceramic
Lid: Plastic
All metalized features are gold plated
Part is epoxy sealed
Marking:
2216: Part number
YY: Part Assembly year
WW: Part Assembly week
MXXX: Batch ID

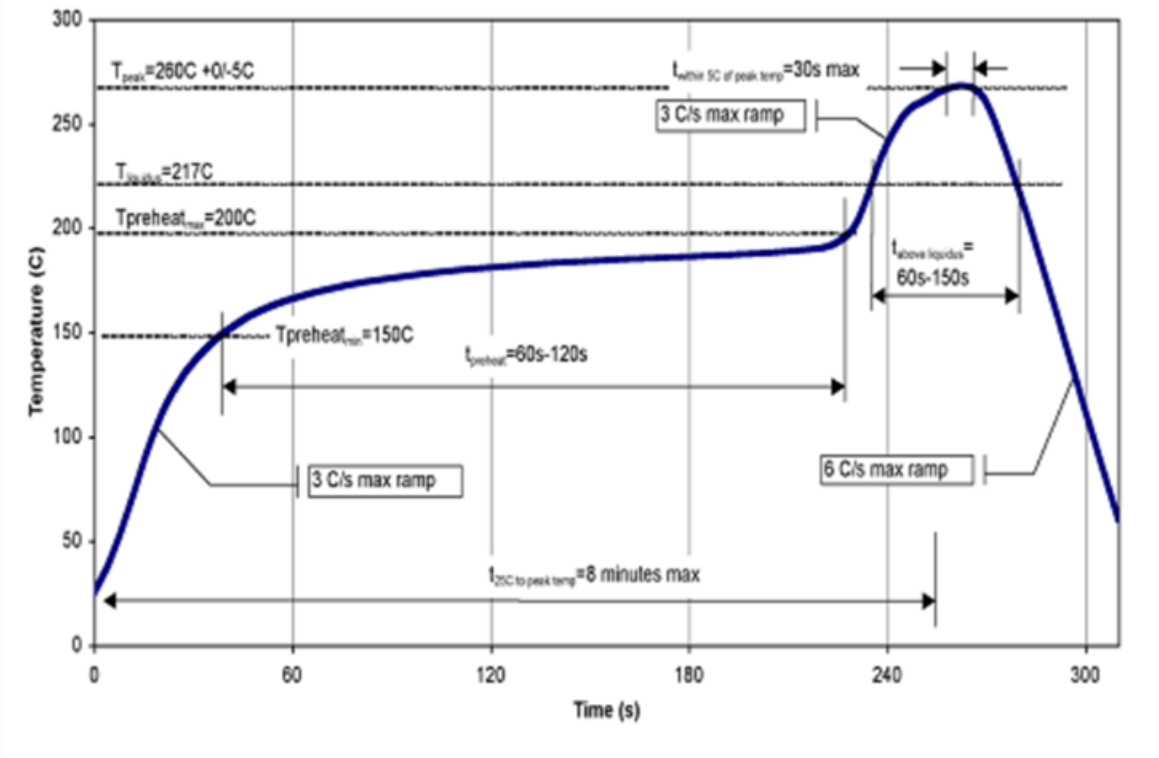
Assembly Notes

Compatible with lead-free soldering processes with 260°C peak reflow temperature.

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended.

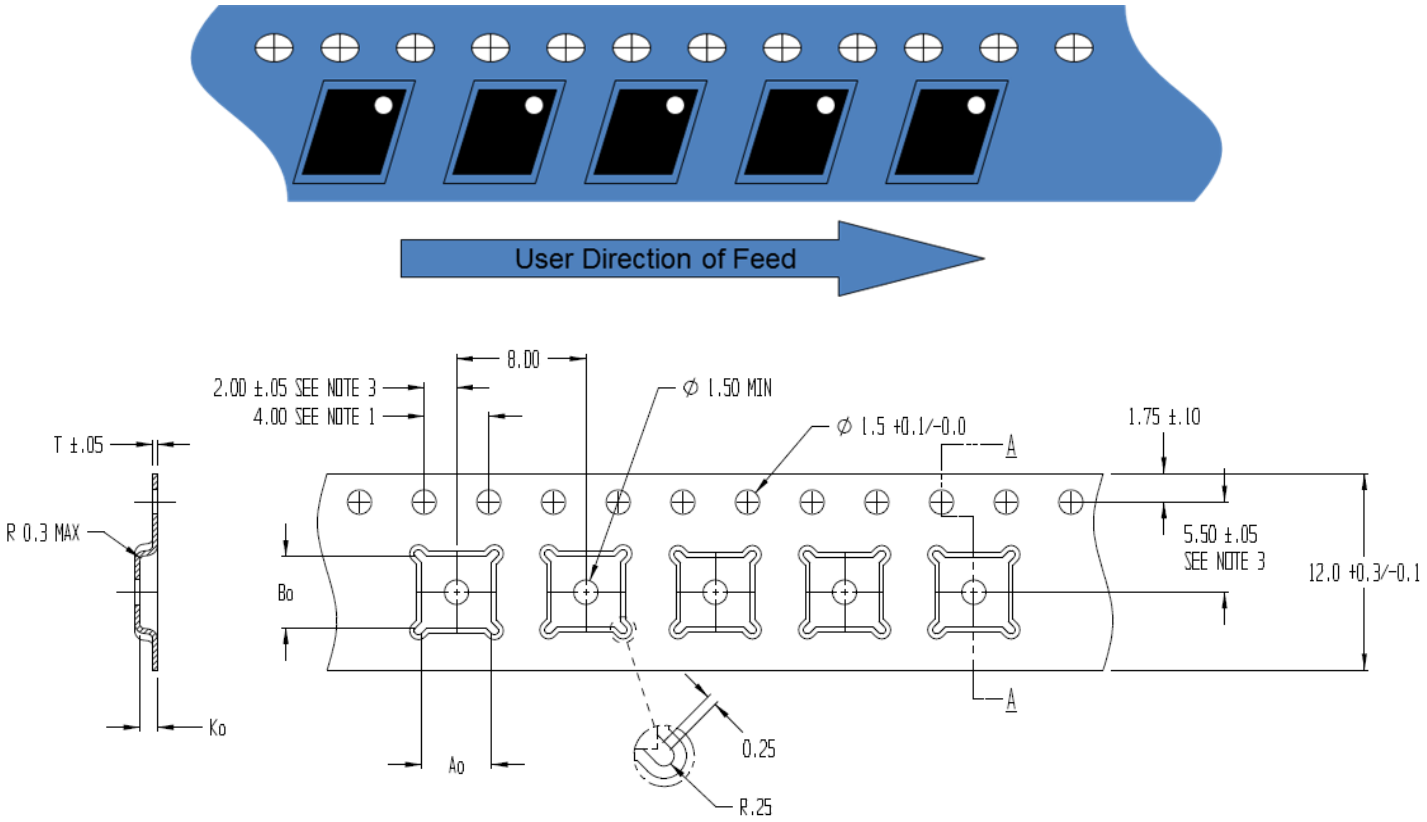
Contact plating: Ni-Au.

Solder rework not recommended.



Recommended Soldering Temperature Profile

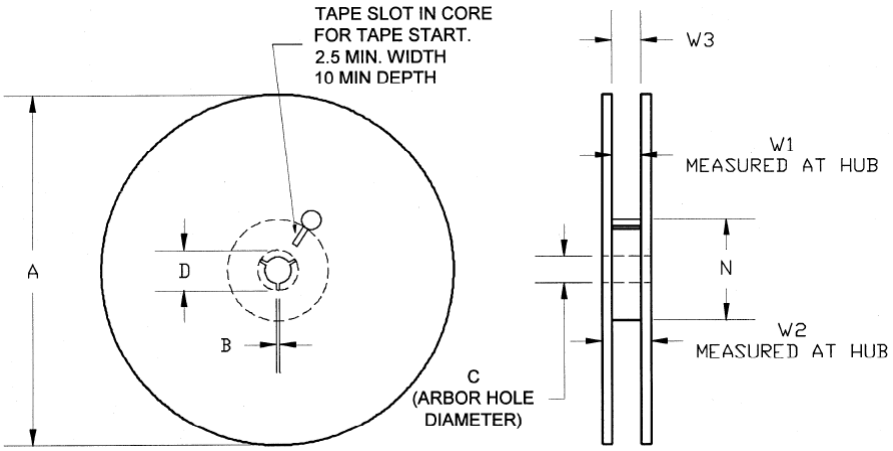
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.209	5.3
	Width	B0	0.209	5.3
	Depth	K0	0.065	1.65
	Pitch	P1	0.315	8.0
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.0
	Cavity to Perforation - Width Direction	F	0.217	5.5
Cover Tape	Width	C	0.362	9.2
Carrier Tape	Width	W	0.472	12.0

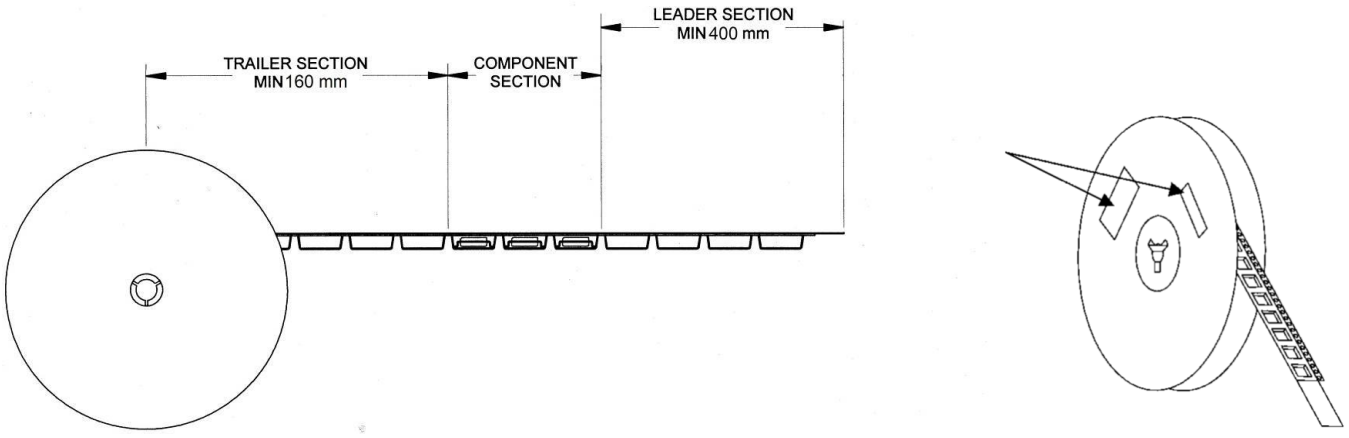
Tape and Reel Information – Reel Dimensions

Standard T/R size = 1000 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.795	20.2

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	C2A	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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