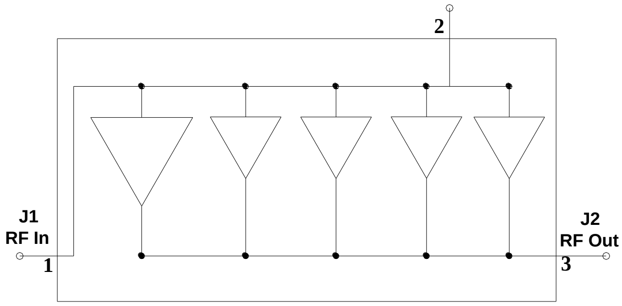
Applications

- Commercial and military radar
- Communications
- Electronic Warfare

Product Features

- Frequency Range: 0.03 – 2.5GHz
- P_{SAT}: 40dBm at PIN = 27dBm
- P1dB: >32dBm
- PAE: >52%
- Large Signal Gain: 13dB
- Small Signal Gain: 19dB
- IM3 @ 120mA POUT< 33dBm/tone: -30dBc
- IM5 @ 120mA POUT< 33dBm/tone: -30dBc
- Bias: V_D = 30V, I_{DQ} = 360mA, V_G = -2.5V Typical
- Wideband Flat Power
- Chip Dimensions: 2.4 x 1.8 x 0.10 mm

Functional Block Diagram



General Description

TriQuint's TGA2237 is a wideband distributed amplifier fabricated on TriQuint's production 0.25um GaN on SiC process. The TGA2237 operates from 0.03 – 2.5GHz and provides 10W of saturated output power with 13dB of large signal gain and greater than 52% power-added efficiency.

The broadband performance supports both radar and communication applications across defense and commercial markets as well as electronic warfare. The TGA2237 is fully matched to 50Ω at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Pad Configuration

Pad No.	Symbol
1	RF In
2	V_G
3	RF Out, V_D

Ordering Information

Part	ECCN	Description
TGA2237	EAR99	0.03 – 2.5GHz 10W GaN Power Amplifier

Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	40V
Gate Voltage Range (V_G)	-8 to 0V
Drain Current (I_D)	1350mA
Gate Current (I_G)	-2.4 to 8.4mA
Power Dissipation (P_{DISS}), 85°C	19W
Input Power (P_{IN}), CW, 50Ω, 85°C,	33dBm
Input Power (P_{IN}), CW, VSWR 10:1, V_D = 30V, 85°C	30dBm
Channel Temperature (T_{CH})	275°C
Mounting Temperature (30 Seconds)	320°C
Storage Temperature	-55 to 150°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	30V
Drain Current (I_{DQ})	360mA
Drain Current Under RF Drive (I_{D_Drive})	660mA
Gate Voltage (V_G)	-2.5V (Typ.)

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25^{0}C, V_D = 30V, I_{DQ} = 360mA, V_G = -2.5V Typical

Parameter	Min	Typical	Max	Units
Operational Frequency Range	0.03		2.5	GHz
Small Signal Gain		19		dB
Input Return Loss		> 10		dB
Output Return Loss		> 12		dB
Output Power (Pin = 27dBm)		40		dBm
Power Added Efficiency (Pin = 27dBm)		> 52		%
Power @ 1dB Compression (P1dB)		> 32		dB
IM3 @ 120mA POUT/Tone < 33dBm		-30		dBc
IM5 @ 120mA POUT/Tone < 33dBm		-30		dBc
Small Signal Gain Temperature Coefficient		-0.02		dB/°C
Output Power Temperature Coefficient		-0.002		dBm/°C
Recommended Operating Voltage:	25	30	32	V

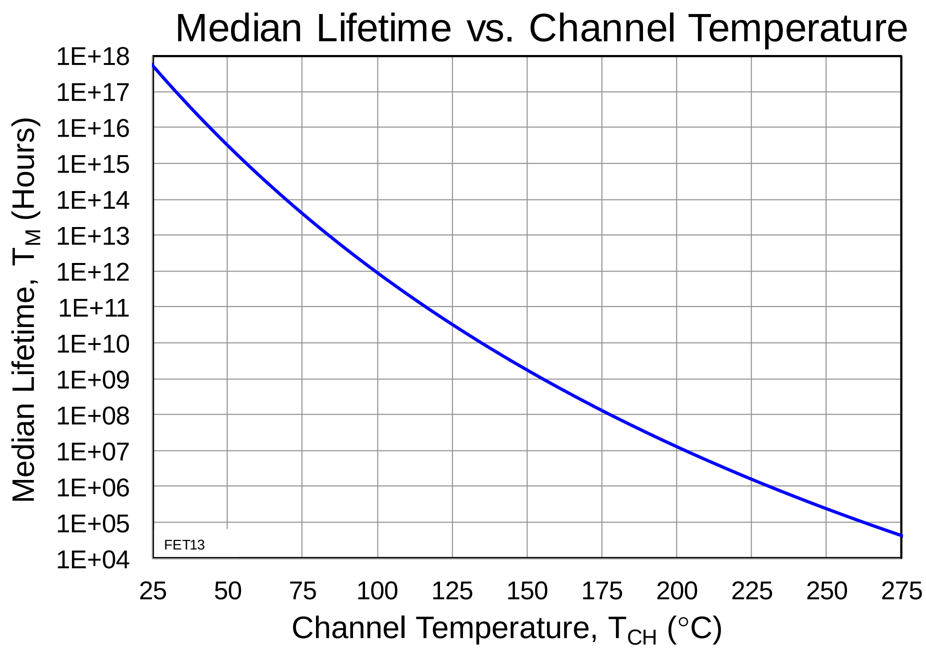
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, V_D **= 30V**, I_{DQ} = 360mA	10	ºC/W
Channel Temperature (T_{CH}) (Under RF drive)	T_{base} = 85°C, V_D **= 30V**, $I_{D\ Drive}$ = 633mA, POUT = 40dBm, P_{DISS} = 9W	175	°C
Median Lifetime (T_M)		1.3 x 10^7	Hrs

Notes:
1. Thermal resistance measured to back of carrier plate. MMIC mounted on 40 mils CuMo (80/20) carrier using 1.5 mil AuSn.

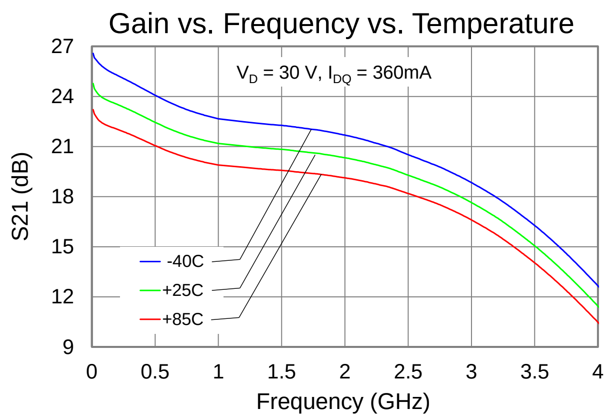
Median Lifetime

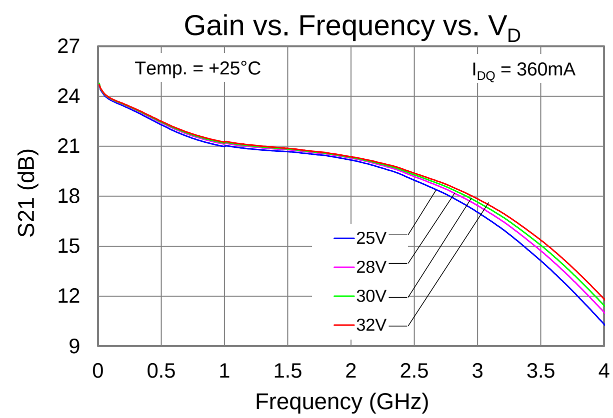
Test Conditions: V_D = 40 V; Failure Criteria = 10% reduction in I_{D_MAX}

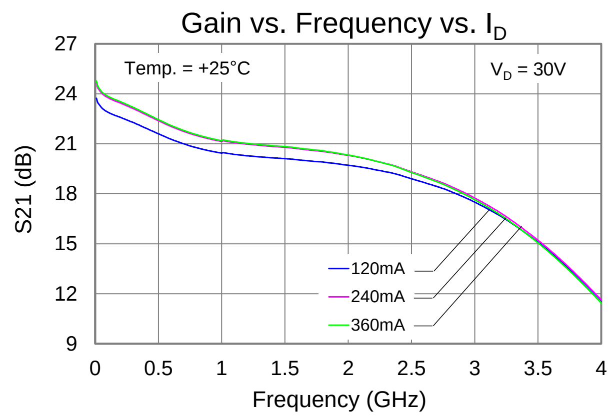


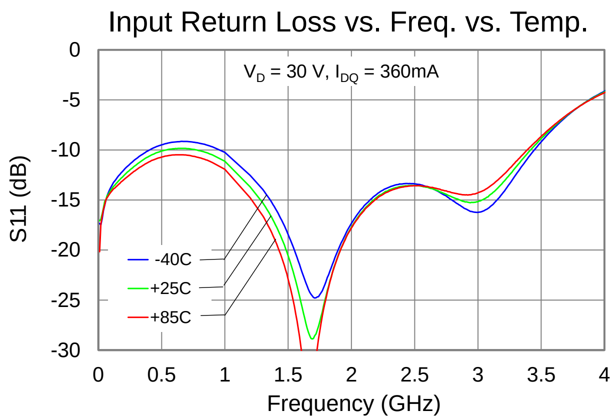
Typical Performance

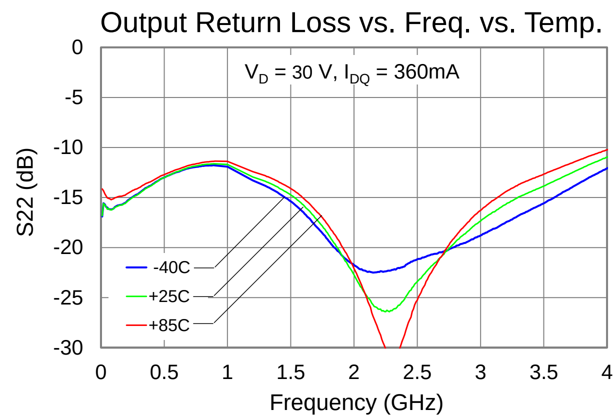
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 10)







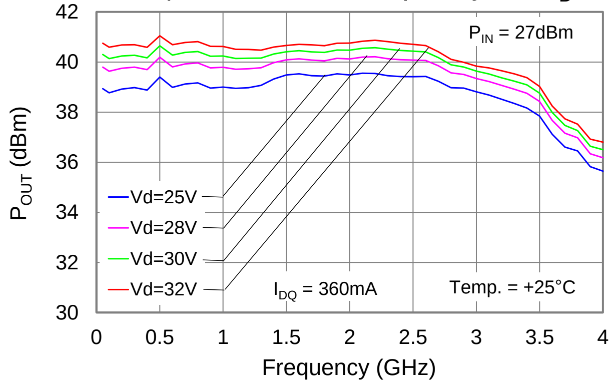




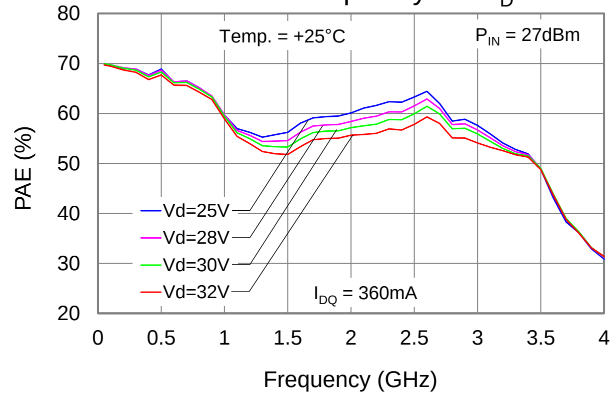
Typical Performance

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 10)

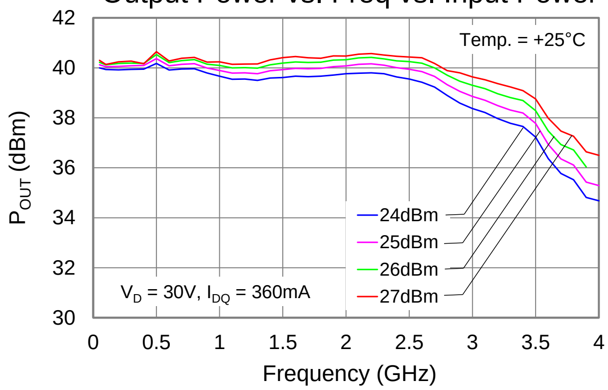
Output Power vs. Frequency vs. V_D



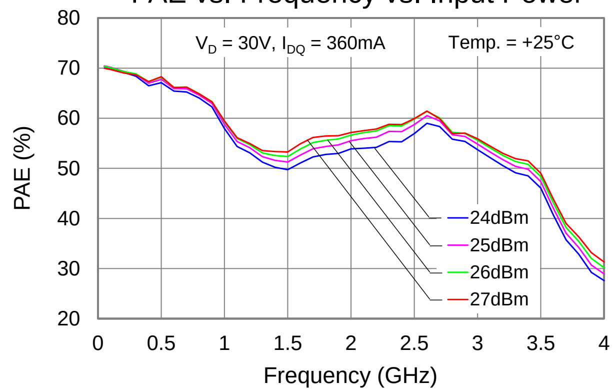
PAE vs. Frequency vs. V_D



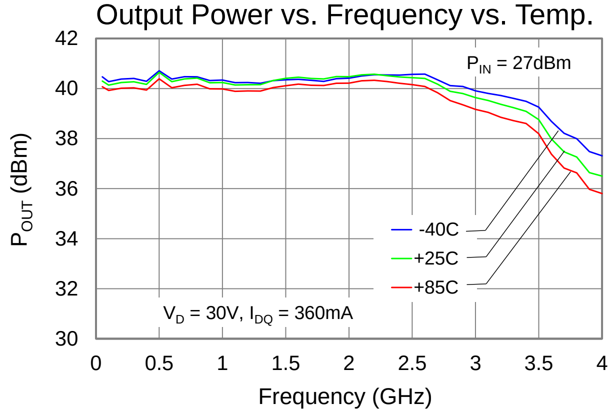
Output Power vs. Freq vs. Input Power



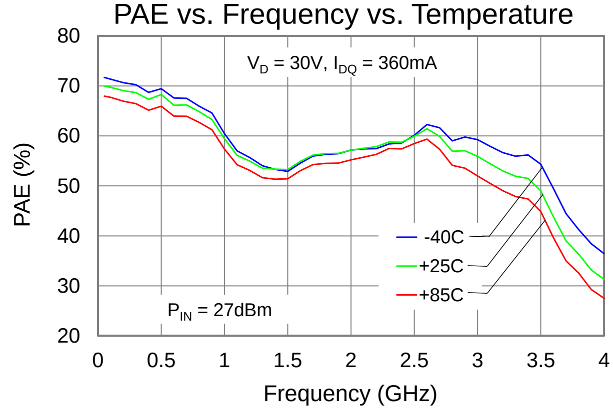
PAE vs. Frequency vs. Input Power



Output Power vs. Frequency vs. Temp.



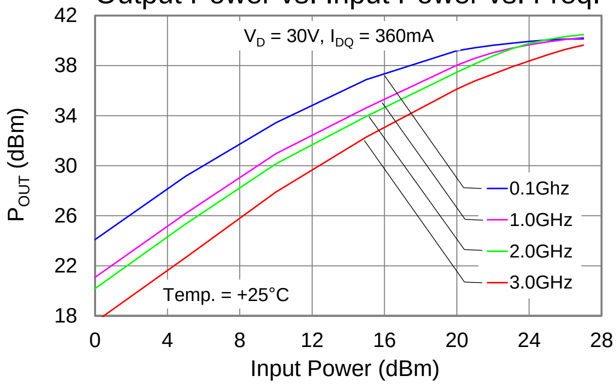
PAE vs. Frequency vs. Temperature



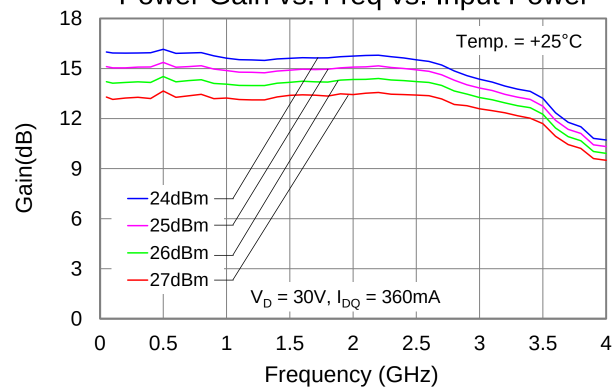
Typical Performance

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 10)

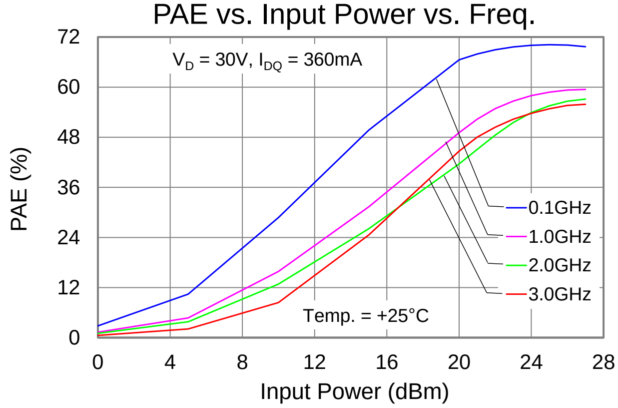
Output Power vs. Input Power vs. Freq.



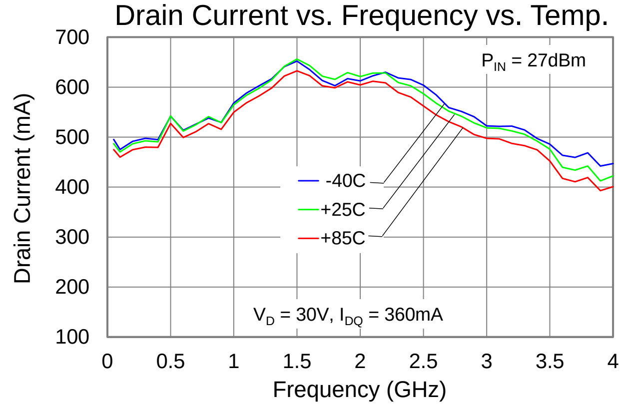
Power Gain vs. Freq vs. Input Power



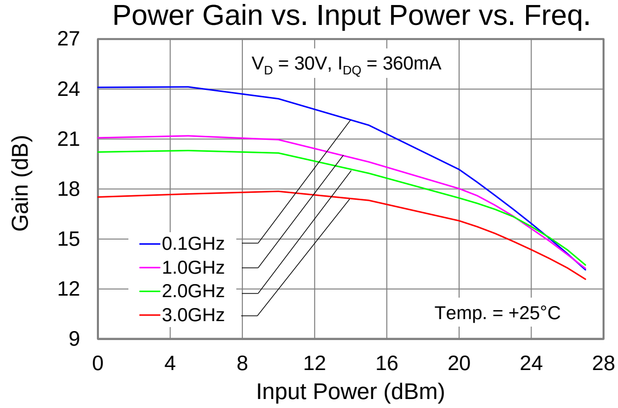
PAE vs. Input Power vs. Freq.



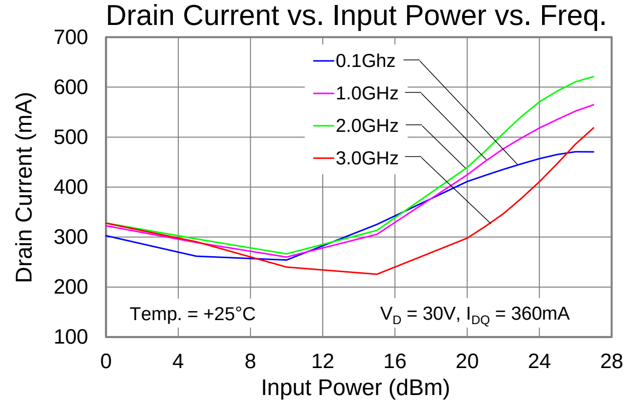
Drain Current vs. Frequency vs. Temp.



Power Gain vs. Input Power vs. Freq.

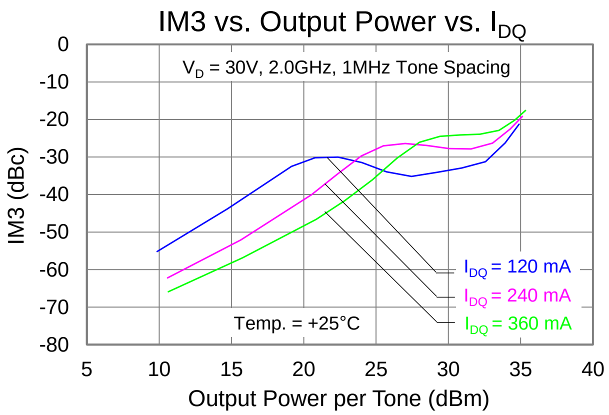


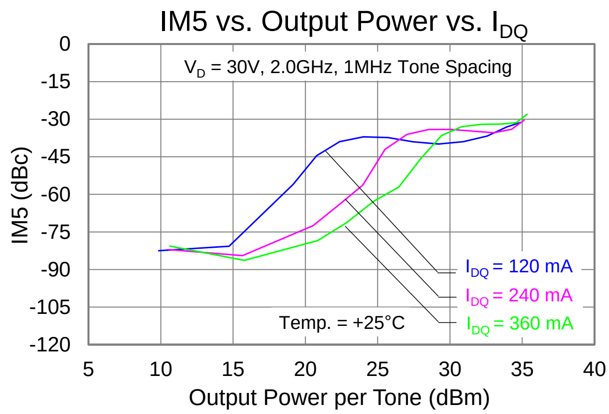
Drain Current vs. Input Power vs. Freq.

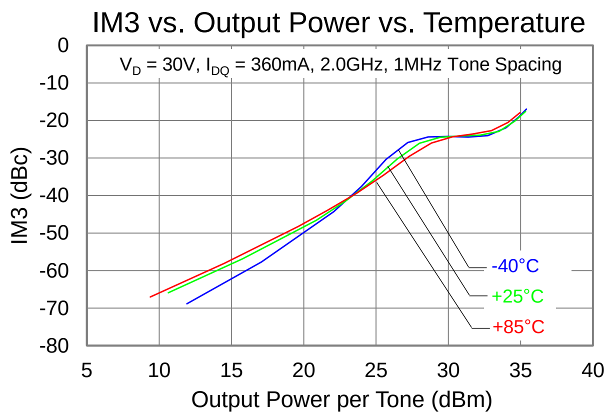


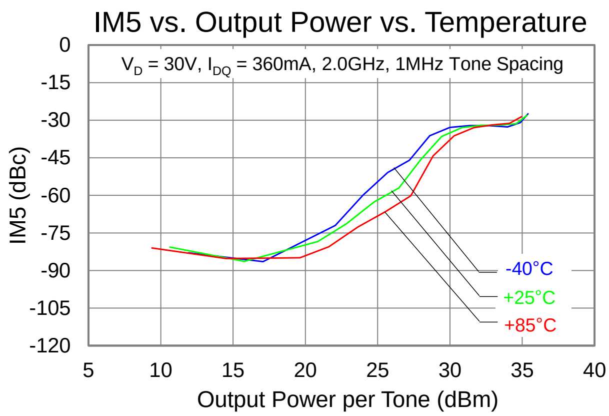
Typical Performance

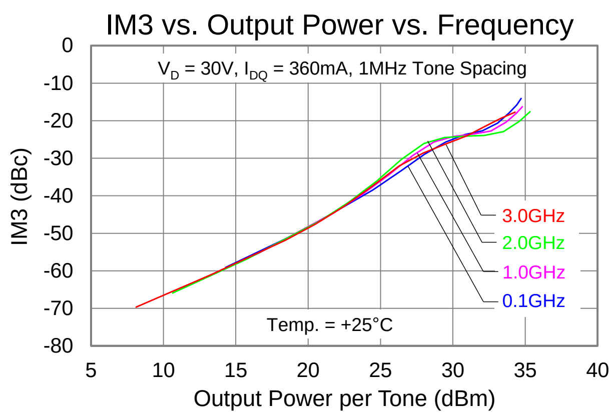
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 10)

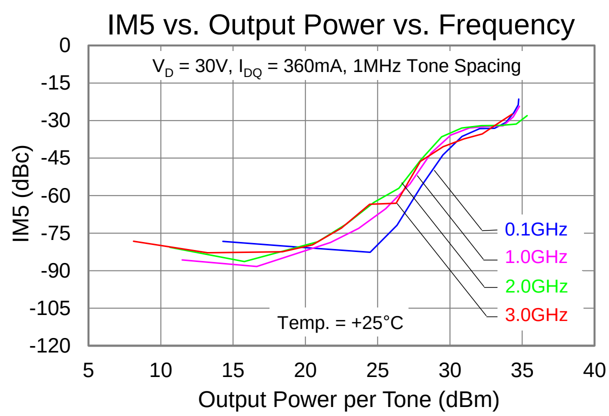








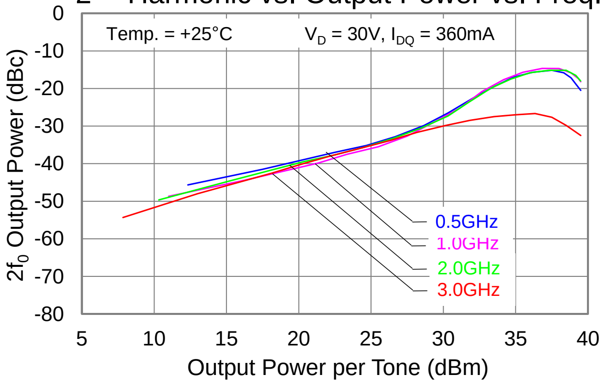




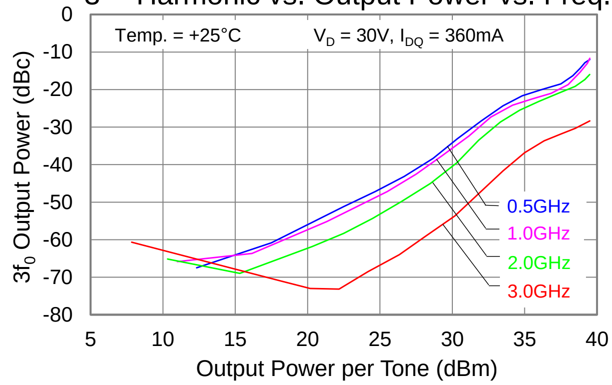
Typical Performance

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 10)

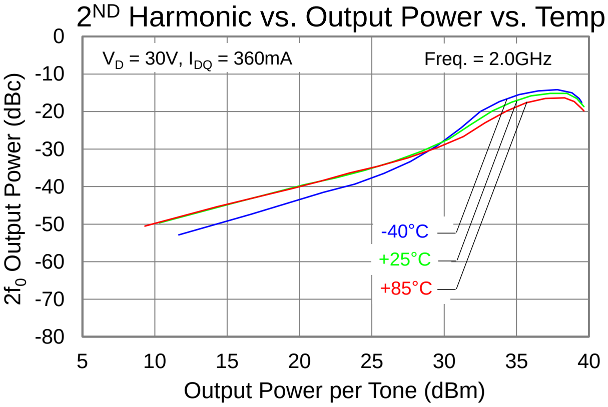
2ND Harmonic vs. Output Power vs. Freq.



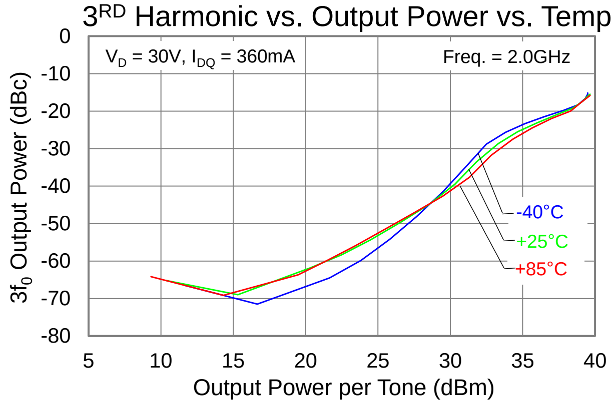
3RD Harmonic vs. Output Power vs. Freq.



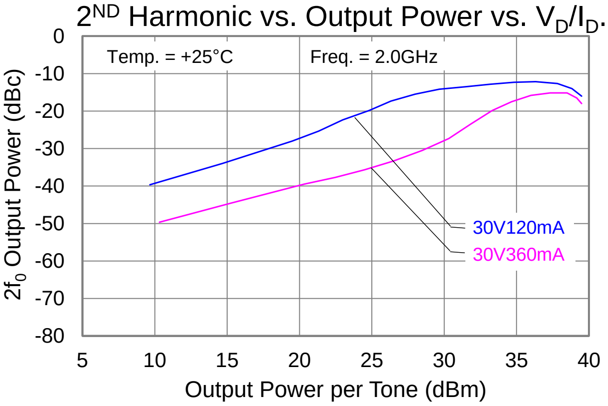
2ND Harmonic vs. Output Power vs. Temp.



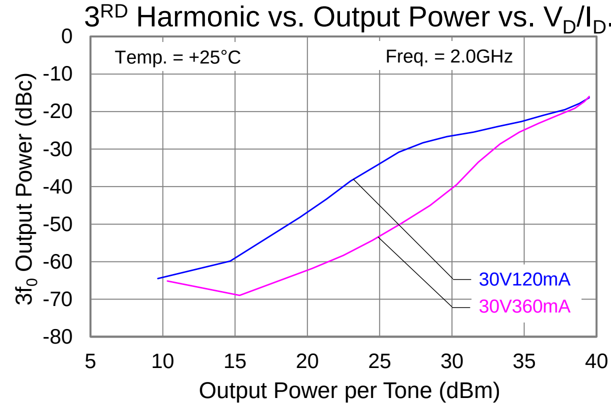
3RD Harmonic vs. Output Power vs. Temp.



2ND Harmonic vs. Output Power vs. V_D/I_D.

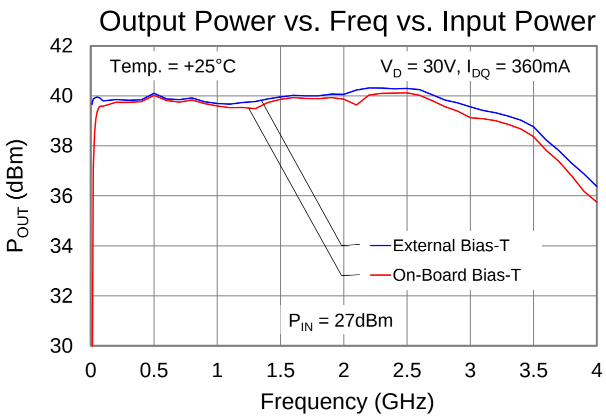


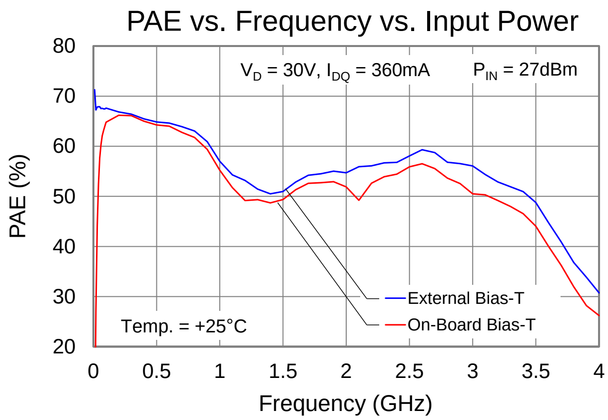
3RD Harmonic vs. Output Power vs. V_D/I_D.



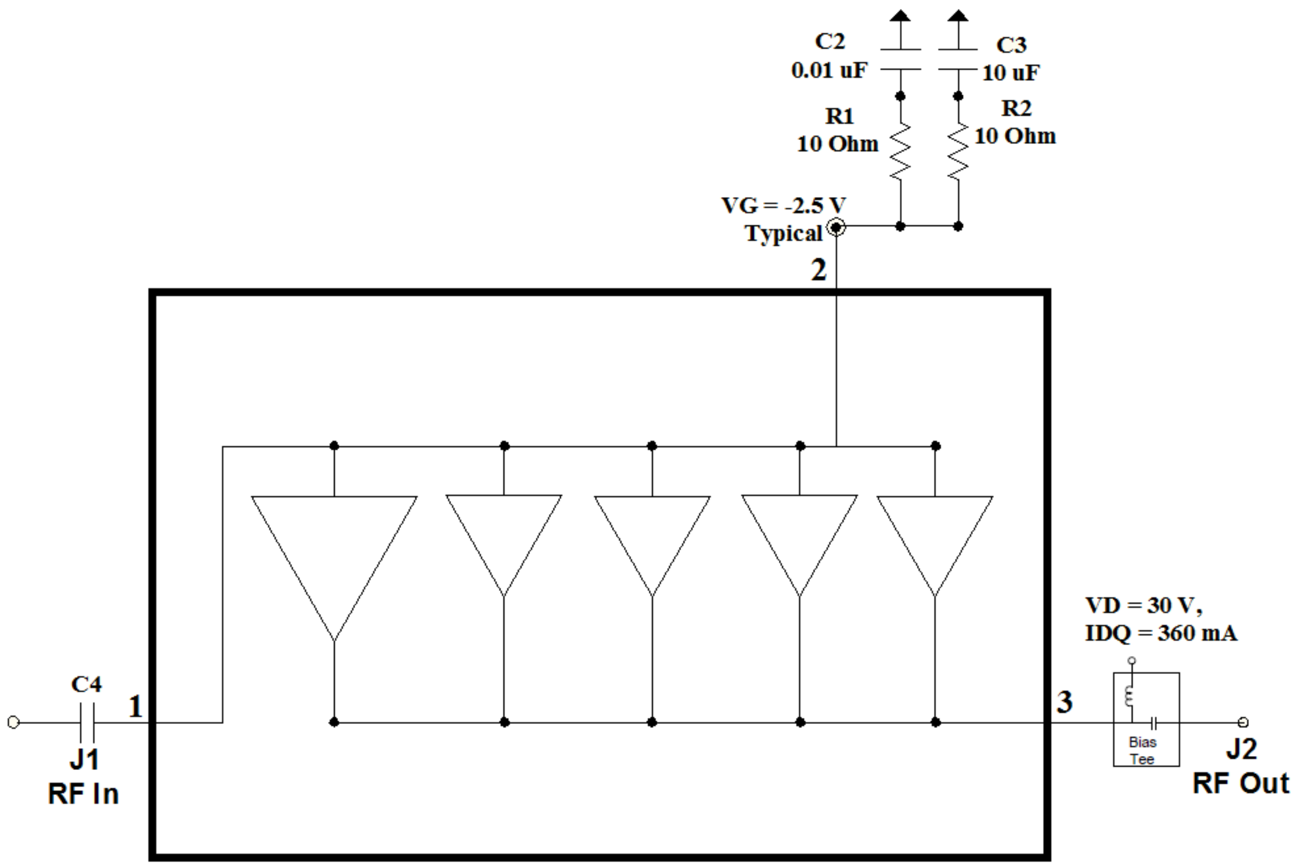
Typical Performance

The plots below reflect performance measured between external bias tee and on-board bias tee
(See application circuit on pages 10 and 12)





Application Circuit (Coaxial input DC block and coaxial output bias tee)



Notes:

1. Coaxial input DC block (C4) is used for input port (RF In.)
2. External wide bandwidth Bias-Tee is used for output port (RF Out). V_D is applied through the output Bias-Tee.

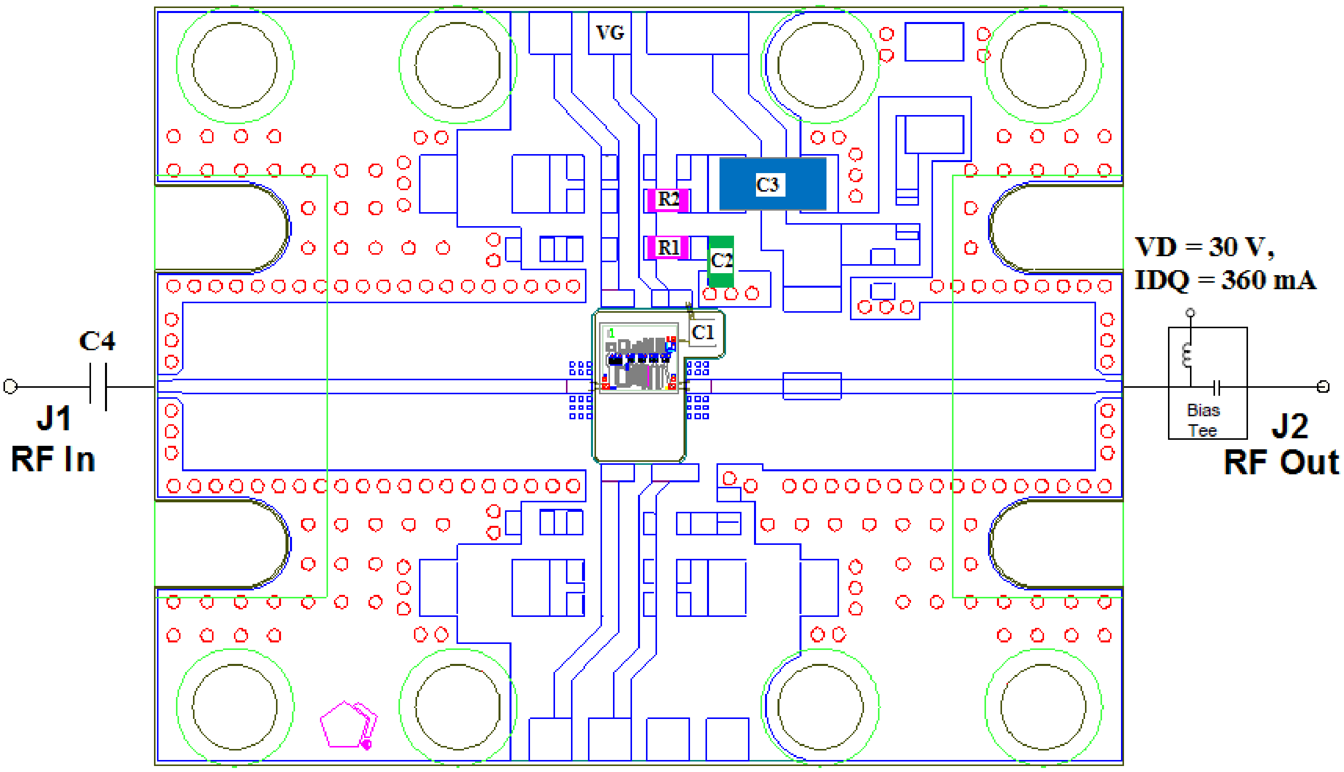
Bias-up Procedure

1. Set I_D limit to 700mA, I_G limit to 5mA
2. Set V_G to -5.0V
3. Set V_D +30V
4. Adjust V_G more positive until I_{DQ} = 360mA (V_G ~ -2.5V Typical)
5. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Reduce V_G to -5.0V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

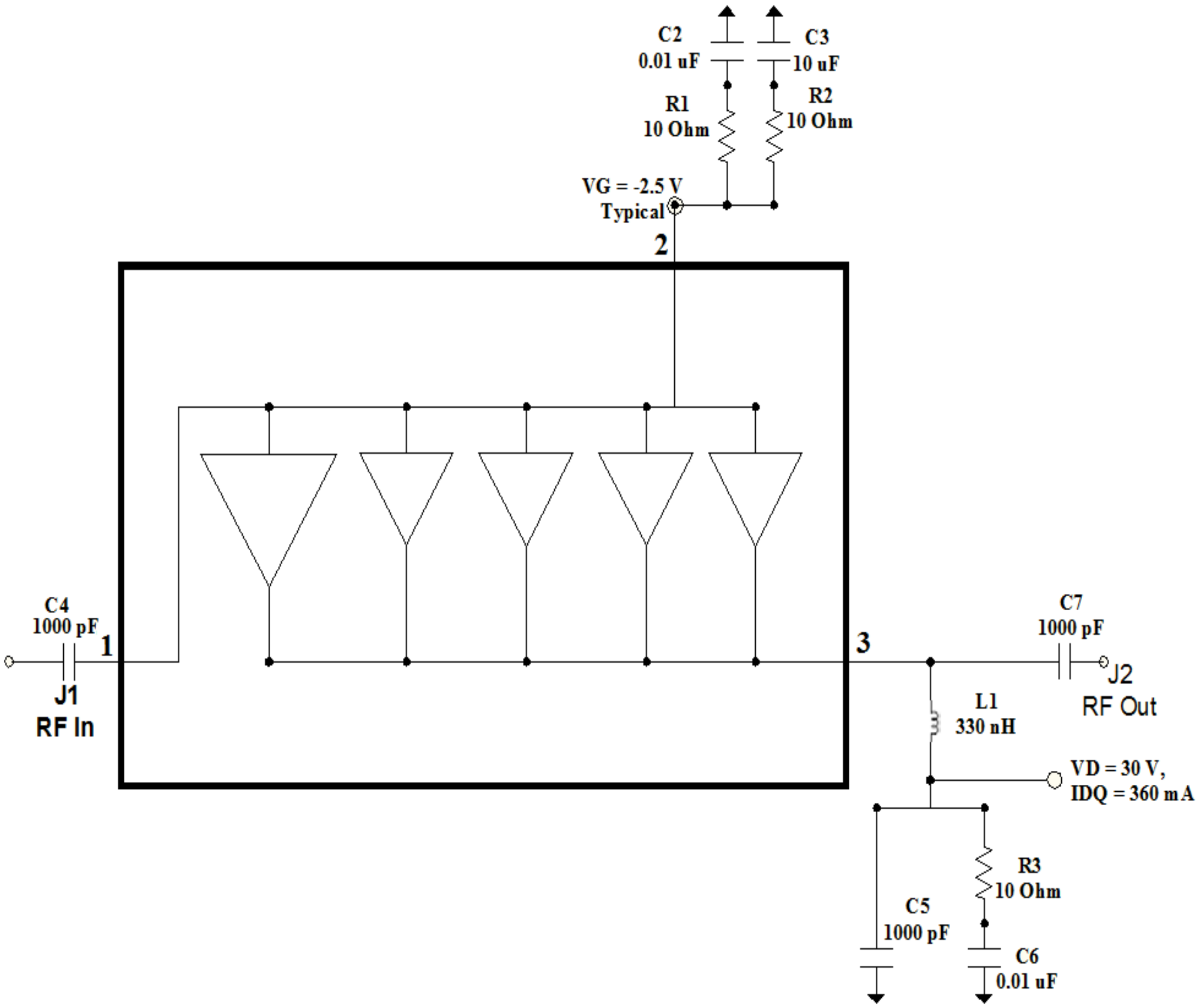
Assembly Drawing (Coaxial input DC block and coaxial output bias tee)



Bill of Materials

Reference Design	Value	Description	Manufacturer	Part Number
C1	1000pF	SLC, 50V	Various	
C2	0.01uF	Cap, 0402, 50V, 10%, X7R	Various	
C3	10uF	Cap, 1206, 50V, 10%, X7R	Various	
C4		DC Block	Various	
R1 – R2	10Ω	Res, 0402	Various	

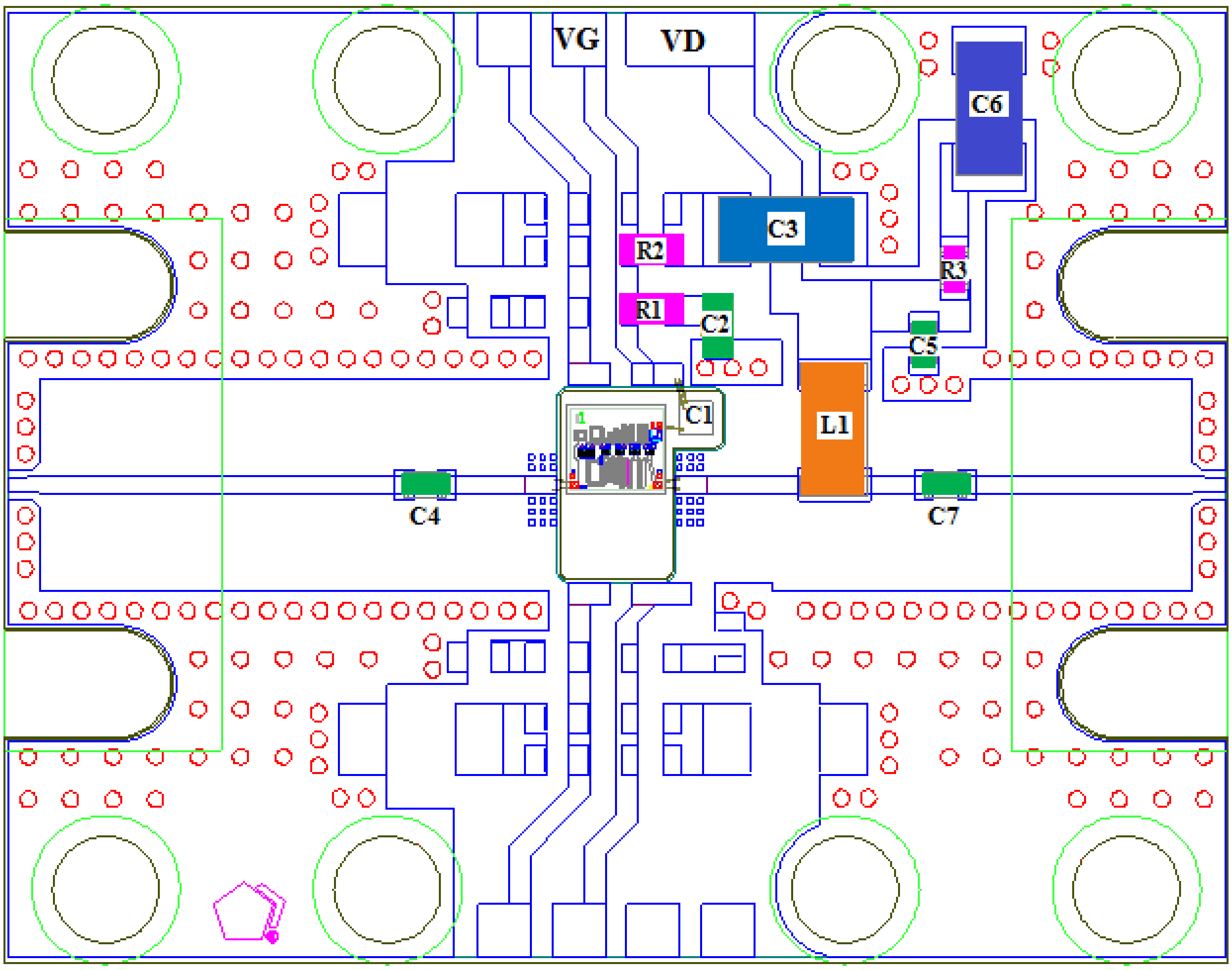
Application Circuit (Option with board-level DC blocks and output bias tee)



Note:

1. Performance of the MMIC with surface mount DC blocks and bias tee components may be degraded relative to the coaxial option. These components should be optimized for the desired operational bandwidth.

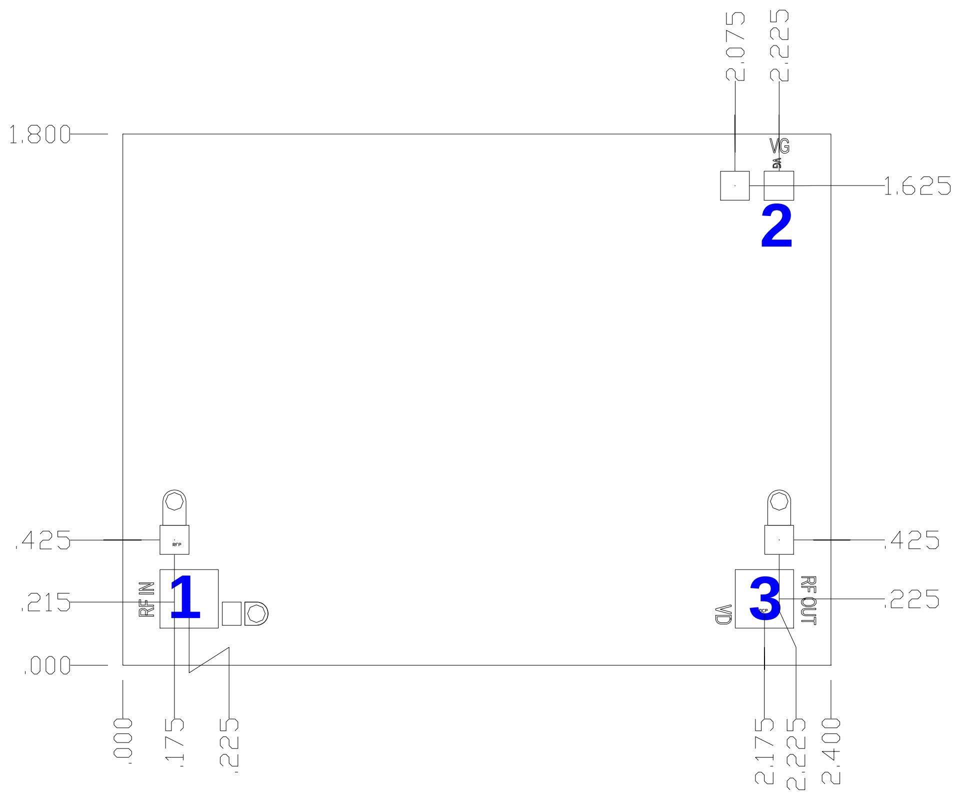
Evaluation Board Layout with On-Board DC Blocks and Output Bias-T Option



Bill of Materials For On-Board Bias-Tee

Reference Design	Value	Description	Manufacturer	Part Number
C4, C5, C7	1000pF	Cap, 0402, 100V, 10%, X7R	Various	
C6	0.01uF	Cap, 1206, 100V, 10%, X7R	Various	
L1	330nH	Ind, 1206, 100V, 10%, X7R	Various	
R3	10Ω	Res, 0402	Various	

Mechanical Drawing & Bond Pad Description



Unit: millimeters
Thickness: 0.10
Die x, y size tolerance: +/- 0.050
Chip edge to bond pad dimensions are shown to center of pad
Ground is backside of die

Bond Pad	Symbol	Pad Size	Description
1	RF In	0.198 x 0.198	RF Input; DC block is required.
2	V_G	0.100 x 0.100	Gate voltage, bias network is required; see Application Circuit on pages 10 and 12 as an example.
3	RF Out/ V_D	0.198 x 0.198	Output; Drain voltage, bias network is required; see Application Circuit on pages 10 and 12 as an example.

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

Solderability

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_{4}0_{2}$) Free
- PFOS Free
- SVHC Free

ECCN

US Department of Commerce: EAR99

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email:	**info-sales@triquint.com**	**Fax:**	**+1.972.994.8504**

For technical questions and application information: **Email: info-products@triquint.com**

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