TGA2627-SM

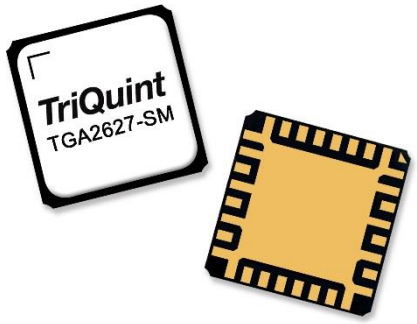
6 – 12 GHz GaN Driver Amplifier

Product Description

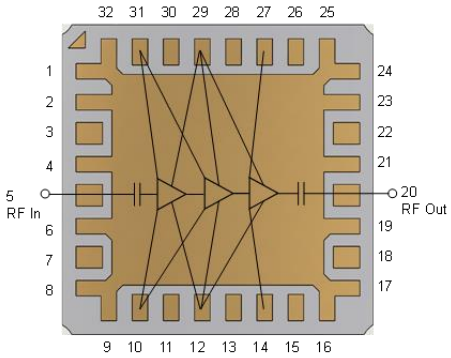
Qorvo's TGA2627-SM is a push-pull driver amplifier fabricated on Qorvo's TQGaN25 0.25um GaN on SiC production process. The TGA2627-SM operates from 6 to 12 GHz and provides 32 dBm of output power with 18 dB of large signal gain and greater than 20 % power-added efficiency. The push-pull topology yields > 40dB of harmonic suppression at Psat.

Using GaN MMIC technology and air-cavity ceramic QFN packaging, the TGA2627-SM provides a low cost driver solution that provides the added benefit of operating on the same voltage rail as the corresponding GaN HPA. It can also serve as the output power amplifier on lower power architectures.

The TGA2627-SM is offered in a 5x5 mm air-cavity QFN with an aluminum nitride base and LCP lid. It is well-matched to 50 ohms and includes integrated DC blocking caps on both RF ports allowing for simple system integration.



Functional Block Diagram



Top View

Product Features

- Frequency Range: 6 - 12 GHz
- Push-Pull Configuration
- Low Harmonic Content; -40 dBc @ Psat
- Small Signal Gain: 27 dB
- Power: 32 dBm
- PAE: 24 % @ 32 dBm RF output
- Harmonic Suppression: 40 dBc @ Psat
- IM3: -20 dBc @ 26 dBm RF output
- Input Return Loss: 15 dB
- Output Return Loss: 10 dB
- Bias: V_D = 25 V, I_{DQ} = 200 mA
- Package Dimensions: 5.0 x 5.0 x 1.42 mm

Applications

- Commercial and military radar
- Communications
- Electronic Warfare (EW)

Ordering Information

Part No.	Description
TGA2627-SM	6 – 12 GHz 2W GaN Driver Amplifier
1121067	TGA2627-SM Evaluation Board

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_D)		25		V
Drain Current (I_{DQ})		200		mA
Drain Current Under RF Drive (I_{D_DRIVE})		See plots		mA
Gate Voltage (V_G)		−2.5		V
Gate Current Under RF Drive (I_{G_DRIVE})		See plots		mA
Temperature (T_{BASE})	−40		+85	°C

Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Min	Typ	Max	Units
Operating Frequency Range	6		12	GHz
Output Power (@ Pin = 13 dBm)		32		dBm
Power Added Efficiency (@ Pin = 13 dBm)		24		%
Small Signal Gain		27		dB
Input Return Loss		16		dB
Output Return Loss		10		dB
IM3 (P_{OUT}/tone < 26 dBm)		-20		dBc
2nd Harmonic Suppression		-40		dBc
3rd Harmonic Suppression		-40		dBc
Output Power Temperature Coefficient		-0.012		dB/°C

Test conditions unless otherwise noted: T_{BASE} = +25 °C, V_D = +25 V, IDQ= 200 mA, VG = -2.5V typical, CW Mode
Data de-embedded to reference planes

Absolute Maximum Ratings

Parameter	Range / Value	Units
Drain Voltage (V_D)	40	V
Gate Voltage Range (V_G)	-8 to 0	V
Drain Current (I_D)	550	mA
Gate Current (I_G) at Tch = 200 °C	11.2	mA
Power Dissipation (P_{DISS}), 85 °C	12.3	W
Input Power (P_{IN}), CW, 50 Ω, V_D=25 V, I_{DQ}=100 mA, 85 °C,	30	dBm
Input Power (P_{IN}), CW, VSWR 10:1, V_D=25 V, I_{DQ}=100 mA, 85 °C	27	dBm
Mounting Temperature (30 Seconds)	260	°C
Storage Temperature	-55 to 150	°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

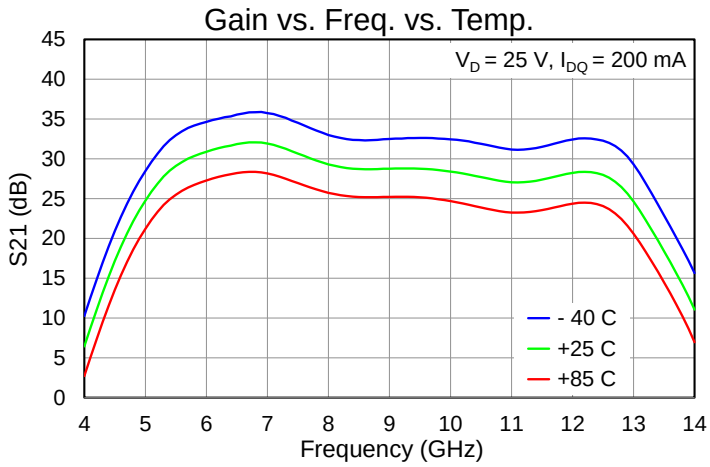
Thermal and Reliability Information

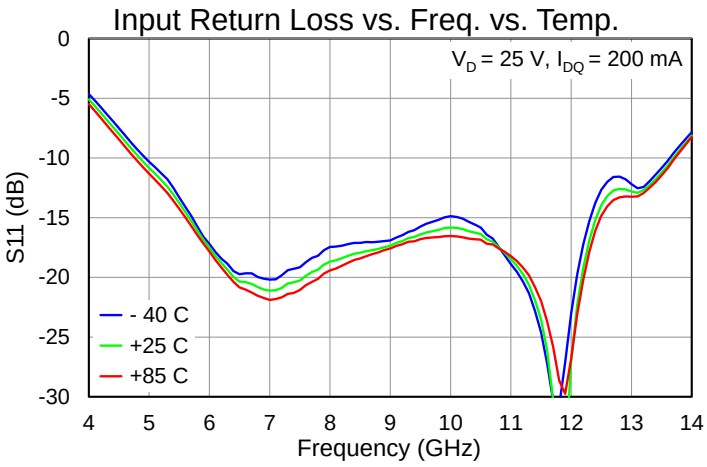
Parameter	Values	Units	Conditions
Under Drive, Thermal Resistance (θ_{JC}) (1,2,3)	7.12	°C/W	T_{BASE} = 85 °C, V_D = +25 V, CW I_{D_DRIVE} = 390 mA P_{IN} = +15 dBm, P_{OUT} = +31 dBm, P_{DISS} = 8.5 W
Channel Temperature (T_{CH})	145.5	°C	

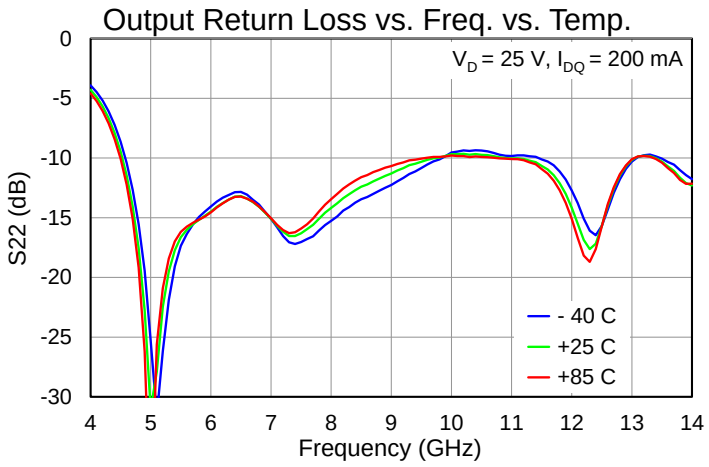
Notes:
1. Thermal resistance is measured to package backside
2. Base or ambient temperature is 85 °C
3. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Performance Plots – Small Signal

Test conditions unless otherwise specified: V_D = 25 V, I_{DQ} = 200 mA, V_G = -2.5 V Typical, CW, 25 °C



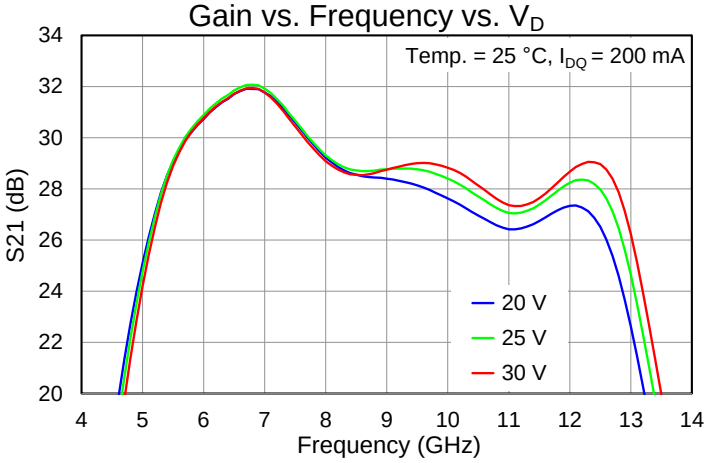




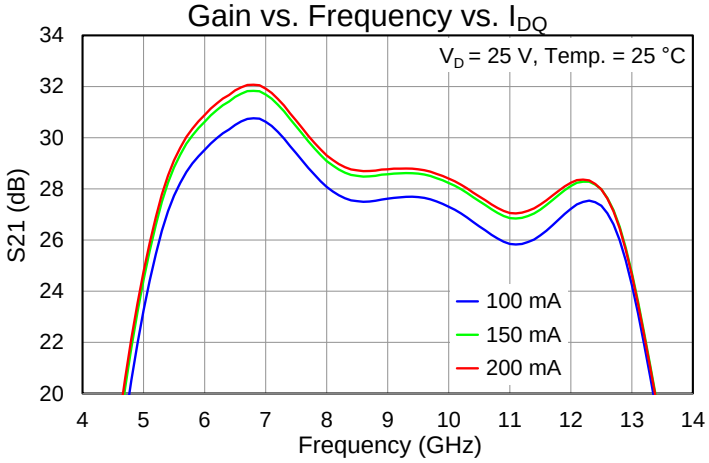
Performance Plots – Small Signal

Test conditions unless otherwise specified: V_D = 25 V, I_{DQ} = 200 mA, V_G = -2.5 V Typical, CW, 25 °C

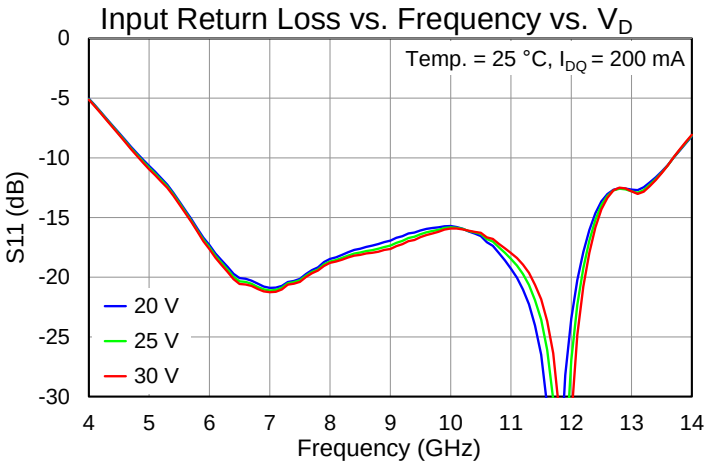
Gain vs. Frequency vs. V_D



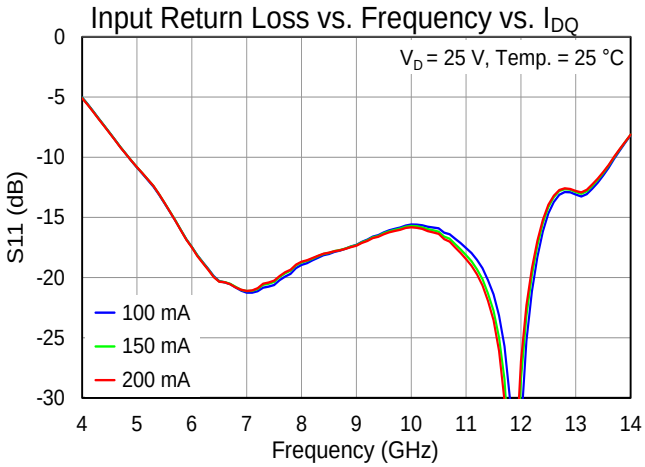
Gain vs. Frequency vs. I_{DQ}



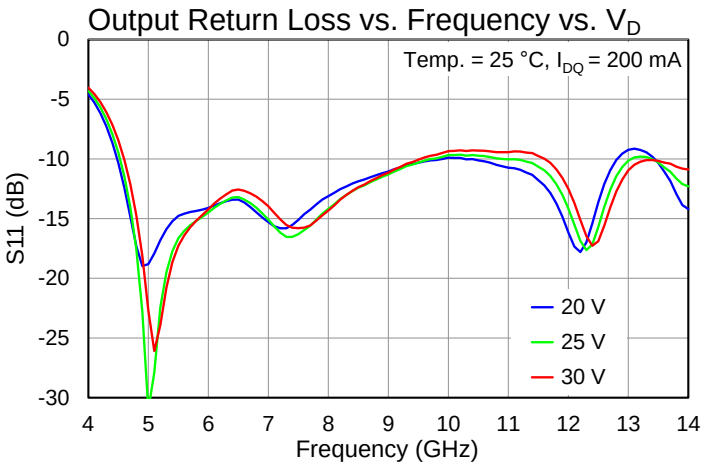
Input Return Loss vs. Frequency vs. V_D



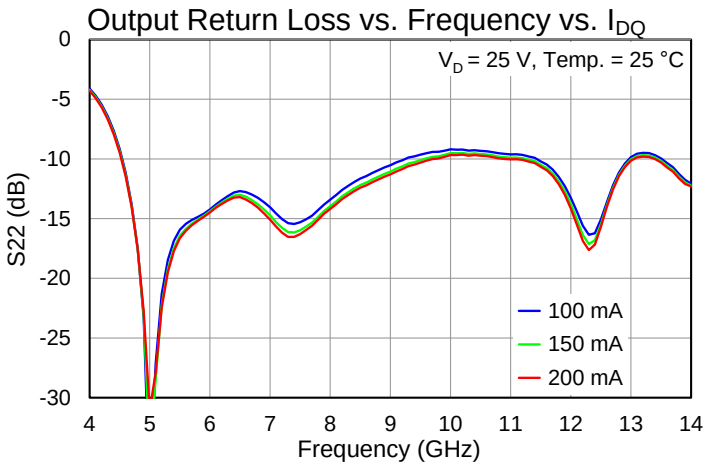
Input Return Loss vs. Frequency vs. I_{DQ}



Output Return Loss vs. Frequency vs. V_D



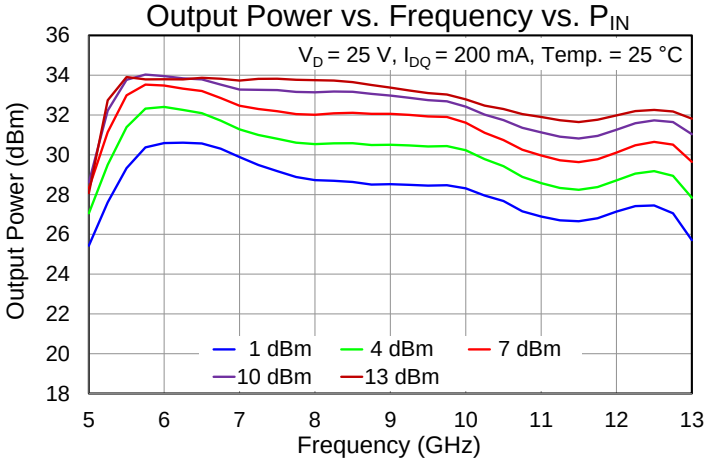
Output Return Loss vs. Frequency vs. I_{DQ}



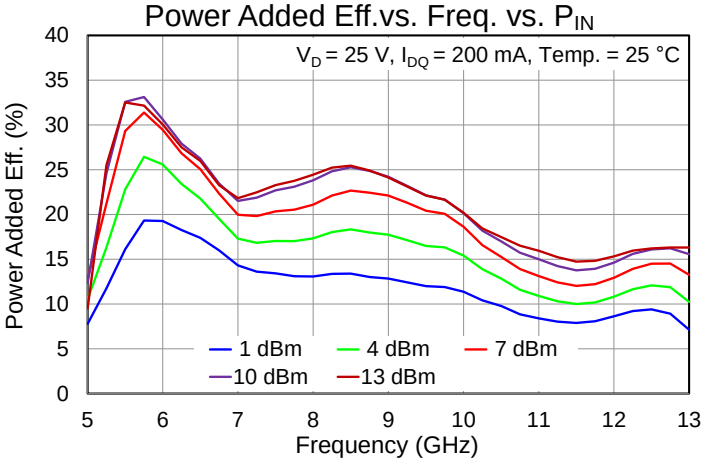
Performance Plots – Large Signal

Test conditions unless otherwise specified: V_D = 25 V, I_{DQ} = 200 mA, V_G = -2.5 V Typical, CW, 25 °C

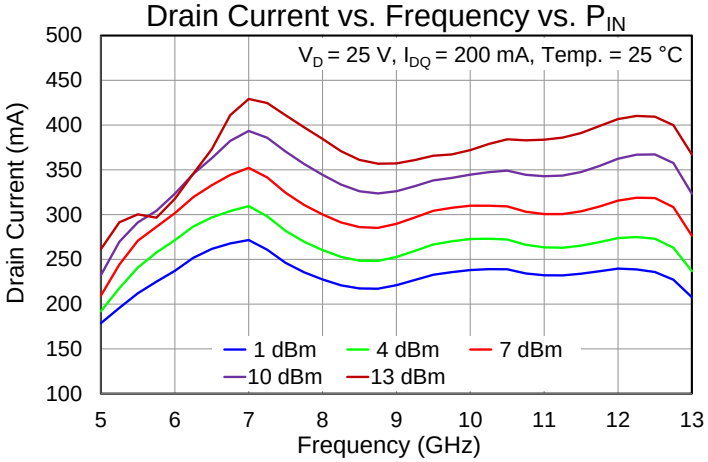
Output Power vs. Frequency vs. P_{IN}



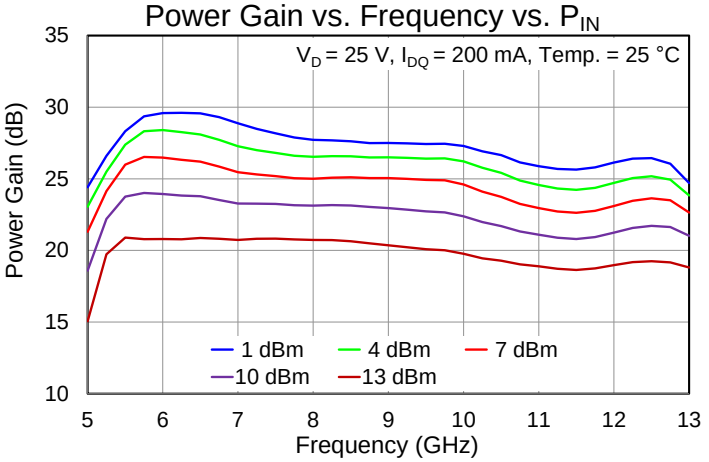
Power Added Eff.vs. Freq. vs. P_{IN}



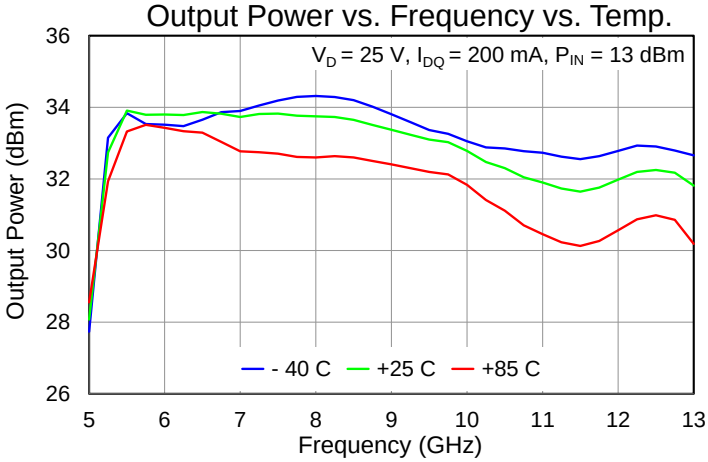
Drain Current vs. Frequency vs. P_{IN}



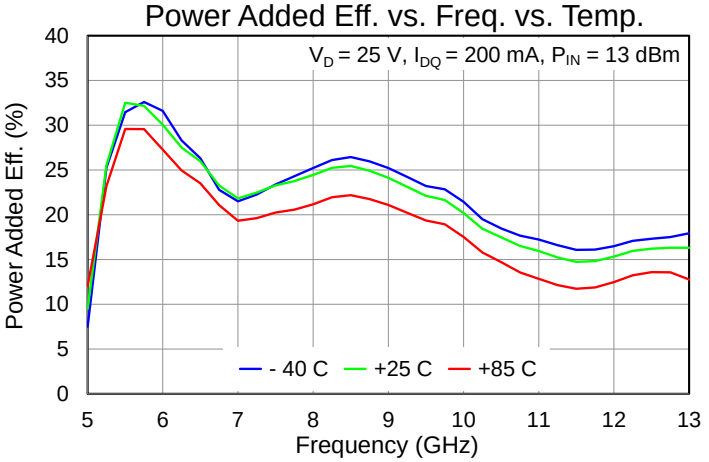
Power Gain vs. Frequency vs. P_{IN}



Output Power vs. Frequency vs. Temp.



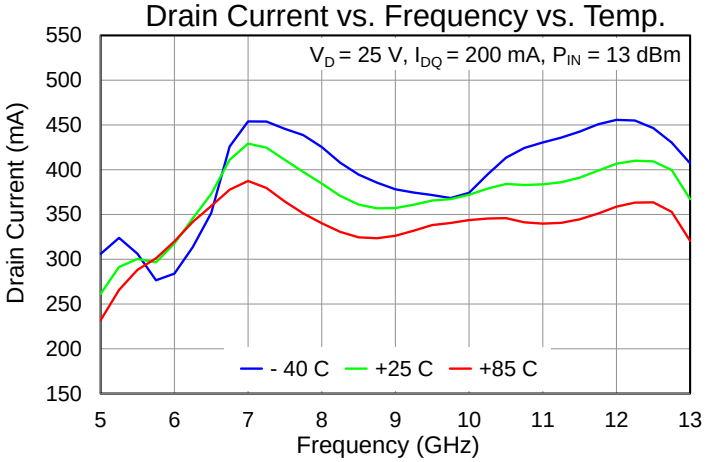
Power Added Eff. vs. Freq. vs. Temp.



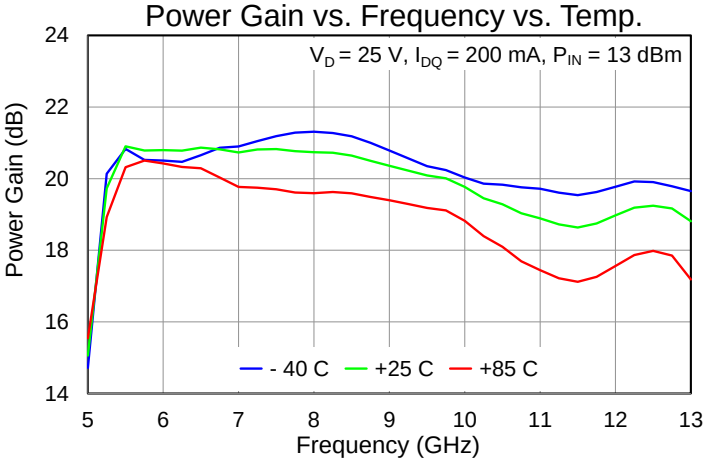
Performance Plots – Large Signal

Test conditions unless otherwise specified: V_D = 25 V, I_{DQ} = 200 mA, V_G = -2.5 V Typical, CW, 25 °C

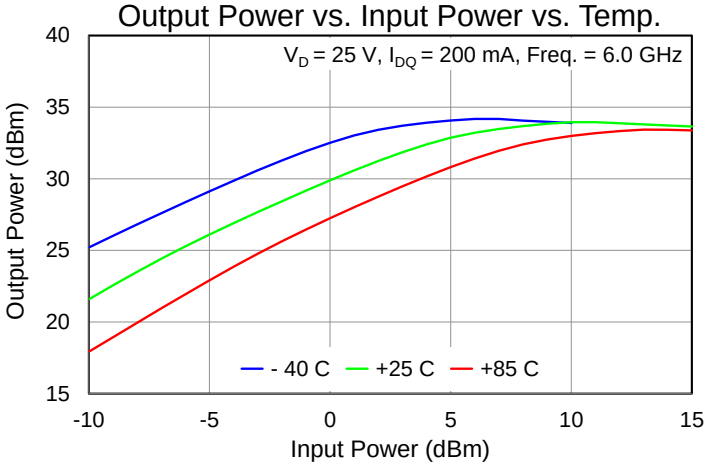
Drain Current vs. Frequency vs. Temp.



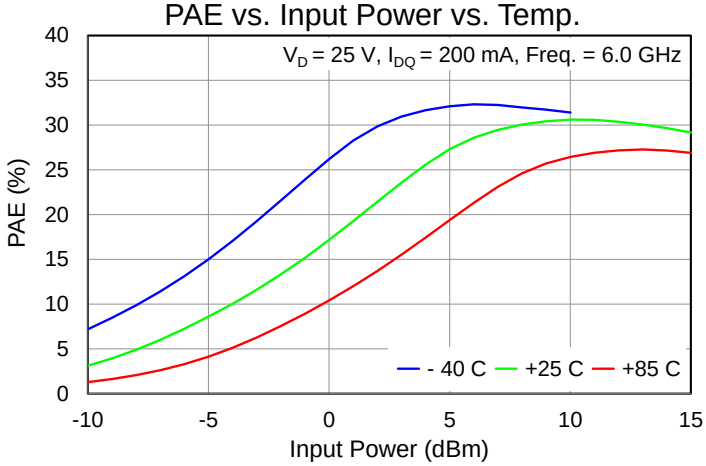
Power Gain vs. Frequency vs. Temp.



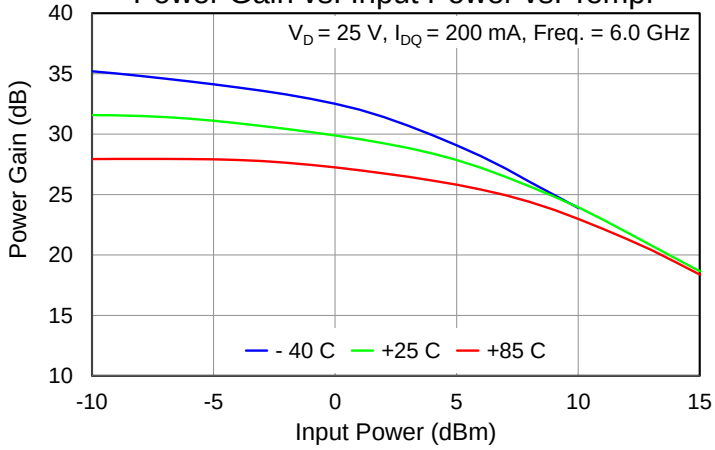
Output Power vs. Input Power vs. Temp.



PAE vs. Input Power vs. Temp.



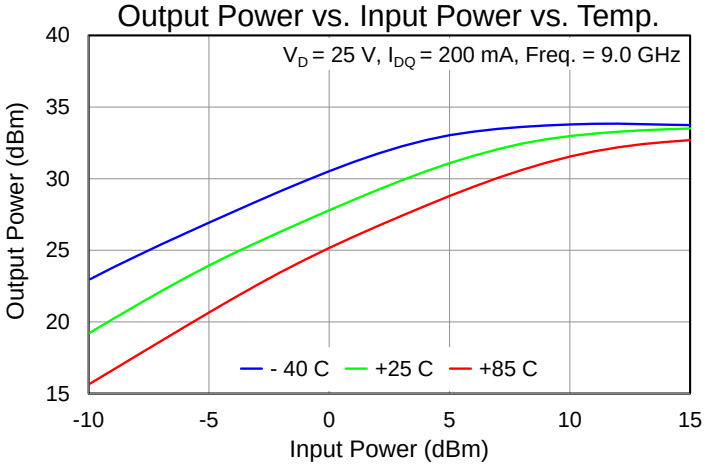
Power Gain vs. Input Power vs. Temp.



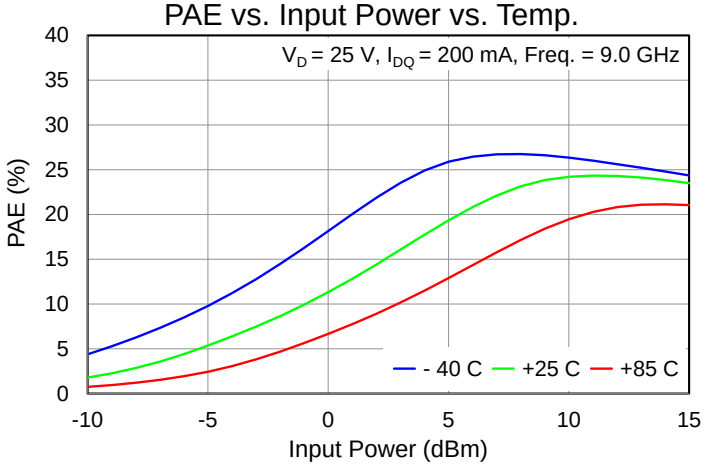
Performance Plots – Large Signal

Test conditions unless otherwise specified: V_D = 25 V, I_{DQ} = 200 mA, V_G = -2.5 V Typical, CW, 25 °C

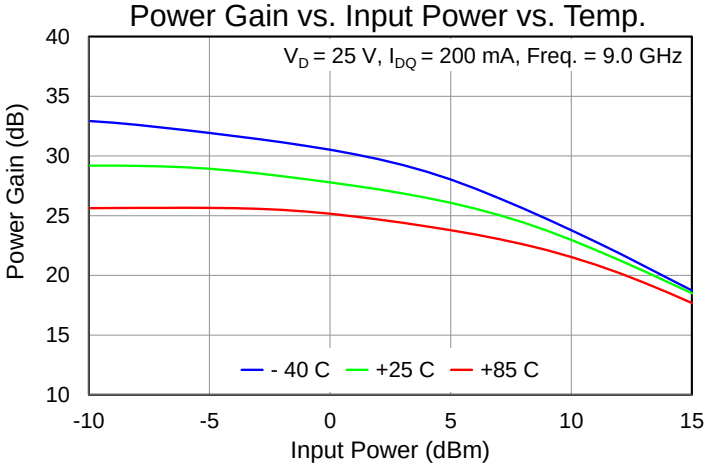
Output Power vs. Input Power vs. Temp.



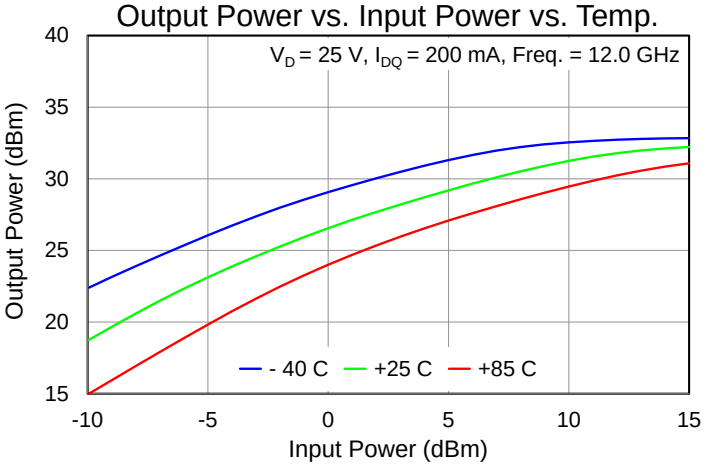
PAE vs. Input Power vs. Temp.



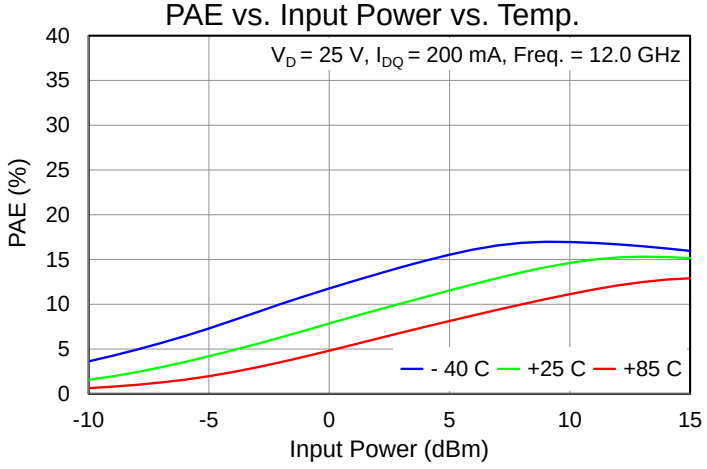
Power Gain vs. Input Power vs. Temp.



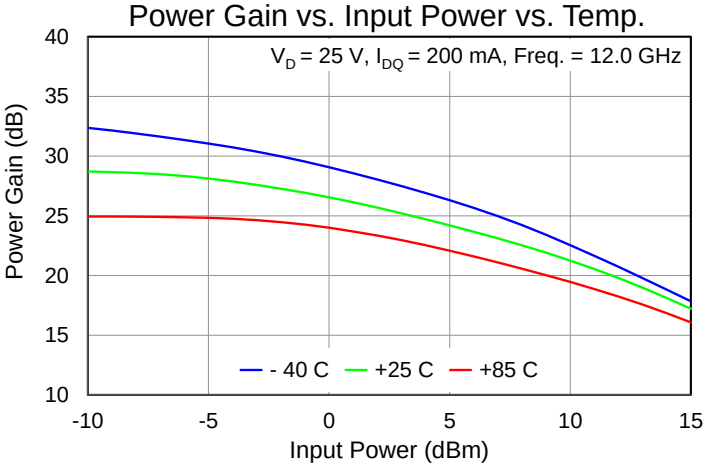
Output Power vs. Input Power vs. Temp.



PAE vs. Input Power vs. Temp.



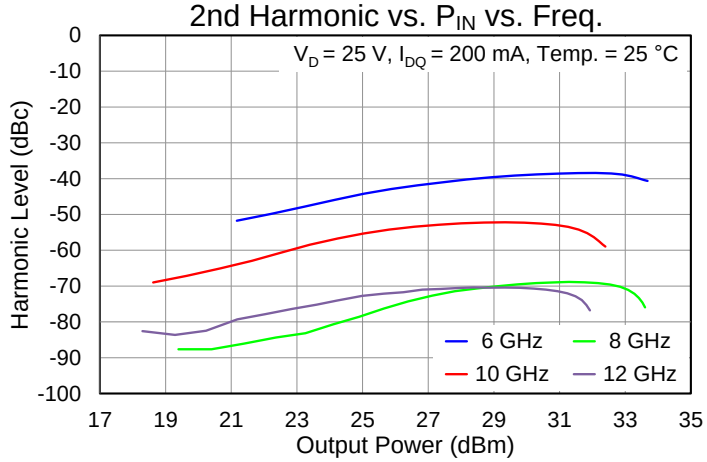
Power Gain vs. Input Power vs. Temp.



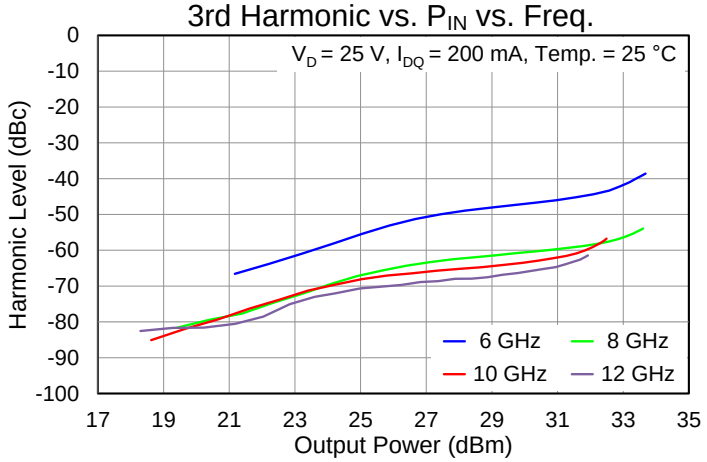
Performance Plots – Harmonics and Linearity

Test conditions unless otherwise specified: V_D = 25 V, I_{DQ} = 100 mA, V_G = -2.5 V Typical, CW, 25 °C

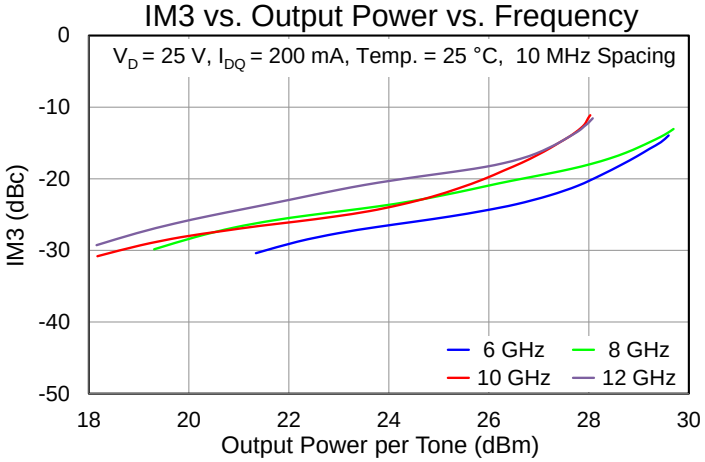
2nd Harmonic vs. P_{IN} vs. Freq.



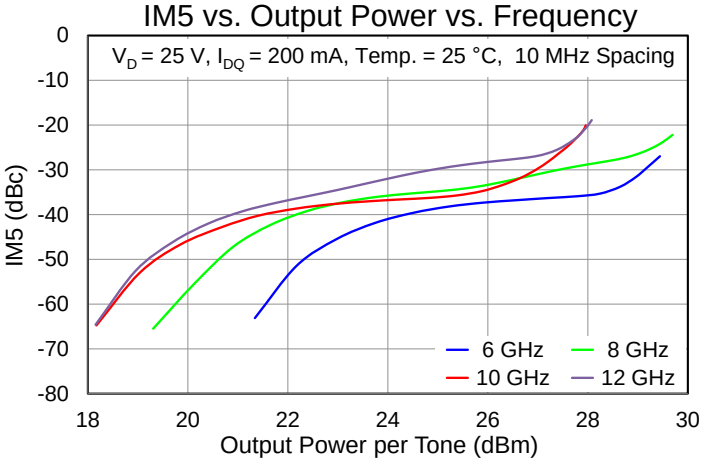
3rd Harmonic vs. P_{IN} vs. Freq.



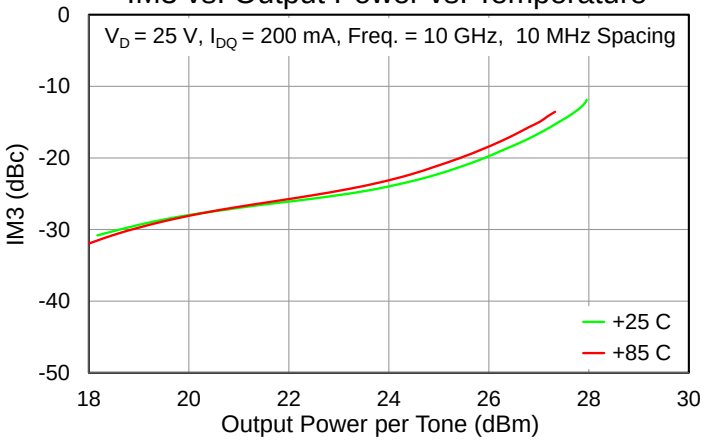
IM3 vs. Output Power vs. Frequency



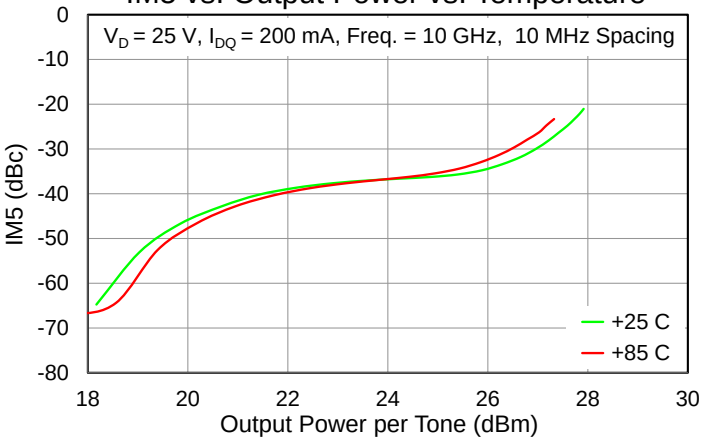
IM5 vs. Output Power vs. Frequency



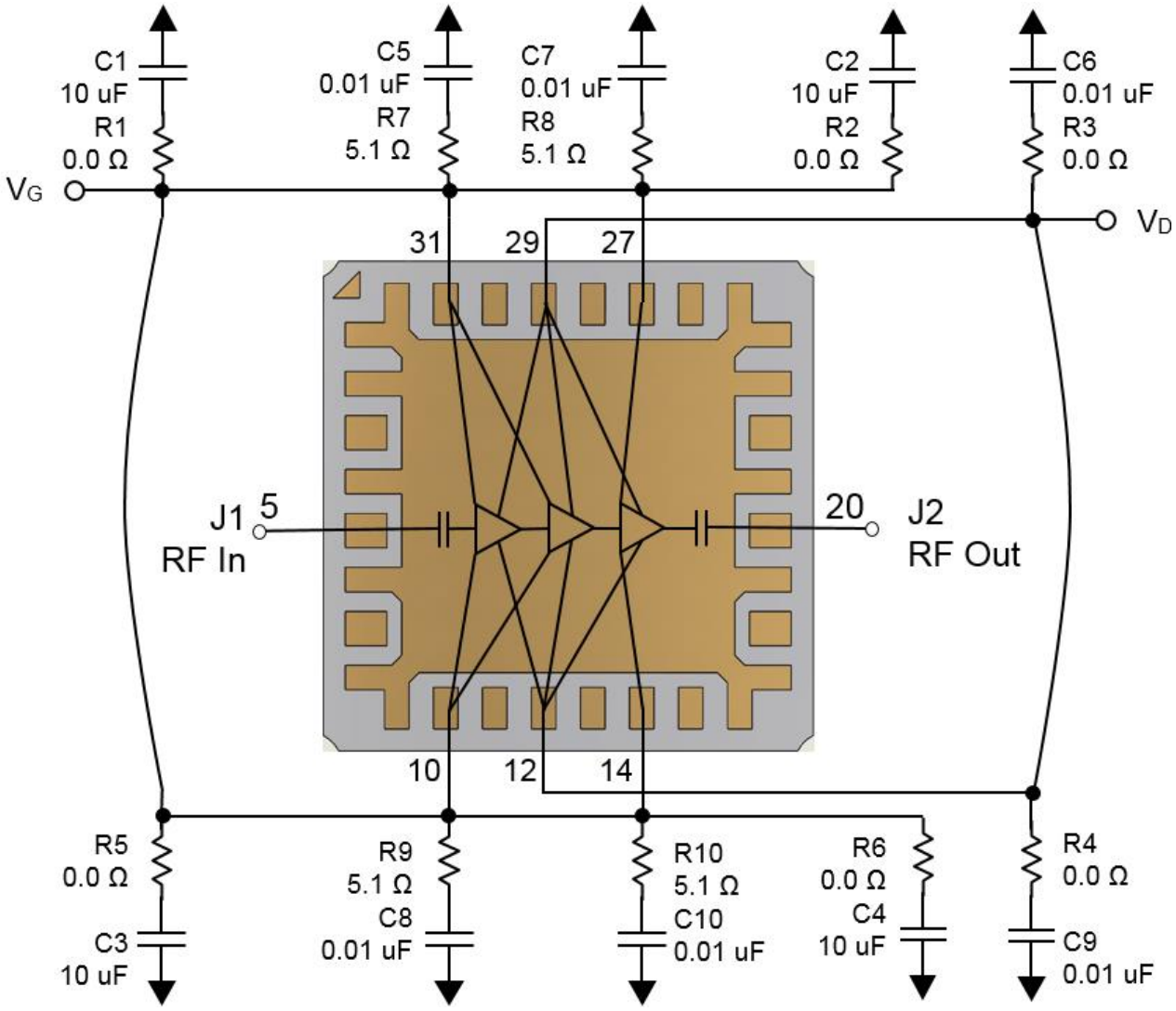
IM3 vs. Output Power vs. Temperature



IM5 vs. Output Power vs. Temperature



Application Circuit



Note: Device shown is for top view
Both sides V_D and V_{G12} and V_{G3} must be biased and recommend to connect together as shown

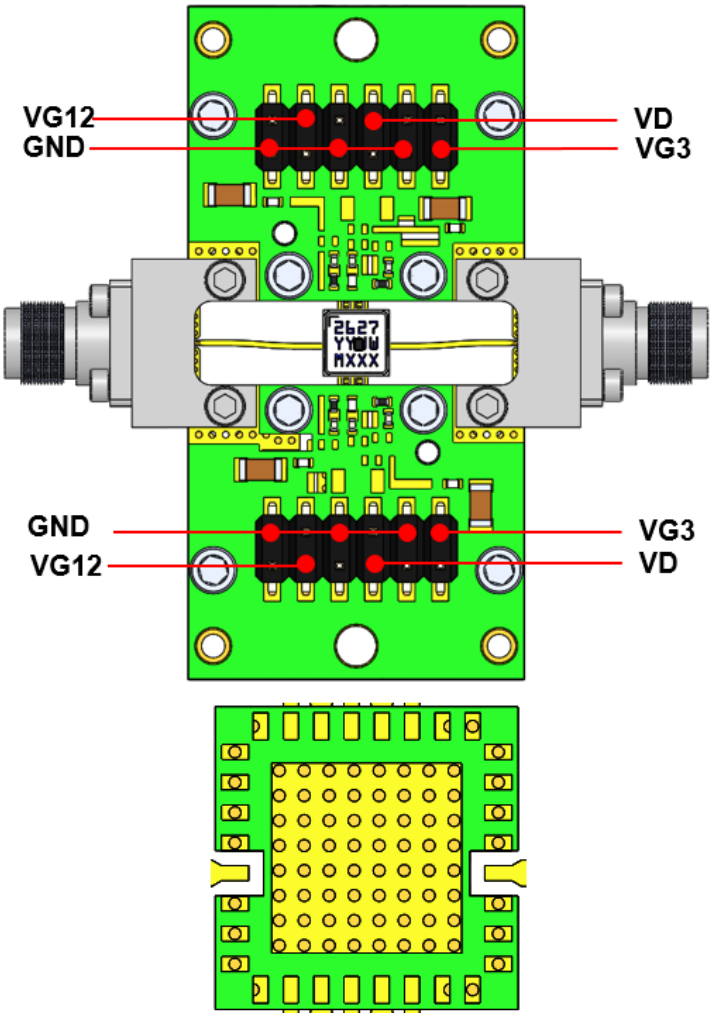
Bias Up Procedure

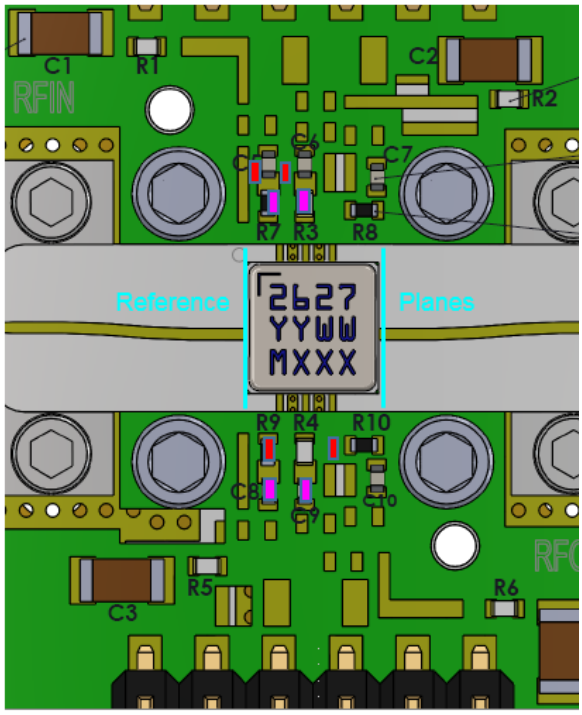
1. Set I_D limit to 320 mA, I_G limit to 4 mA
2. Apply −5 V to V_G
3. Apply +25 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 100 mA (V_G ~ −2.5 V Typ.).
5. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

EVB and BOM





- C5 - C10, 0.01 uF
- C1 - C4, 10 uF
- R7 - R10, 5.1 Ohm
- R1 - R6, 0 Ohm

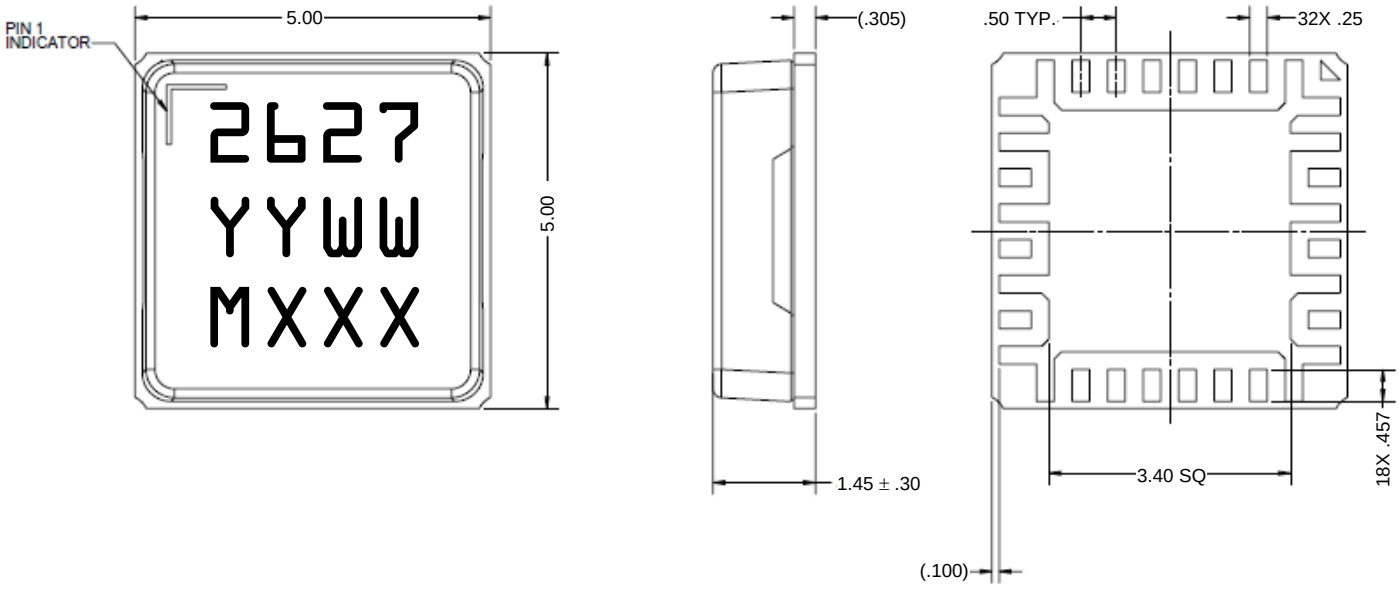
RF Layer is 0.008" thick Rogers Corp. RO4003C, ε_r = 3.38. Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-5.

The trace pattern shown has been developed and tested for optimized assembly at Qorvo Semiconductor. The PCB land pattern has been developed to accommodate lead tolerances. Since processes vary from company to company, careful process development is recommended

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C5 – C10	0.01 pF	Cap., 50V, 10% X7R, 0402	Various	
C1 – C4	10 uF	Cap., 50V, 10% X5R, 1206	Various	
R7 – R10	5.1 Ohms	Resistor, 0402	Various	
R1 – R6	0.0 Ohms	Resistor, 0402	Various	

Pin Configuration and Description



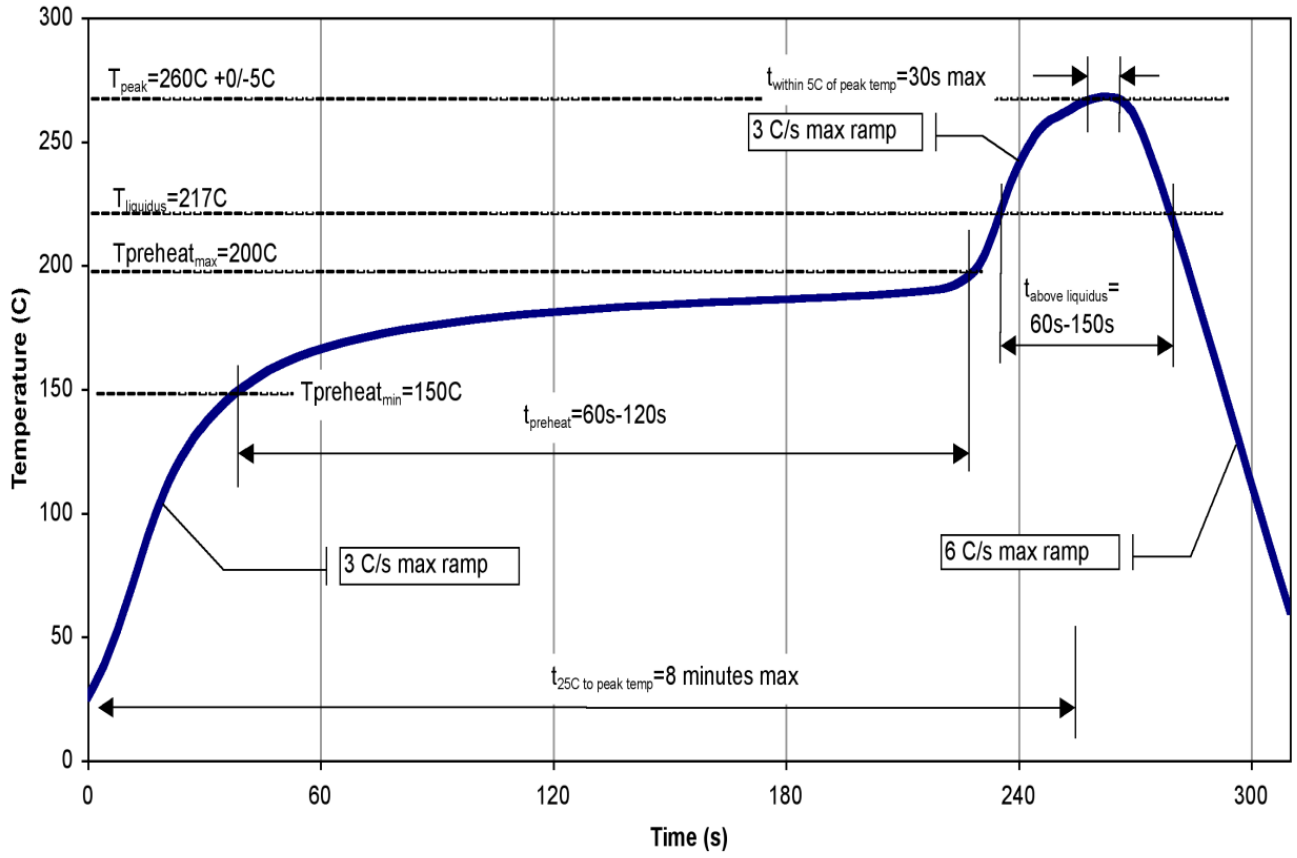
Dimensions in mm
Package lead finish: Ni / Au plating with minimum gold thickness of 0.1 um
Materials: Base: Ceramic, Lid: Plastic, Part is epoxy sealed
Part Marking: 2627: Part Number, YY = Part Assembly Year, WW = Part Assembly Week, MXXX = Batch ID

Pin No.	Label	Description
1-4, 6-9,11, 13, 15-19, 21-26, 28, 30, 32	GND	Connected to ground paddle (33); must be grounded to PCB to improve isolation.
5	RF Input	RF input, matched to 50 Ω, DC blocked
10, 31	V_{G12}	Gate voltage, 1st and 2nd stages. Bias network required on both sides.
12, 29	V_D	Drain voltage. Bias network required on both sides.
14, 27	V_{G3}	Gate voltage, 3rd stage. Bias network required on both sides.
20	RF Output	RF output, matched to 50 Ω, DC blocked
33	GND	Backside paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

Solderability

1. Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C.
2. The use of no-clean solder to avoid washing after soldering is recommended.

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C3	ESDA / JEDEC JS-002-2014
MSL – Convection Reflow 260 °C	3	JEDEC standard IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: **1-844-890-8163**

Web: www.qorvo.com

Email: customer.support@qorvo.com

For technical questions and application information: **Email:** appsupport@qorvo.com

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