TGA2814-SM

3.1–3.5 GHz 80 W GaN Power Amplifier

General Description

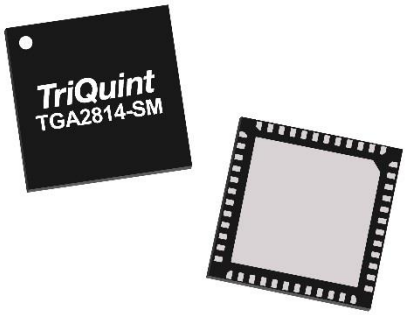
Qorvo's TGA2814-SM is a high-power, S-band amplifier fabricated on Qorvo's production 0.25 um GaN on SiC process (QGaN25).The TGA2814-SM covers 3.1–3.5 GHz and provides >80 W of saturated output power, 24 dB of large-signal gain, and achieves 55 % power-added efficiency.

The TGA2814-SM can also support a variety of operating conditions to best support system requirements. With good thermal properties, it can support a range of bias voltages and performs well under pulse operation.

With DC blocking capacitors on both RF ports, which are matched to 50 ohms, the TGA2814-SM is ideal for both commercial and military radar systems.

Lead-free and RoHS compliant.

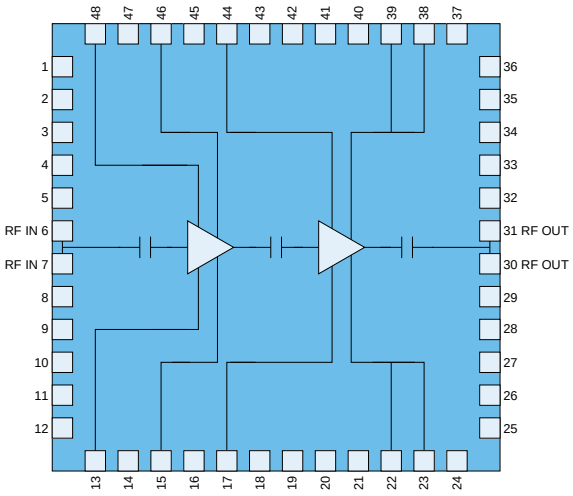
Evaluation boards are available on request.



Product Features

- Frequency Range: 3.1–3.5 GHz
- Output Power: 49.5 dBm (at Pin = 25 dBm)
- Power Gain >24 dB (at Pin = 25 dBm)
- PAE: 55% (at Pin = 25 dBm)
- Bias: V_D = 30 V, I_{DQ} = 200 mA
- Package Dimensions: 7.0 x 7.0 x 0.85 mm

Functional Block Diagram



Applications

- Military Radar
- Commercial Radar

Ordering Information

Part	Description
TGA2814-SM	3.1–3.5 GHz 80 W GaN Power Amplifier
TGA2814-SM EVB	TGA2814-SM Evaluation Board

Absolute Maximum Ratings

Parameter	Value/Range
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	–8 to 0 V
Drain Current (I_D)	8.5 A
Gate Current (I_G)	See graph pg. 10
Power Dissipation (P_{DISS})	166 W
Input Power, CW, 50 Ω, 85 °C, (P_{IN})	30 dBm
Input Power, V_{SWR} 3:1, V_D = 30 V, PW = 15 ms, DC = 30%, 85 °C, (P_{IN})	27 dBm
Storage Temperature	–55 to 150 °C

Note:

1. Max. Input Power ratings based on die data

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value/Range
Drain Voltage (V_D)	30 V
Drain Current (I_{DQ})	200 mA
Drain Current Under RF Drive (I_{D_Drive})	5500 mA
Gate Voltage Range (V_G)	−2.9 to −2.0 V (Typ.)

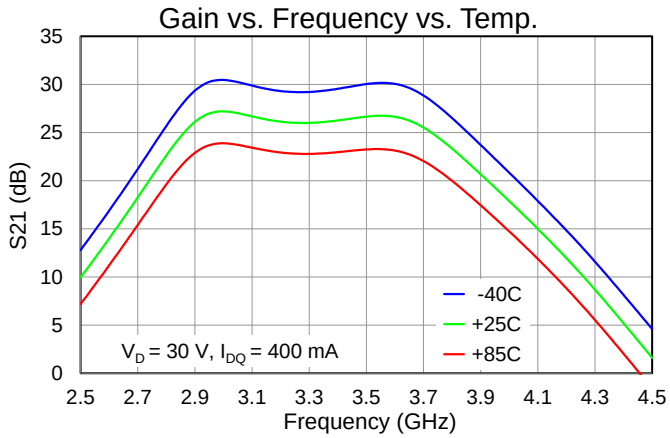
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

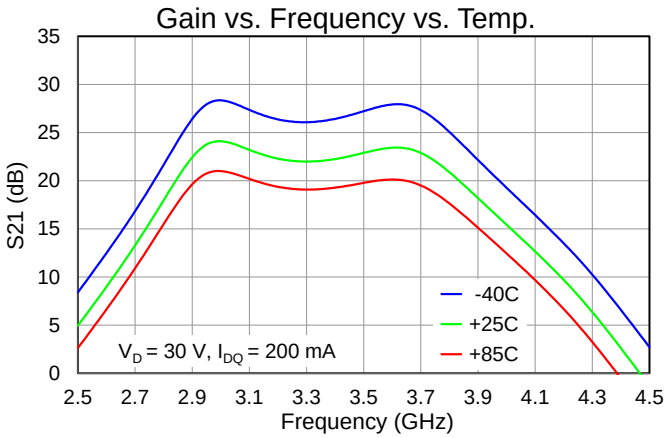
Electrical Specifications

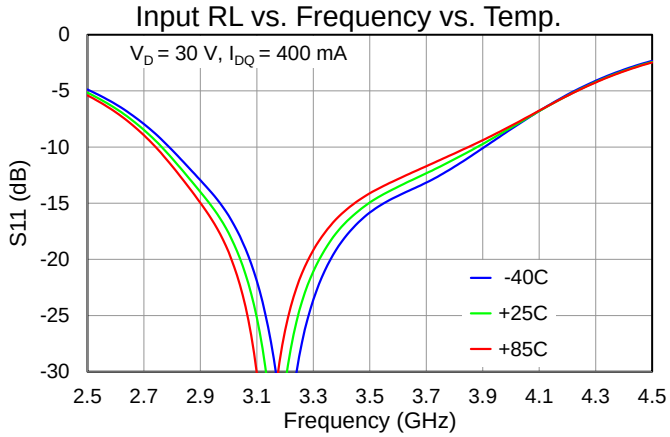
Test conditions unless otherwise noted: 25 °C, V_D = 30 V, I_{DQ} = 200 mA, PW = 100 us, D_C = 10 %

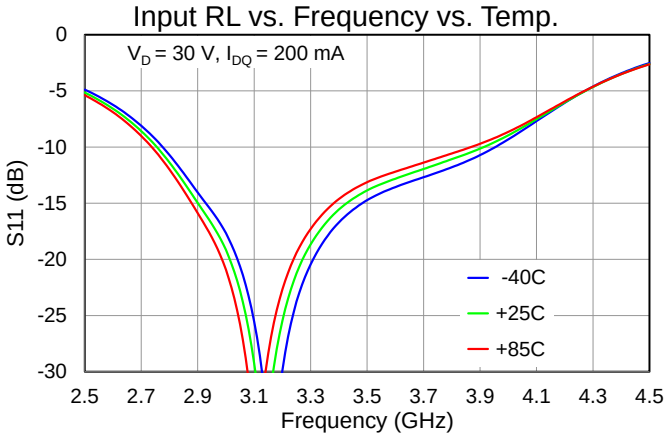
Parameter	Min	Typical	Max	Units
Operational Frequency Range	3.1		3.5	GHz
Input Return Loss (at I_{DQ} = 400 mA)		>12		dB
Output Return Loss (at I_{DQ} = 400 mA)		>7		dB
Small Signal Gain (at I_{DQ} = 400 mA)		>26		dB
Power Gain @ Saturation (Pin = 24 dBm)		>24		dB
Output Power @ Saturation (Pin = 24 dBm)		>49.5		dBm
Power Added Efficiency (Pin = 24 dBm)		>55		%
Output Power Temperature Coefficient		–0.006		dBm/°C

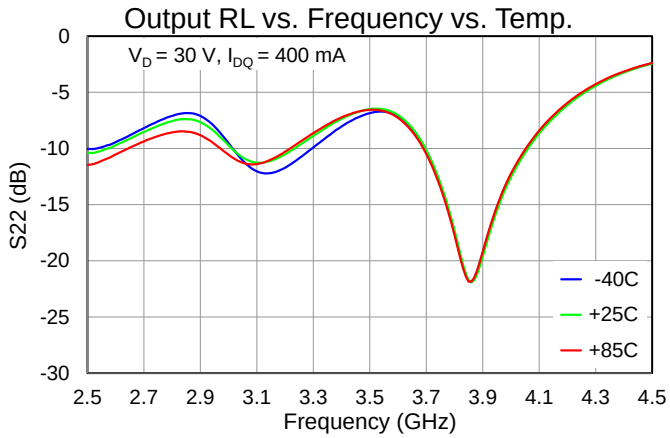
Typical Performance – Small Signal

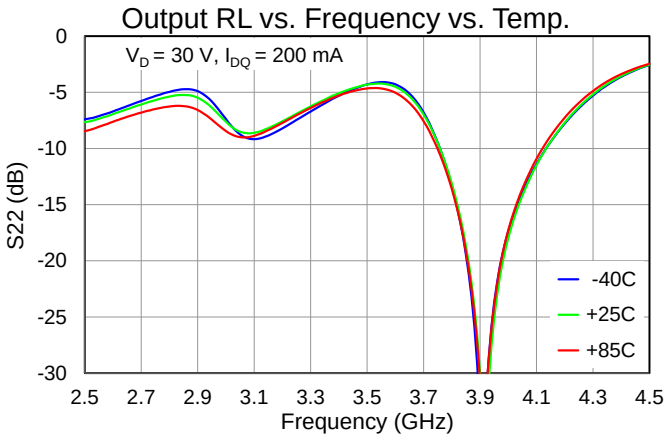




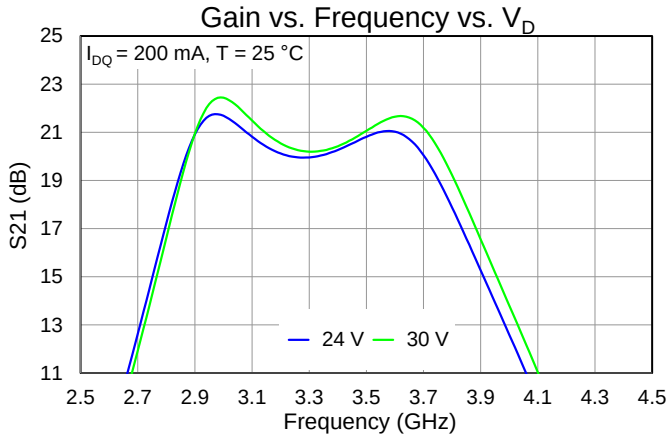


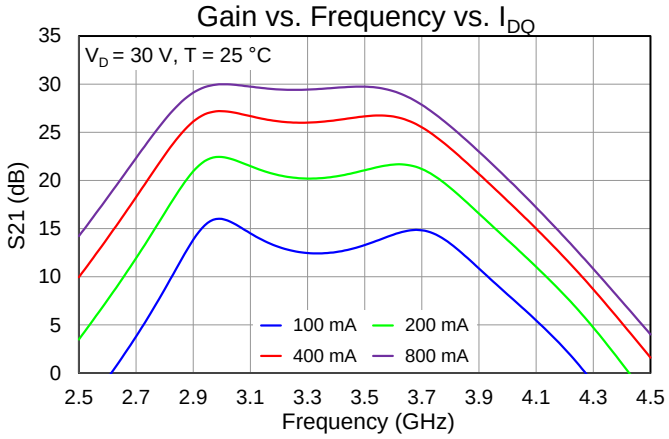


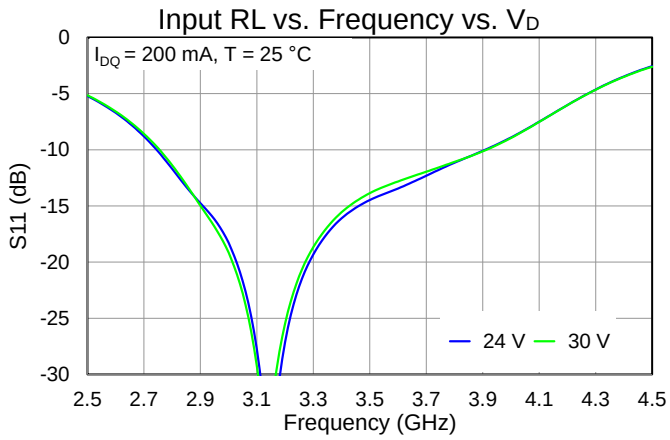


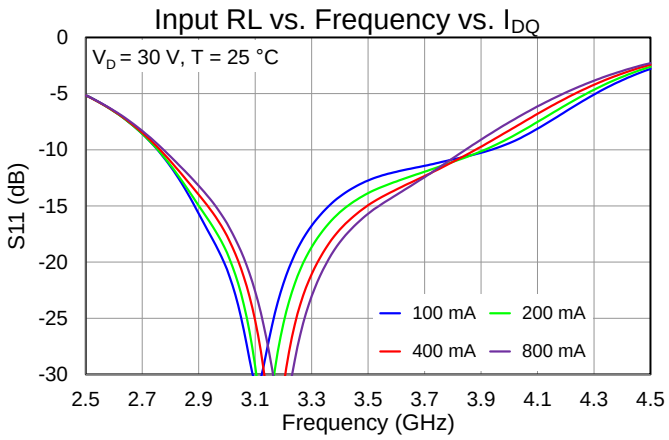


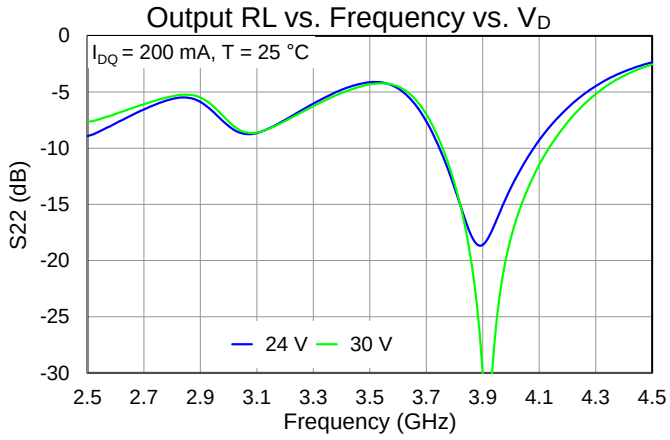
Typical Performance – Small Signal

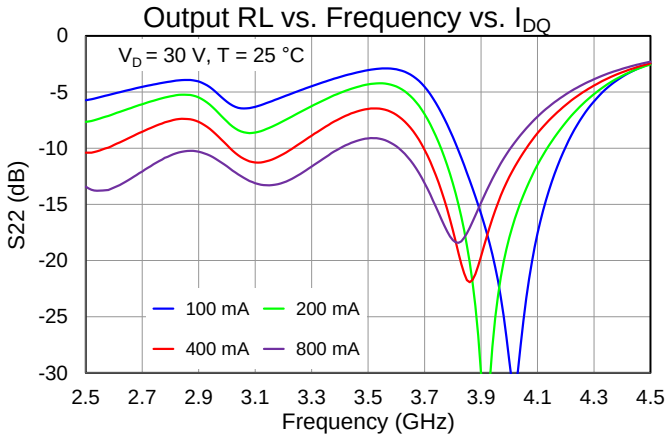






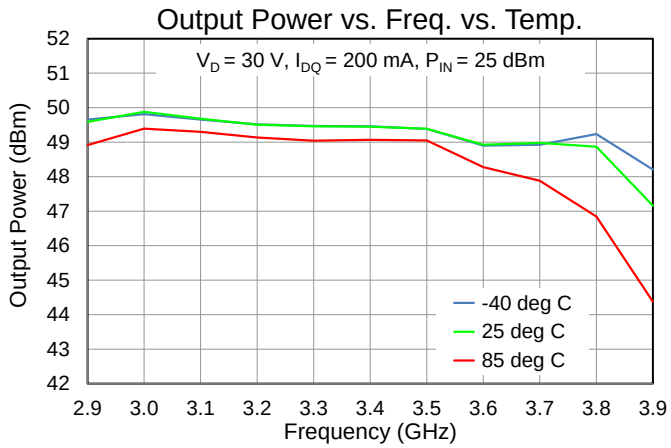


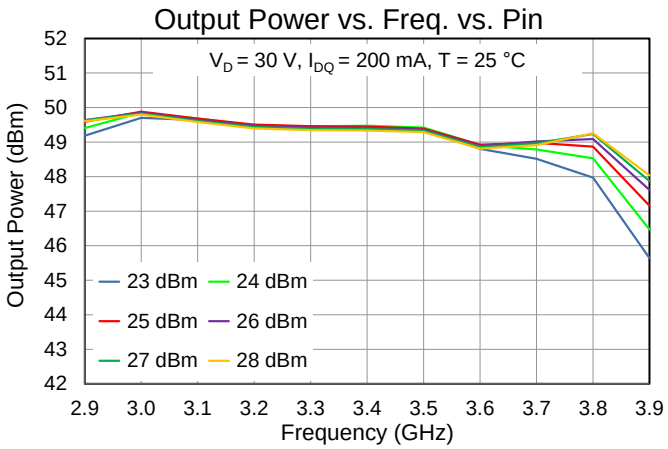


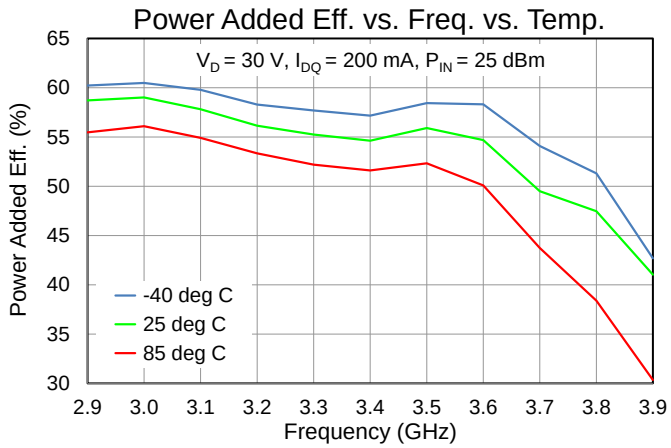


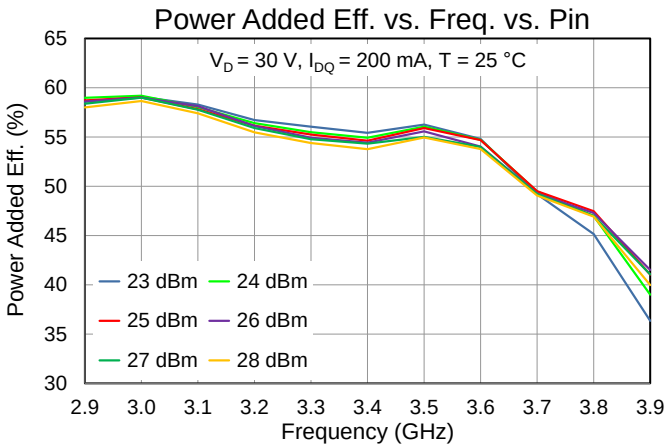
Typical Performance – Large Signal

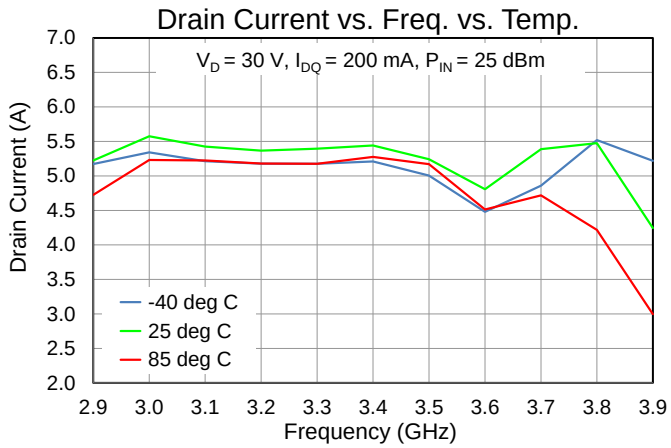
Test conditions unless otherwise noted: 25 °C, V_D = 30 V, I_{DQ} = 200 mA, PW = 100 us, DC = 10 %

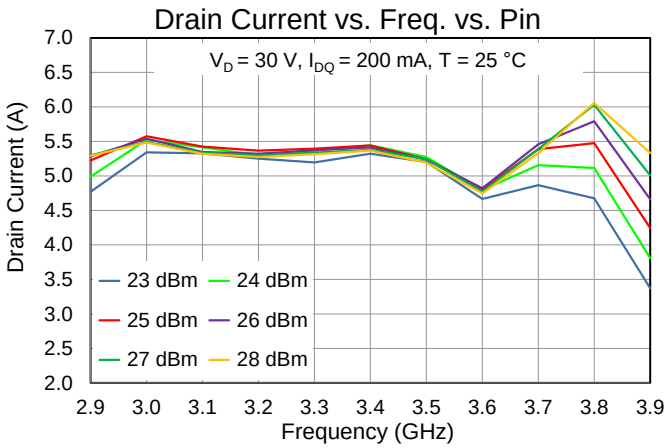












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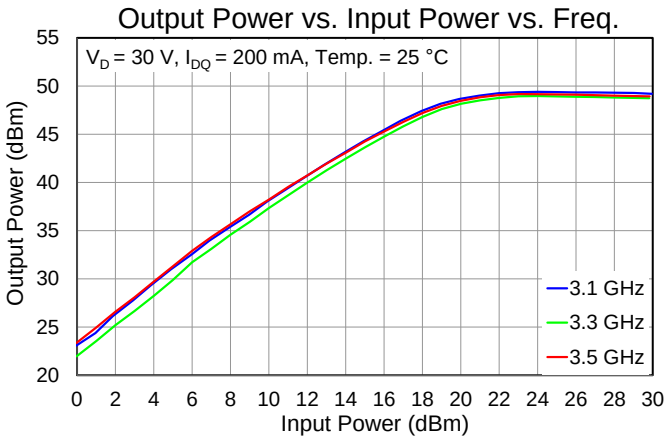

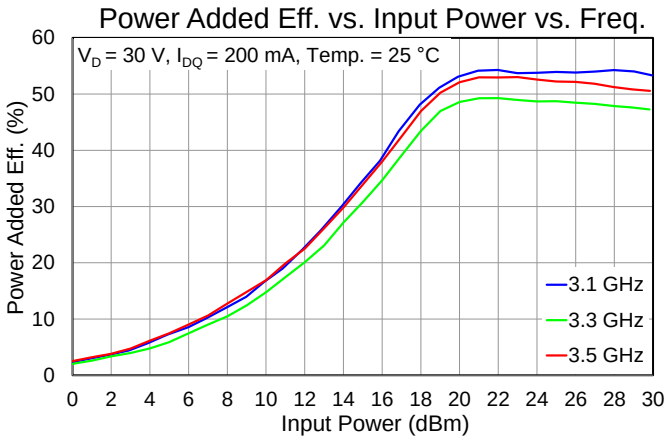

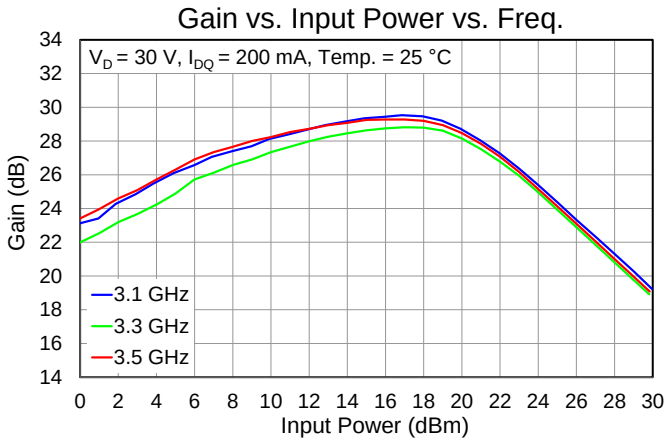

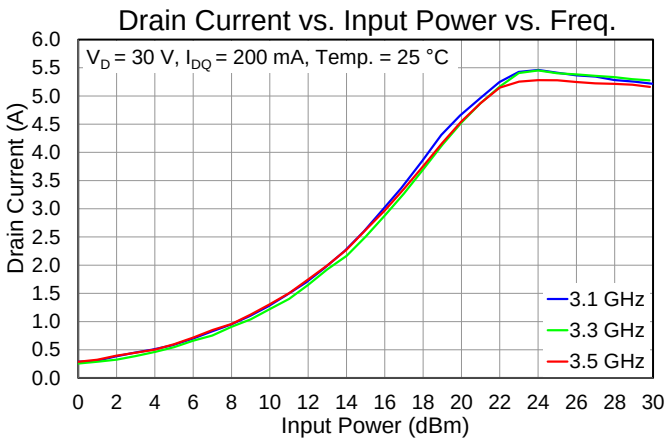

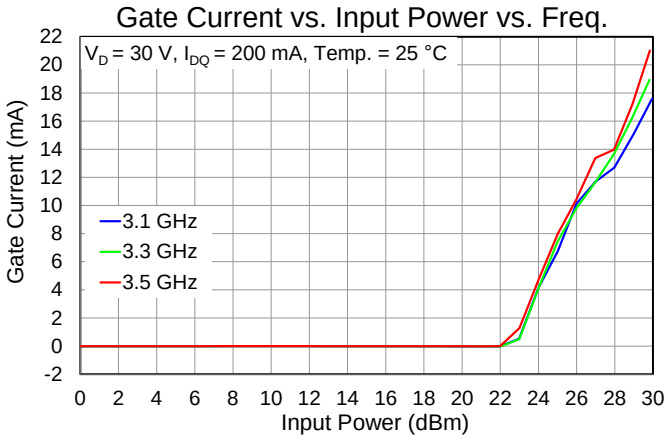

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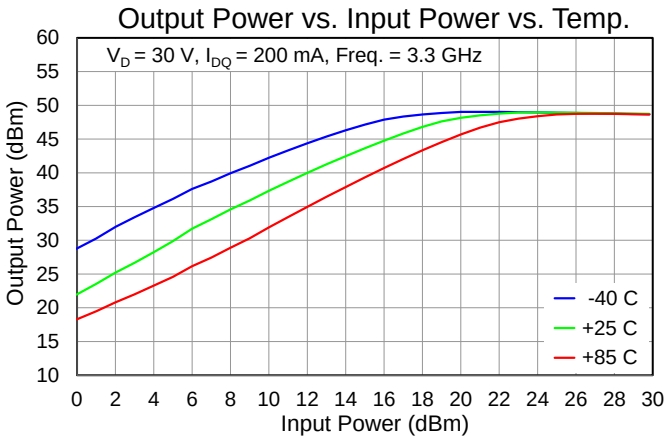

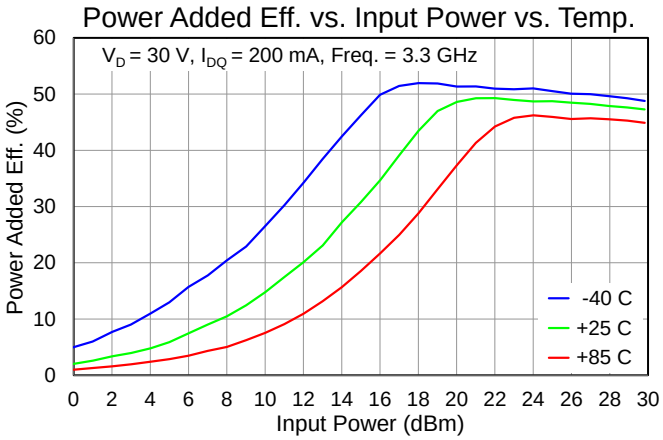

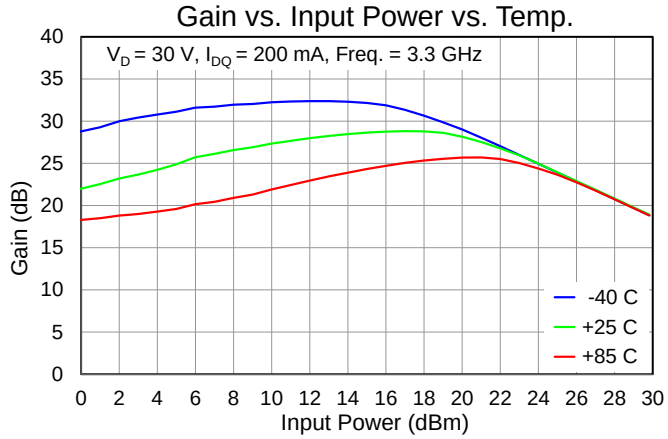

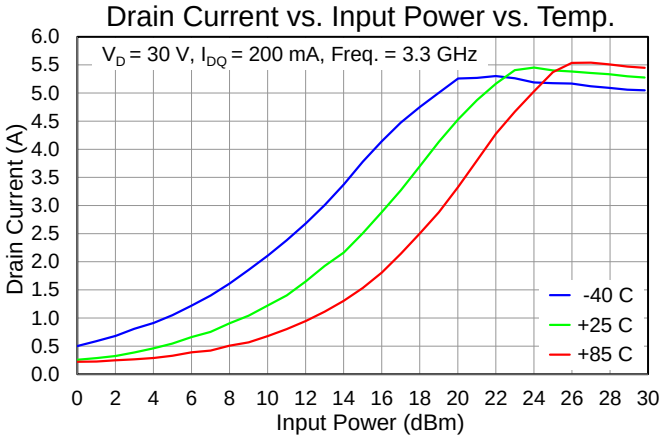

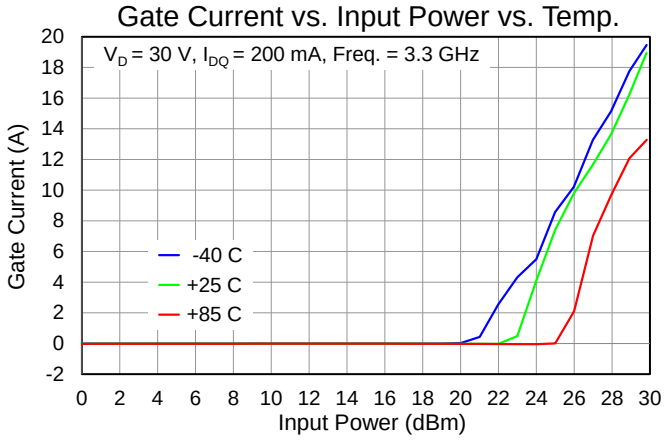

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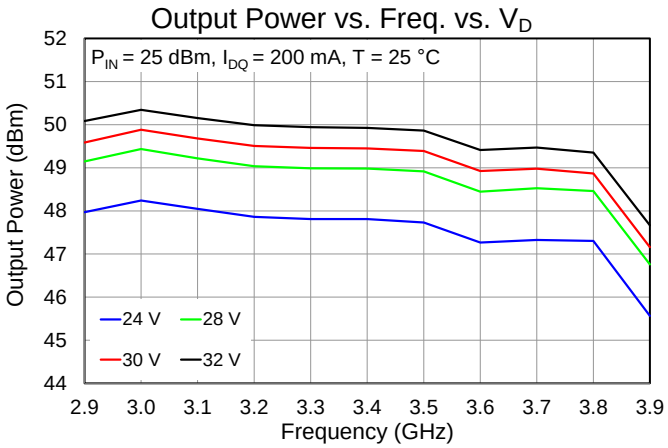

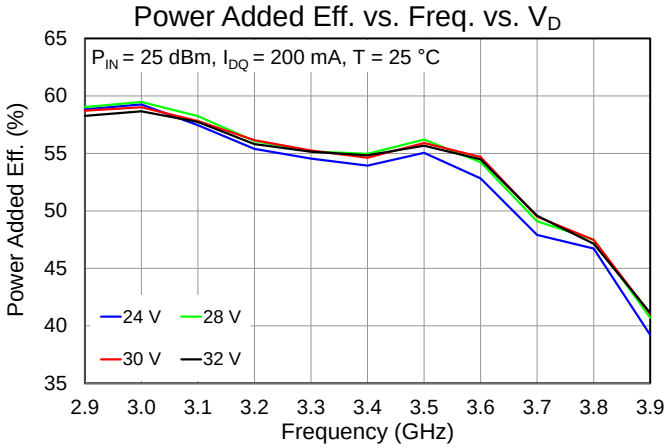

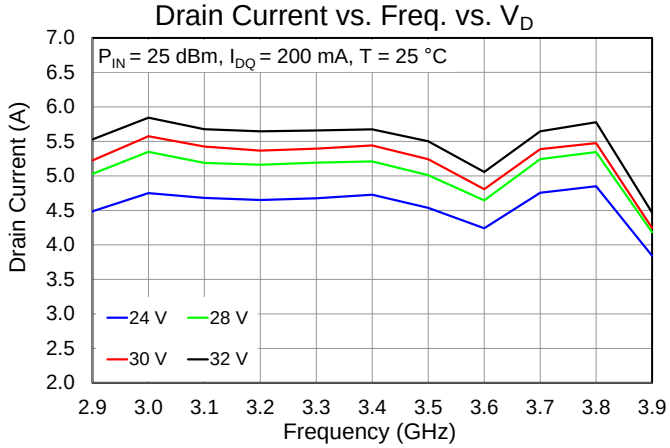

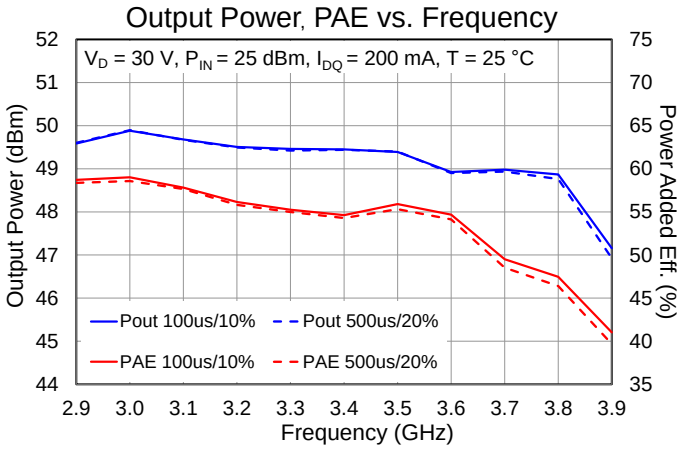

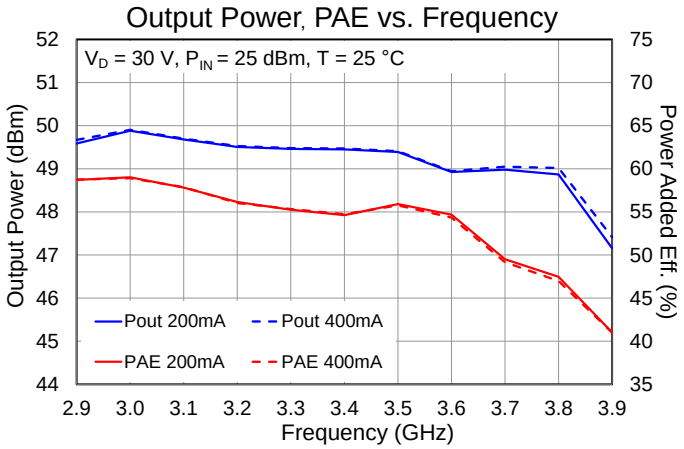

Typical Performance – Large Signal

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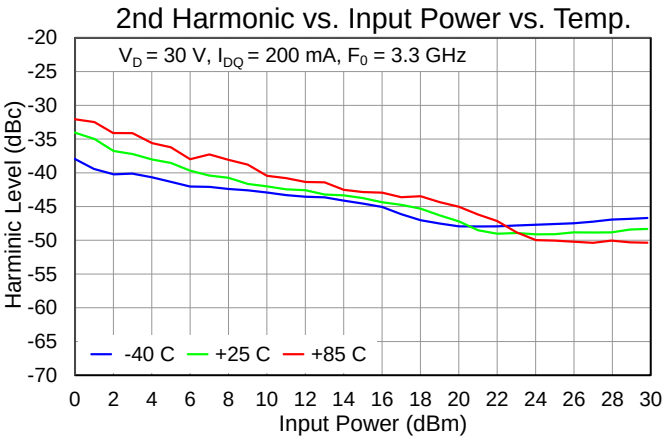
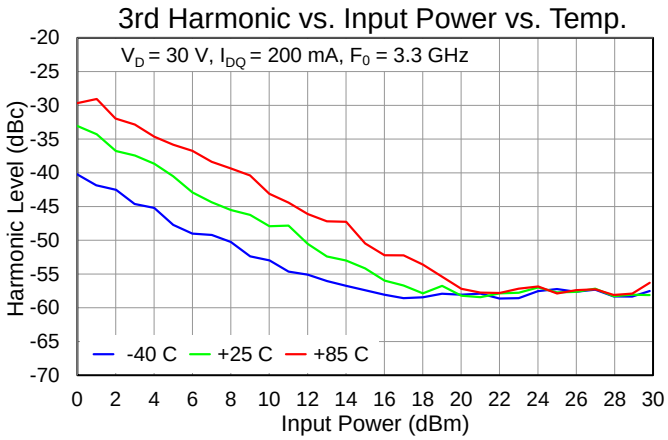


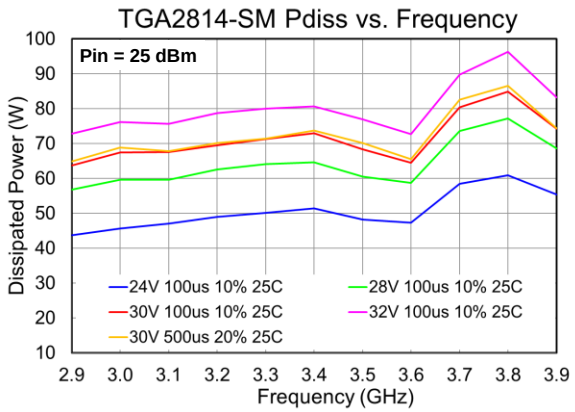


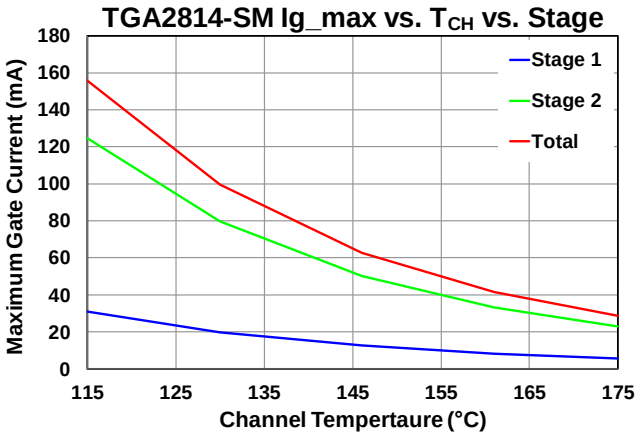
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC})(1)	T_{BASE} = 85 °C, V_D = 30 V, I_{DQ} = 200mA, Quiescent operation (DC only, no RF)	0.29	ºC/W
Channel Temperature (T_{CH})		86.7	°C
Thermal Resistance (θ_{JC})(1)	TBASE = 85 °C, V_D = 30 V, I_D = 5.3 A, P_{IN} = 25 dBm, P_{OUT} = 49.5 dBm, PW = 100 us, DC = 10 %, P_{DISS} = 58 W	0.47	ºC/W
Channel Temperature (T_{CH})		112.4	°C
Thermal Resistance (θ_{JC})(1)	T_{BASE} = 85 °C, V_D = 32 V, I_D = 5.7 A, Pin = 25 dBm, P_{OUT} = 50.0 dBm, PW = 100 us, DC = 10 %, P_{DISS} = 72 W	0.50	ºC/W
Channel Temperature (T_{CH})		120.8	°C

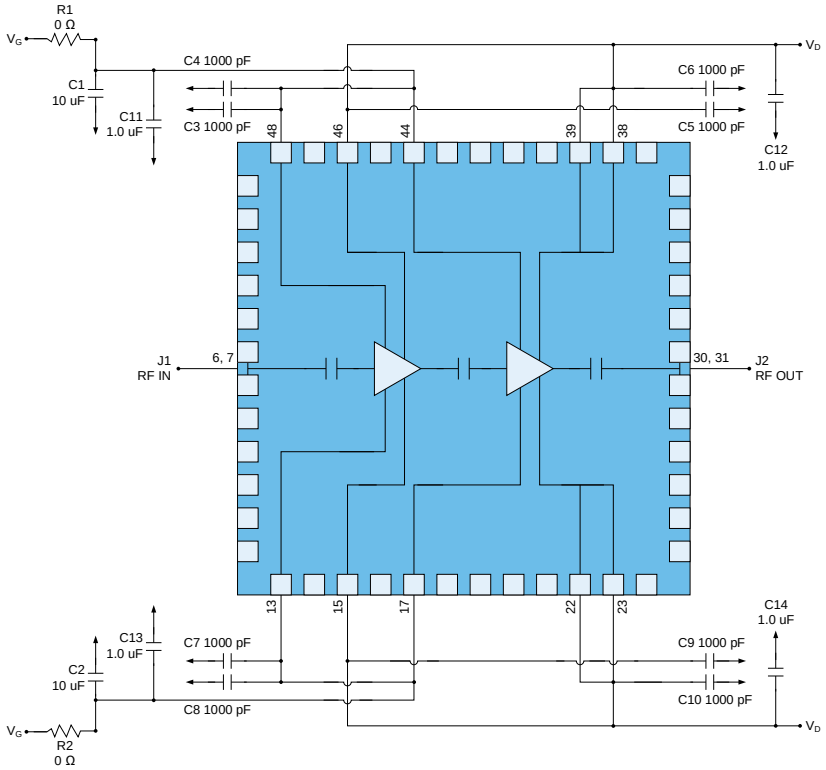
Notes:
1. Thermal resistance referenced back of the package.
2. IR scan equivalent. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates.

Power Dissipation and Max. Gate Current



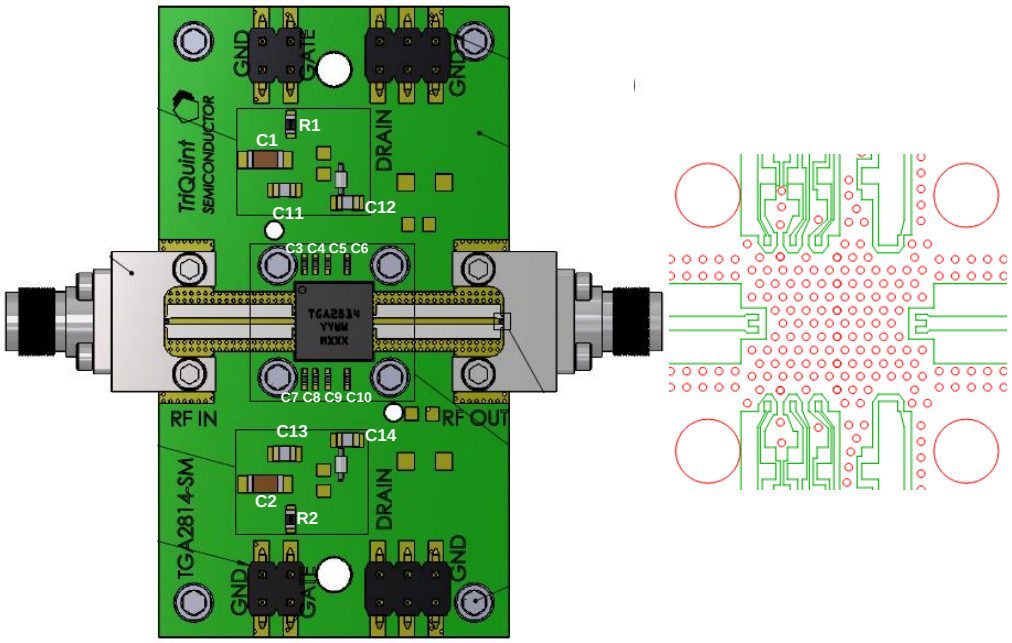


Application Circuit



Bias-up Procedure	Bias-down Procedure
Set I_D limit to 6 A, I_G limit to 30 mA	Turn off RF signal
Apply -5.0 V to V_G	Reduce V_G to -5.0 V. Ensure I_{DQ} ~ 0 mA
Apply +30 V to V_D	Set V_D to 0 V
Adjust V_G more positive until I_{DQ} = 200 mA (V_G ~ –2.90 V Typical)	Turn off V_D supply
Apply RF signal	Turn off V_G supply

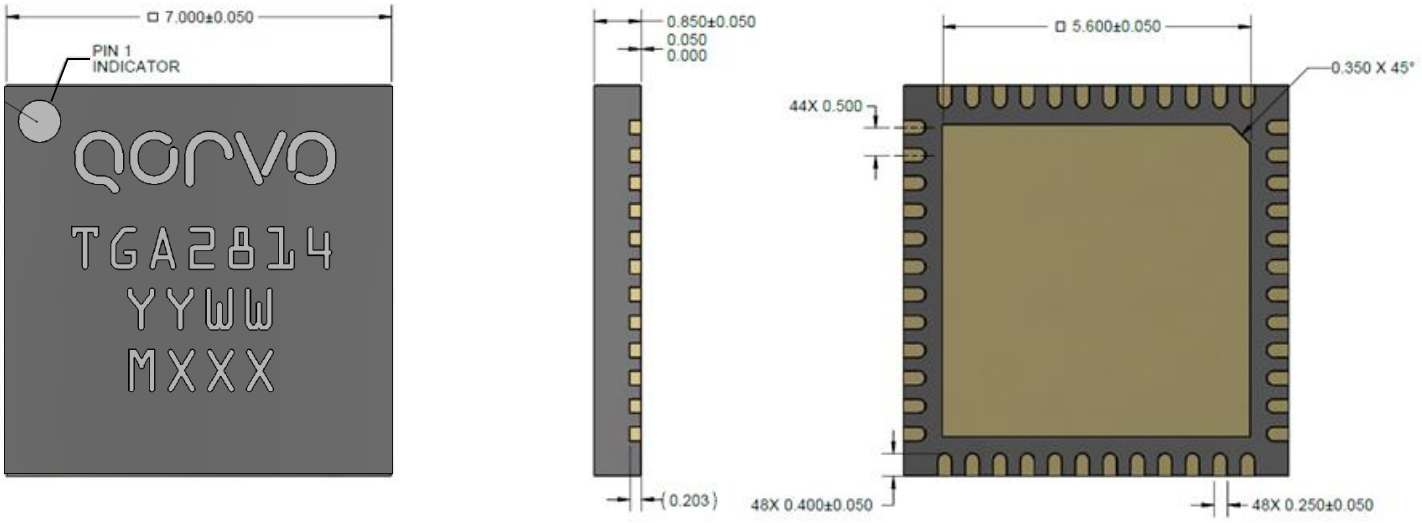
Evaluation Board, Mounting Detail, Bill of Materials



RF Layer is 0.008” thick Rogers Corp. RO40003C (ε_r = 3.35). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-02A-5.

Reference Des.	Component	Value	Manuf.	Part Number
C1, C2	Surface Mount Cap	10 uF, 20 %, 50 V (1206), X5R	Various	
C3–C10	Surface Mount Cap	1000 pF, 10 %, 50 V (0402), X7R	Various	
C11–C14	Surface Mount Cap	1.0 uF, 10 %, 25 V (0402), X7R	Various	
R1, R2	Surface Mount Res	0 Ohm, 5 % (0603)	Various	

Mechanical Drawing

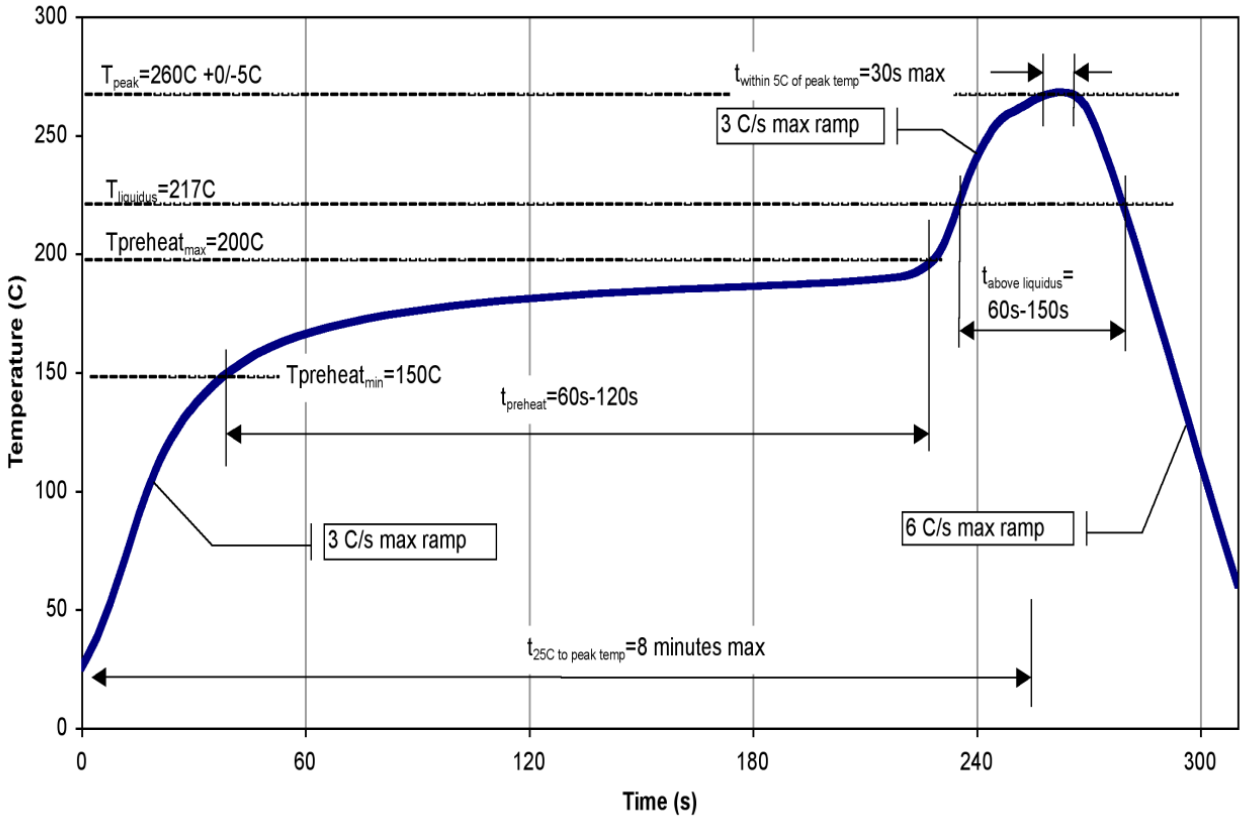


DIMENSIONS ARE IN MILLIMETERS
PACKAGE LEADS ARE GOLD PLATED.
PART IS MOLD ENCAPSULATED
YY IS THE CALENDAR YEAR
WW IS THE WEEK NUMBER
MXXX IS THE BATCH ID

Pad Descriptions

Pad No.	Symbol	Description
1-5, 8-12, 14, 16, 18-21, 24-29, 32-37, 40-43, 45, 47, 49	GND	Ground connection.
6, 7	RF Input	50 Ohm RF input. Pad is capacitively coupled to block on-chip DC voltages.
13, 48	V_{G1}	1st Stage Gate Voltage; bias network is required; must be biased from both sides (V_{G1} and V_{G2} can be tied together in application)
15, 46	V_{D1}	1st Stage Drain Voltage; bias network is required; must be biased from both sides (V_{D1} and V_{D2} can be tied together in application)
17, 44	V_{G2}	2nd Stage Gate Voltage; bias network is required; must be biased from both sides (V_{G1} and V_{G2} can be tied together in application)
22, 23, 38, 39	V_{D2}	2nd Stage Drain Voltage; bias network is required; must be biased from both sides (V_{D1} and V_{D2} can be tied together in application)
30, 31	RF Output	50 Ohm RF output. Pad is capacitively coupled to block on-chip DC voltages

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	0B	ANSI/ESDA/JEDEC JS-001
ESD – Charge Device Model (CDM)	C3	ANSI/ESDA/JEDEC JS-002
MSL Rating	1	JEDEC IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.
This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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