# TGA2817-SM

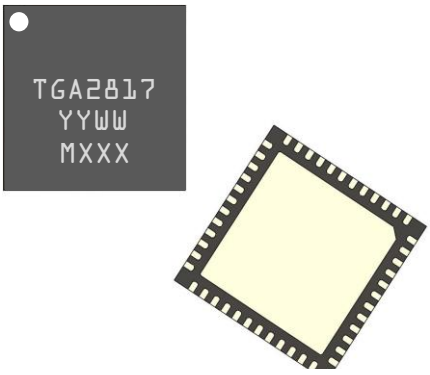
## S-Band 60 W GaN Power Amplifier

## General Description

Qorvo's TGA2817-SM is a high-power, S-band amplifier fabricated on Qorvo's TQGaN25 0.25 um GaN on SiC production process. Covering 2.9-3.5 GHz, the TGA2817-SM provides > 48 dBm of saturated output power and > 24 dB of large-signal gain while achieving > 54 % power added efficiency.

The TGA2817-SM can also support a variety of operating conditions to best support system requirements. With good thermal properties, it can support a range of bias voltages and will perform well under pulse applications. The TGA2817-SM is matched to 50 ohms with integrated DC blocking caps on both I/O ports. It is ideal for use in both commercial and military radar systems.

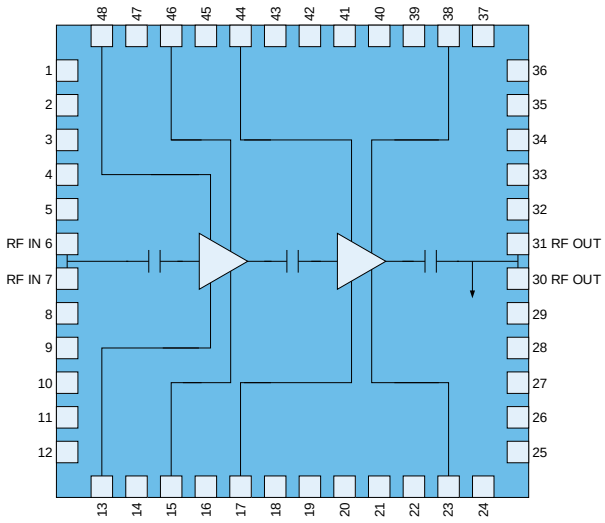
Lead-free and RoHS compliant




## Product Features

- Frequency Range: 2.9–3.5 GHz
- $P_{OUT}$: > 48 dBm (at $P_{IN}$ = 24 dBm)
- Large Signal Gain: > 24 dB (at $P_{IN}$ = 24 dBm)
- PAE: > 54 % (at $P_{IN}$ = 24 dBm)
- Bias: $V_D$ = 28 V, $I_{DQ}$ = 200 mA
- Package Dimensions: 7.00 x 7.00 x 0.85 mm

## Functional Block Diagram




## Applications

- Military Radar
- Commercial Radar

## Ordering Information

| Part | Description |
|---|---|
| TGA2817-SM | S-Band 60 W GaN Power Amplifier |
| TGA2817-SM_EVB | TGA2817-SM Evaluation Board |

## Absolute Maximum Ratings

| Parameter | Value/Range |
|---|---|
| Drain Voltage ($V_D$) | 40 V |
| Drain Current ($I_{D1}$/$I_{D2}$) | 1.4 / 5.8 A |
| Gate Current ($I_G$) | See graph, page 8 |
| Dissipated Power ($P_{DISS}$) | 92 W |
| Input Power: 50 Ω, 85 °C (1) | 30 dBm |
| Input Power: 3:1 VSWR, 85 °C (1) | 28 dBm |
| Soldering Temperature | 260 °C |
| Storage Temperature | −55 to 150 °C |

Notes:
1. Based on die performance.

Operation of this device outside the parameter ranges given above may cause permanent damage.

## Recommended Operating Conditions

| Parameter | Value/Range |
|---|---|
| Drain Voltage ($V_D$) | 28 V |
| Drain Current (quiescent, $I_{DQ}$) | 200 mA |
| Drain Current (under drive ,$I_{D\_DRIVE}$) | 4.6 A |
| Gate Voltage Range ($V_G$) | −2.8 to −2.0 V |
| Operating Temperature | −40 to 85 °C |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

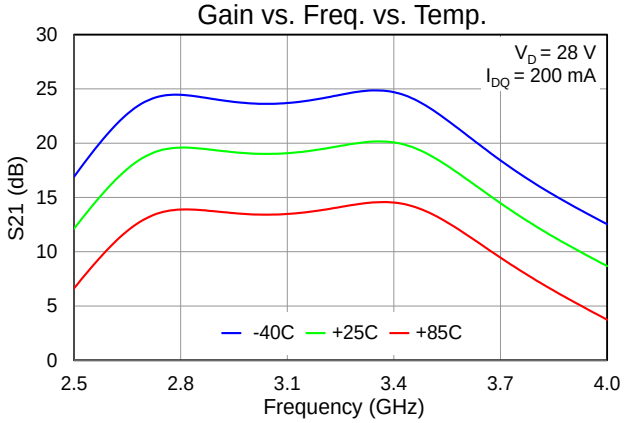
Test conditions, unless otherwise noted: 25 °C, $V_D$ = 28 V, $I_{DQ}$ = 200 mA, Pulse Width = 100 us, Duty Cycle = 10%

| Parameter | Condition | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| Operational Frequency | | 2.9 | | 3.5 | GHz |
| Output Power ($P_{IN}$ = 24 dBm) | 2.9 GHz | 47.2 | 48 | | dBm |
| | 3.1 GHz | 47.2 | 48 | | dBm |
| | 3.3 GHz | 47.4 | 48 | | dBm |
| Power Added Efficiency ($P_{IN}$ = 24 dBm) | 2.9 GHz | 49.5 | 54 | | % |
| | 3.1 GHz | 48.0 | 54 | | % |
| | 3.3 GHz | 47.0 | 54 | | % |
| Large Signal Gain ($P_{IN}$ = 24 dBm) | | | 24 | | dB |
| Input Return Loss | | | >8 | | dB |
| Gate Leakage ($V_D$ = 10 V, $V_G$ = −3.7 V) | | −30.6 | −0.46 | −0.0001 | mA |
| Output Power Temperature Coefficient | | | −0.006 | | dBm/°C |

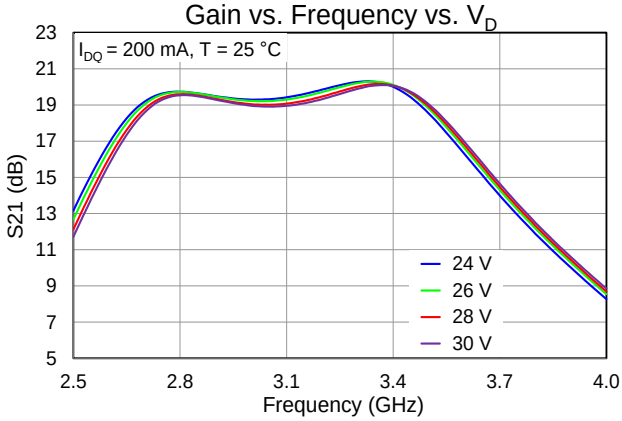
## Typical Performance

Test conditions unless otherwise noted: Temp. = 25 °C

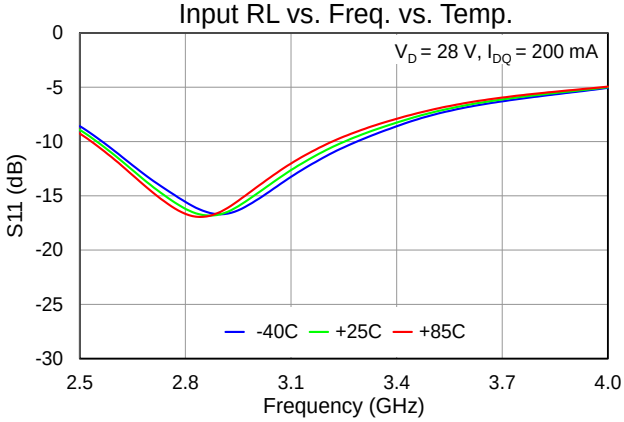
Gain vs. Freq. vs. Temp.



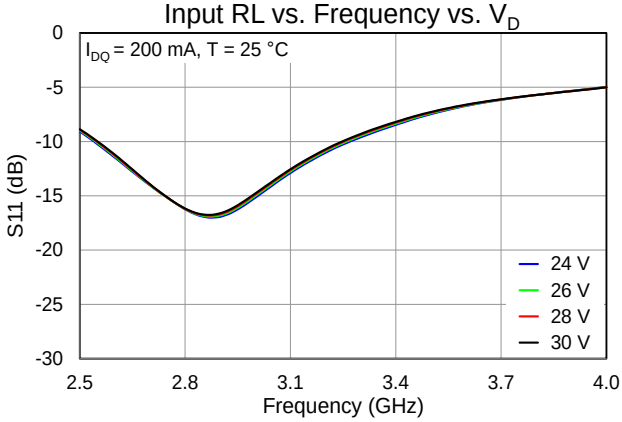

Gain vs. Frequency vs. $V_D$



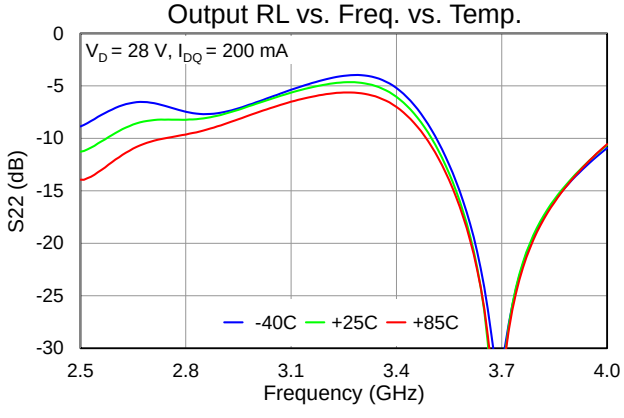

Input RL vs. Freq. vs. Temp.



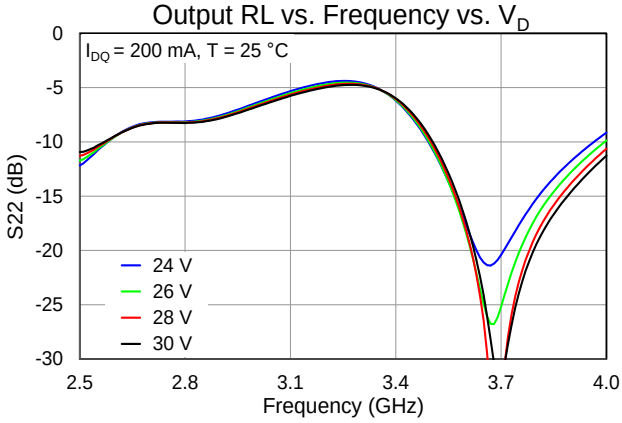

Input RL vs. Frequency vs. $V_D$




Output RL vs. Freq. vs. Temp.



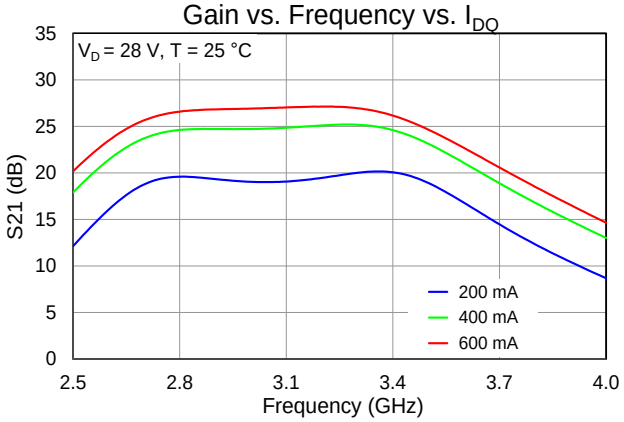

Output RL vs. Frequency vs. $V_D$



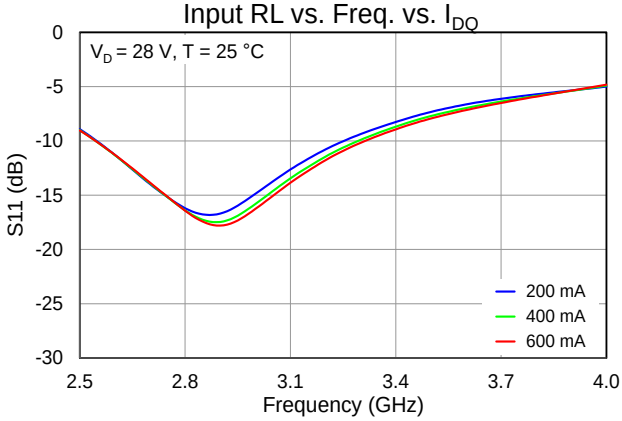
## Typical Performance

Test conditions unless otherwise noted: Temp. = 25 °C

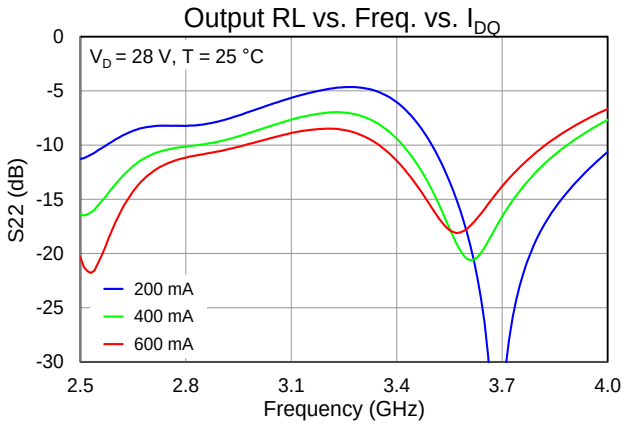
Gain vs. Frequency vs. $I_{DQ}$




Input RL vs. Freq. vs. $I_{DQ}$



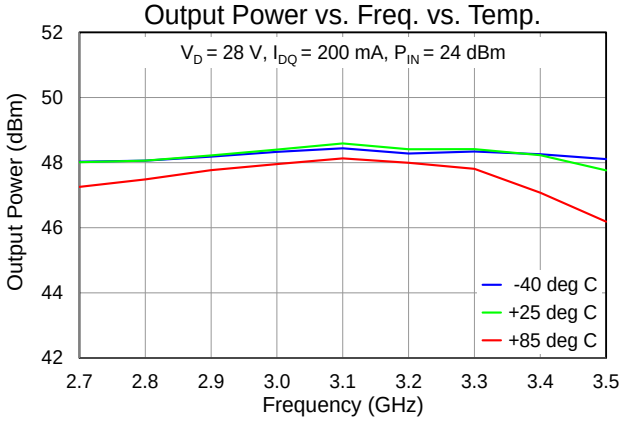

Output RL vs. Freq. vs. $I_{DQ}$



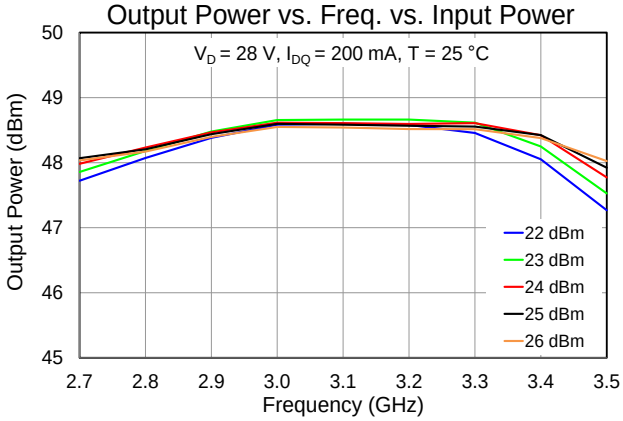
## Typical Performance

Test conditions unless otherwise noted: Temp. = 25 °C, Pulsed input power PW = 100 us, Duty Cycle = 10%

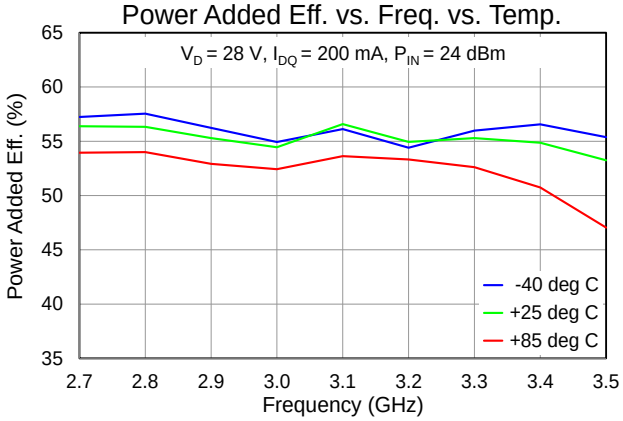
Output Power vs. Freq. vs. Temp.



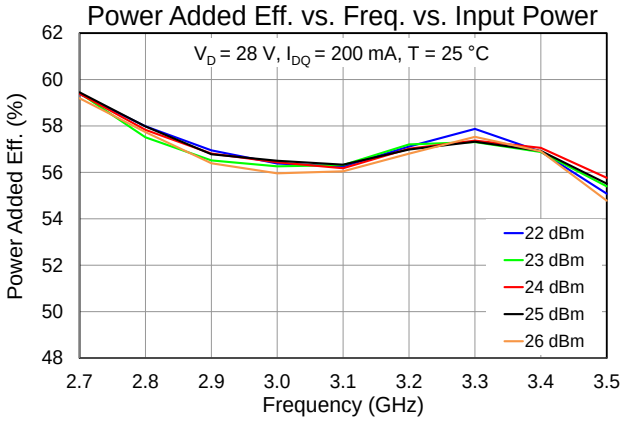

Output Power vs. Freq. vs. Input Power



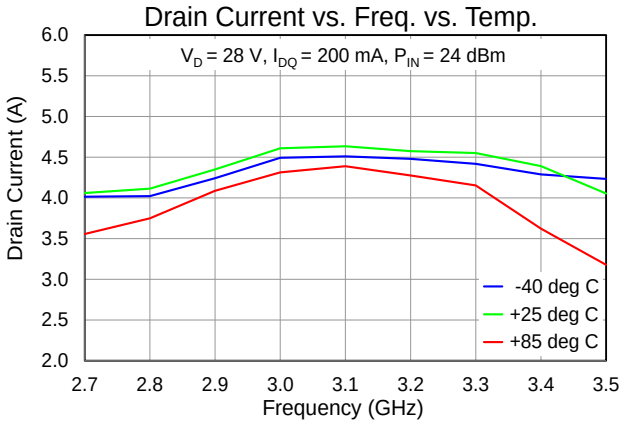

Power Added Eff. vs. Freq. vs. Temp.



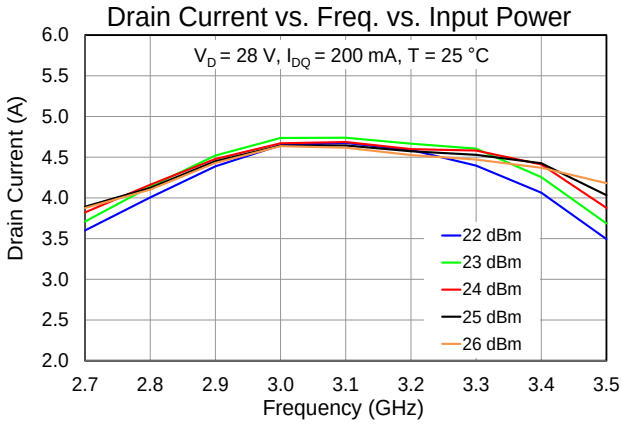

Power Added Eff. vs. Freq. vs. Input Power




Drain Current vs. Freq. vs. Temp.



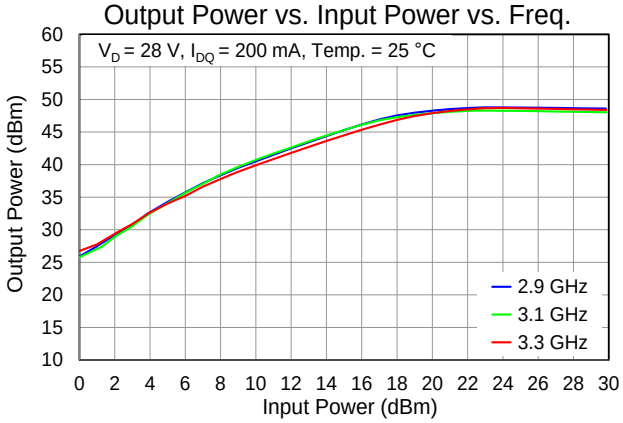

Drain Current vs. Freq. vs. Input Power



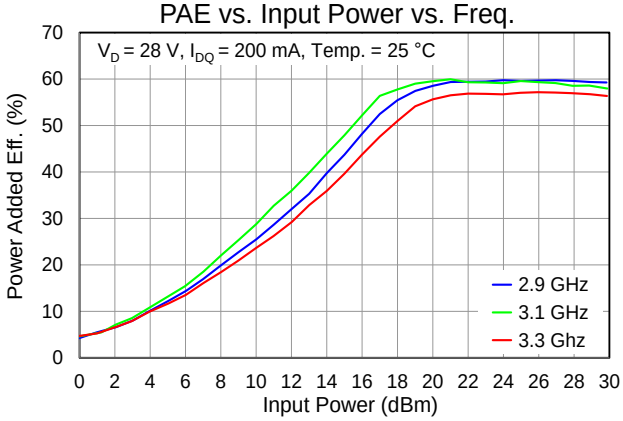
## Typical Performance

Test conditions unless otherwise noted: Pulsed input power PW = 100 us, Duty Cycle = 10%

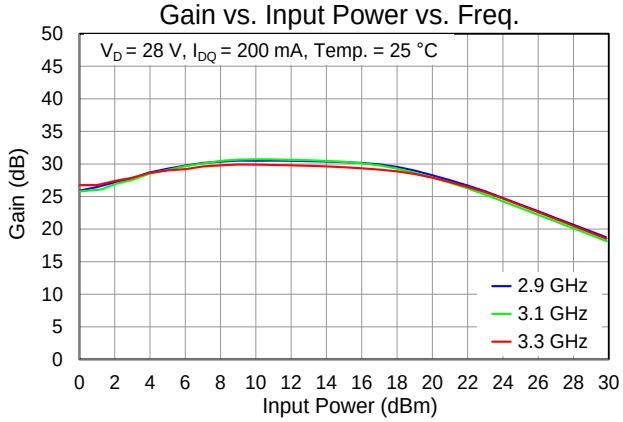
Output Power vs. Input Power vs. Freq.



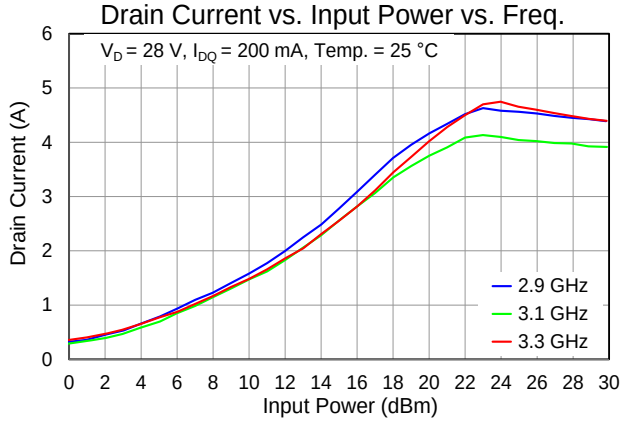

PAE vs. Input Power vs. Freq.



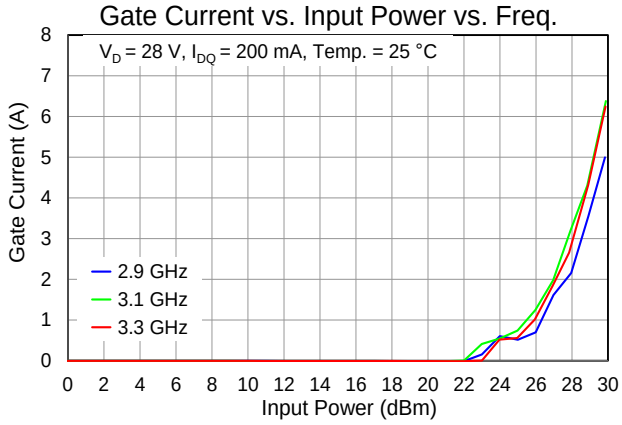

Gain vs. Input Power vs. Freq.




Drain Current vs. Input Power vs. Freq.



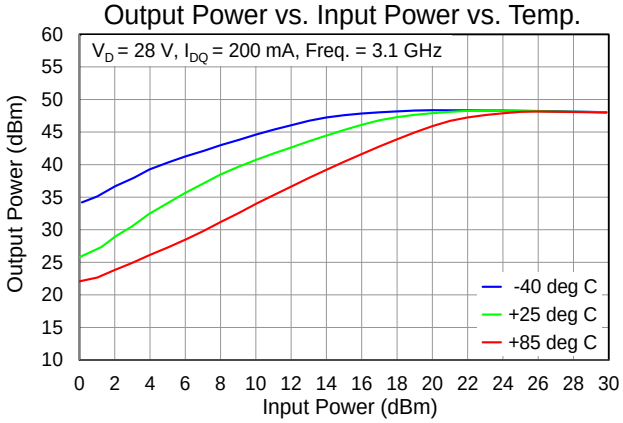

Gate Current vs. Input Power vs. Freq.



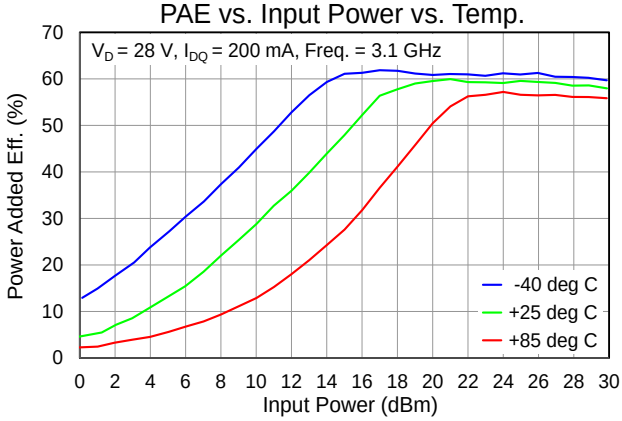
## Typical Performance

Test conditions unless otherwise noted: Pulsed input power PW = 100 us, Duty Cycle = 10%

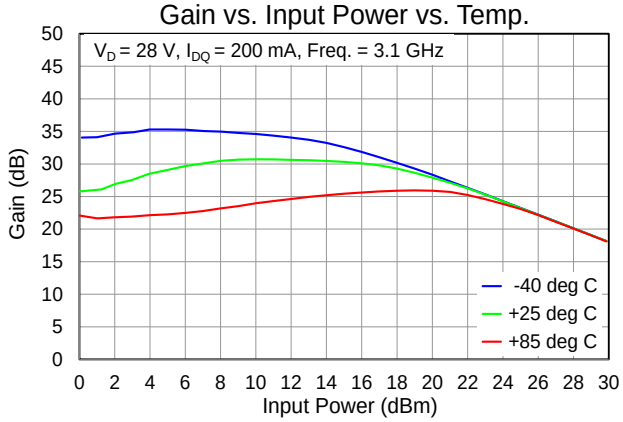
Output Power vs. Input Power vs. Temp.



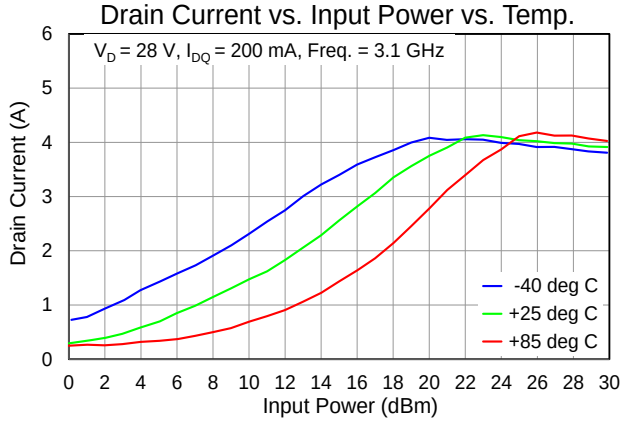

PAE vs. Input Power vs. Temp.



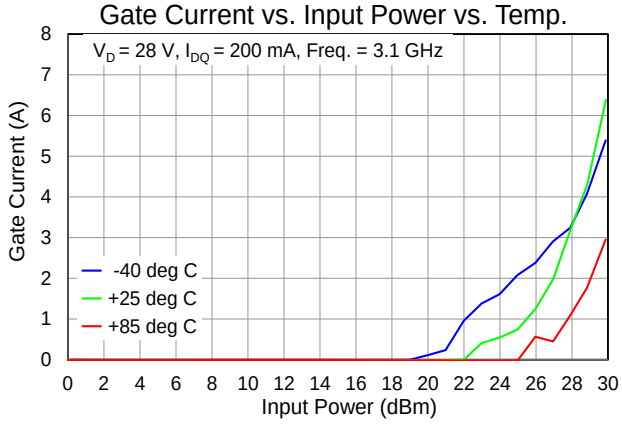

Gain vs. Input Power vs. Temp.




Drain Current vs. Input Power vs. Temp.




Gate Current vs. Input Power vs. Temp.

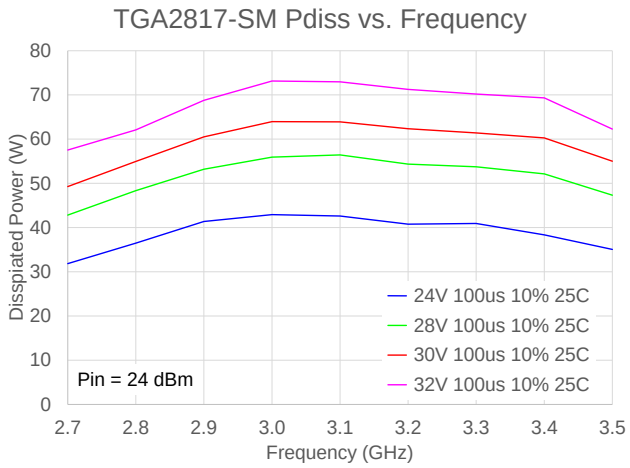


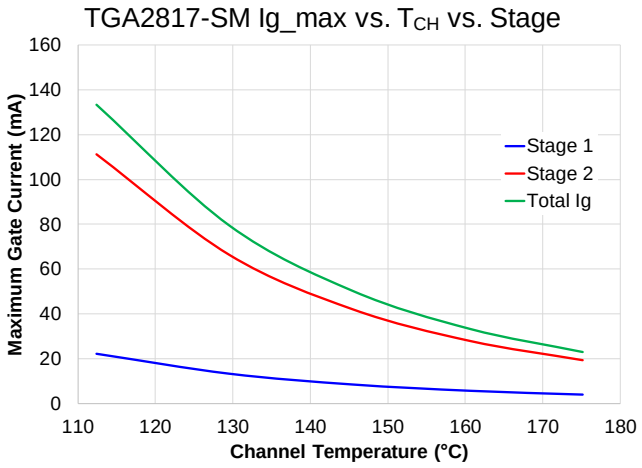
## Thermal and Reliability Information

| Parameter | Test Conditions | Value | Units |
|---|---|---|---|
| Thermal Resistance ($\theta_{JC}$) (1) | $T_{BASE}$ = 85 °C, $V_D$ = 28 V, $I_D$ = 200 mA (quiescent DC, small signal), $P_{DISS}$ = 6.4 W | 0.396 | °C/W |
| Channel Temperature ($T_{CH}$) (2) | | 87.5 | °C |
| Thermal Resistance ($\theta_{JC}$) (1) | $T_{BASE}$ = 85 °C, $V_D$ = 28 V, $I_D$ = 4.5 A, $P_{IN}$ = 24 dBm $P_{OUT}$ = 48.5 dBm, PW = 100 us, DC = 10%, $P_{DISS}$ = 53 W | 0.476 | °C/W |
| Channel Temperature ($T_{CH}$) (2) | | 110.2 | °C |
| Thermal Resistance ($\theta_{JC}$) (1) | $T_{BASE}$ = 85 °C, $V_D$ = 32 V, $I_D$ = 5.1 A, $P_{IN}$ = 24 dBm, $P_{OUT}$ = 49.4 dBm, PW = 100 us, DC = 10%, $P_{DISS}$ = 74 W | 0.492 | °C/W |
| Channel Temperature ($T_{CH}$) (2) | | 121.4 | °C |

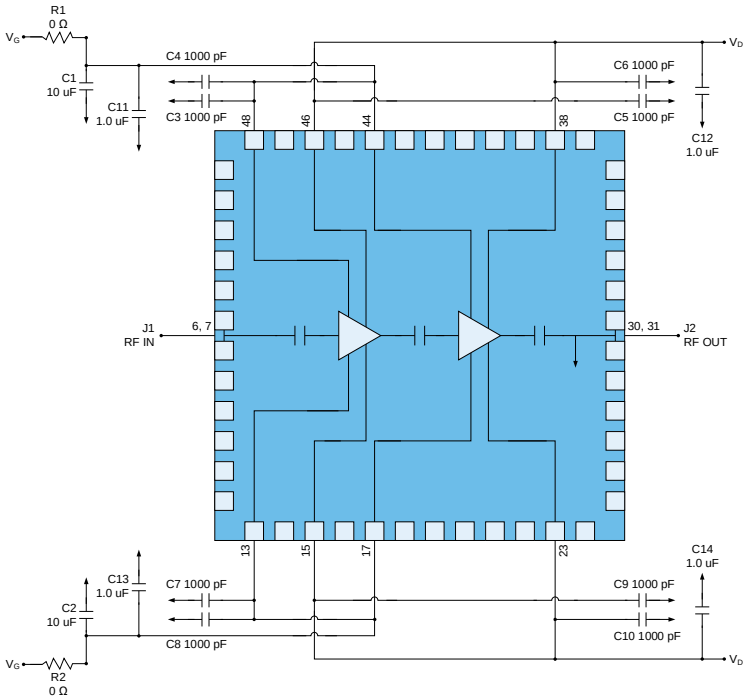
Notes:
1. Thermal resistance is determined to the back of the package (at 85 °C).
2. IR scan equivalent. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

## Power Dissipation and Maximum Gate Current



## Application Circuit



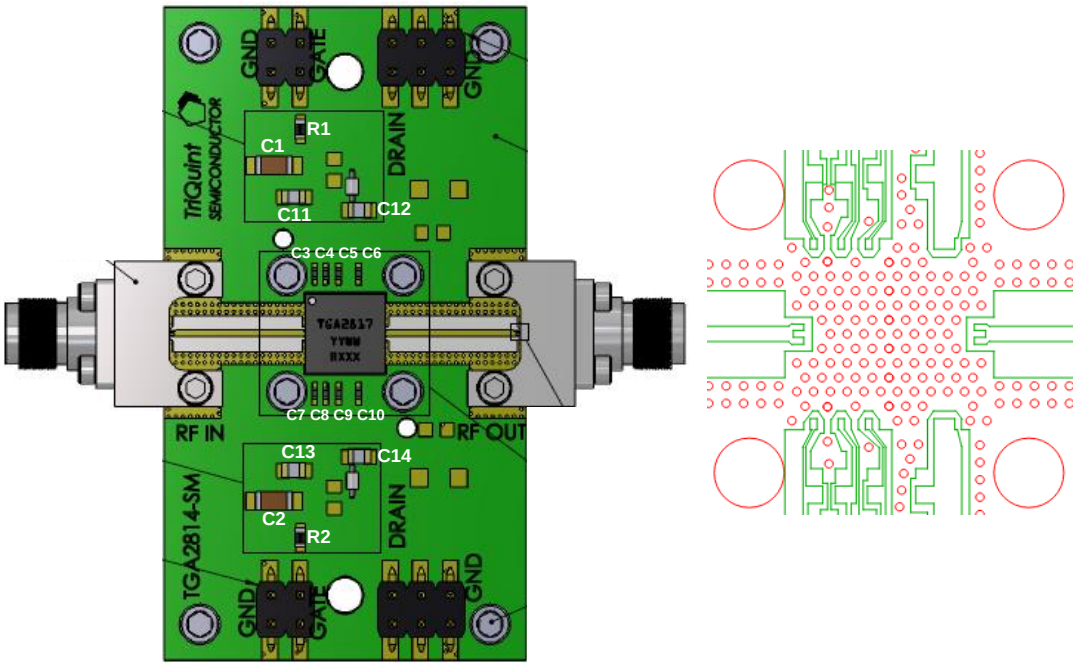

Notes:

1. $V_G$ and $V_D$ must be biased from both sides (top and bottom).

| Bias-up Procedure |
|---|
| Set $I_D$ limit to 6000 mA, $I_G$ limit to 40 mA |
| Set $V_G$ to −6.0 V |
| Set $V_D$ +28 V |
| Adjust $V_G$ more positive until $I_{DQ}$ = 200 mA |
| Apply RF signal |

| Bias-down Procedure |
|---|
| Turn off RF signal |
| Reduce $V_G$ to −6.0 V. Ensure $I_{DQ}$ ~ 0 mA |
| Set $V_D$ to 0 V |
| Turn off $V_D$ supply |
| Turn off $V_G$ supply |

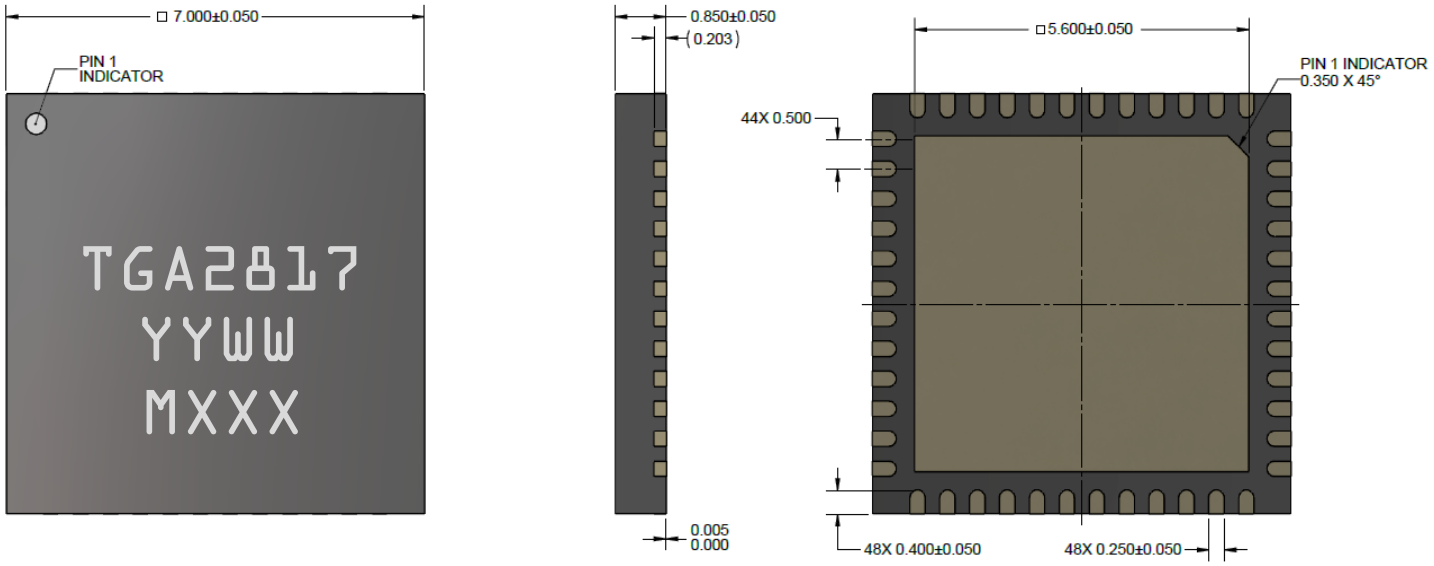
## Evaluation Board and Mounting Detail




RF Layer is 0.008" thick Rogers Corp. RO40003C ($\varepsilon_r$ = 3.35). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-02A-5.

| Reference Design | Component | Value | Manufacture | Part Number |
|---|---|---|---|---|
| C1, C2 | Surface Mount Cap | 10 uF, 20 %, 50 V (1206), X5R | Various | |
| C3–C10 | Surface Mount Cap | 1000 pF, 10 %, 50 V (0402), X7R | Various | |
| C11–C14 | Surface Mount Cap | 1.0 uF, 10 %, 25 V (0402), X7R | Various | |
| R1, R2 | Surface Mount Res | 0 Ohm, 5 % (0603) | Various | |

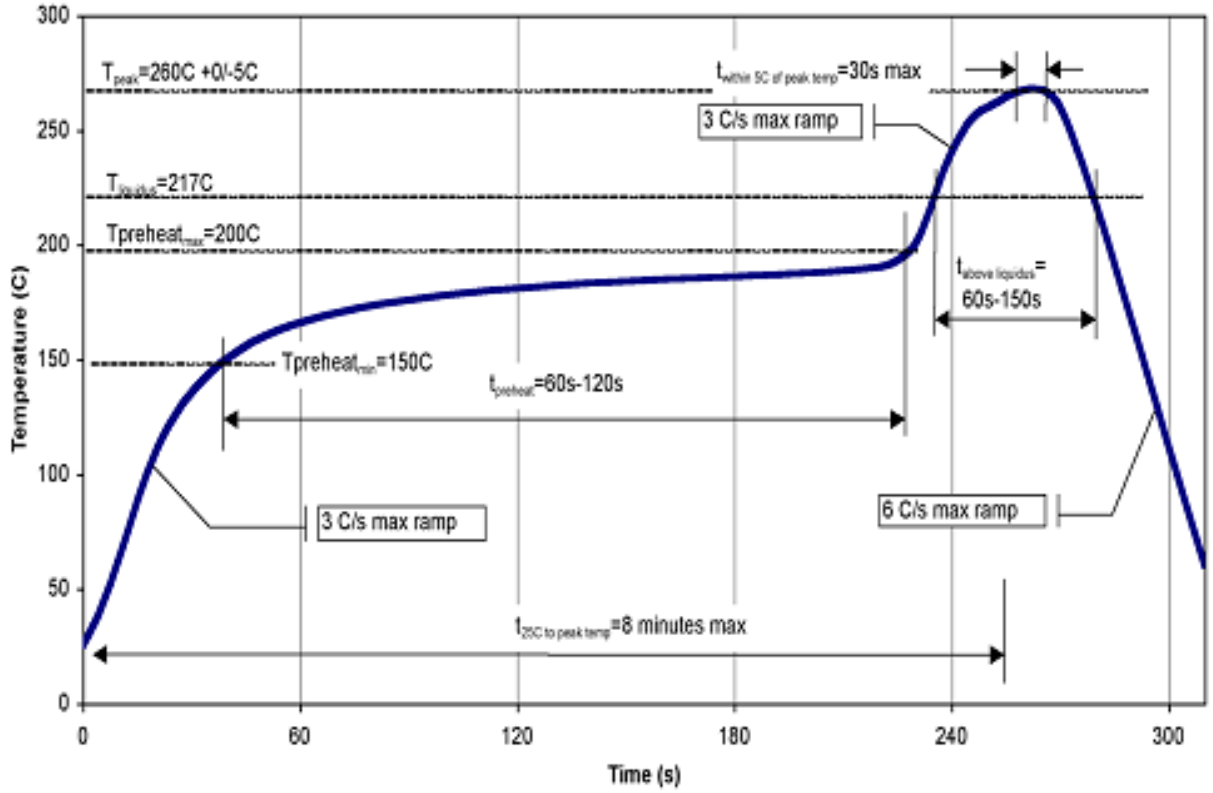
## Mechanical Drawing and Pad Description




Package Leads are Gold Plated
Part is Mold Encapsulated
Dimensions are in mm
Tolerances: .XX = ± .25, .XXX = ± .127
Markings:
TGA2817: Part Number
YY: Assembly Year
WW: Assembly Week
MXXX: Batch ID

| Pad No. | Symbol | Description |
|---|---|---|
| 1-5, 8-12, 14, 16, 18-22, 24-29, 32-37, 39-43, 45, 47, 49 | GND | Ground connection. |
| 6, 7 | RF Input | 50 Ohm RF input. Pad is capacitively coupled to block on-chip DC voltages. |
| 13, 48 | $V_{G1}$ | 1st Stage Gate Voltage; bias network is required; must be biased from both sides ($V_{G1}$ and $V_{G2}$ can be tied together in application) |
| 15, 46 | $V_{D1}$ | 1st Stage Drain Voltage; bias network is required; must be biased from both sides ($V_{D1}$ and $V_{D2}$ can be tied together in application) |
| 17, 44 | $V_{G2}$ | 2nd Stage Gate Voltage; bias network is required; must be biased from both sides ($V_{G1}$ and $V_{G2}$ can be tied together in application) |
| 23, 38 | $V_{D2}$ | 2nd Stage Drain Voltage; bias network is required; must be biased from both sides ($V_{D1}$ and $V_{D2}$ can be tied together in application) |
| 30, 31 | RF Output | 50 Ohm RF output. Pad is capacitively coupled to block on-chip DC voltages. Pad is DC grounded. |

## Recommended Soldering Temperature Profile



## Handling Precautions

| Parameter | Rating | Standard |
|---|---|---|
| ESD - Human Body Model (HBM) | 1C | JEDEC/JS-001-2014 |
| ESD- Charge Device Model (CDM) | C3 | JEDEC/JS-002-2014 |
| MSL - Moisture Sensitivity Level | MSL3 | JEDEC/IPC/JEDEC J-STD-020 |

Caution!
ESD-Sensitive Device

## Solderability

Compatible with the latest version of J-STD-020 Lead Free solder, 260 °C.

## RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations.

**Web: www.qorvo.com**

**Tel: 1-844-890-8163**

**Email: customer.support@qorvo.com**

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