TGA3042

7 – 10.5 GHz 4.5 W GaN Power Amplifier

Product Description

Qorvo's TGA3042 is a wideband high power MMIC amplifier fabricated on Qorvo's production 0.15um GaN on SiC process (QGaN15). The TGA3042 operates from 7 – 10.5 GHz and typically provides 4.5 W saturated output power with power-added efficiency of 38.5% and large-signal gain of 23.5 dB. This combination of wideband performance provides the flexibility designers are looking for to improve system performance while reducing size and cost.

The TGA3042 is matched to 50Ω with integrated DC blocking capacitors on both RF I/O ports simplifying system integration. The wideband performance makes it ideally suited in support of multiple radar and communication bands.

The TGA3042 is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

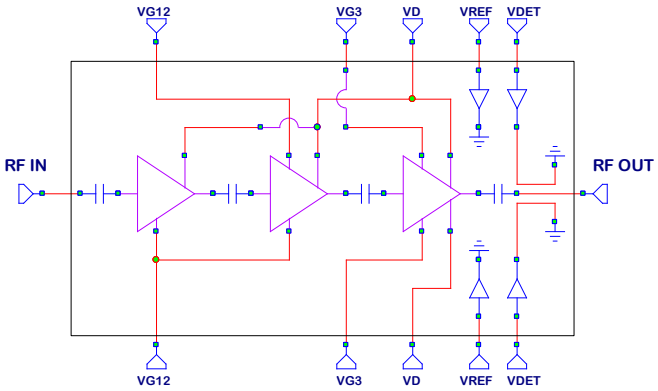
Lead-free and RoHS compliant.

Product Features

- Frequency Range: 7 – 10.5 GHz
- P_{OUT}: 36.5 dBm at P_{IN} = 13 dBm
- PAE: 38.5 % at P_{IN} = 13 dBm
- Large Signal Gain: 23.5 dB at P_{IN} = 13 dBm
- Small Signal Gain: 32 dB
- Bias: V_D = 20 V, I_{DQ} = 200 mA, V_G = −2.2 V Typical
- Chip Dimensions: 2.75 x 1.4 x 0.10 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Radar
- Communications

Ordering Information

Part No.	Description
TGA3042	7 – 10.5 GHz 4.5 W GaN Power Amplifier

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	−8 to 0V
Drain Current (I_D)	720 mA
Gate Current (I_G)	See chart, pg. 13
Power Dissipation (P_{DISS}), 85°C	15.4 W
Input Power (P_{IN}), CW, 50Ω, V_D=20 V, I_{DQ}=200 mA, 85 °C	23 dBm
Input Power (P_{IN}), CW, VSWR 3:1, V_D=20 V, I_{DQ}=200 mA 85 °C	23 dBm
Mounting Temperature (30 seconds)	320 °C
Storage Temperature	−55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value / Range
Drain Voltage (V_D)	20 V
Drain Current (I_{DQ})	200 mA
Gate Voltage (V_G), Typical	−2.2 V

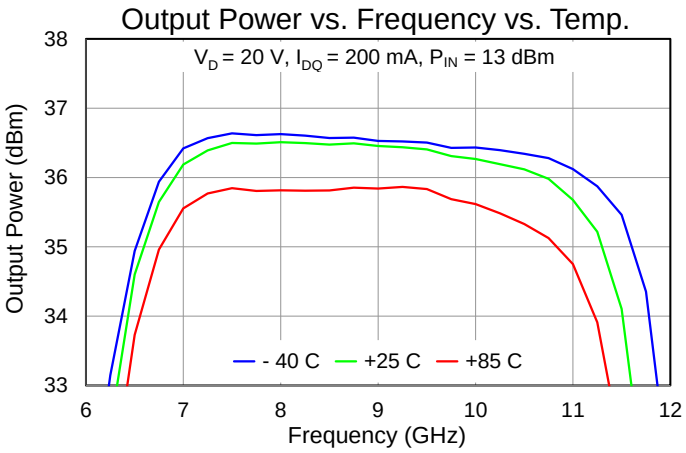
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

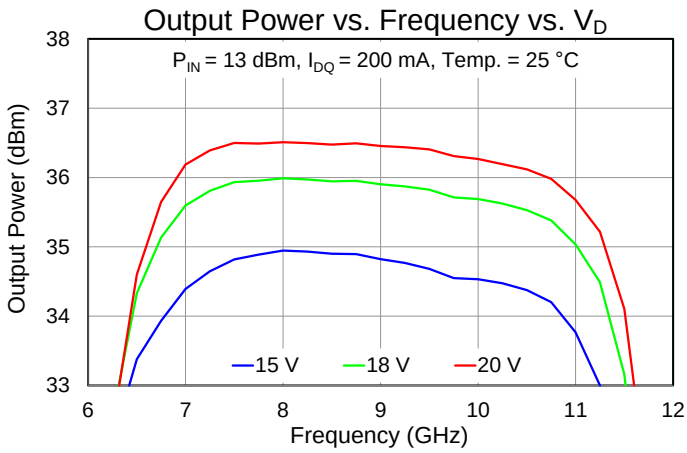
Electrical Specifications

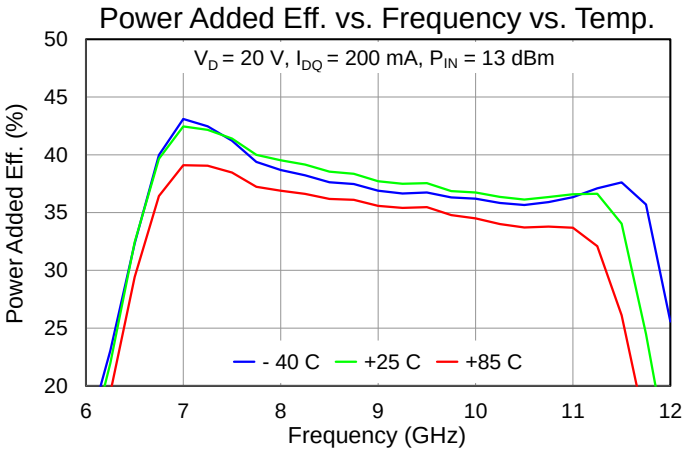
Parameter		Min	Typ	Max	Units
Operational Frequency Range		7		10.5	GHz
Output Power (Pin = 13 dBm)	7.0 GHz 9.0 GHz 10.5 GHz		36.2 36.5 36.1		dBm dBm dBm
Power Added Efficiency (Pin = 13 dBm)	7.0 GHz 9.0 GHz 10.5 GHz		42.5 37.9 36.3		% % %
3rd Order Intermodulation Level (P_{OUT}/Tone= 26 dBm)	7.0 GHz 9.0 GHz 10.5 GHz		−23.3 −24.0 −23.8		dBc dBc dBc
Small Signal Gain	7.0 GHz 9.0 GHz 10.5 GHz		33.1 32.5 31.0		dB dB dB
Input Return Loss	7.0 GHz 9.0 GHz 10.5 GHz		16 26 16		dB dB dB
Output Return Loss	7.0 GHz 9.0 GHz 10.5 GHz		12 10 13		dB dB dB
Output Power Temperature Coefficient (25 – 85 °C)			−0.011		dB/°C
Sm. Signal Gain Temperature Coefficient			−0.055		dB/°C

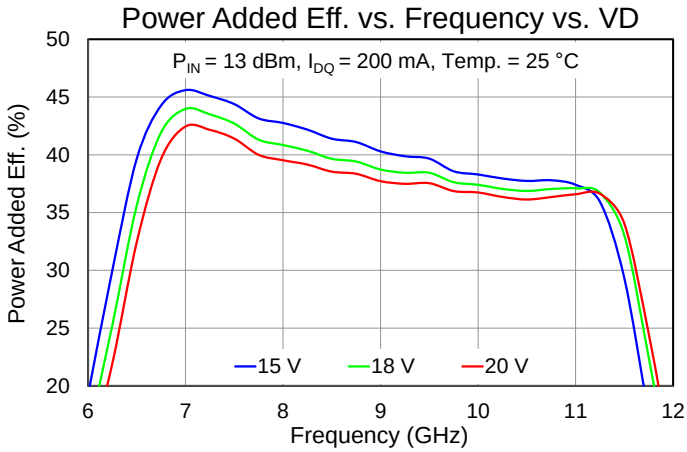
Test conditions, unless otherwise noted: 25 °C, V_D = 20 V, I_{DQ} = 200 mA, V_G = −2.2 V Typical

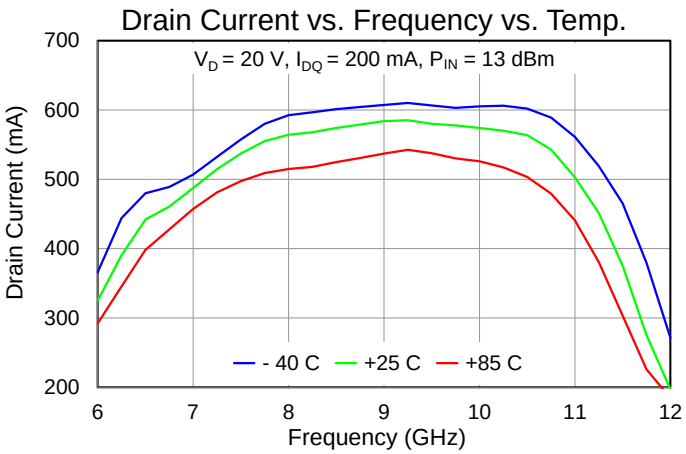
Performance Plots – Large Signal (CW)

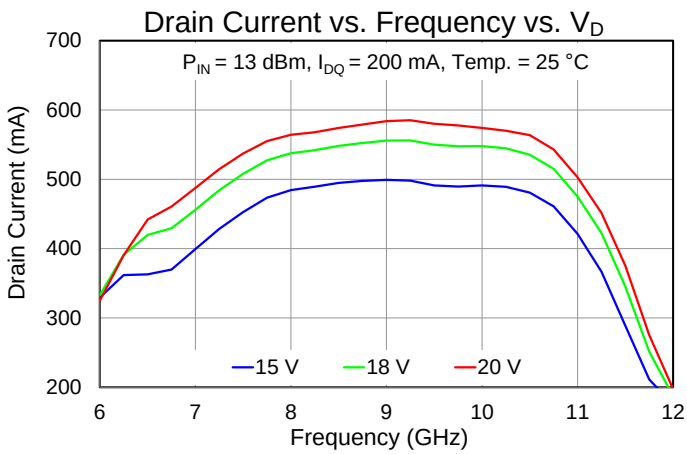




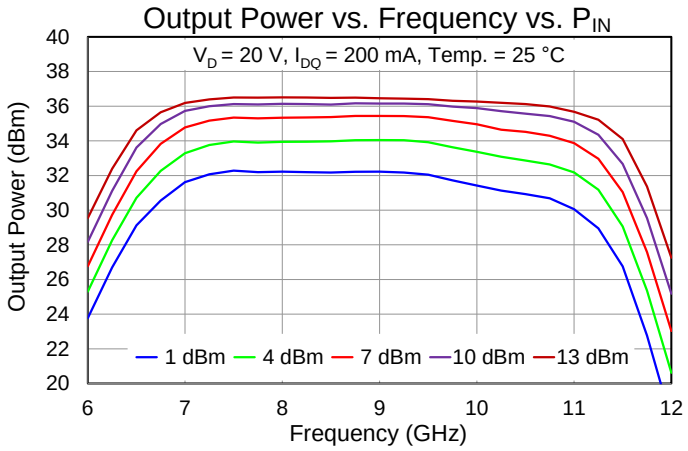


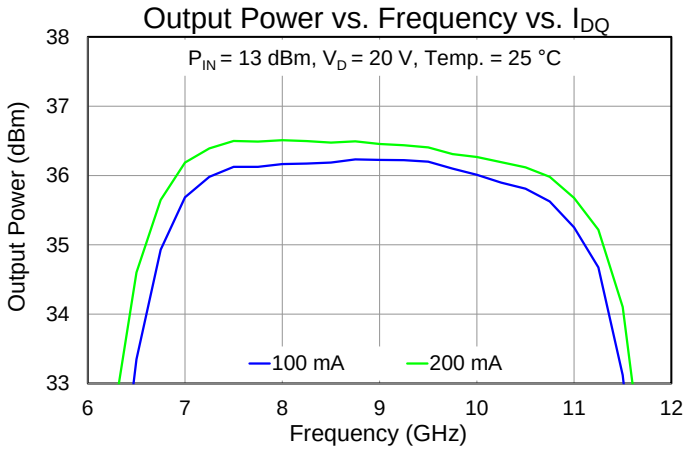


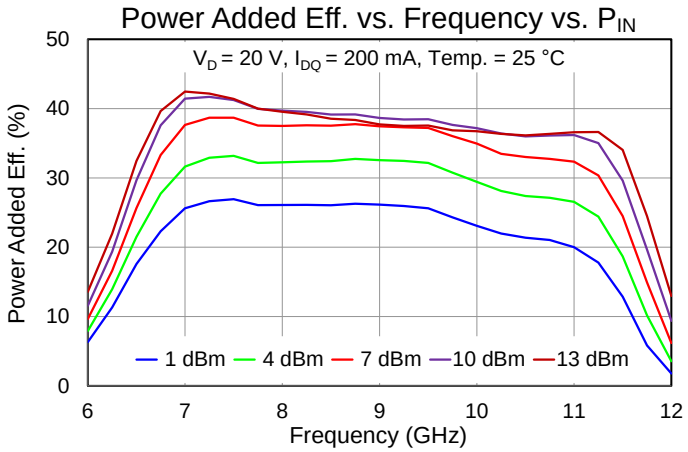


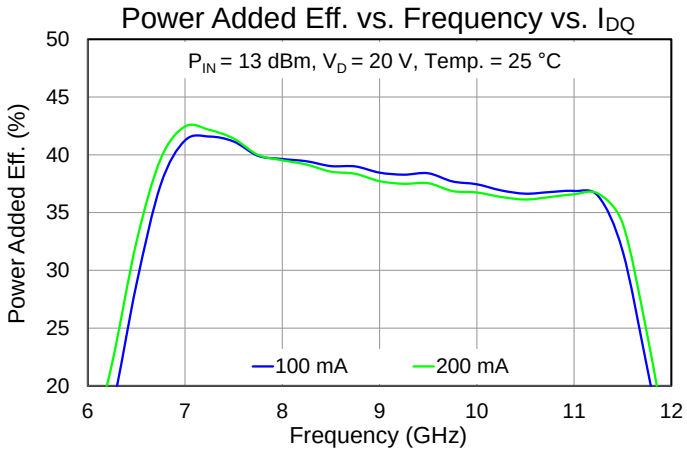


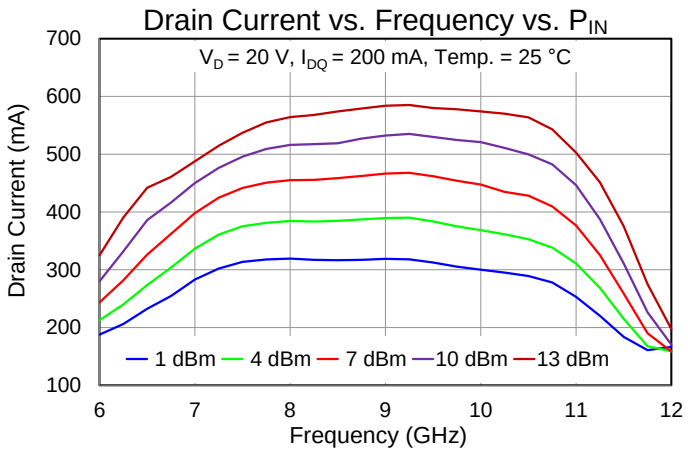
Performance Plots – Large Signal (CW)

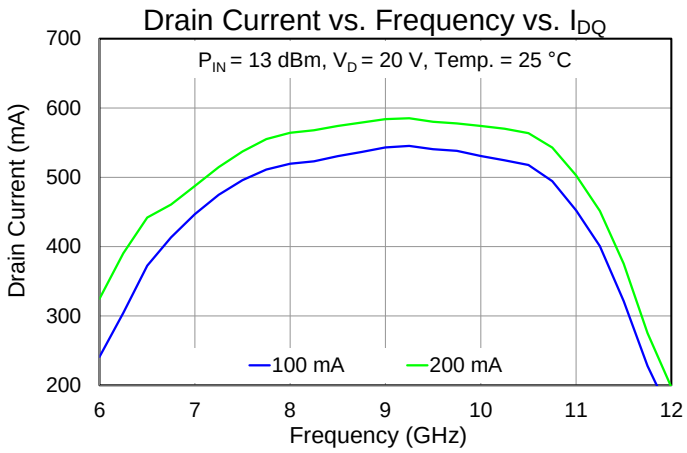




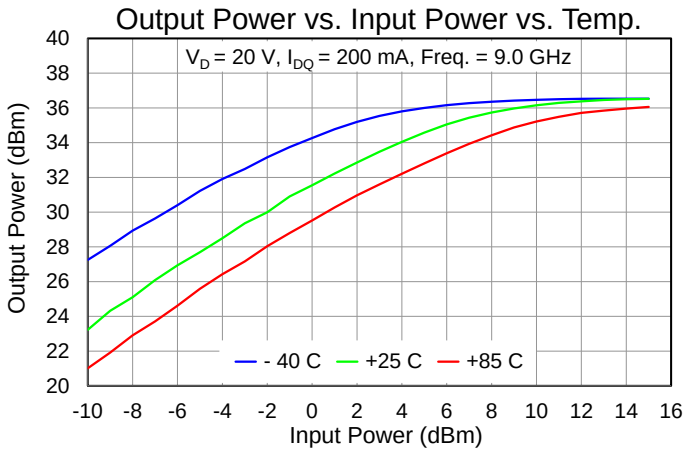


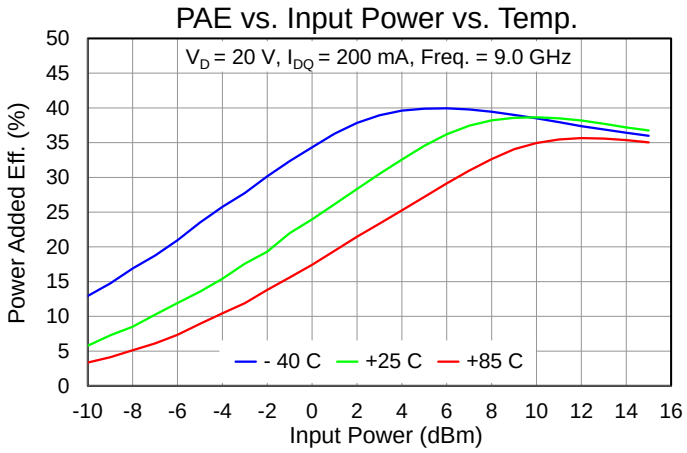


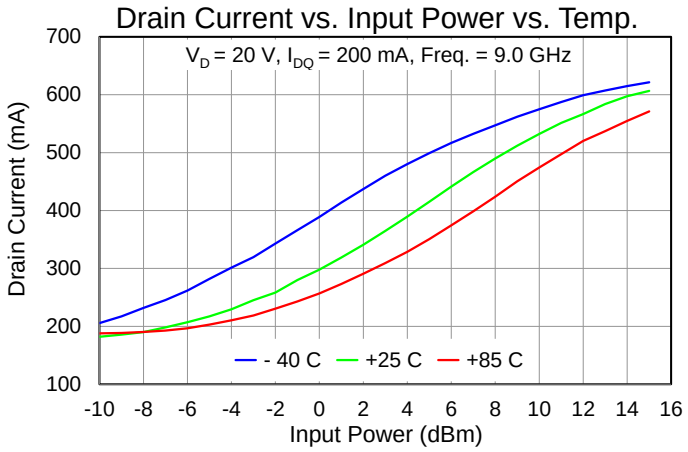


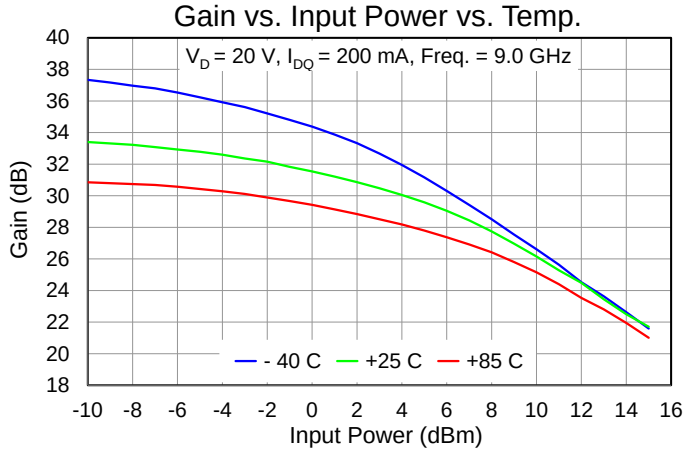


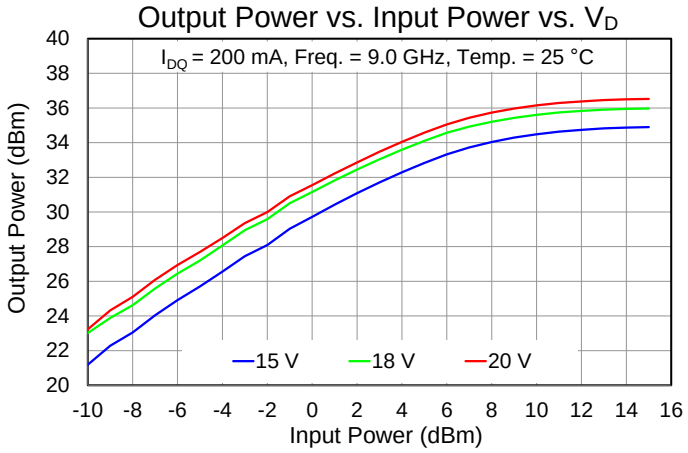
Performance Plots – Large Signal (CW)

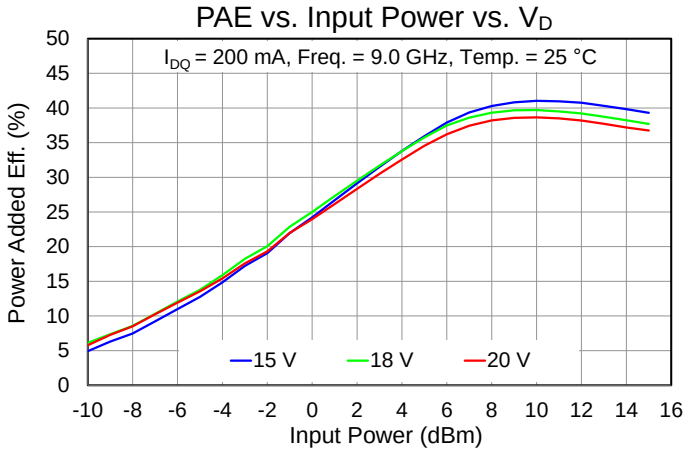




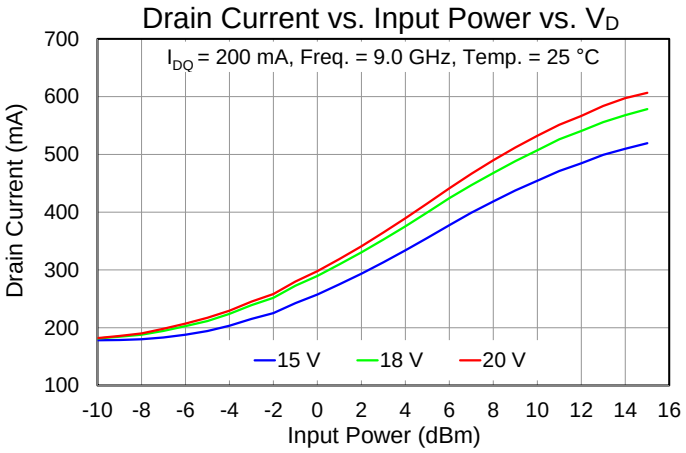


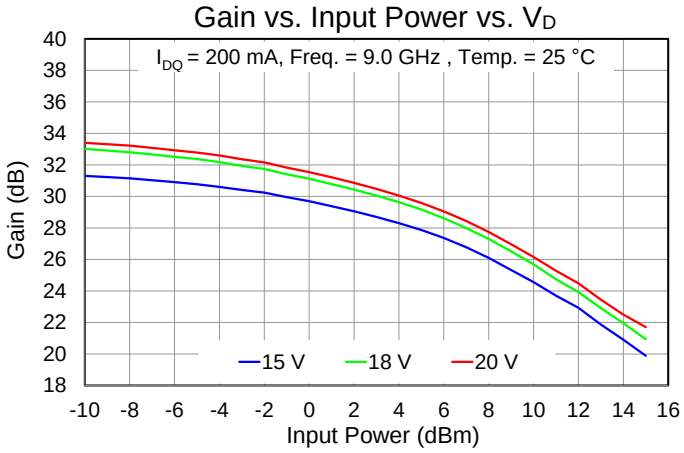


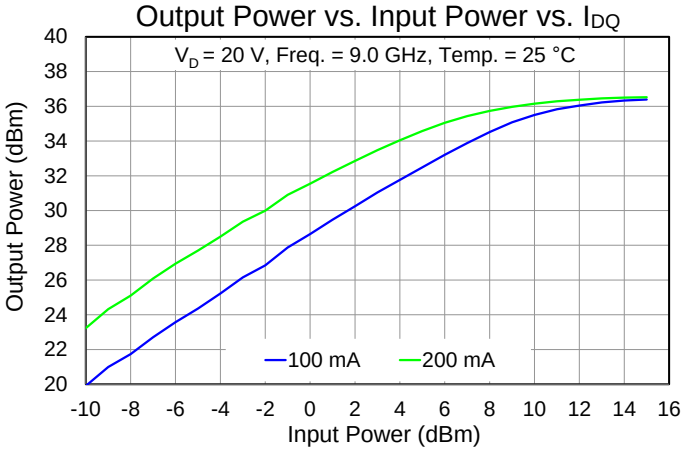


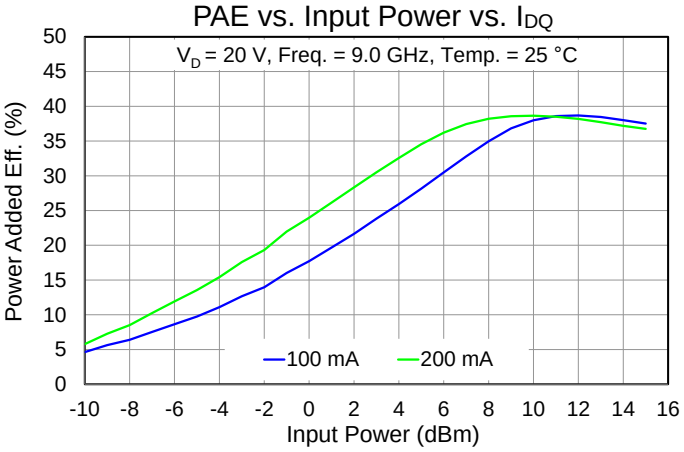


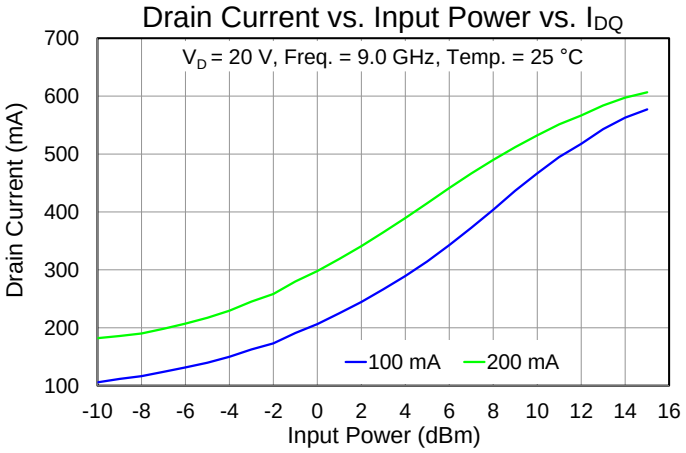
Performance Plots – Large Signal (CW)

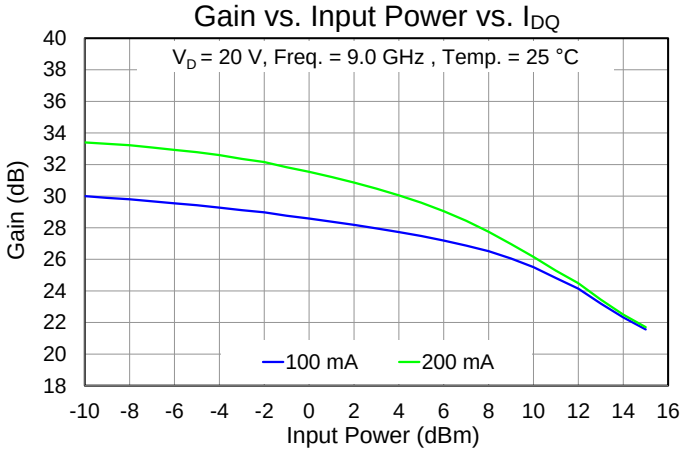






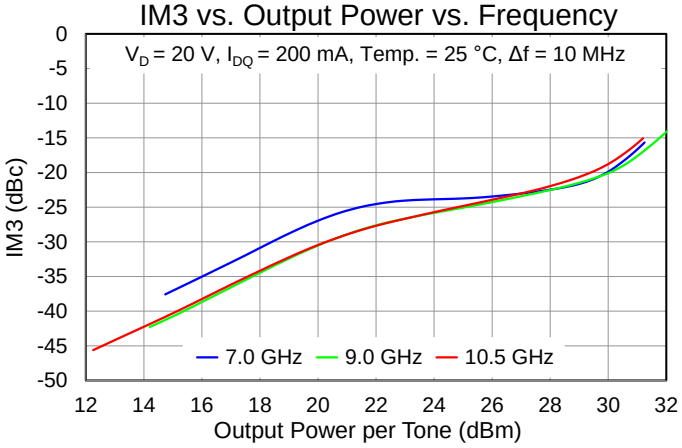




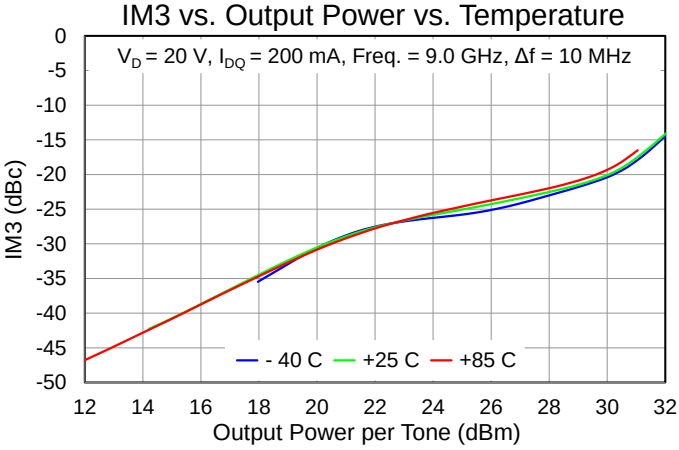


Performance Plots – Linearity

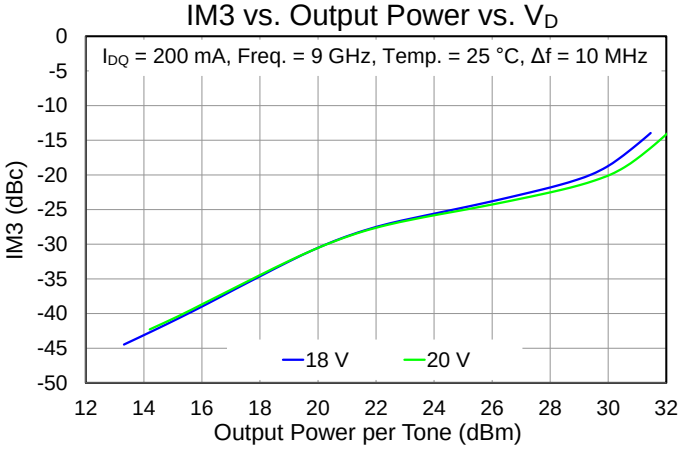
IM3 vs. Output Power vs. Frequency



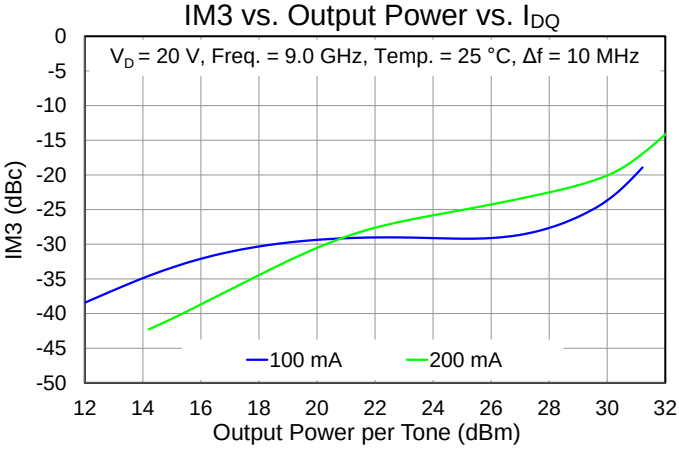
IM3 vs. Output Power vs. Temperature



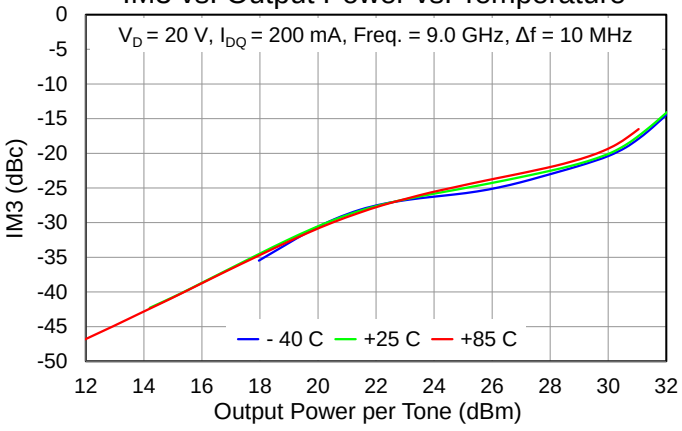
IM3 vs. Output Power vs. V_D



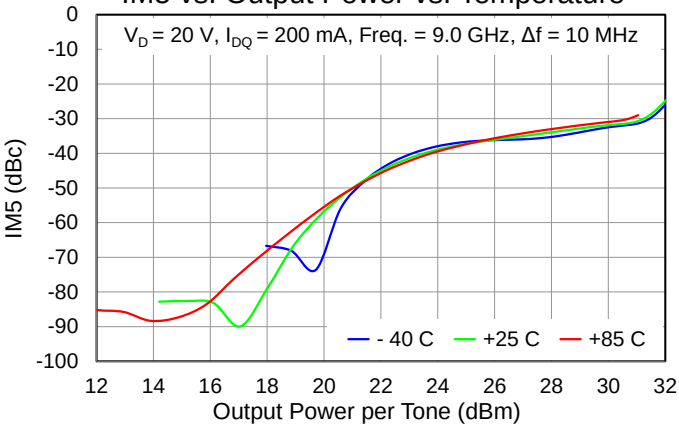
IM3 vs. Output Power vs. I_{DQ}



IM3 vs. Output Power vs. Temperature

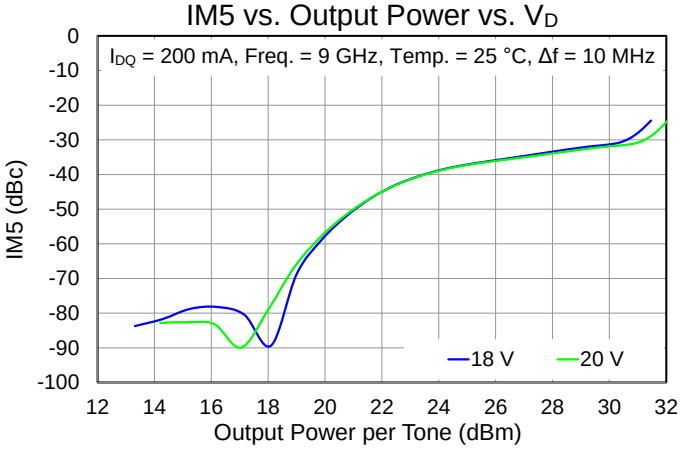


IM5 vs. Output Power vs. Temperature

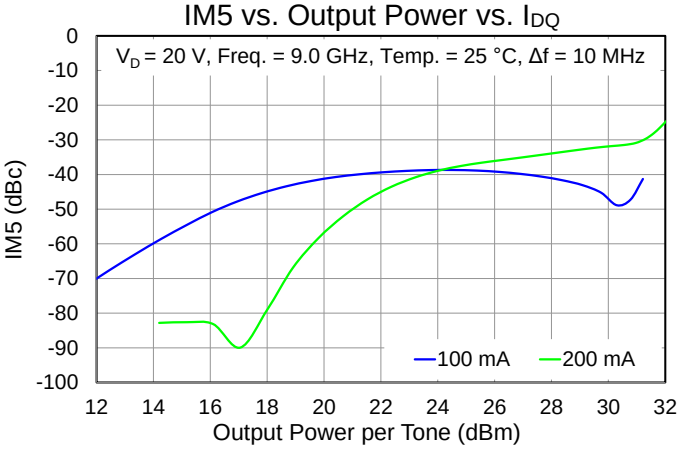


Performance Plots – Linearity, Harmonics

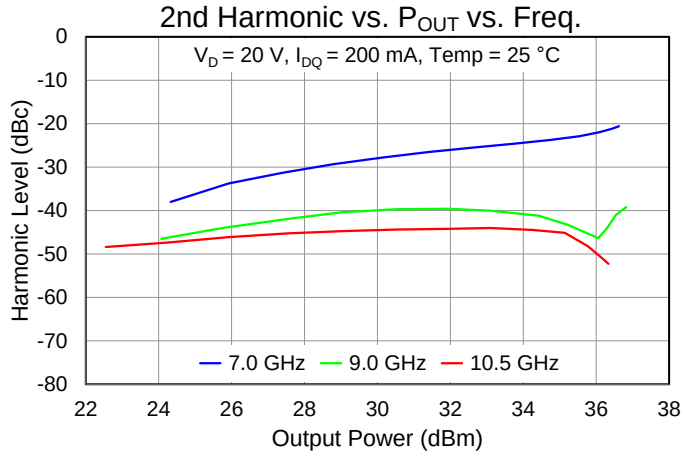
IM5 vs. Output Power vs. V_D



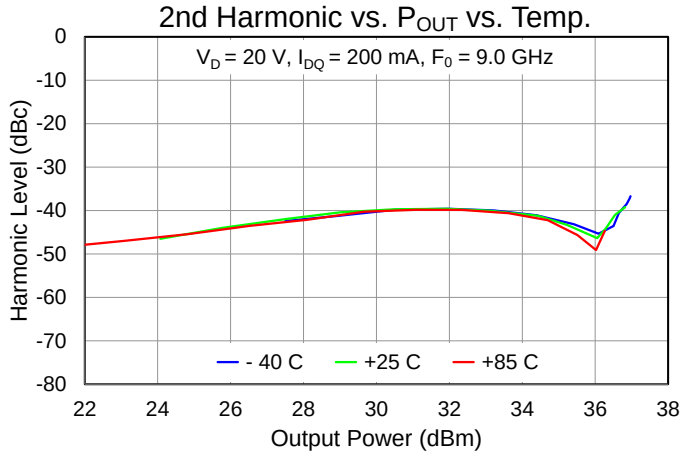
IM5 vs. Output Power vs. I_{DQ}



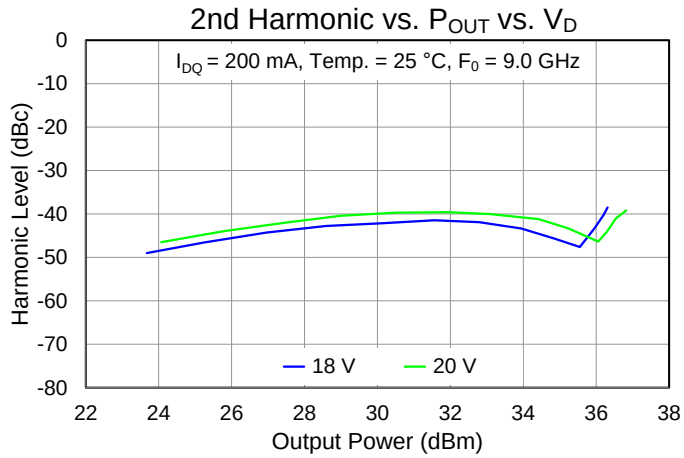
2nd Harmonic vs. P_{OUT} vs. Freq.



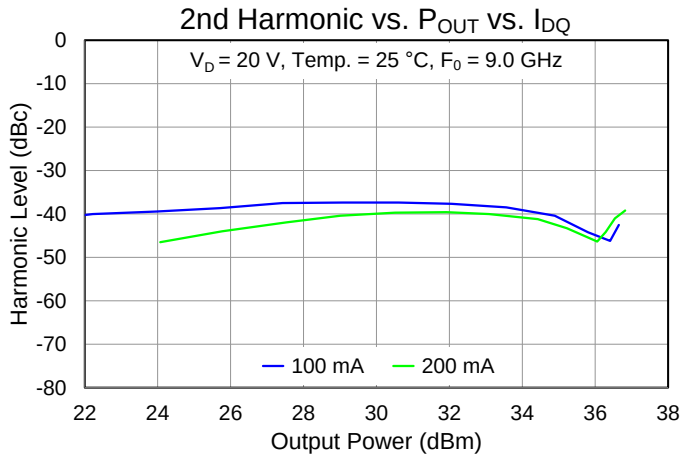
2nd Harmonic vs. P_{OUT} vs. Temp.



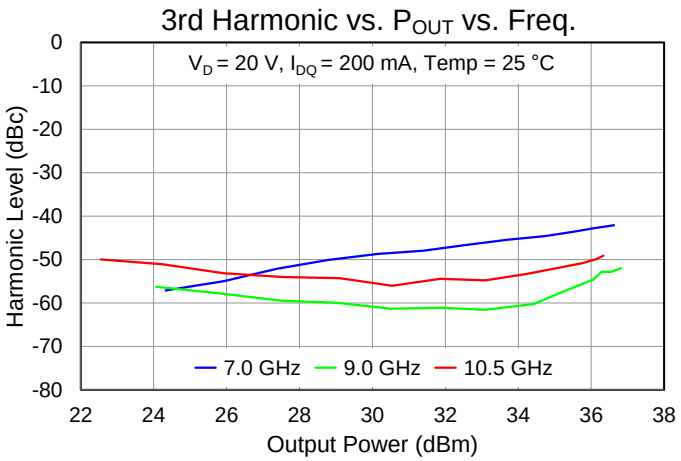
2nd Harmonic vs. P_{OUT} vs. V_D

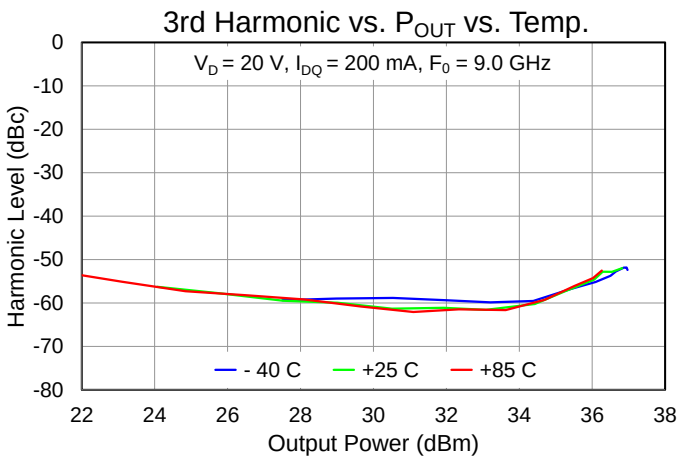


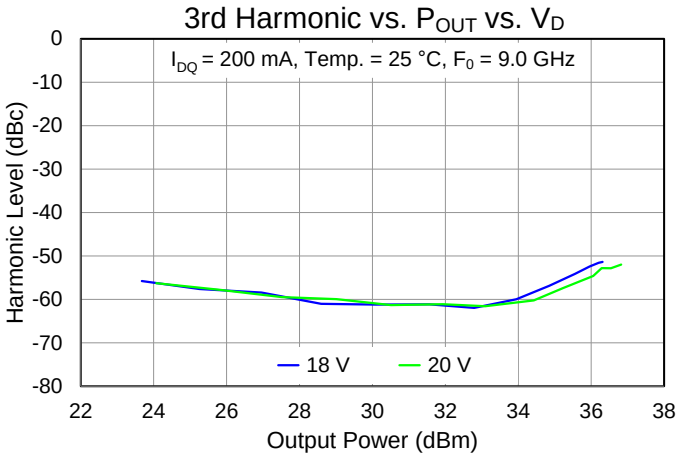
2nd Harmonic vs. P_{OUT} vs. I_{DQ}

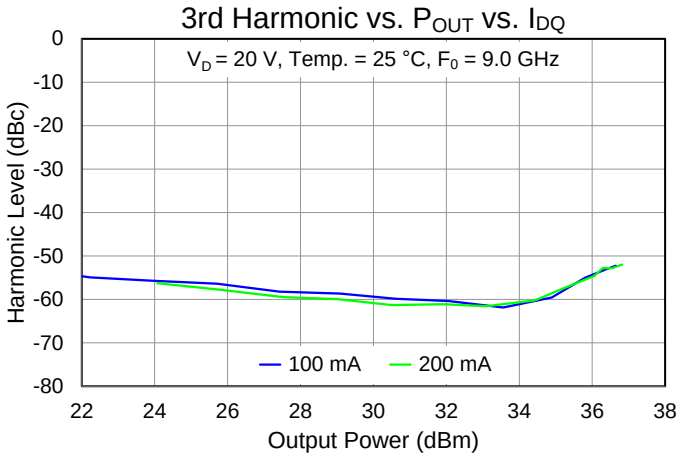


Performance Plots – Harmonics



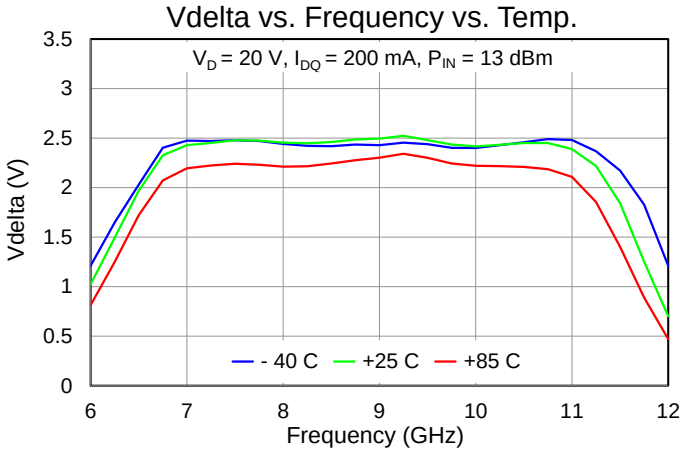


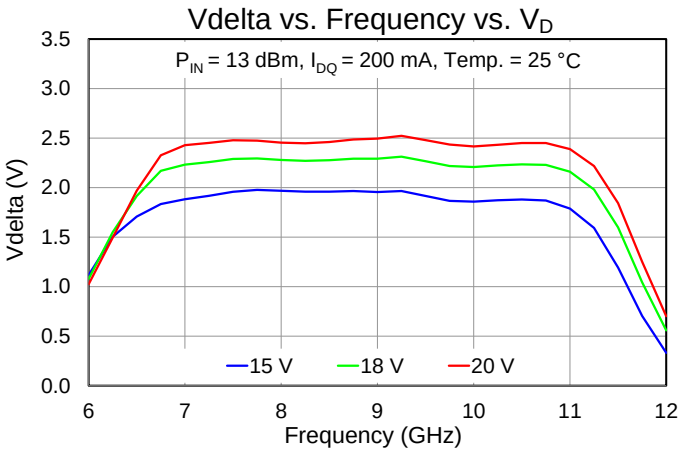


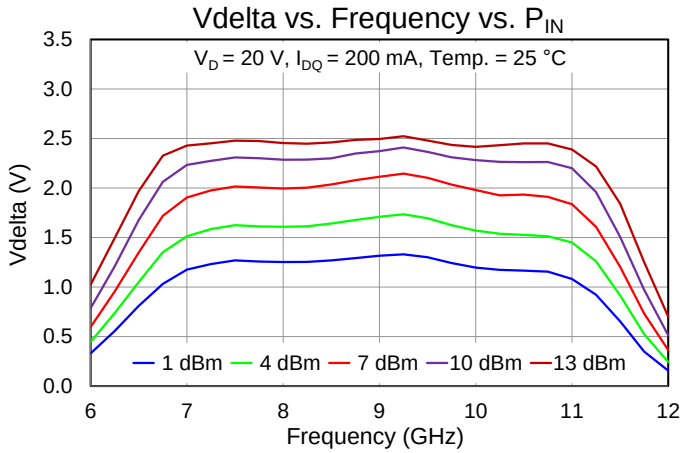


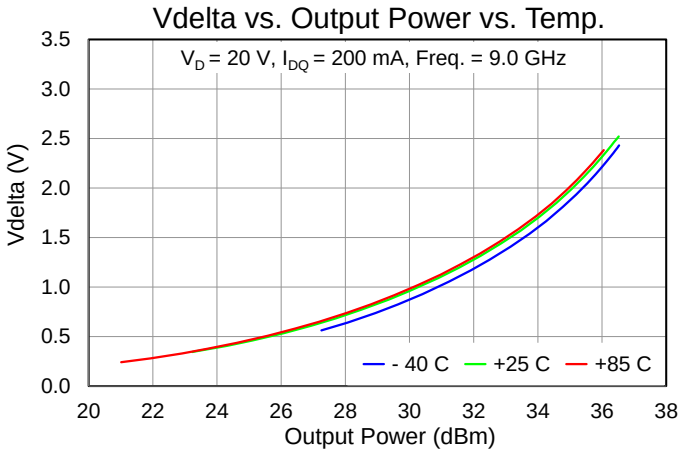
Performance Plots – Detector Voltage

Note: $V_{DELTA} = V_{REF} - V_{DET}$



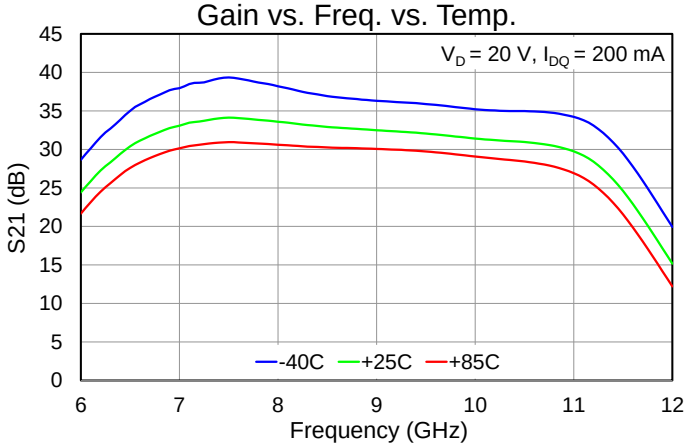




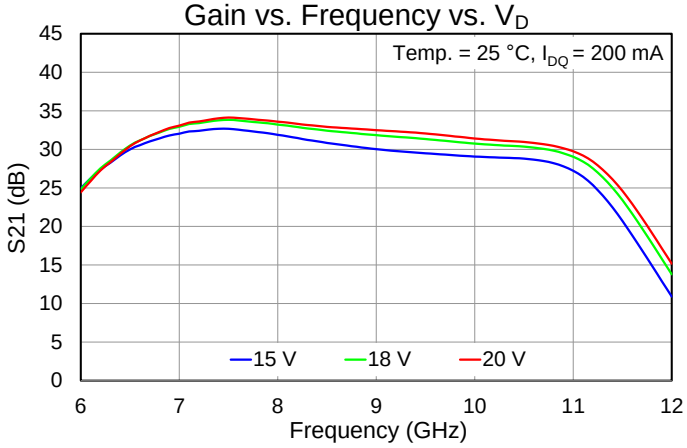


Performance Plots – Small Signal

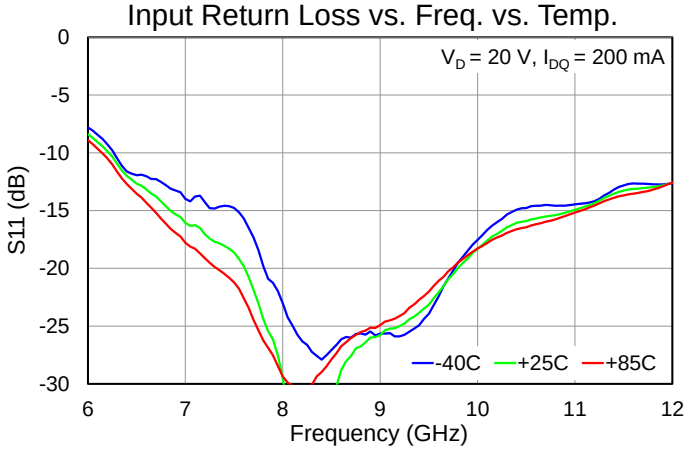
Gain vs. Freq. vs. Temp.



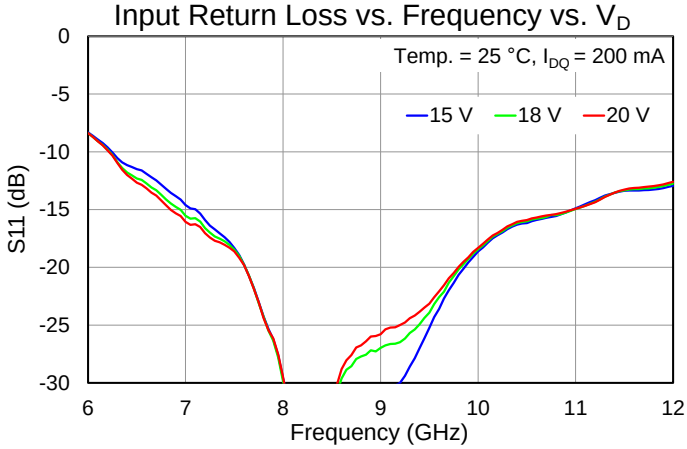
Gain vs. Frequency vs. V_D



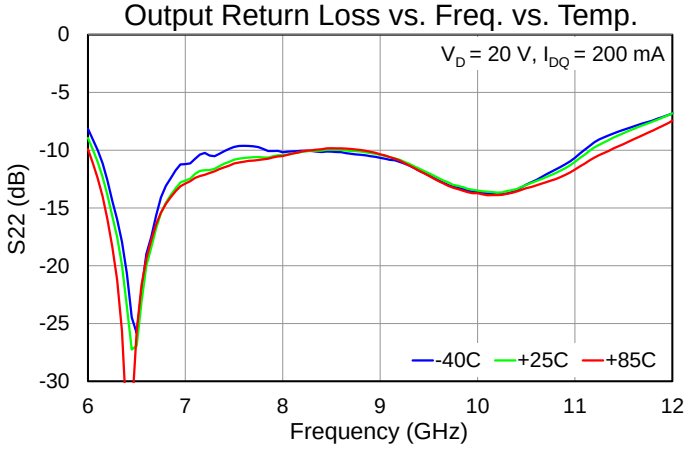
Input Return Loss vs. Freq. vs. Temp.



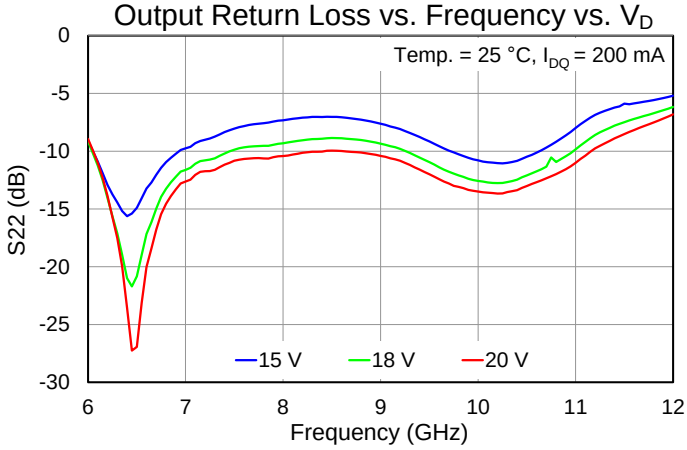
Input Return Loss vs. Frequency vs. V_D



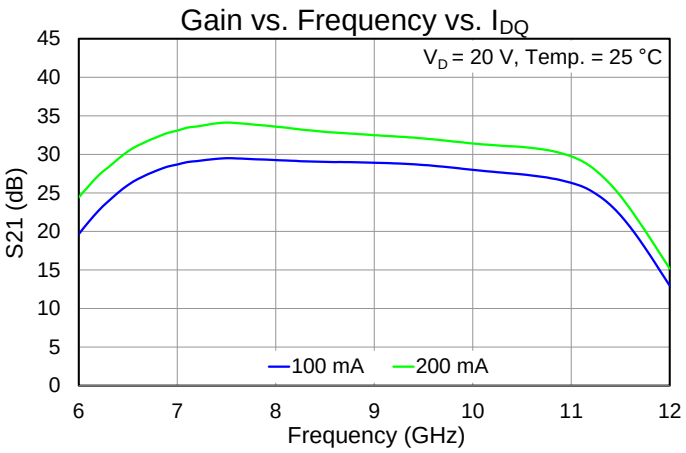
Output Return Loss vs. Freq. vs. Temp.

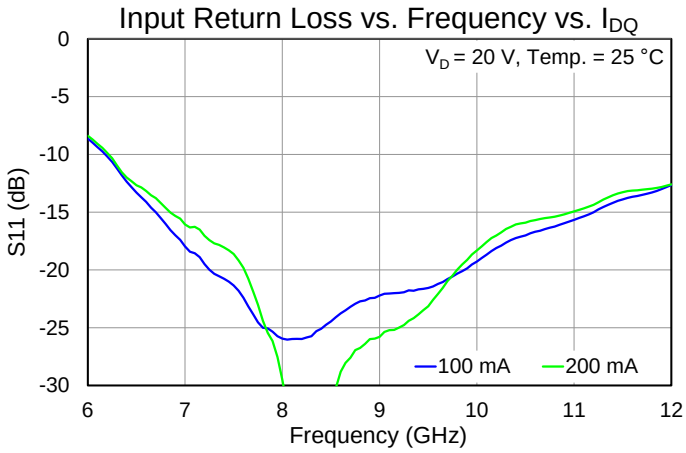


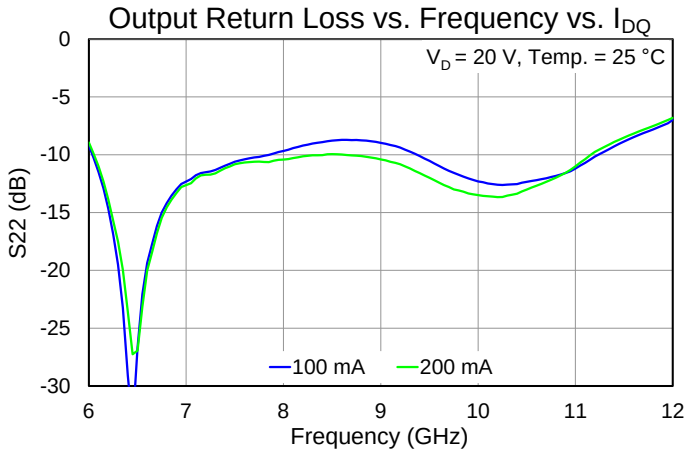
Output Return Loss vs. Frequency vs. V_D



Performance Plots – Small Signal





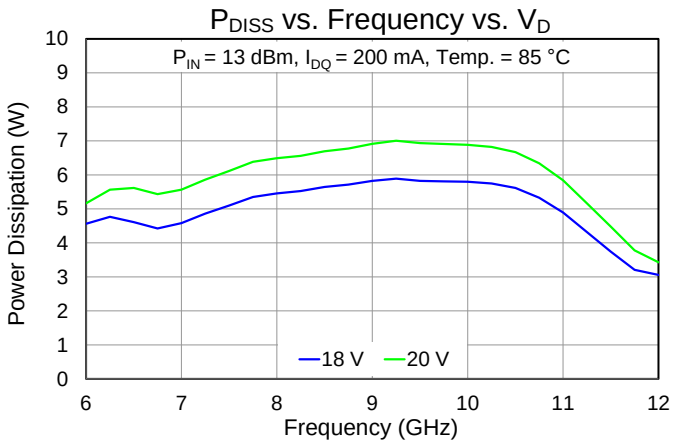


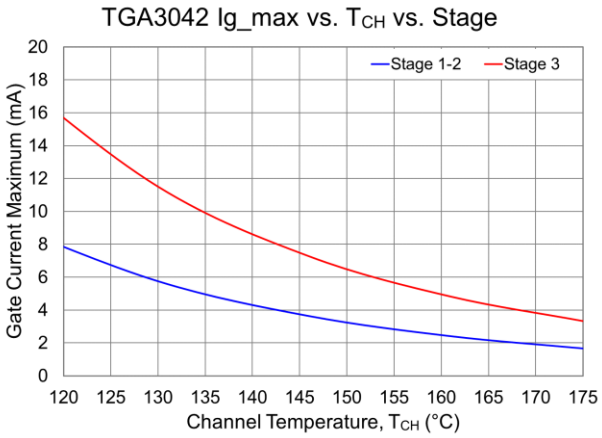
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = +20 V, I_{DQ} = 200 mA, P_{DISS} = 4.0 W	6.25	°C/W
Channel Temperature (T_{CH}) (Quiescent, No RF)		110	°C
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = +20 V, I_{DQ} = 200 mA, Freq = 9.25 GHz, P_{IN} = 13 dBm, I_{D_Drive} = 542 mA, P_{OUT} = 35.8 dBm, P_{DISS} = 7.0 W	6.43	°C/W
Channel Temperature (T_{CH}) (Under RF drive)		130	°C

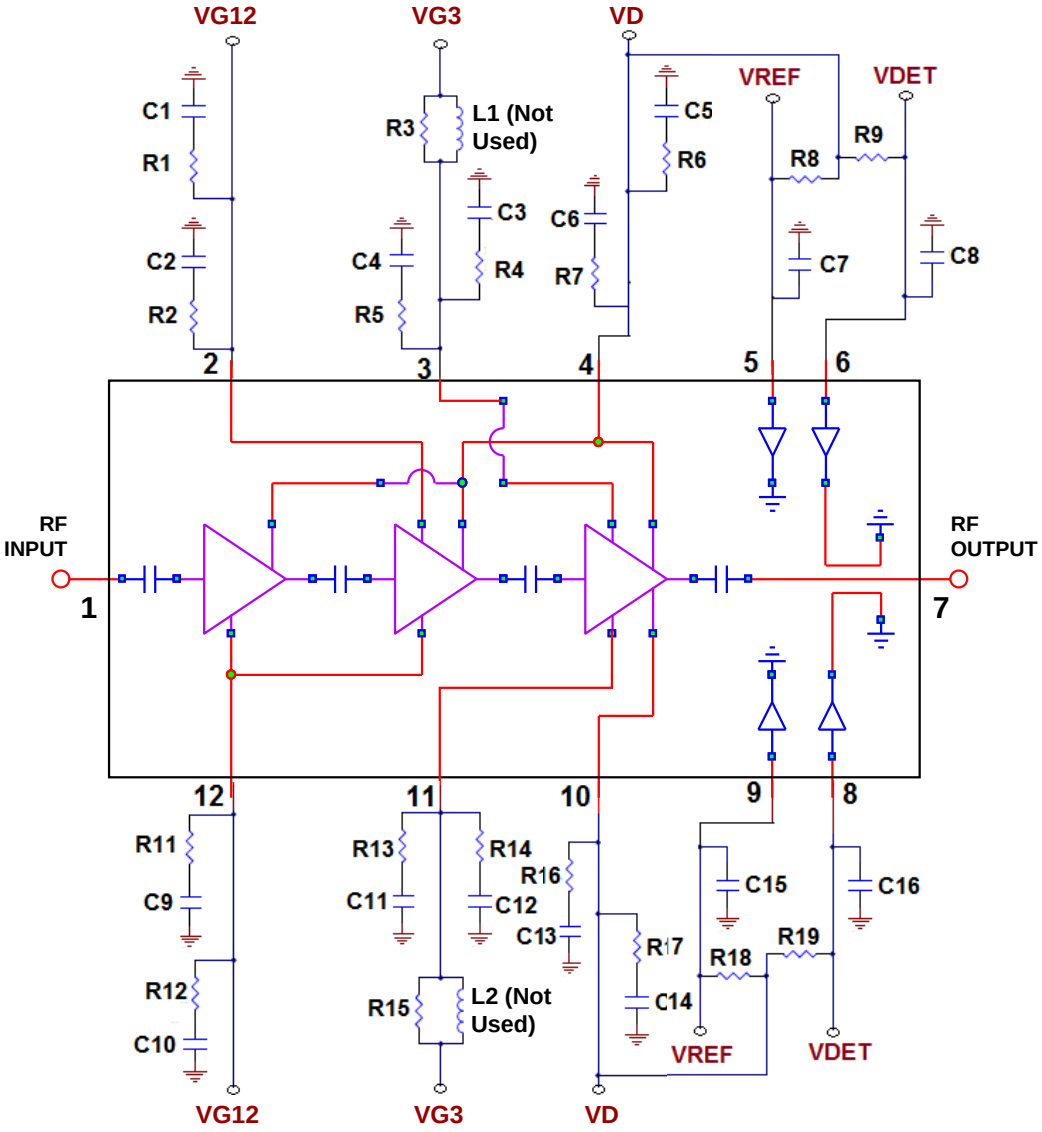
Notes:
1. Thermal resistance measured to back of carrier plate slug. MMIC mounted to 20 mil CuMo using AuSn eutectic.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Power Dissipation and Max Gate Current





Applications Information and Pad Layout



Note: $V_{DELTA} = V_{REF} - V_{DET}$

TGA3042 can be biased from either the top side or bottom side. Bypassing components required for the side(s) being biased.

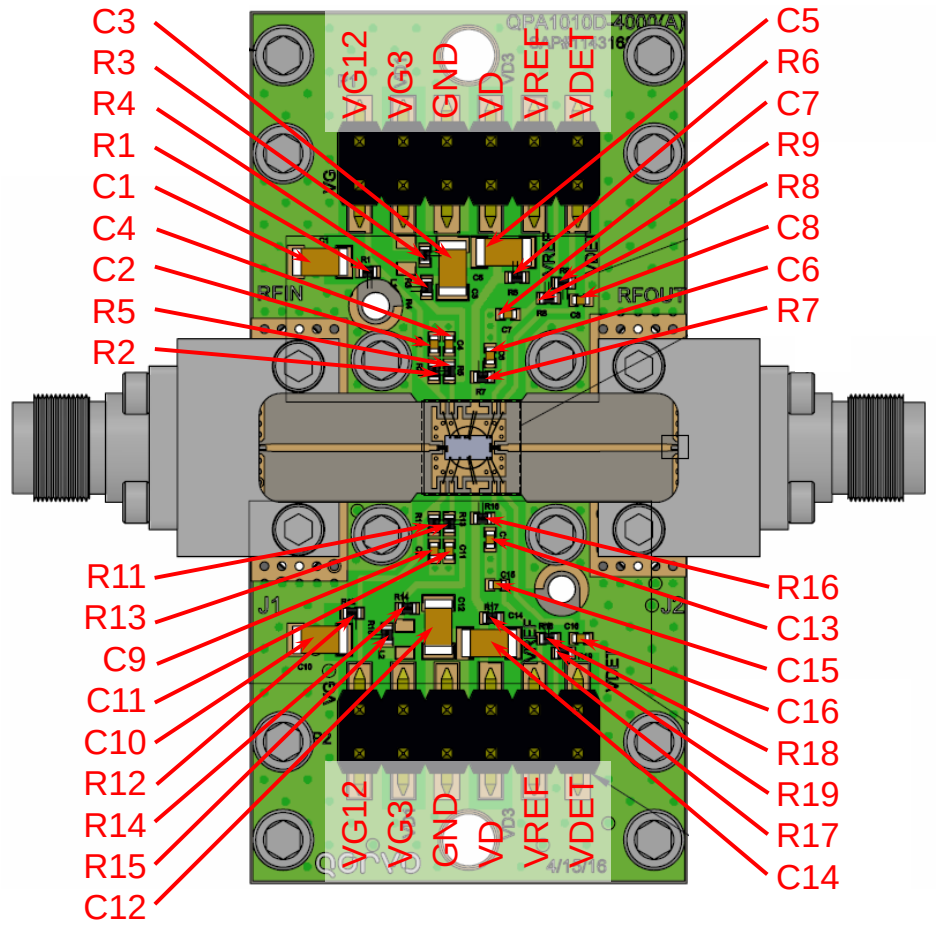
Bias Up Procedure

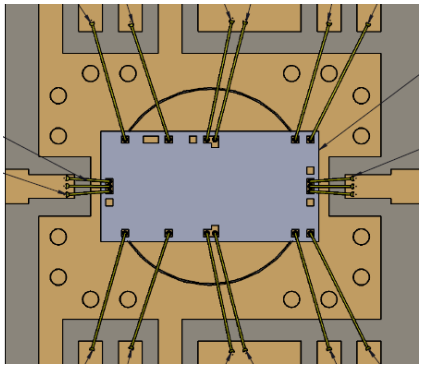
1. Set I_D limit to 1000 mA, I_G limit to 20 mA
2. Apply −5 V to V_G
3. Apply +20 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 200 mA (V_G ~ −2.2 V Typ.).
5. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board (EVB) Layout Assembly





Mounting Detail

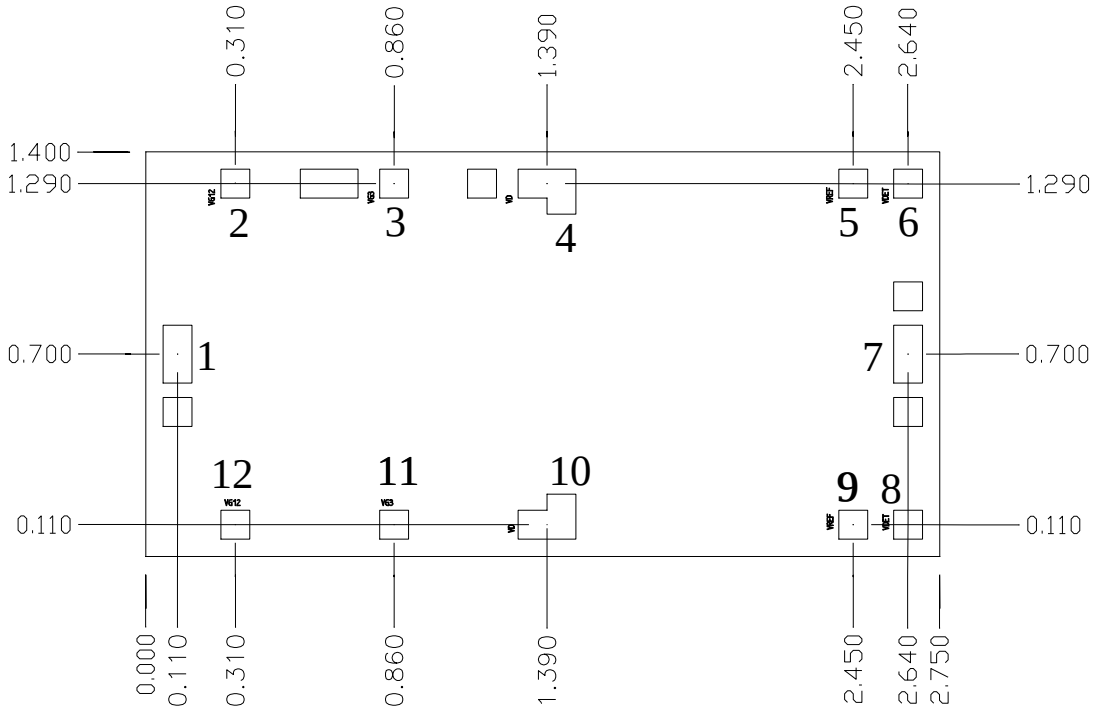
Note:

1. PCB is a multilayer PCB: all metal thicknesses 0.5 oz.; upper core 1 is Rogers 4003C, 8 mil thick; lower core is 370HR, 6 mil thick; pre-preg is an epoxy coated glass fabric; PCB is coined in the center section (circled area in pmounting detail) to provide required thermal management. 25 ± 3 mil finished PCB thickness
2. TGA3042 can be biased from either the top side or the bottom side. Bypassing components are required for the side(s) being biased.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1, C3, C5, C10. C12, C14	1 uF	CAP, 1206, 50 V, 5 %, X7R	Various	–
C2, C4, C6, C7, C8, C9, C11, C13, C15, C16	1000 pF	CAP, 0402, 100 V, 10 %, X7R	Various	–
R1, R2, R4 – R7, R11 – R14, R16, R17	5.1 Ohm	RES, 0402, 1/10W, 5 %	Various	–
R8, R9, R18, R19	25.5 K Ohm	RES, 0402, 1/16W, 1 %	Various	–
R3, R15	0 Ohm	RES, 0402, 1/10W	Various	–
J1, J2	NA	End Launch Connector, 2.92 mm	Southwest Microwave	1092-01A-5

Mechanical Information



Units: millimeters
Thickness: 0.10
Die x,y size tolerance: ± 0.050
Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (mm)	Description
1	RF IN	0.100 x 0.200	RF Input; matched to 50 Ω, DC blocked
2, 12	V_{G12}	0.100 x 0.100	Gate voltage for stages 1 & 2, bias network is required; see Application Circuit on page 14 as an example.
3, 11	V_{G3}	0.100 x 0.100	Gate voltage for stage 3, bias network is required; see Application Circuit on page 14 as an example.
4, 10	V_D	0.200 x 0.100	Drain voltage, bias network is required; see Application Circuit on page 14 as an example.
5, 9	V_{REF}	0.100 x 0.100	Reference voltage for Power detector
6, 8	V_{DET}	0.100 x 0.100	Power detector voltage
7	RF OUT	0.100 x 0.100	RF Output; matched to 50 Ω, DC blocked

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	TBD	ESDA / JEDEC JS-001-2012

Caution!
ESD-Sensitive Device

Solderability

Use only AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free
- Qorvo Green

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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