

Product Overview

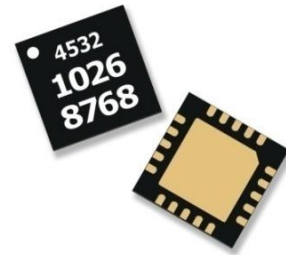
The TriQuint TGA4532-SM is a K-Band Power Amplifier. The TGA4532-SM operates from 17.7 - 19.7 GHz and is designed using TriQuint's power pHEMT production process.

The TGA4532-SM typically provides 32.5 dBm of saturated output power with small signal gain of 23 dB.

The TGA4532-SM is available in a low-cost, surface mount 20 lead 4x4 QFN package and is ideally suited for Point-to-Point Radio.

Lead-free and RoHS compliant

Evaluation Boards are available upon request.



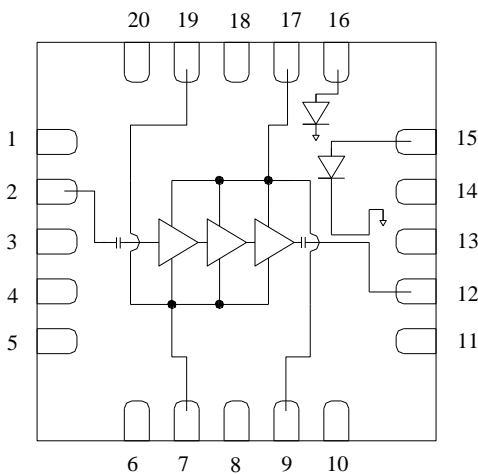
QFN 20 lead 4.0 x 4.0 mm

Key Features

- Frequency Range: 17.7 – 19.7 GHz
- Power: 32.5 dBm Psat, 31 dBm P1dB
- Gain: 23 dB
- TOI: 41 dBm at 20 dBm/tone
- NF: 7 dB
- Integrated Power Detector
- Bias: $V_d = 6\text{ V}$, $I_{dq} = 900\text{ mA}$, $V_g = -0.68\text{ V}$ Typical
- Package Dimensions: 4.0 x 4.0 x 0.85 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Point-to-Point Radio
- K-band Sat-Com

Ordering Information

| Part No. | ECCN | Description |
|------------|-------|------------------------|
| TGA4532-SM | EAR99 | K-Band Power Amplifier |

Standard T/R size = 500 pieces on a 7" reel

Absolute Maximum Ratings

| Parameter | Rating |
|-----------------------------------|----------------|
| Drain Voltage, Vd | +6.5 V |
| Gate Voltage, Vg | -4 to 0 V |
| Drain to Gate Voltage, Vd – Vg | 10 V |
| Drain Current, Id | 1960 mA |
| Gate Current, Ig | -8.2 to 113 mA |
| Power Dissipation, Pdiss | 12.7 W |
| RF Input Power, CW, T = 25°C | 26 dBm |
| Channel Temperature, Tch | 200 °C |
| Mounting Temperature (30 Seconds) | 260 °C |
| Storage Temperature | -40 to 150 °C |

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|---------------------------------|-----|-------|-----|-------|
| Drain Voltage (V _D) | | 6 | | V |
| I _{DQ} | | 900 | | mA |
| I _{D_Drive} (Under RF) | | 1200 | | mA |
| V _G | | -0.68 | | V |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

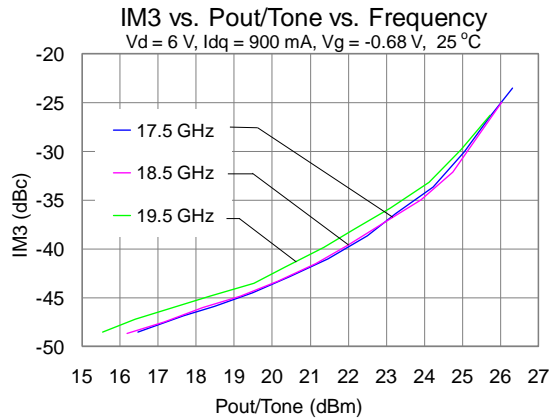
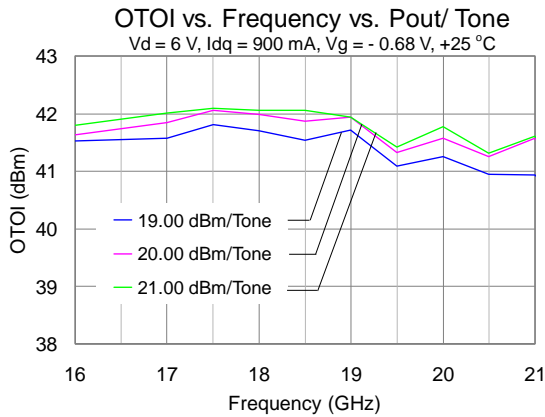
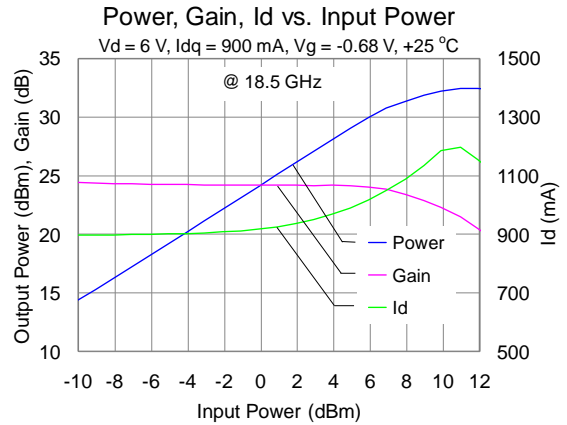
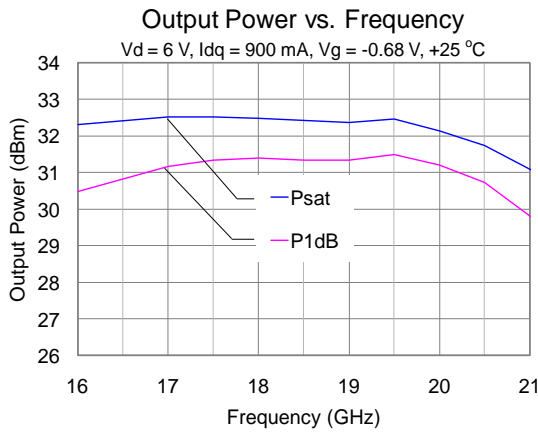
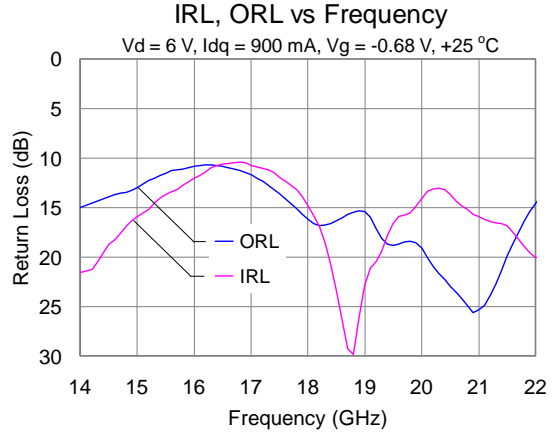
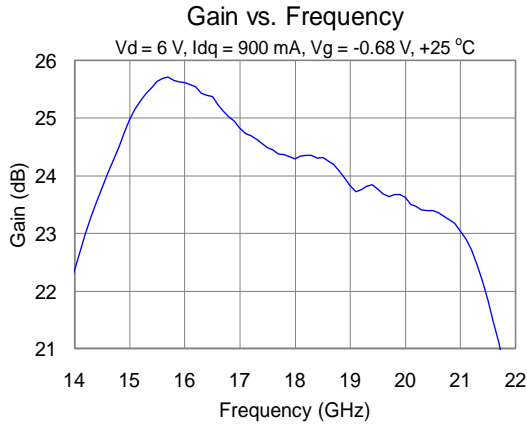
| Parameter | Conditions ⁽¹⁾ | Min | Typ | Max | Units |
|--------------------------------------|---------------------------|------|--------|------|--------|
| Operational Frequency Range | | 17.7 | | 19.7 | GHz |
| Gain | | 19 | 23 | | dB |
| Input Return Loss | | 10 | 12 | | dB |
| Output Return Loss | | 10 | 15 | | dB |
| Output Power at Saturation, Psat | | | 32.5 | | dBm |
| Output Power at 1dB Gain Compression | | 29.5 | 31 | | dBm |
| Output TOI | | 38 | 41 | | dBm |
| Noise Figure | | | 7 | | Db |
| Gain Temperature Coefficient | | | -0.023 | | dB/°C |
| Power Temperature Coefficient | | | -0.005 | | dBm/°C |

Notes:

1. Test conditions unless otherwise noted: VD=6V, IDQ=900mA, VG=-0.68V typical, Temp = +25 °C

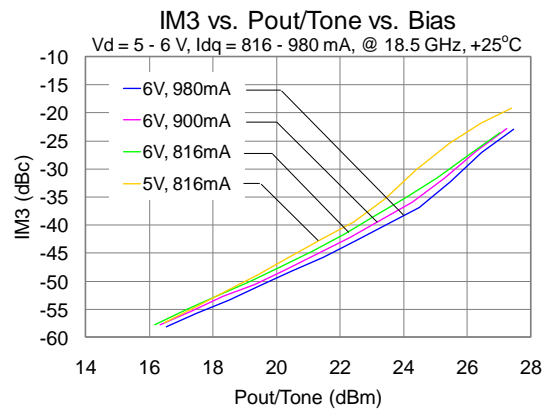
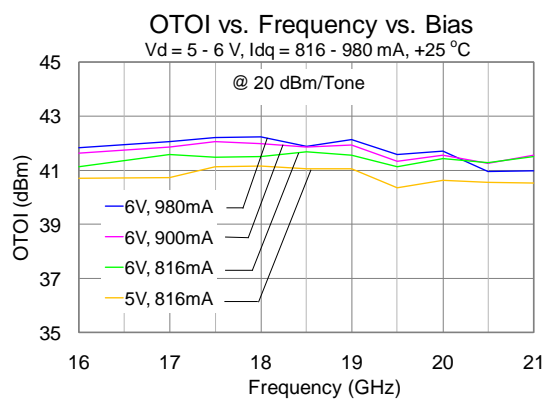
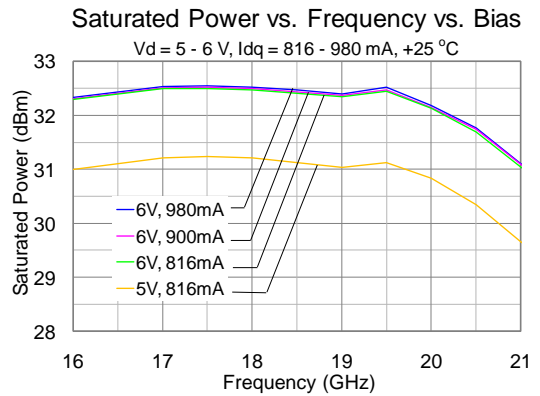
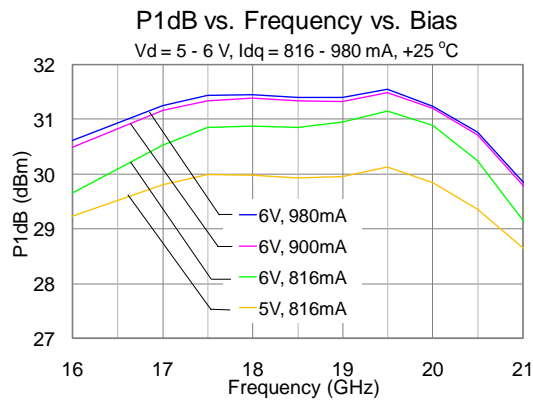
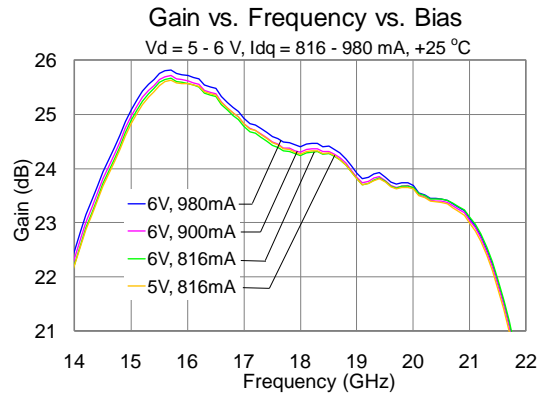
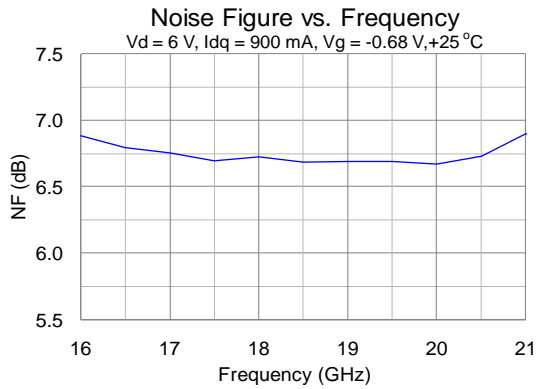
Performance Plots

Test conditions unless otherwise noted: $V_D=6V$, $I_{DQ}=900mA$, $V_G=-0.68V$ typical, Temp = $+25^\circ C$



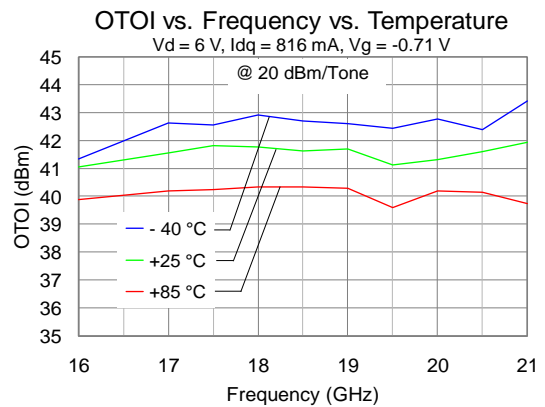
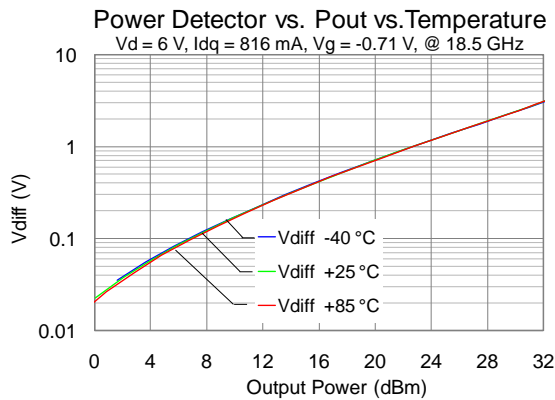
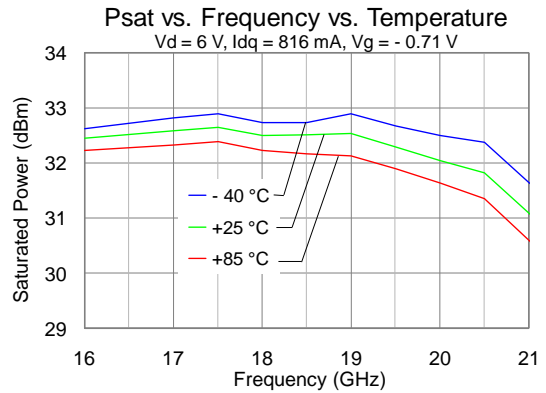
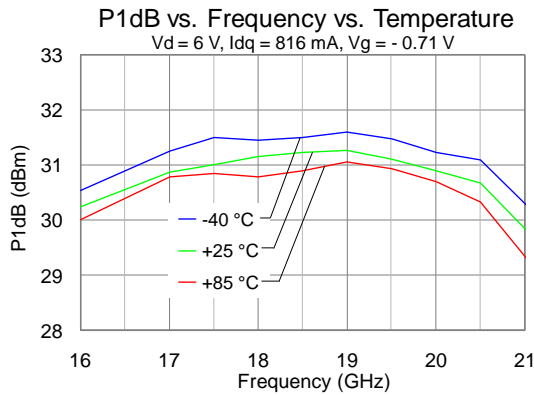
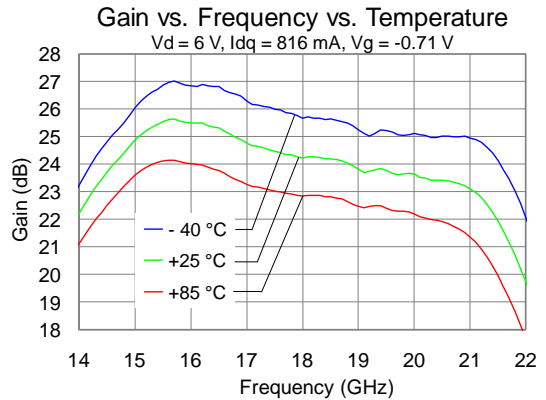
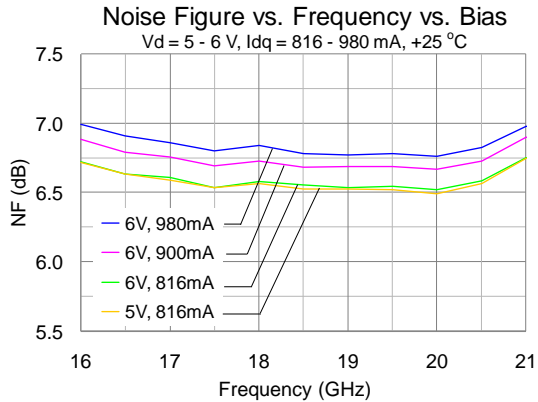
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Test conditions unless otherwise noted: $V_D=6V$, $I_{DQ}=900mA$, $V_G=-0.68V$ typical, Temp = +25 °C



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Thermal and Reliability Information

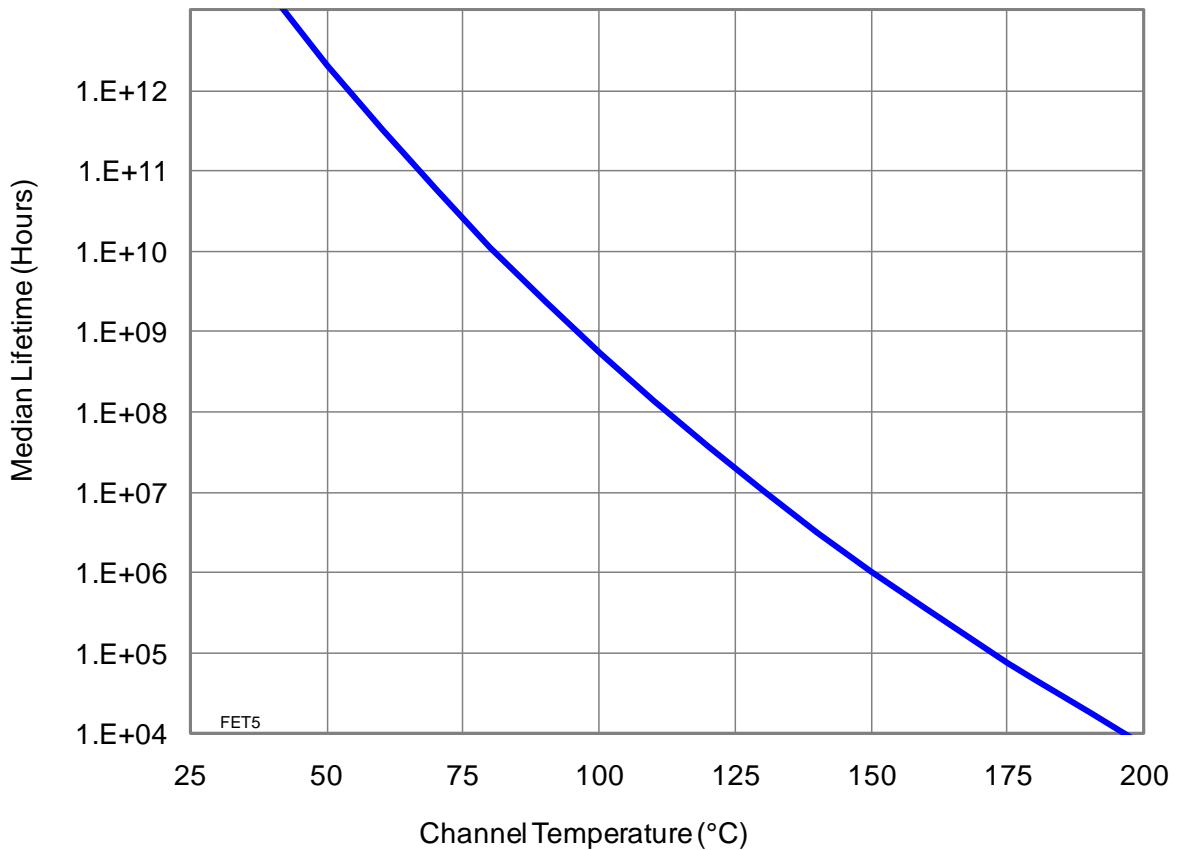
| Parameter | Test Conditions | Value | Units |
|---|---|-----------------------|-------|
| Thermal Resistance (θ_{JC}) ⁽¹⁾ | CW | 8.51 | °C/W |
| Channel Temperature, T _{CH} | T _{baseplate} = +85 °C, V _D = +6 V, I _{DQ} = 900 mA, | 131 | °C |
| Median Lifetime (T _M) | P _{DISS} = 5.4 W | 9.5 x 10 ⁶ | Hrs |
| Thermal Resistance (θ_{JC}) ⁽¹⁾ | CW | 4.17 | °C/W |
| Channel Temperature, T _{CH} (Under RF) | T _{baseplate} = +85 °C, V _D = +6 V, I _D = 1200 mA, | 131 | °C |
| Median Lifetime (T _M) | P _{OUT} = 32.5 dBm, P _{DISS} = 5.4 W | 9.5 x 10 ⁶ | Hrs |

Notes:

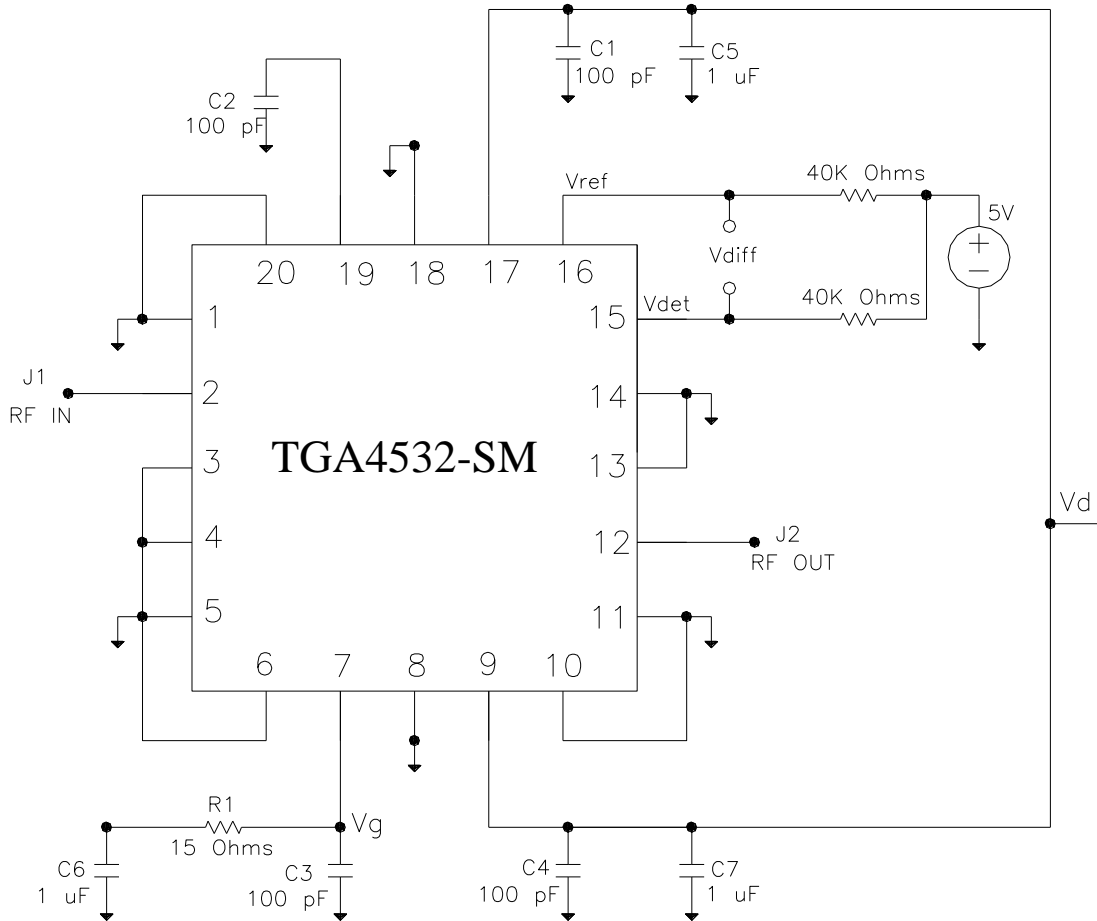
- Channel operating temperature will directly affect the device median lifetime (T_M). For maximum life, it is recommended that the channel temperatures be maintained at the lowest possible levels. Thermal resistance measured at back of package.

Median Lifetime

Test Conditions: V_D = +6 V; Failure Criteria is 10% reduction in I_{D_MAX}



Application Circuit



Notes:

1. V_G can be biased from either side (pin 7 or pin 19), and the non-biased side can be left open.
2. V_D must be biased from both sides (pin 9 and pin 17).

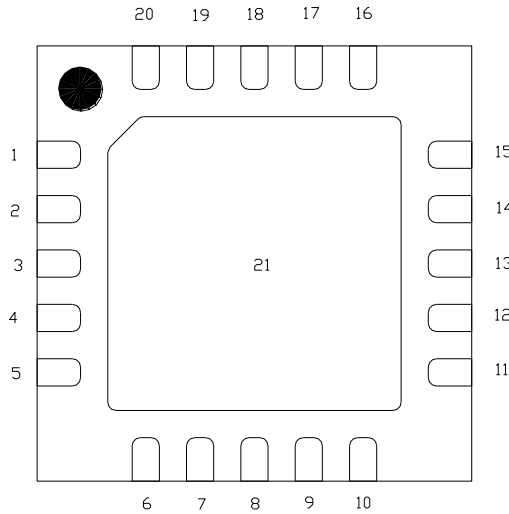
Bias Up Procedure

1. Apply -1.5 V to V_G
2. Apply $+6\text{ V}$ to V_D ; ensure I_{DQ} is approx. 0 mA
3. Adjust V_G until $I_{DQ} = 900\text{ mA}$ ($V_G \sim -0.68\text{ V Typ.}$).
4. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to -1.5 V ; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

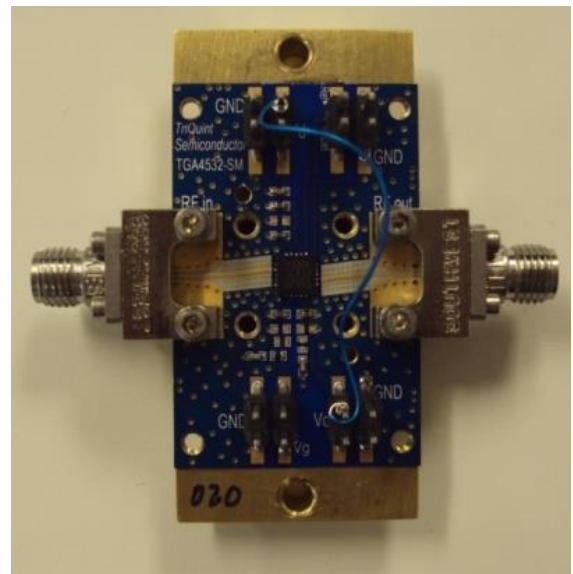
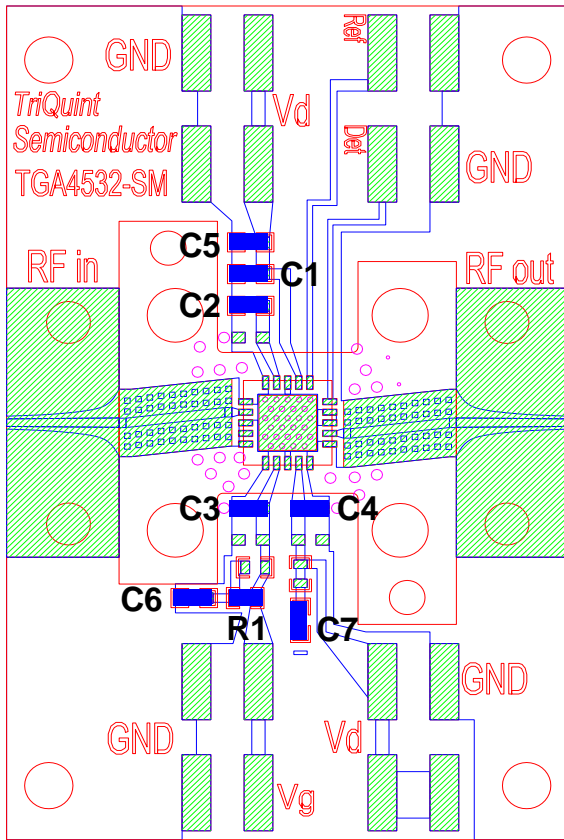
Pad Configuration and Description



TOP VIEW

| Pad No. | Label | Description |
|-----------------------------------|--------|---|
| 1, 3, 4, 5, 6, 10, 11, 13, 14, 20 | N/C | No internal connection; must be grounded on PCB |
| 2 | RF IN | Input, matched to 50 ohms |
| 7, 19 | Vg | Gate voltage. Bias network is required; see Application Circuit on page 7 as an example. Can be biased from either pin. |
| 8, 18 | GND | Internal grounding; can be grounded or left open on PCB |
| 12 | RF OUT | Output, matched to 50 ohms |
| 9, 17 | Vd | Drain voltage. Bias network is required; see Application Circuit on page 7 as an example. Both pins must be biased. |
| 15 | Vdet | Detector diode output voltage. Varies with RF output power. |
| 16 | Vref | Reference diode output voltage. |
| 21 | GND | Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see Mounting Configuration on page 11 for suggested footprint. |

Evaluation Board (EVB) Layout Assembly



Note: PCB is a multilayer

1. All 4 metal thicknesses are 0.5 oz
2. Upper core 1 is Rogers 4003C
3. Microstrip line width = 0.0175"

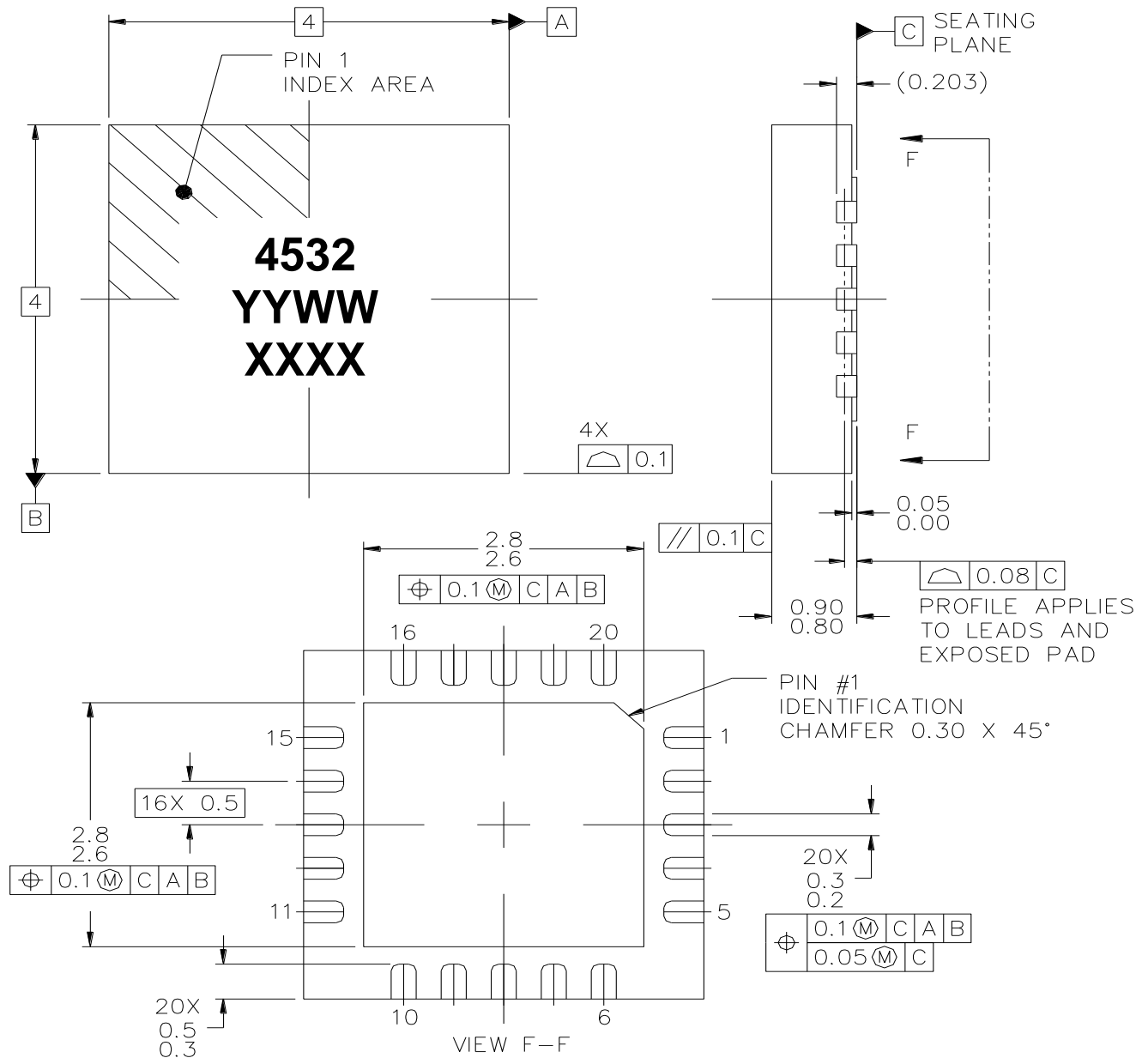
Bill of Material – TGA4532 Evaluation board

| Reference Des. | Value | Description | Manuf. | Part Number |
|----------------|---------|---------------------------|---------|-------------|
| n/a | n/a | Printed Circuit Board | Qorvo | |
| C1, C2, C3, C4 | 100 pF | Cap, 0402, 50V, 5%, NPO | various | |
| C5, C6, C7 | 1 uF | Cap, 0603, 50V, 5%, COG | various | |
| R1 | 15 Ohms | Res, 0402, 1/16W, 5%, SMD | various | |

Package Marking and Dimensions

Marking: Part Number – TGA4532-SM

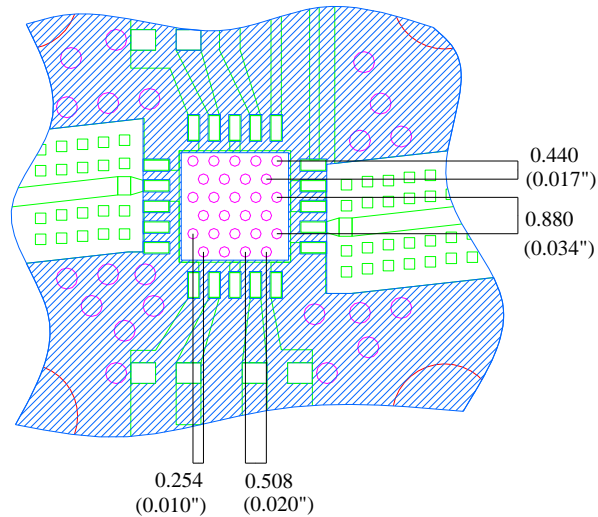
Vendor and Lot Code – "YY" is last two digits of manufacturing year, "WW" is the work week; "XXXX" is a generated number.



Notes:

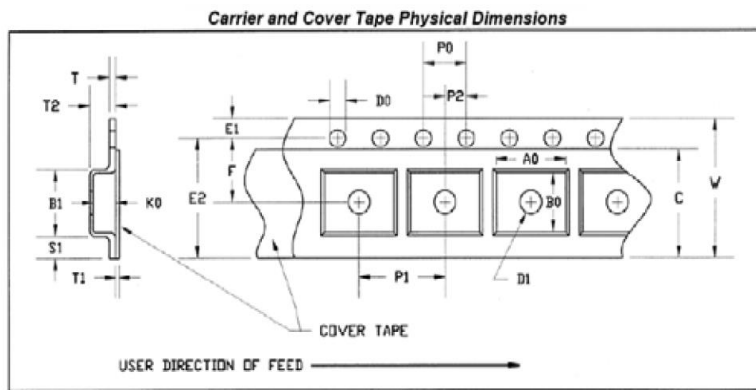
This package is lead-free/RoHS-compliant with an embedded heat spreader, and the plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and tin-lead (maximum 245 °C reflow temperature) soldering processes.

PCB Mounting Pattern



- Notes:
1. All dimensions are in millimeters (inches). Angles are in degrees.
 2. Ground vias are critical for the proper performance of this device. Vias should have a final plated thru diameter of .2524 mm (.010").
 3. A heatsink underneath the area of the PCB for the mounted device is recommended for proper thermal operation.
 4. The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Tape and Reel Information – Carrier and Cover Tape Dimensions



| Feature | Measure | Symbol | Size (in) | Size (mm) |
|---------------------|--|--------|-----------|-----------|
| Cavity | Length | A0 | 0.171 | 4.35 |
| | Width | B0 | 0.171 | 4.35 |
| | Depth | K0 | 0.043 | 1.1 |
| | Pitch | P1 | 0.315 | 8.0 |
| Centerline Distance | Cavity to Perforation - Length Direction | P2 | 0.079 | 2.0 |
| | Cavity to Perforation - Width Direction | F | 0.217 | 5.5 |
| Cover Tape | Width | C | 0.362 | 9.2 |
| Carrier Tape | Width | W | 0.472 | 12.0 |

Handling Precautions

| Parameter | Rating | Standard |
|------------------------------|----------|---------------------|
| ESD – Human Body Model (HBM) | Class 1A | JEDEC JESD22-A114 |
| MSL Rating | Level 1 | JEDEC/IPC J-STD-020 |



Caution!
 ESD-Sensitive Device

Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering process.
 Solder profiles available upon request. Use of no-clean solder to avoid washing after soldering is recommended.
 Contact plating: NiAu

RoHS Compliance

This part is compliant with 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

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