TGP2615

15 -19 GHz 6-Bit Digital Phase Shifter (+Vc)

Product Description

Qorvo's TGP2615 is a 6-bit digital phase shifter fabricated on Qorvo's high-performance 0.15-µm GaAs pHEMT process. It operates over 15 to 19 GHz and provides 360° of phase coverage with an LSB of 5.625°. It also achieves a low RMS phase error of 4°, with 8 dB average insertion loss over all states.

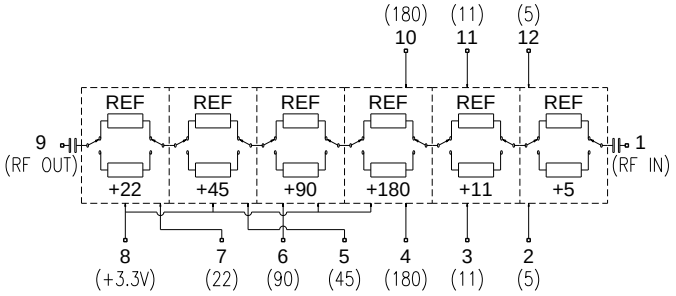
The TGP2615 uses positive switch logic, eliminating the need for a negative voltage rail. This combined with low insertion loss and a high degree of resolution makes the TGP2615 ideally suited for phased-array radar and satellite communications applications.

Product Features

- 6-Bit Digital Phase Shifter
- Frequency Range: 15 to 19 GHz
- 360° Coverage, LSB = 5.625°
- RMS Phase Error: 4°
- RMS Amplitude Error: 1 dB
- Insertion Loss: 7 dB
- Input Return Loss: >10 dB
- Output Return Loss: >9 dB
- Input IP3: >34 dBm
- Input P1dB: >24 dBm
- Control Voltage: 0/+3.3 V
- Chip Dimensions: 2.11 x 1.47 x 0.10 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details

Block Diagram



Applications

- Phased Array Rada
- Satellite Communications

Ordering Information

Part No.	Description
TGP2615	TGP2615 15-19 GHz 6-Bit Phase Shifter, Waffle Pack, Qty 100
TGP2615 EVB	TGP2615 Evaluation Board

Absolute Maximum Ratings

Parameter	Value
Control and Reference Voltages	6 V
Control Current	1 mA
Power Dissipation	0.8 W
Input Power, CW, 50 Ω, 85°C	30 dBm
Channel Temperature	200 °C
Mounting Temperature (30 Seconds)	320 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions may reduce device reliability.

Recommended Operating Conditions

Parameter	Value
Control Voltage (5˚, 11˚, 22˚, 45˚, 90˚, 180˚)	0/+3.3 V
Reference Voltage (V_{REF})	+3.3 V
Current (I_{REF}, I_{CTRL})	10 µA
Temperature Range	-40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed overall operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25°C. Control Voltage (REF, 5^0, 11^0, 22^0, 45^0, 90^0, 180^0) = 0/+3.3 V; See Bias Truth Table.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		15		19	GHz
Insertion Loss	Average across all phase states		6 - 8		dB
Input Return Loss	Average across all phase states		>10		dB
Output Return Loss	Average across all phase states		>9		dB
RMS Phase Error			4		deg
RMS Amplitude Error			1		dB
Input P1dB			>24		dBm
Input IP3	Tone spacing = 10 MHz Pin/Tone = 15 dBm		>34		dBm
Insertion Loss Temperature Coefficient	Average all phase states, 19 GHz		0.002		dB/°C

Bias and Truth Table

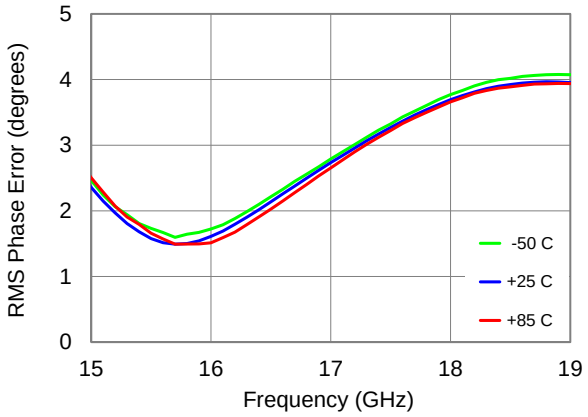
Control voltage Logic “0” = +0 to +0.2 V; Logic “1” = +3.3 to +5 V

Phase Shift	5^0	11^0	22^0	45^0	90^0	180^0	REF
0° (Reference)	0	0	0	0	0	0	1
5°	1	0	0	0	0	0	1
11°	0	1	0	0	0	0	1
22°	0	0	1	0	0	0	1
45°	0	0	0	1	0	0	1
90°	0	0	0	0	1	0	1
180°	0	0	0	0	0	1	1
355°	1	1	1	1	1	1	1

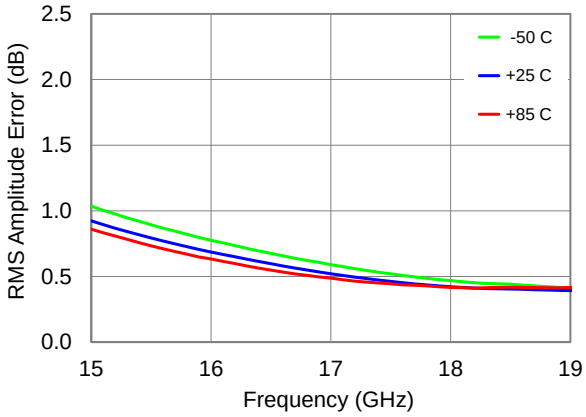
Performance Plots – Small Signal

Test conditions unless otherwise noted: 25 °C

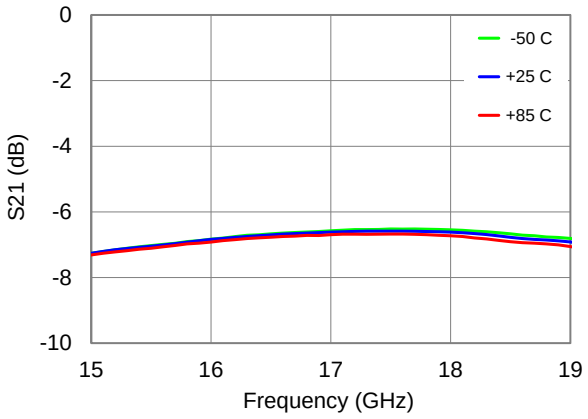
RMS Phase Error vs Frequency
All Phase States, V_{REF} = 3.3 V



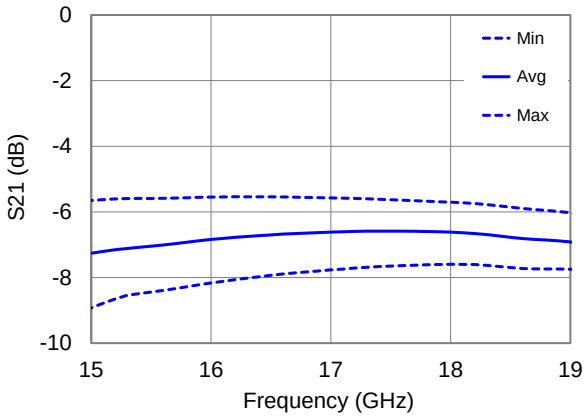
RMS Amplitude Error vs Frequency
All Phase States, V_{REF} = 3.3 V



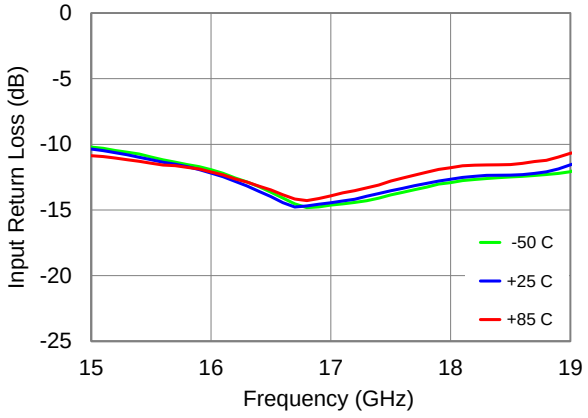
Average Insertion Loss vs Frequency
All Phase States, V_{REF} = 3.3 V



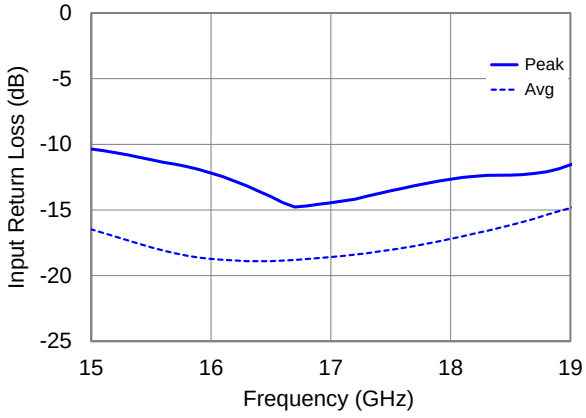
Peak Insertion Loss vs Frequency
All Phase States, 25 °C, V_{REF} = 3.3 V



Peak S11 vs Frequency
All Phase States, V_{REF} = 3.3 V



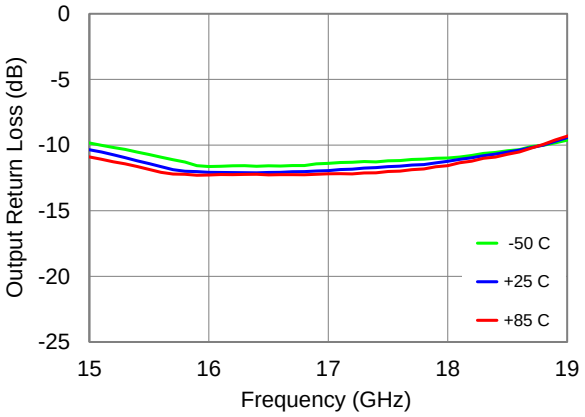
S11 vs Frequency
All Phase States, 25 °C, V_{REF} = 3.3 V



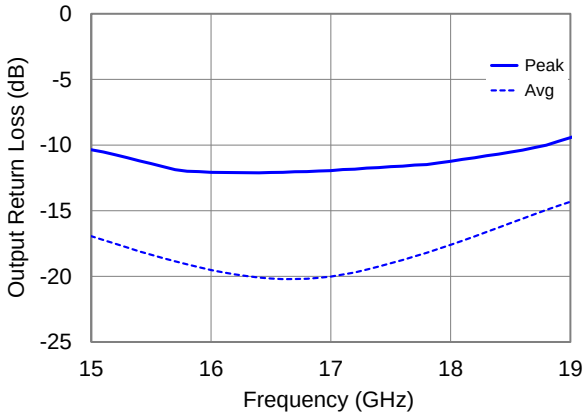
Performance Plots – Small Signal & Large Signal

Test conditions unless otherwise noted: 25 °C

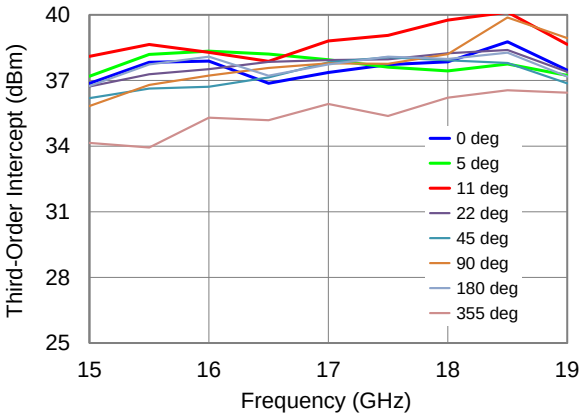
Peak S22 vs Frequency
All Phase States, V_{REF} = 3.3 V



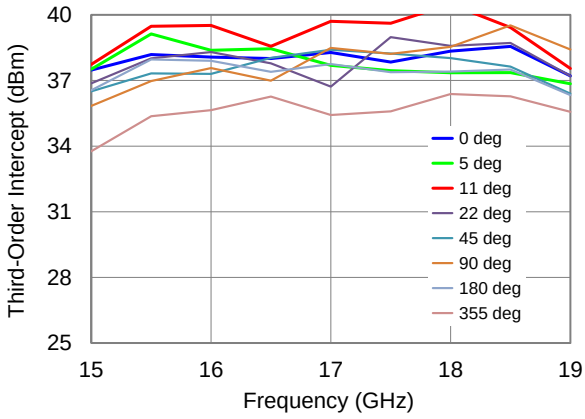
S22 vs Frequency
All Phase States, 25 °C, V_{REF} = 3.3 V



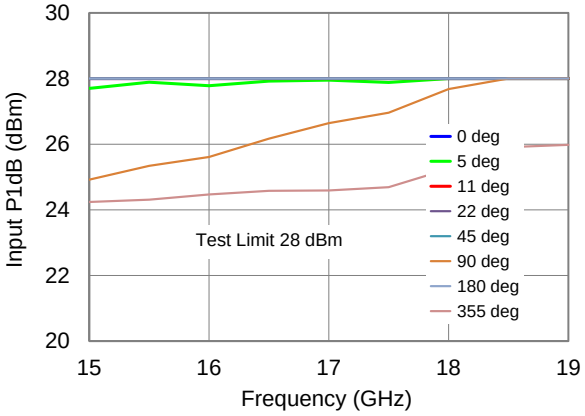
Input TOI vs Frequency
Major Phase States, 25 °C, V_{REF} = 3.3 V



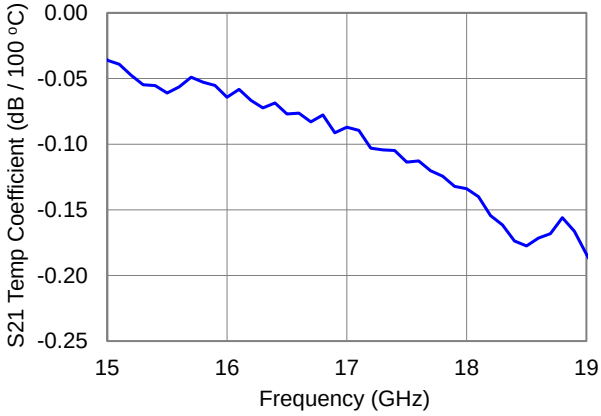
Input TOI vs Frequency
Major Phase States, 85 °C, V_{REF} = 3.3 V



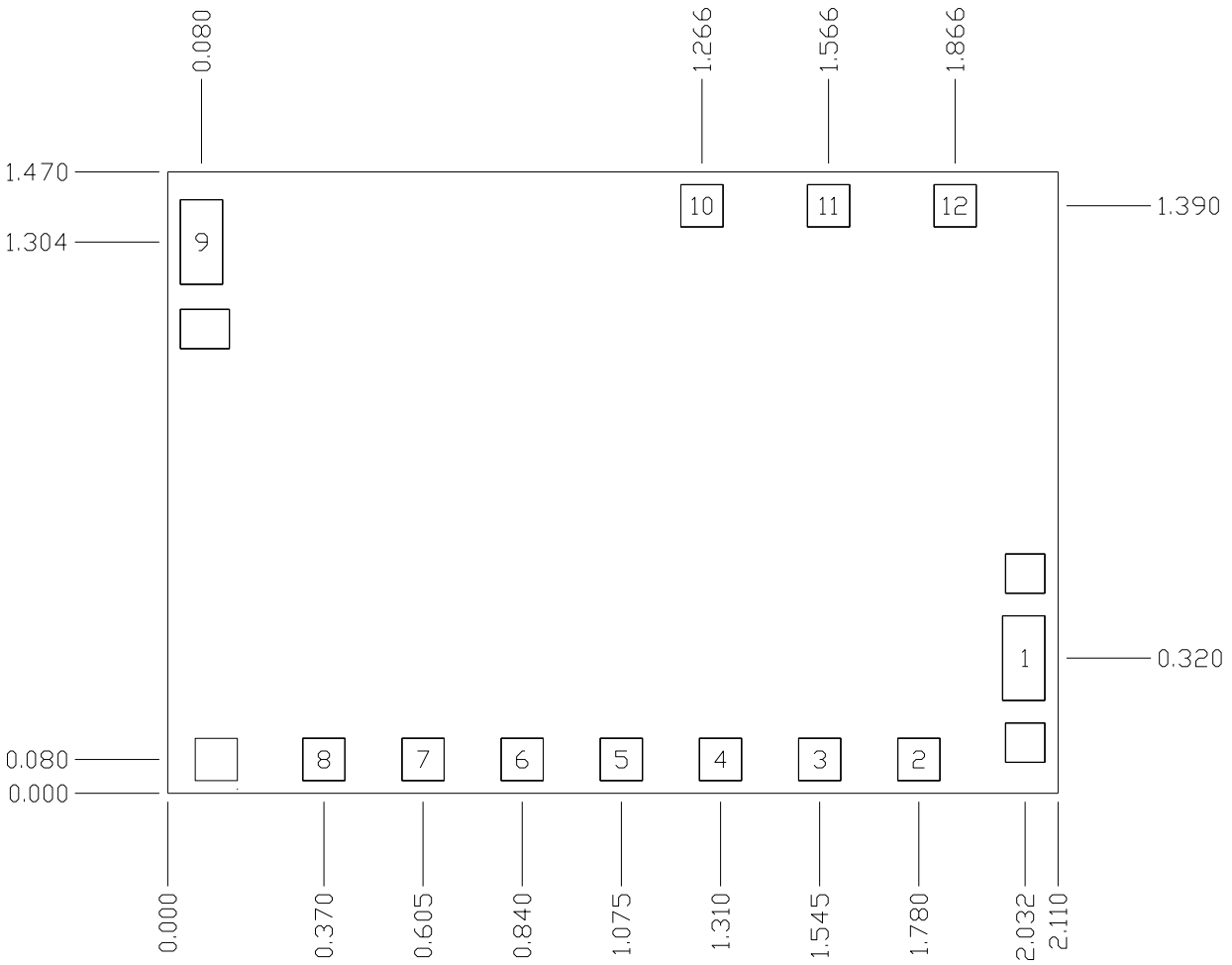
Input P1dB vs Frequency
Major Phase States, 25 °C, V_{REF} = 3.3 V



Loss Temperature Coefficient vs Frequency
All Phase States, -50 to +85 °C, V_{REF} = 3.3 V



Mechanical Information and Bond Pad Description

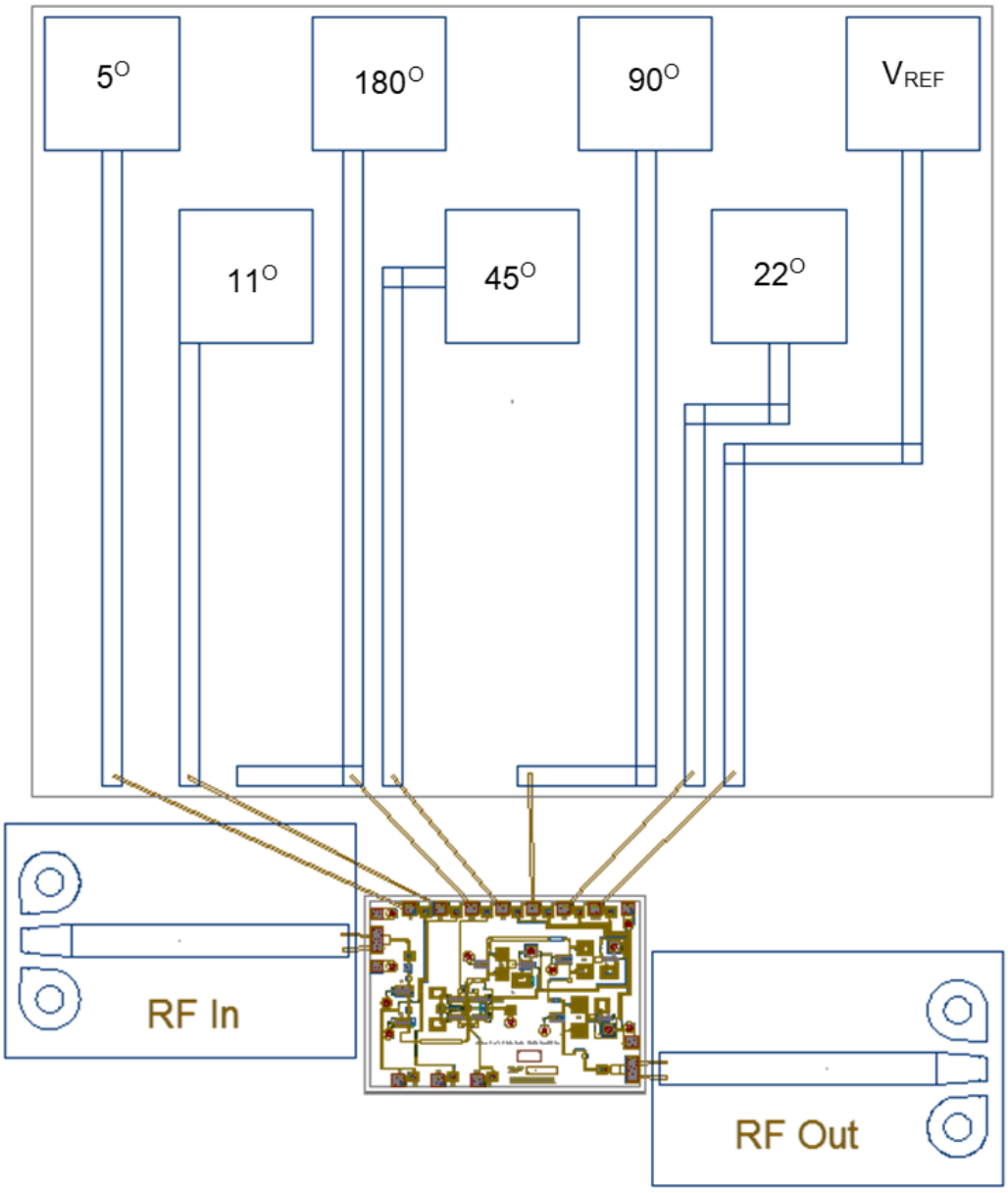


Unit: millimeters, Die thickness: 0.10, Die x, y size tolerance: ± 0.050
Chip edge to bond pad dimensions are shown to center of pad, Ground is backside of die

Bond Pad	Symbol	Description	Pad Size
1	RF IN	RF Input; 50 Ω; DC-Blocked	0.100 x 0.200
2	5°	5° Bit Control	0.100 x 0.100
3	11°	11° Bit Control	0.100 x 0.100
4	180°	180° Bit Control	0.100 x 0.100
5	45°	45° Bit Control	0.100 x 0.100
6	90°	90° Bit Control	0.100 x 0.100
7	22°	22° Bit Control	0.100 x 0.100
8	V_{REF}	Reference voltage for logic “1”	0.100 x 0.100
9	RF OUT	RF Output; 50 Ω; DC-Blocked	0.100 x 0.200
10	180°	180° Bit Alternate Control	0.100 x 0.100
11	11°	11° Bit Alternate Control	0.100 x 0.100
12	5°	5° Bit Alternate Control	0.100 x 0.100

Assembly Drawing and Application Information

1. The spacing between MMIC and TFN at RF In and RF Out is <5 mils typical.
2. RF connections: Bond two 1-mil diameter, <20 mils length gold bond wires at RF In and RF Out for optimum RF performance.
3. For fixtured testing, device was rotated 180 degrees from orientation in the page-1 chip photograph.



Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e., conductive epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- Conductive epoxy die attach is recommended for PCB mounting.
- Bonding pads plating: Au.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

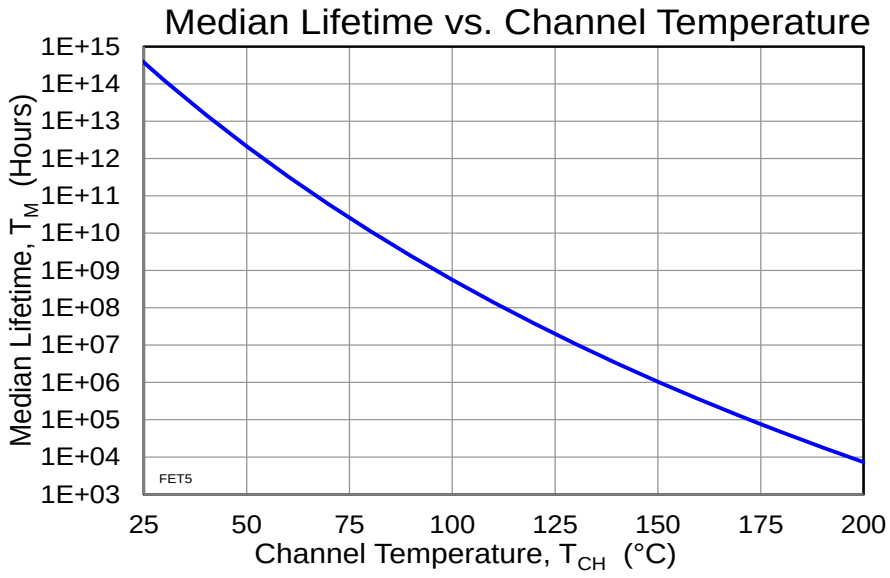
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Channel Temperature (T_{CH})	$T_{BASEPLATE}$ = 85°C	85	°C
Median Lifetime (T_M)		5.2E+9	Hrs

Notes:
1. Under normal (lifetime) operating conditions, self-heating is not a significant contributor to channel temperature.

Median Lifetime

Test Conditions: 6.0 V; Failure Criterion = 10% reduction in I_{DQ_MAX}



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 0B	ESDA / JEDEC JS-001-2014

Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: **1-844-890-8163**

Web: **www.qorvo.com**

Email: customer.support@qorvo.com

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